

A CHANNEL-LEAKAGE MONITOR FOR SILICON WAFER SCRIBE TESTING
WITHOUT MECHANICAL ACCESS



by
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ACKNOWLEDGEMENTS

This work is dedicated to my father. Rest in peace dad...



ABSTRACT

A CHANNEL-LEAKAGE MONITOR FOR SILICON WAFER SCRIBE TESTING WITHOUT MECHANICAL ACCESS

A novel sensor topology has been developed for measuring the channel leakage current of a MOSFET in scribe test. Being integrated with a wireless beacon platform powered by indoor illumination, it eliminates all aspects of mechanical access including stepping, micro-metric alignment and contact. The sensor has been developed in the form of a three-stage ring oscillator, where each stage has been built with a MOSFET device-under-test whose m segments function as the load and one segment functions as the driver. Unlike the existing ring-oscillator type leakage sensors, its frequency is not corrupted by the highly uncertain channel leakage current of any MOSFET of complementary conductance. It therefore provides the most reliable measurement among the ring-oscillator class of leakage sensors.

What enables the proposed leakage sensor to eliminate the conventional mechanical access in scribe test is its nanowatt-level power consumption, which can be supplied directly by photovoltaic conversion from environmental illumination. To this end, a test monitor that integrates the sensor with a platform of photovoltaic supply and two-way communication link has been designed. Downlink has been realized with visible light communication, which enables the user to select either PMOS or the NMOS version of the sensor. Uplink has been realized with a beacon of an ultra-wide-band impulse radio. It transmits bursts of a pulse train, whose repetition rate is equal to sensor frequency. The much slower repetition frequency of the bursts is determined by the acquisition time of adequate photovoltaic energy. A small loop antenna placed approximately 1 cm above the test monitor without any critical alignment is capable of detecting the transmitted pulses.

ÖZET

SİLİSYUM PUL ÜZERİNDE MEKANİK ERİŞİMSİZ ÇİZİK TESTİ YAPABİLEN BİR KANAL KAÇAĞI MONİTÖRÜ

Bu çalışmada, MOSFET kanal kaçak akımını çizik testi kapsamında ölçecek özgün bir sensör topolojisi geliştirilmiştir. Bu sensör, enerjisini iç mekan aydınlanmasından alan bir kablosuz çakar platformu ile tümleştirilmesi sayesinde, mekanik erişimin öteleme, hizalama ve temas gereksinmelerinin tümünü ortadan kaldırmıştır. Sensör üç katlı bir halka osilatörü olarak düzenlenmiştir. Her katta, test altındaki MOSFET'e ait m segmentten oluşan bir yük ve bir segmentten oluşan bir sürücü vardır. Frekansı, halka osilatörü kullanan mevcut kaçak sensörlerinin aksine, test edilenin dışında herhangi bir MOSFET'e ait kanal kaçağına bağlı değildir. Bu nedenle halka osilatörlü kanal kaçağı sensör sınıfındaki mevcut topolojilerden daha güvenilir bir ölçme sonucu alınması sağlanmıştır.

Tez kapsamında geliştirilen kaçak sensörünün çizik testindeki alışlagelmiş mekanik erişime alternatif oluşunun kaynağında nanowatt düzeyinde güçle çalışabilme yeteneği yer alır. Bu düzeyde bir gücü doğrudan doğruya ortam aydınlanmasından fotovoltaiik dönüşümle sağlamak mümkündür. Bu amaçla, sensörü fotovoltaiik besleme ve iki yönlü iletişim sağlayan bir platformla bir araya getiren bir monitör tasarlanmıştır. Görünür ışık iletişimine dayanan veri iletimi sayesinde kullanıcıya PMOS veya NMOS sensör seçme olanağı sağlanırken, monitörden veri iletimi ise çok geniş bantlı bir darbeleri radyo ile gerçekleştirilmiştir. Radyonun yayınladığı darbe serisi paketlerinde taşıyıcı 3.3 GHz merkez frekansına sahipken, tekrarlama frekansı sensör frekansı ile belirlenmektedir. Çok daha düşük olan paket tekrarlama frekansı da yeterli fotovoltaiik enerjinin biriktirilme periyodu ile belirlenmektedir. Test monitörünün yayınladığı darbe frekansının monitörden yaklaşık 1 cm yukarıda, küçük bir halka antenle ve kritik bir hizalama gerektirmeden algılanabilmesi sağlanmıştır.

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LIST OF SYMBOLS/ABBREVIATIONS

$A_{d(0)}$	DC differential gain of OTA/OPAMP
C_L	Load capacitance
C_{ox}	Oxide capacitance per unit area
E	Irradiance
f	Frequency
f_{cl}	Closed-loop bandwidth
f_{fp}	Full-power bandwidth
G_A	Available gain
g_m	Transconductance
I_B	Bias current
I_D	Drain current
I_{diode}	Diode current
I_{off}	Leakage current
I_{OJN}	Equivalent dark current of negative photodiode
I_{OJP}	Equivalent dark current of positive photodiode
I_{photo}	Photogenerated current
K, B_1	Stability factors
k	Boltzmann constant
q	Elementary charge
r_d	Small-signal diode resistance
r_o	Output resistance
S_{JN}	Slope factor of negative photodiode
S_{JP}	Slope factor of positive photodiode
S	Sub-threshold slope
T	Temperature
V_B	Bias voltage
v_C	Comparator output voltage
V_{DD}	Positive supply voltage

V_{DIR}	Differential input range
V_{DSSAT}	Drain-Source saturation voltage
V_{GS}	Gate-Source voltage
V_{GT}	Overdrive voltage
V_-	Inverting input of OTA/OPAMP
V_+	Non-inverting input of OTA/OPAMP
v_O	Unregulated boosted voltage
v_{PD}	Photodetector voltage
V_P	Peak voltage
V_{REF}	Reference voltage
V_{SS}	Negative supply voltage
V_{TH}	Logic threshold voltage
V_T	Threshold voltage
η	Sub-threshold slope factor
I	Photogenerated current per unit irradiance
λ	Wavelength
μ	Mobility
ω_H	High-cutoff frequency
ω_L	Low-cutoff frequency
ϕ_1, ϕ_2	Non-overlapping clocks
3D	Three dimensional
AC	Alternating current
ATE	Automated test equipments
CMOS	Complementary metal oxide semiconductor
CP	Charge pump
dB	Decibels
DC	Direct current
DNW	Deep n-well
EM	Electro-magnetic

GaAs	Gallium Arsenide
GBW	Gain-bandwidth product
GHz	Gigahertz
GSM	Groupe Spécial Mobile
HBT	Heterojunction bipolar transistor
Hz	Hertz
IEEE	Institute of Electrical and Electronics Engineers
InGaP	Indium Gallium Phosphide
I/O	Input-output
IR-UWB	Ultra wide band impulse radio
JSSC	Journal of Solid-State Circuits
LC	Inductor-capacitor
LNA	Low-noise amplifier
MIM	Metal-insulator-metal
MM	Mixed-mode
MOSCAP	Metal oxide silicon capacitor
MOSFET	Metal oxide semiconductor field effect transistor
MOS	Metal oxide semiconductor
NF	Noise figure
NMOS	N-type metal oxide semiconductor field effect transistor
NOR	Not or
NW	N-well
OPAMP	Operational amplifier
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PMOS	P-type metal oxide semiconductor field effect transistor
PW	P-well
RF	Radio frequency
RX	Receiver
SMA	Sub-miniature version a
SMD	Surface mounted device

SMU	Source-measure unit
SOTA	Symmetrical operational transconductance amplifier
SPICE	Simulation program with integrated circuit emphasis
THD	Total harmonic distortion
TIA	Trans-impedance amplifier
TX	Transmitter
UMC	United Microelectronics Corporation
U.S.	United States
UWB	Ultra wide band
VLC	Visual light communication
VSWR	Voltage standing wave ratio
XCP	Cross-coupled pair

1. OBJECTIVES

1.1. INTRODUCTION

Fabricated silicon wafers are subjected to a parametric test for identifying the ones qualified for the subsequent sort test. Also known as “scribe test”, this test is performed by measuring a few basic MOSFET parameters such as threshold voltage, saturation drive current and/or channel leakage current on monitor devices placed inside scribe lines or dedicated dies.[1] Electrical access to these devices is established by mechanical means involving stepping, micrometric alignment and contacting, which necessitate not only an expensive stepper/aligner but also a customized probe card.

In the case of channel-leakage measurement, the probe card has to be assembled on a ceramic base for maximizing the DC isolation performance, which adds to the cost of testing. Yet another contribution to cost comes from the practice of conducting these tests in a controlled environment in order to avoid imprecision due to the temperature and vibration sensitive alignment accuracy and contact pressure of the probes.[2] Furthermore, these probes have to be periodically cleaned with an abrasive as they accumulate dirt over time and be eventually replaced due to repetitive abrasion.[2] Mechanical contact may even cause reliability problems in thinned wafers or wafers containing high-k dielectrics.[2]

In this work, a novel sensor topology is proposed for measuring the channel leakage current of a MOSFET in scribe test. Once integrated with a wireless beacon platform powered by indoor illumination, it will eliminate all aspects of mechanical access including stepping, micrometric alignment and contact. The sensor is in the form of a three-stage ring oscillator, where each stage is built with a MOSFET device-under-test whose m segments function as the load and one segment functions as the driver. Unlike the existing ring-oscillator type leakage sensors, its frequency is not corrupted by the highly uncertain channel leakage current of any MOSFET of opposite conductance. It is therefore expected to provide the most reliable measurement among the ring-oscillator class of leakage sensors. Another best-of-class property expected from this sensor is the linearity by which its frequency is related

to the leakage current.

What enables the proposed leakage sensor to eliminate the conventional mechanical access in scribe test is its nanowatt-level power consumption, which can be supplied directly by photovoltaic conversion from environmental illumination. To this end, a test monitor that integrates the sensor with a platform of supply and two-way communication link has been designed. Down-link is based on visible light communication. It enables the user to select either PMOS or the NMOS version of the sensor. Up-link is a beacon of an ultra-wide-band impulse radio. It transmits bursts of a pulse train, where the carrier frequency of each pulse is in the GHz range, and the frequency of pulses is identical to sensor frequency. The much slower repetition frequency of the bursts is determined by the acquisition time of adequate photovoltaic energy. Design has targeted detectability with a small loop antenna placed approximately 1 cm above the test monitor without any critical alignment requirement.

1.2. LITERATURE SURVEY

The history of searching alternative techniques for removing mechanical access and micrometric alignment in a scribe test goes back to mid 2000s. Energy and data transfer into the wafer and data transfer from the wafer using far-field radio link have been proposed in 2005, but no integrated prototype has been realized.[4],[5] There are also several works which use radio link for data transfer only.[3],[6],[10] These studies, however still use mechanical contacts for energy transfer which we intend to eliminate throughout this work.

Another approach is to establish an inductive link between wafer and reader [7],[11]. Like the previous studies, this approach still uses mechanical contact for energy transfer. Another disadvantage of this approach is that the required proximity between reader and wafer is in the orders of micrometers range and which also necessitates tight alignment specifications.

A third approach is to establish capacitive coupling between reader and wafer. But this approach also requires tight alignment specifications and uses mechanical contact for energy transfer. [9],[12-15]

Based on the literature survey, there is only one approach which does not require mechanical contact. In this technique, energy is transferred via blue laser and the data transfer is performed via optical or capacitive coupling.[8],[16] There is no data transfer from reader to wafer since this work has been designed directly for scribe testing. Apart from the techniques listed above, this work is integrated together with the monitoring circuit and commercialized by Tau-Metrix Company. Micrometric alignment problem still exists since the laser which transfers energy from reader to wafer needs to be focused on a photodiode whose area is around $100\text{ }\mu\text{m}^2$.

In summary, it is obvious that all the techniques which aim to remove mechanical contact in a scribe test still suffer from micrometric alignment problem and use mechanical contact for energy transfer except for one approach. Possible reason for not abandoning contacting for energy transfer might be the traditional belief about the required power level which is thought to be met with mechanical contacts only. As an example, the work done in [15] uses a ring-oscillator for monitoring, and consumes $125\text{ }\mu\text{W}$ power and fed from the photodiode having 1 mA of short-circuit current and 850 mV of open circuit voltage. These voltage and current levels can not be met by a photodiode powered by indoor illumination. This restriction leads to the conclusion that the circuits used for monitoring scribe test parameters should be revisited and redesigned to consume less power; thereby can be fed directly from the photodiodes under indoor illumination.

Conventional sensors that are used for measuring channel-leakage in scribe tests consist of MOSFET arrays with accessibility of all terminals.[17-20] The measurement of channel-leakage is performed with the DC current-voltage curve of these arrays obtained with traditional automated test equipments (ATE). This technique is totally incompatible with the method which does not rely on mechanical access. Ring-oscillator type sensors which are capable of converting channel leakage to a frequency of an impulse train, on the other hand, are commonly used in scribe and sort test.[8],[21-29] These sensors are also studied directly in three U.S. patents [30-32] and IEEE JSSC periodicals [33]. Omitting the minor differences, these sensors have no difference and except for one work, they do not give information about the operating power. Only the work in [33] states that the power consumption of the sensor is 76 nW when operating with 0.8 V supply voltage. This power

level is greater than the level targeted in this work approximately two orders of magnitude. Furthermore, the minimum supply voltage is depicted as 0.5 V which is greater than the level supplied from an on-chip photovoltaic converter.

Still, it is possible to make proper modifications to the sensor in [33] for operating with an unregulated photovoltaic voltage level (≈ 0.4 V) and nanowatt-scale power consumption. The main problem of conventional sensors is the weak conversion linearity between channel-leakage and frequency due to being affected other uncertain parameters rather than the MOSFET-under-test. These non-idealities have not mentioned in the related works, but defined with a modeling and verification effort in this work. The modeling and verification results of the conventional and proposed sensors are presented in Section 2.2.

As far as removing mechanical contacting procedure is concerned, proposed sensor should be powered directly from photodiodes with acceptable dimensions under indoor illumination. For removing tight alignment specifications, an on-chip UWB antenna has been used. This antenna is expected to transmit the data provided by the channel leakage sensor up to ≈ 1 cm above from the wafer. Since the UWB antenna requires higher power levels which indoor-illuminated photodiodes can not provide, a continuous-time operation is not possible. A beacon architecture is needed to store sufficient energy and use it for transmitting the data periodically. The proposed sensor topology should satisfy the following specifications in order to be integrated with a beacon platform:

- To be powered by an unregulated photovoltaic voltage source with nanowatt-scale power level (≈ 0.4 V).
- To convert channel leakage current to a frequency of an impulse sequence.
- Conversion linearity between channel leakage and frequency is to be maximized without being affected by any other uncertain parameter.

In this work, a fully contactless scribe-line monitor for measuring I_{off} is described. It is powered by scavenging indoor light without necessitating any kind of tight alignment at all. A visual light communication (VLC) downlink enables the user to select one of two integrated leakage sensors for readout. Measured data are transmitted by an integrated

ultra-wideband impulse-radio (IR-UWB) uplink. Considering the limited space available inside scribe lines for photovoltaic converter placement, and the relatively low irradiance of indoor lighting, the amount of power available for the monitor is extremely low. IR-UWB is of course inherently efficient in this respect. Leakage sensors, baseband blocks and VLC are also made efficient by following a minimalist design approach to their architecture and circuitry. These units consume a total of 64 nW power supplied directly by photovoltaic converters without regulation. IR-UWB transmitter is powered by a voltage-boosted supply. Direct powering of the majority of the components also helps keep the footprint small for scribe-line integration of the entire monitor. Experimental work, including final verification, was carried out on three successive 0.18 μm CMOS implementations, which are referred to as Chip-1, Chip-2 and Chip-3 in the following sections.

1.3. PROPOSED LEAKAGE MONITOR ARCHITECTURE

Shown in Fig. 1.1 is the architecture of the proposed monitor. Light-gray blocks are power supplied directly by positive and/or negative photovoltaic converters. Dark-gray blocks use the supply voltage generated by a voltage booster. The dashed lines show the supply rails connected to these blocks. Voltage divider is a passive block operating without power supply. Notice the presence of two sensors measuring I_{off} in NMOS and PMOS devices. Each generates a pulse train, whose frequency is proportional to the measured value of I_{off} . A selection unit selects one of these pulse trains by closing either SN or SP for transmission by an IR-UWB. Selection is based on whether or not a VLC receiver detects pulse modulation in the incident light.

In dark, all blocks of the monitor are inactive, switch S1 is closed. Incidence of light automatically activates all light-gray blocks. As a result, a ring oscillator powered directly from photodiodes generates two-phase clock signals whose amplitude is equal to $V_{DD1} - V_{SS1}$. These non-overlapping clock signals drive the charge pump (CP) and begin charging the storage capacitors C1 and C2 during the charging phase. Once the voltage level on C1 and C2 reaches a predetermined value, S1 is opened via a level shifter for disconnecting C1 from C2. C1 provides necessary power supply the for level-shifters which are used to convert the photovoltaic signals up to v_{O1} . The reason for separating C1 from C2 during transmission

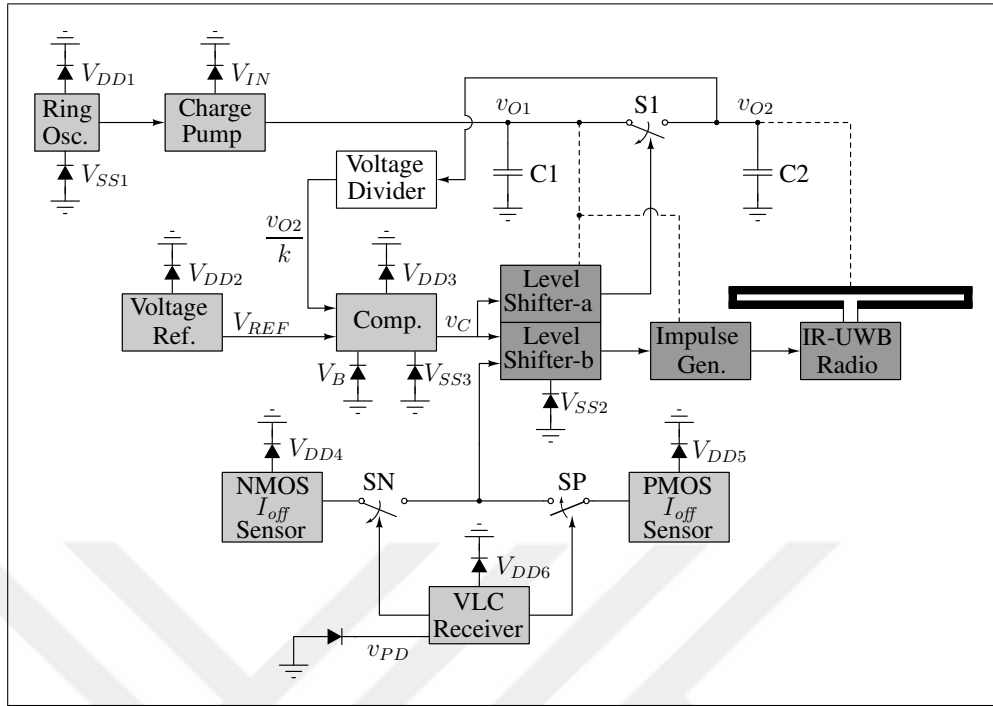


Figure 1.1. Proposed leakage-current monitor architecture.

is to prevent the supply voltage v_{O1} of level shifters and impulse generator from dropping significantly, because the width of the impulses driving the IR-UWB depends strongly on this particular supply voltage. The IR-UWB radio, now driven by the impulse generator, and power-supplied by C2, transmits one impulse for each sensor pulse it receives. The value of I_{off} is thus converted to impulse repetition frequency.

The reference voltage V_{REF} is compared with v_{O2}/k which is a fraction of the voltage on C2. This is why a voltage divider is needed to compare the reference voltage with the downscale copy of v_{O2} . Once v_{O2} decreases down to a predetermined value, radio transmission stops, C1 and C2 are connected in parallel, and the charge storing phase is initiated. One of the two phases which are energy-storage and radio transmission is followed by the other as long as there is sufficient amount of ambient light in the environment.

This work was supported in part by the Scientific and Technological Research Council of Turkey under grant 116E256. The project was completed in 36 months. Design and characterization of the blocks in Figure 1.1 were performed in Chip-1 and Chip-2. Building the fully-integrated form of the proposed monitor was realized in Chip-3.

Chip-1 includes the electrical and physical design of following blocks:

- Photodiode sets.
- Channel-leakage sensor of core MOSFETs in the technology library.
- Discrete replica of each MOSFET of leakage sensor, whose terminals are accessible out of the Chip.
- VLC Receiver.
- Voltage Booster and Storage Capacitors.
- Voltage Reference , Voltage Divider and Comparator.

Chip-2 includes the electrical and physical design of following blocks:

- Level Shifter, Impulse Generator, Transmitter and Antenna unit which is driven by on-chip channel leakage sensors or external signals.
- Independent replicas of units designed in Chip-1 that need revision.

Chip-3 consists of all blocks for verifying the whole system in a fully-integrated form. Design and verification of each chip are presented in their dedicated chapters.

2. DESIGN AND CHARACTERIZATION OF CHIP-1

As stated in Section 1.3, developing the fully integrated form of the proposed architecture has been achieved by taping out three individual chips since a fully experimental characterization of the blocks is needed before putting them together in a whole system.

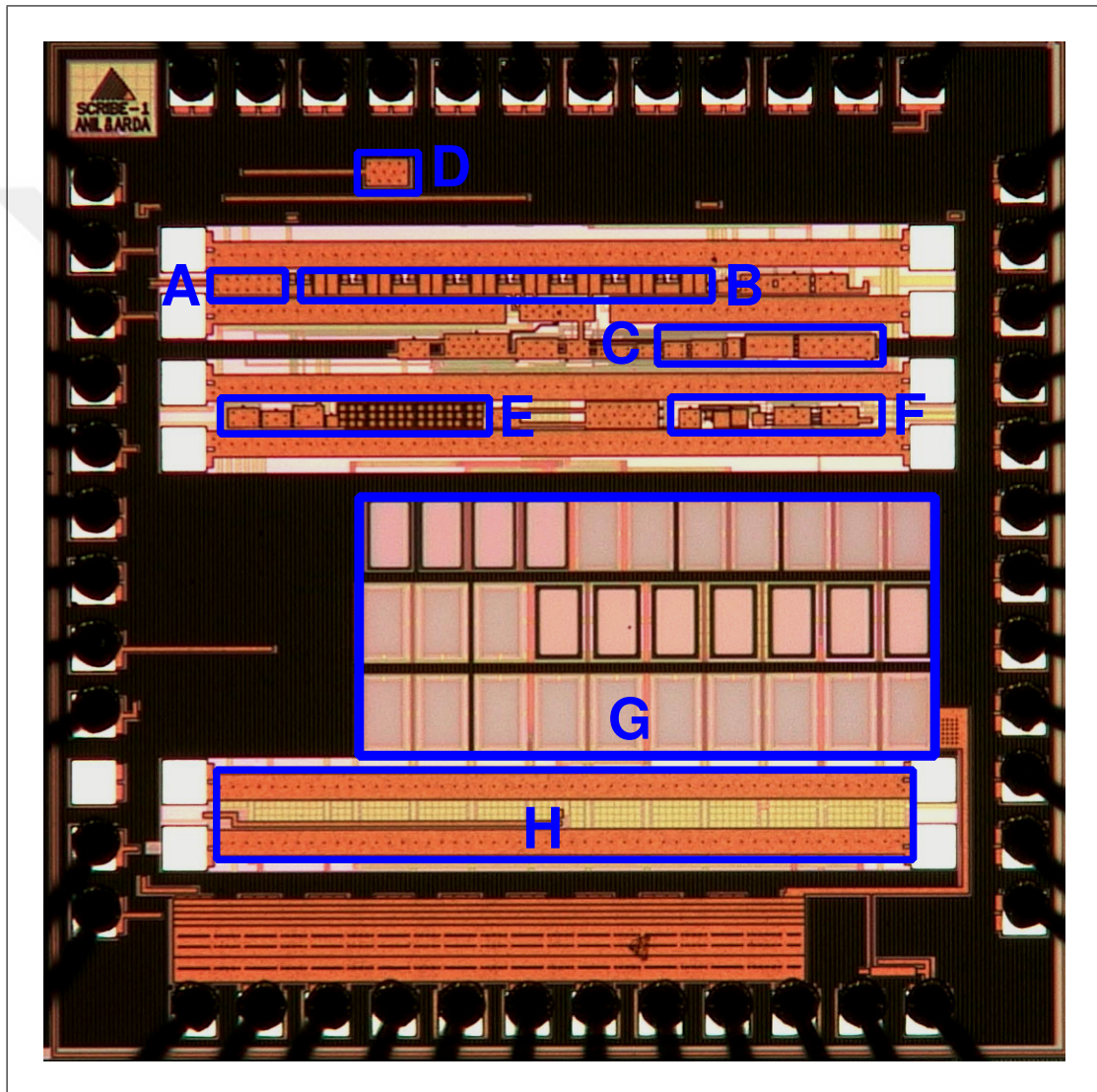


Figure 2.1. Photomicrograph of Chip-1.

This chapter discusses the design and characterization of the blocks that have been taped out in Chip-1. Fig 2.1 shows the photomicrograph of Chip-1 which was fabricated in UMC 0.18 μm CMOS with a footprint of $1525 \times 1525 \mu\text{m}$. Table 2.1 lists the functional blocks which are marked in Fig 2.1.

A block diagram is not provided since the main focus of this tapeout is the silicon validation of individual blocks. Each block is introduced in its dedicated section together with its experimental results.

Table 2.1. Blocks that have been taped out in Chip-1.

A:	Ring oscillator and clock generator
B:	Charge pump
C:	Leakage sensors
D:	Discrete replica of MOS devices
E:	Voltage reference, voltage divider, comparator
F:	VLC receiver
G:	Photovoltaic converters
H:	Storage capacitors

2.1. PHOTOVOLTAIC CONVERTER BLOCKS

Shown in Fig. 2.2 is the cross sectional view of the photovoltaic converters that which harvest energy from indoor illumination. The positive unit is based on a deep n-well (DNW) structure, in which, the p-well (PW) generates the positive supply voltage V_{DD} with respect to an interconnected combination of DNW, n^+ -active and p-substrate. The negative unit relies on a regular n-well (NW) for generating the negative supply voltage V_{SS} with respect to p^+ -active interconnected with p-substrate.

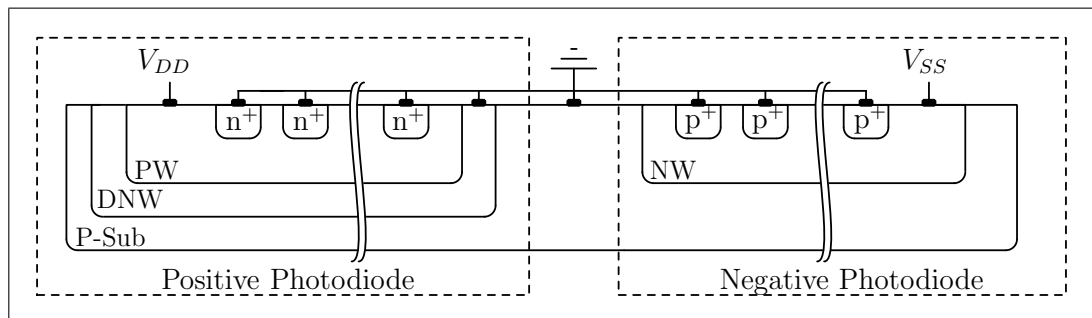


Figure 2.2. Cross-sectional view of photovoltaic converters.

Since the proposed leakage monitor is aimed to be operated with unregulated photovoltaic power supply, the current-voltage characteristics of positive and negative photovoltaic converters should be well-defined. Fig 2.3 shows the equivalent circuit which represents a loaded positive photovoltaic converter. I_{diode} defines the diode current of the photovoltaic converter whereas I_{photo} defines the photo-generated current.

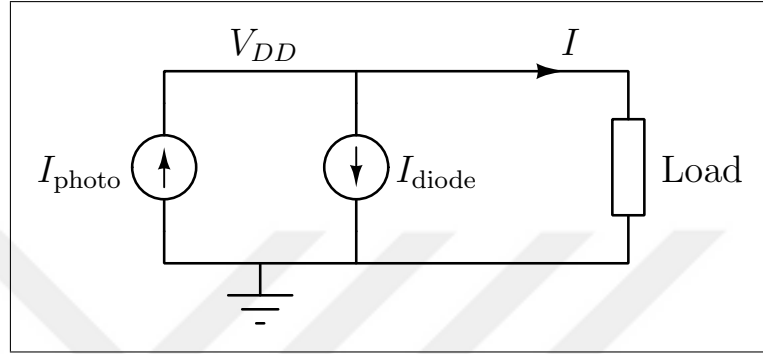


Figure 2.3. Equivalent circuit of loaded positive photovoltaic converter.

The current flowing through the load is written as

$$I = I_{\text{photo}} - I_{\text{diode}} \quad (2.1)$$

Photo-generated current is defined as

$$I_{\text{photo}} = \Gamma \cdot E \quad (2.2)$$

where Γ ($\text{nA} \cdot \text{cm}^2/\text{W}$) is the current per unit irradiance and E (W/cm^2) is the irradiance. Diode current I_{diode} is defined as

$$I_{\text{diode}} = I_{OJP} \cdot 10^{\left(\frac{V_{DD}}{S_{JP}}\right)} \quad (2.3)$$

where I_{OJP} defines the equivalent dark current which flows through the diode when its terminals are shorted in a dark environment. V_{DD} and S_{JP} are the voltage across the terminals of the diode and the slope factor respectively. Using (2.2) and (2.3) in (2.1), power-

supply port characteristics of the positive photovoltaic converter is obtained as

$$I = \Gamma \cdot E - I_{OJP} \cdot 10^{\left(\frac{V_{DD}}{S_{JP}}\right)} \quad (2.4)$$

Positive photovoltaic converters are assembled by paralleling multiple $60 \mu\text{m} \times 100 \mu\text{m}$ photodiode units. Experimental current-voltage characteristics of a single photodiode unit under $1 \text{ mW}/\text{cm}^2$ D65 irradiance, is shown in Fig. 2.4. Also plotted is the equation (2.4) which models the power-supply port characteristics of the photovoltaic converter. The extracted values of equation (2.4) are found as: $\Gamma = 10.5 \text{ nA} \cdot \text{cm}^2/\text{mW}$, $I_{OJP} = 5 \text{ fA}$ and $S_{JP} = 65 \text{ mV}/\text{decade}$.

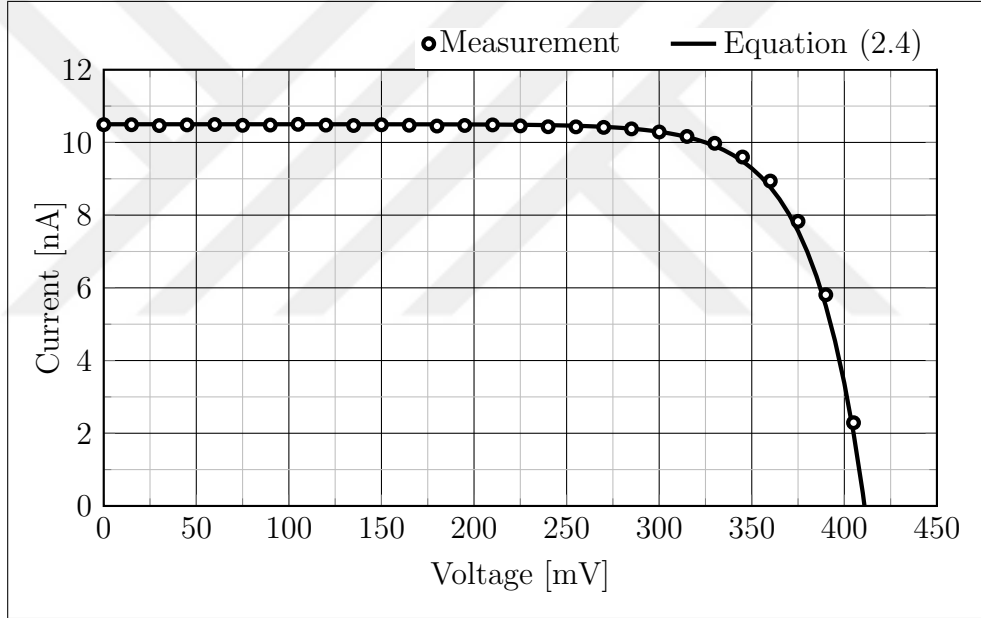


Figure 2.4. Measured current-voltage curve of positive photovoltaic converter.

Fig. 2.5 shows the equivalent circuit which represents a loaded negative photovoltaic converter. I_{diode} defines the diode current of the photovoltaic converter whereas I_{photo} defines the photo-generated current. The current flowing through the load and the photo-generated current can still be defined using (2.1) and (2.2) respectively. Diode current I_{diode} is defined as

$$I_{\text{diode}} = I_{OJN} \cdot 10^{\left(\frac{-V_{SS}}{S_{JN}}\right)} \quad (2.5)$$

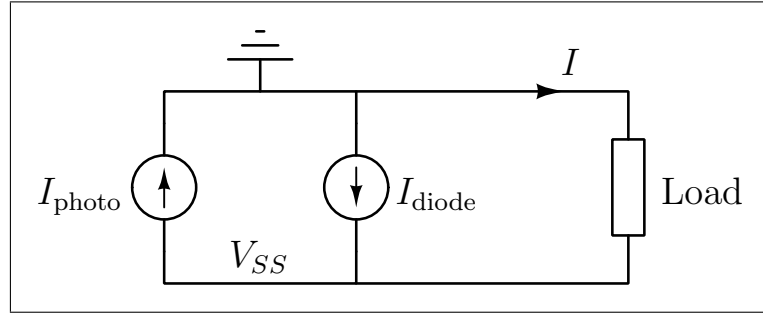


Figure 2.5. Equivalent circuit of loaded negative photovoltaic converter.

where I_{OJN} defines the equivalent dark current which flows through the diode when its terminals are shorted in a dark environment. V_{SS} and S_{JN} are the voltage across the terminals of the diode and the slope factor respectively. Using (2.2) and (2.5) in (2.1), power-supply port characteristics of the negative photovoltaic converter is obtained as

$$I = \Gamma \cdot E - I_{OJN} \cdot 10^{\left(\frac{-V_{SS}}{S_{JN}}\right)} \quad (2.6)$$

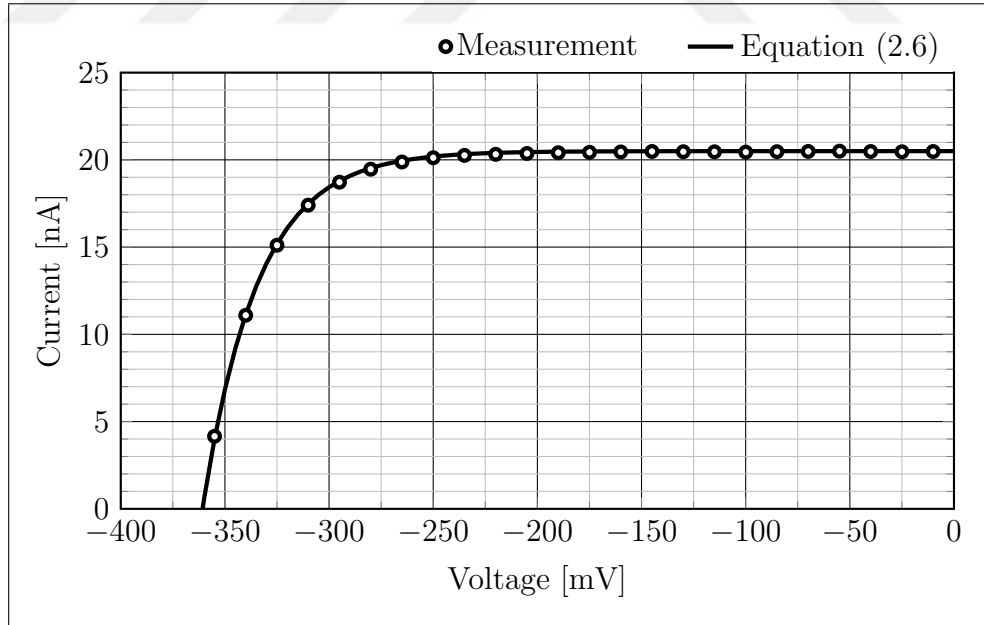


Figure 2.6. Measured current-voltage curve of negative photovoltaic converter.

Negative photovoltaic converters are assembled by paralleling multiple $60 \mu\text{m} \times 100 \mu\text{m}$ photodiode units. Experimental current-voltage characteristics of a single photodiode unit under 1 mW/cm^2 D65 irradiance, is shown in Fig. 2.6. Also plotted is the equation (2.6)

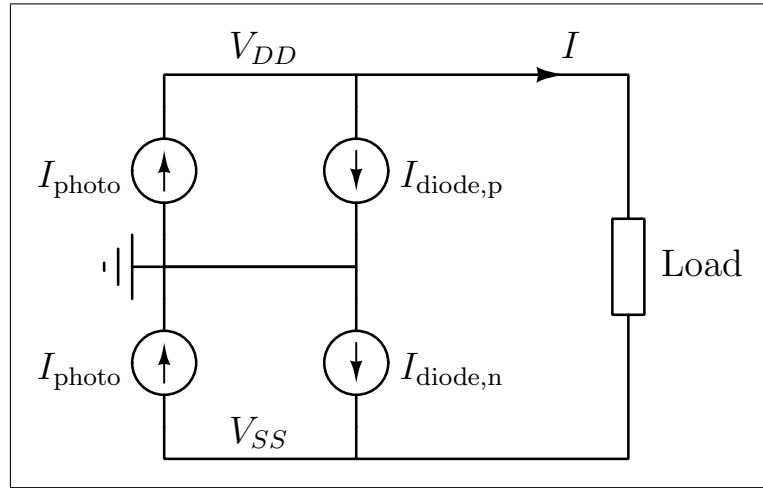


Figure 2.7. Dual-supply configuration.

which models the power-supply port characteristics of the photovoltaic converter. The extracted values of equation (2.6) are found as: $\Gamma = 20.5 \text{ nA} \cdot \text{cm}^2/\text{mW}$, $I_{OJN} = 25 \text{ fA}$ and $S_{JN} = 61 \text{ mV/decade}$. The apparent disparity between the short-circuit currents necessitates the assembly of twice as many positive units as negative ones in order to establish a balanced dual-supply power scheme.

Shown in Fig. 2.7 is the equivalent circuit of a load operating with dual-supply configuration. If the short-circuit currents of positive and negative photovoltaic converters are equalized by proper selection of number of photodiodes, the port characteristics of the dual-supply configuration is given by

$$I = I_{photo,eq} - I_{diode,eq} \quad (2.7)$$

where $I_{photo,eq}$ and $I_{diode,eq}$ define the equivalent photo-generated current and equivalent diode current respectively. Considering the short-circuit current of positive and negative photovoltaic converters are equalized by proper selection of number of photodiodes, $I_{photo,eq}$ is equal to I_{photo} . Equivalent diode current $I_{diode,eq}$ is described by

$$I_{diode,eq} = I_{OJ} \cdot 10^{\left(\frac{V_{DD}-V_{SS}}{S_J}\right)} \quad (2.8)$$

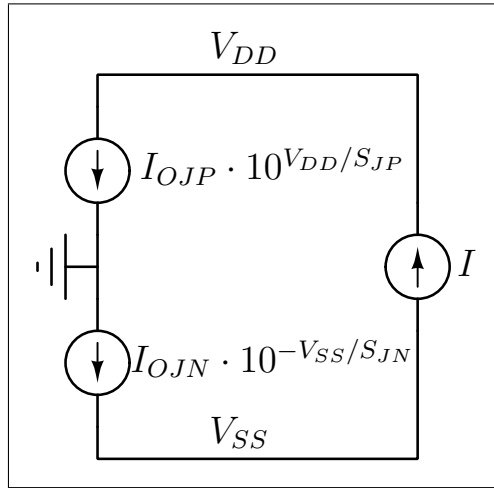


Figure 2.8. Extraction of equivalent slope parameter.

where I_{OJ} and S_J represent the equivalent dark-current and equivalent slope factor respectively. The expression of S_J in terms of S_{JN} and S_{JP} can be derived using the circuit shown in Fig. 2.8.

The circuit shown in Fig. 2.8, considers the situation when there is no illumination; hence not photo-generated current. The dual supply converter is loaded with an ideal current source whose current is given by

$$I = I_{OJP} \cdot 10^{\left(\frac{V_{DD}}{S_{JP}}\right)} = I_{OJN} \cdot 10^{\left(\frac{-V_{SS}}{S_{JN}}\right)} \quad (2.9)$$

If the amount of current is increased by a factor of ten, equation (2.9) is modified as

$$I \cdot 10 = I_{OJP} \cdot 10^{\left(\frac{V_{DD}+S_{JP}}{S_{JP}}\right)} = I_{OJN} \cdot 10^{\left(\frac{-(V_{SS}-S_{JN})}{S_{JN}}\right)} \quad (2.10)$$

When equation (2.9) and (2.10) are compared, the voltage between positive and negative rail is increased by $S_{JP} + S_{JN}$. The equivalent slope factor, therefore, is defined by

$$S_J = S_{JP} + S_{JN} \quad (2.11)$$

The expression of I_{OJ} in terms of I_{OJP} and I_{OJN} can be derived using the circuit shown

in Fig. 2.9 which considers the situation when there is no illumination; hence not photo-generated current. The ports of dual supply converter is shorted and the voltage of the new common terminal is defined as V_X . Since the diode current of positive and negative

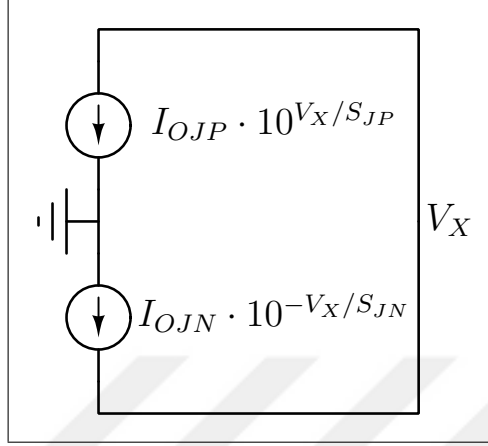


Figure 2.9. Extraction of equivalent dark current.

photodiode should be equal, V_X is found as

$$V_X = \frac{\log\left(\frac{I_{OJN}}{I_{OJP}}\right)}{\frac{1}{S_{JP}} + \frac{1}{S_{JN}}} \quad (2.12)$$

Using equation (2.12) in diode current of either positive or negative photodiode yields the equivalent dark current as

$$I_{OJ} = I_{OJP}^{\frac{S_{JP}}{S_{JP}+S_{JN}}} \cdot I_{OJN}^{\frac{S_{JN}}{S_{JP}+S_{JN}}} \quad (2.13)$$

Using (2.2), (2.11) and (2.13) in (2.7) gives the complete expression of dual supply converter port characteristics which is written as

$$I = \Gamma \cdot E - I_{OJP}^{\frac{S_{JP}}{S_{JP}+S_{JN}}} \cdot I_{OJN}^{\frac{S_{JN}}{S_{JP}+S_{JN}}} \cdot 10^{\left(\frac{V_{DD}-V_{SS}}{S_{JP}+S_{JN}}\right)} \quad (2.14)$$

Using the extracted values of the terms in (2.14), current-voltage characteristics of a dual supply converter under 1 mW/cm² D65 irradiance is plotted with a solid line in Fig. 2.10. As compared to the single supply converter, dual supply converter has nearly twice as much as open-circuit voltage which provides more headroom for the analog circuits and increases the

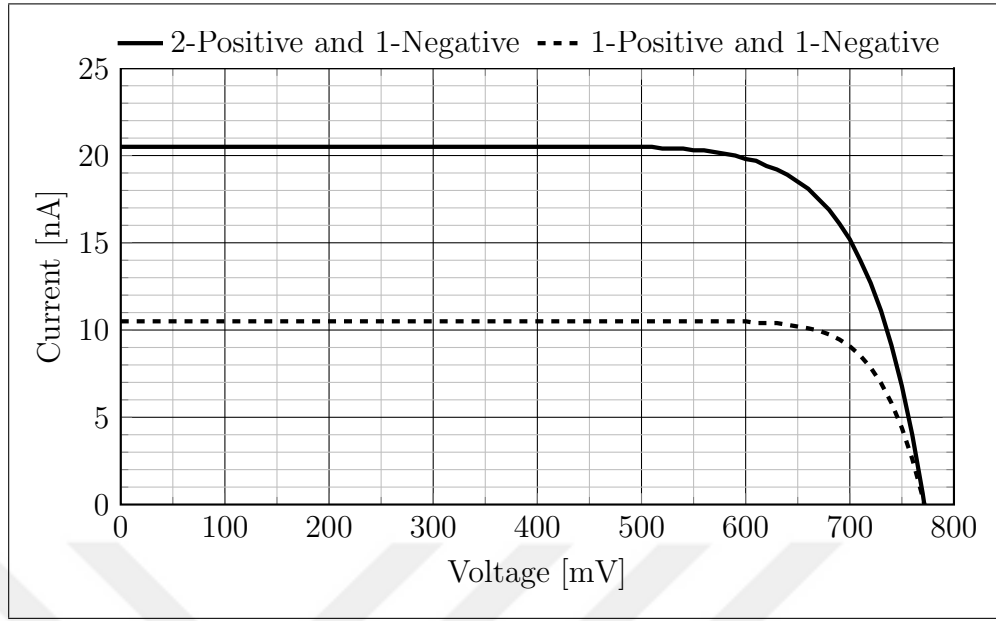


Figure 2.10. Current-voltage curve dual supply converter.

rate function of the charge pump [34]. Also plotted with a dashed line is the current-voltage characteristics of a dual supply converter with unbalanced power scheme using one positive and one negative photovoltaic converters. Having the identical open circuit voltage with the balanced configuration, its short-circuit current, however, is determined by the photovoltaic converter with lower short-circuit current.

2.2. CHANNEL LEAKAGE SENSOR BLOCKS

As depicted in the literature survey, conventional leakage sensors have a weak conversion linearity between channel-leakage and frequency due to being affected other uncertain parameters rather than the MOSFET-under-test. In addition to be powered by an unregulated photovoltaic voltage source with nanowatt-scale power level, the proposed leakage sensor has been aimed to have an improved conversion linearity between channel leakage and frequency by being unaffected by any other uncertain parameter. Before introducing the proposed sensor topology, an analytical model of the conventional leakage sensor has been developed and compared with simulation results in subsection 2.2.1.

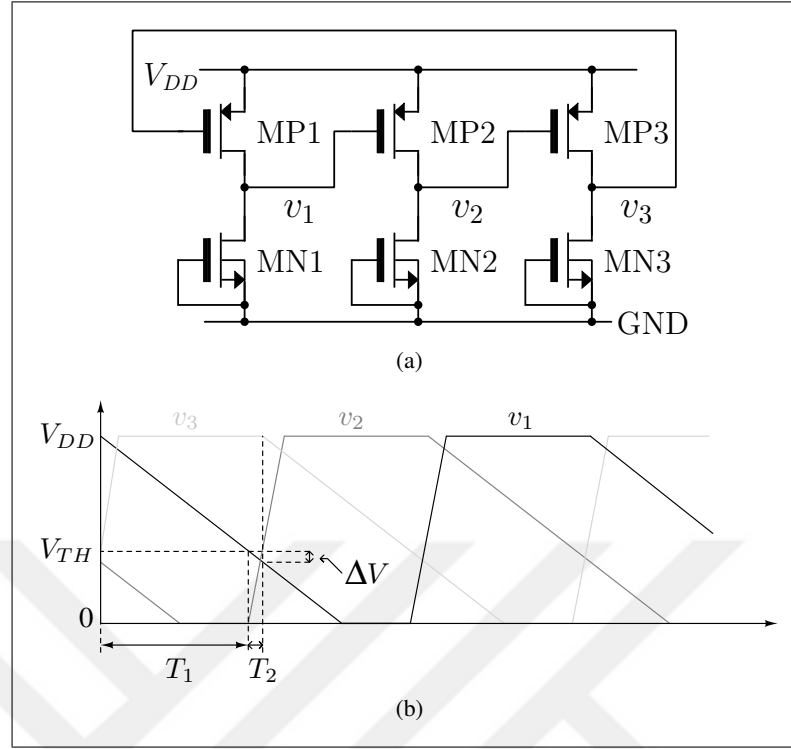


Figure 2.11. Conventional leakage sensor: (a) Schematic. (b) Voltage waveforms.

2.2.1. Conventional Channel Leakage Sensor

The conventional leakage sensor in [33] built with 127 stages and 1270 devices is simplified as a 3 stage ring-oscillator as shown in Fig. 2.11(a). The driver devices are PMOS and the load devices are m replica of NMOS devices. NMOS devices are operating with gate-source short since the leakage current to be measured is of NMOS devices in this configuration. The abstract waveform of each node voltage is shown in Fig. 2.11(b).

Oscillation frequency of the conventional sensor is the summation of three T_1 and three T_2 durations since the oscillator has three stages. T_1 is the time required for the parasitic capacitance on v_1 to discharge over m replicas of MN1. Since MP1 is at cut-off in the beginning of that discharge phase, only I_{offp} flows through the device. Therefore the net current is the difference between the devices MN1 and MP1 respectively. Assuming each node has equal parasitic capacitance of C , T_1 is found as

$$T_1 = C \cdot \frac{V_{DD} - V_{TH}}{m \cdot I_{offn} - I_{offp}} \quad (2.15)$$

T_2 is the time needed for v_2 to reach the logic threshold V_{TH} . But the gate voltage on MP2 that charges the parasitic capacitance on v_2 , is time-dependent. The current of MN2 can be ignored since it is too small compared to the leakage current of MP2. The current of MP2 is defined as

$$I_{MP2} = I_{offp} \cdot \exp \left[\frac{\frac{-q}{kT} \cdot (V_{DD} - v_1)}{\eta_p} \right] \quad (2.16)$$

where η_p is the sub-threshold slope of the PMOS device. v_1 is defined as

$$v_1(t) = \frac{I_{offp} - m \cdot I_{offn}}{C} \cdot t + V_{DD} \quad (2.17)$$

Defining T_2 as the time for v_2 to reach the logic threshold value is evaluated as

$$\int_{T_1}^{T_1+T_2} I_{offp} \cdot \exp \left[\frac{\frac{-q}{kT} \cdot \left(\frac{I_{offp} - m \cdot I_{offn}}{C} \cdot t \right)}{\eta_p} \right] \cdot dt = \int_0^{V_{TH}} C \cdot dv \quad (2.18)$$

The logic threshold value V_{TH} is defined where $I_{MPx} = m \cdot I_{MNx}$. It is therefore defined as

$$V_{TH} = V_{DD} - \frac{kT}{q} \cdot \eta_p \cdot \ln \left(\frac{m \cdot I_{offn}}{I_{offp}} \right) \quad (2.19)$$

Using (2.18) and (2.19), T_2 is found as

$$T_2 = \frac{kT}{q} \cdot \frac{\eta_p \cdot C}{m \cdot I_{offn} - I_{offp}} \cdot \ln \left[1 + \frac{q}{kT} \cdot \frac{V_{DD}}{\eta_p} - \ln \left(\frac{m \cdot I_{offn}}{I_{offp}} \right) \right] \quad (2.20)$$

Using (2.15) and (2.20), oscillation frequency of the conventional leakage sensor is found as

$$f = \frac{1}{3 \cdot (T_1 + T_2)} = \frac{m \cdot I_{offn} - I_{offp}}{\frac{kT}{q} \cdot 3 \cdot C \cdot \eta_p \cdot \ln \left\{ \frac{m \cdot I_{offn}}{I_{offp}} \cdot \left[1 + \frac{V_{DD}}{\eta_p \cdot \frac{kT}{q}} - \ln \left(\frac{m \cdot I_{offn}}{I_{offp}} \right) \right] \right\}} \quad (2.21)$$

In the case of a PMOS test, gate of the PMOS device is shorted to its source and the feedback is applied to the gate of NMOS device. Oscillation frequency is still defined by (2.21) with replacing n and p indices. $I_{offp} < m \cdot I_{offn}$ criteria for NMOS sensor and $I_{offn} < m \cdot I_{offp}$

capacitance seen from the gate of MP2. Each capacitance has both extrinsic and intrinsic components. SPICE calculates these components from

$$C_{dd_{MP1}} = C_{ddi_{MP1}} + W \cdot CGDO + \left[\frac{A_D \times CJ}{\left(1 + \frac{|V_{DB}|}{PB}\right)^{MJ}} + \frac{(P_D - W) \times CJSW}{\left(1 + \frac{|V_{DB}|}{PBSW}\right)^{MJSW}} + \frac{W \times CJSWG}{\left(1 + \frac{|V_{DB}|}{PBSWG}\right)^{MJSWG}} \right] \quad (2.22)$$

$$C_{dd_{MP2}} = C_{ddi_{MP2}} + W \cdot CGDO + \left[\frac{A_D \times CJ}{\left(1 + \frac{|V_{DB}|}{PB}\right)^{MJ}} + \frac{(P_D - W) \times CJSW}{\left(1 + \frac{|V_{DB}|}{PBSW}\right)^{MJSW}} + \frac{W \times CJSWG}{\left(1 + \frac{|V_{DB}|}{PBSWG}\right)^{MJSWG}} \right] \cdot m \quad (2.23)$$

$$C_{gg_{MP2}} = C_{ggi} + W \cdot (CGSO + CGDO) + L \cdot +CGBO \quad (2.24)$$

Input gate voltage V_I is swept between 0 V and V_{DD} to plot the bias dependency of node capacitance C . Taking its average yields $C = 35.4$ fF of capacitance is loading the each node of the ring oscillator.

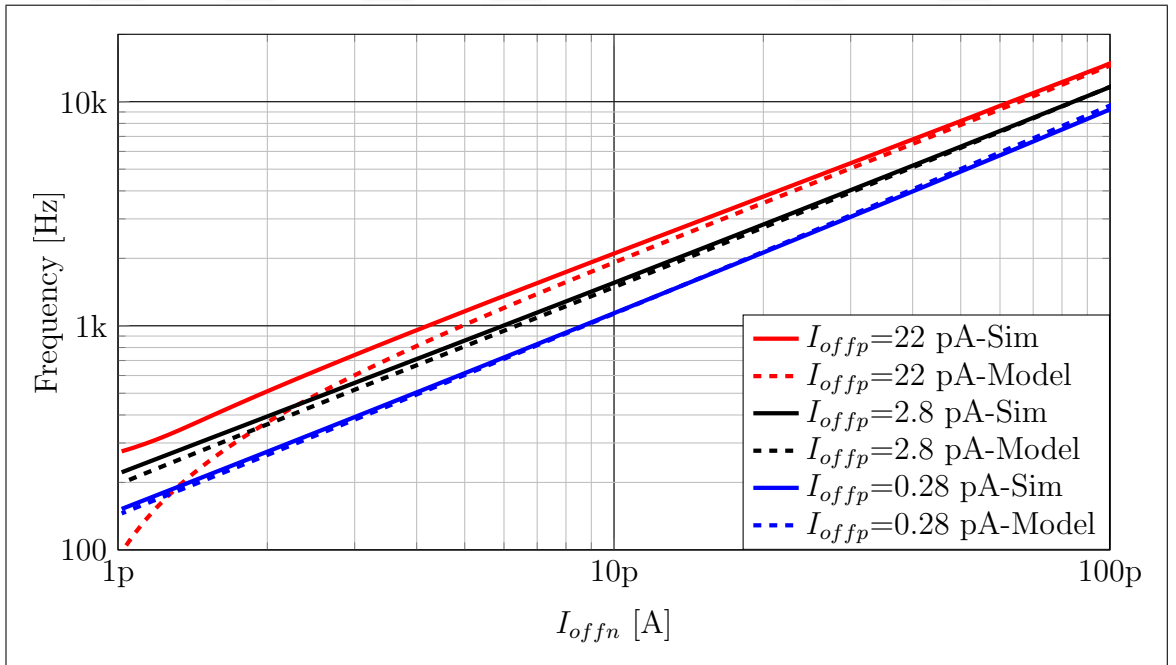


Figure 2.13. Oscillation frequency as a function of leakage currents.

Sub-threshold slope η_p is extracted by plotting the transfer characteristics of a core PMOS device of $L = 0.2 \mu\text{m}$ and $W = 0.5 \mu\text{m}$ with $|V_{DS}| = V_{DD}$. Its value is found as 1.51.

The nominal value of I_{offn} and I_{offp} is extracted with simulation using core PMOS and core NMOS devices of $L = 0.2 \mu\text{m}$ and $W = 0.5 \mu\text{m}$ with $V_{GS} = 0 \text{ V}$ and $|V_{DS}| = V_{DD}$. Their values are $I_{offn} = 10.14 \text{ pA}$ and $I_{offp} = 2.78 \text{ pA}$. Using (2.21), oscillation frequency of the leakage sensor is plotted against two orders of magnitude change in nominal value of I_{offn} and I_{offp} and shown in Fig. 2.13. Also plotted is the oscillation frequency which is extracted with simulation. The model presented in (2.21) exhibits good agreement with the simulation when the criteria $I_{offp} < m \cdot I_{offn}$ is satisfied. When I_{offp} approaches $m \cdot I_{offn}$, however, a mismatch is observed between analytical model and simulation as can be seen in $I_{offp} = 22 \text{ pA}$ and $I_{offn} = 1 \text{ pA}$ corner. Besides, either modeled, or simulated curves exhibit a relative shift between 34 percent and 50 percent against one decade change in I_{offp} . This concludes that the conventional leakage sensors exhibit a high uncertainty of I_{offn} corresponding to a measured frequency.

Another result obtained with the simulation is the weak linearity of the conventional leakage sensor. Regression analysis applied to $I_{offp} = 2.78 \text{ pA}$ trace reveals the correlation between the frequency and leakage as $f \propto I_{offn}^{0.8}$ which is below $f \propto I_{offn}^{0.88}$, the correlation of the same curve predicted by (2.21).

2.2.2. Proposed Channel Leakage Sensor

A radical solution to uncertainty and linearity problems of the conventional leakage sensor is to build the ring oscillator with NMOS-only or PMOS-only inverters. Shown in Fig. 2.14(a) is the electrical schematic of such an NMOS ring oscillator utilized this work. It contains three identical inverter stages, each comprising a load device marked ML1, ML2, or ML3, and a driver device marked MD1, MD2, or MD3. All devices are equipped with source-bulk shorts for the purpose of eliminating the body effect, but this comes at the expense of DNW-type load devices. Also short circuited in load devices are the gate-source ports. As to device sizing, each driver consists of one unit MOSFET of channel leakage I_{off} , whereas each load device comprises m parallel copies of the same unit MOSFET, and therefore exhibits a channel leakage mI_{off} .

Typical output voltage waveforms of the NMOS sensor, as obtained with simulation, are

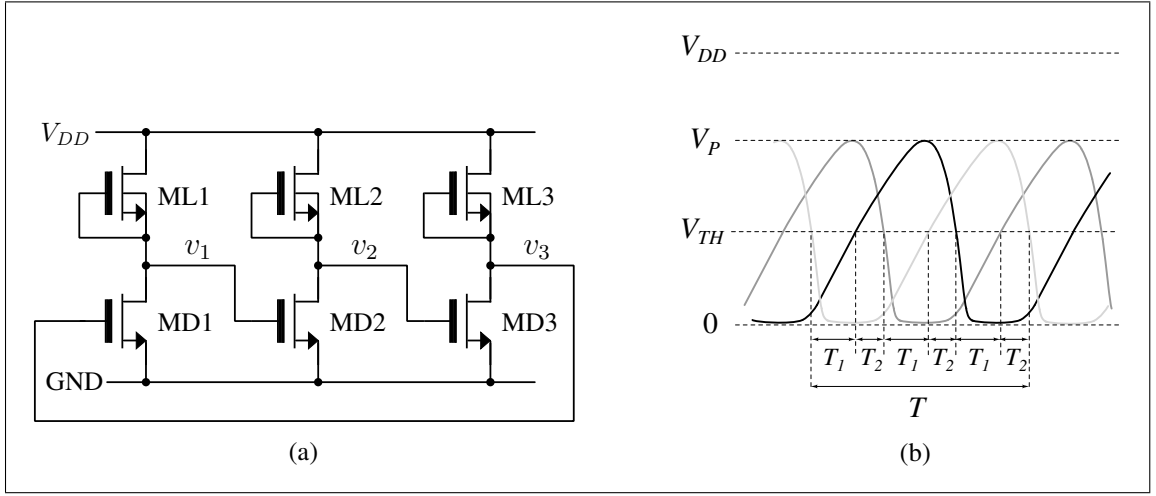


Figure 2.14. Proposed leakage sensor: (a) Schematic. (b) Voltage waveforms.

shown in Fig. 2.14(b). Voltage waveforms are clamped to ground but their swing is not rail to rail. This is how the oscillation frequency is desensitized to the unregulated V_{DD} . Similar to the conventional leakage sensor analysis, logic threshold V_{TH} is defined where the load device current $m \cdot I_{offn}$ is equal to the driver current I_n . Defining the driver current as

$$I_n = I_{offn} \cdot \exp\left(\frac{\frac{q}{kT} \cdot V_{GS}}{\eta_n}\right) \quad (2.25)$$

Logic threshold V_{TH} is found by equating the driver and the load device current that is

$$m \cdot I_{offn} = I_{offn} \cdot \exp\left(\frac{\frac{q}{kT} \cdot V_{TH}}{\eta_n}\right) \quad (2.26)$$

$$V_{TH} = \frac{kT}{q} \cdot \eta_n \cdot \ln(m) \quad (2.27)$$

Unlike the conventional leakage sensor, the logic threshold voltage V_{TH} of the proposed leakage sensor is independent of supply voltage and leakage currents.

Oscillation frequency is equal to the summation of three T_1 and three T_2 durations since the oscillator has three stages. T_1 is the time required for the parasitic capacitance on v_1 to charge over m replicas of ML1 until v_1 reaches the logic threshold value V_{TH} . During that phase, only I_{offn} flows through MD1 since it is at cut-off. Net current, therefore, is the

difference between the currents flowing through ML1 and MD1. Assuming each node has equal parasitic capacitance of C , T_1 is found as

$$T_1 = \frac{C \cdot V_{TH}}{(m-1) \cdot I_{offn}} = \frac{C \cdot \frac{kT}{q} \cdot \eta_n \cdot \ln(m)}{(m-1) \cdot I_{offn}} \quad (2.28)$$

where η_n is the sub-threshold slope of the driver device. T_2 is the time needed for v_2 to reach the logic threshold V_{TH} . But the gate voltage of MD2 is time-dependent. Since the current on MD2 is much greater than the leakage current of M12, that leakage might be neglected. Based on these considerations, T_2 is found as

$$-\int_{T_1}^{T_1+T_2} I_{offn} \cdot \exp\left[\frac{q}{kT} \cdot \frac{(m-1) \cdot I_{offn}}{C \cdot \eta_n}\right] \cdot dt = \int_{V_P}^{V_{TH}} C \cdot dv \quad (2.29)$$

$$T_2 = \frac{kT}{q} \cdot \frac{C \cdot \eta_n}{(m-1) \cdot I_{offn}} \cdot \ln\left[\frac{m-1}{m} \cdot \frac{V_P - V_{TH}}{\eta_n} \cdot \frac{q}{kT} + 1\right] \quad (2.30)$$

where the peak voltage V_P is defined as:

$$V_P = V_{TH} + \frac{kT}{q} \cdot \ln\left[\frac{m-1}{m} \cdot \frac{V_P - V_{TH}}{\eta_n} \cdot \frac{q}{kT} + 1\right] \quad (2.31)$$

Being on left and right-hand side within an logarithmic expression, V_P is found by selecting a proper value for m and iterating. Iteration for $m = 21$ yields

$$V_P = 2.567 \cdot V_{TH} \quad (2.32)$$

Oscillation frequency of the proposed leakage sensor is found using (2.28), (2.30) and (2.32) as

$$f = \frac{q}{kT} \cdot \frac{(m-1) \cdot I_{offn}}{3 \cdot C \cdot \eta_n} \cdot \frac{1}{\ln[1.567 \cdot (m-1) \cdot \ln(m) + m]} \quad (2.33)$$

The circuit schematic and simulated waveforms of the PMOS-only version of the proposed leakage sensor are shown in Fig. 2.15. Qualitatively, there is no difference between the two

versions with the exception that the waveforms of the PMOS version are clamped to V_{DD} . Therefore, a proper selection of m still ensures a supply-independent swing. Oscillation frequency is still defined by (2.33) with replacing n and p indices.

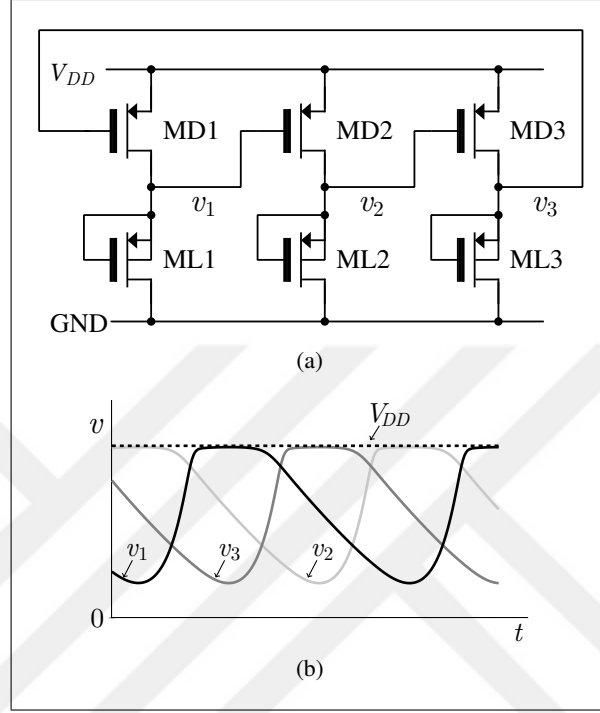


Figure 2.15. PMOS leakage sensor: (a) Schematic. (b) Voltage waveforms.

As compared to Equation (2.21), Equation (2.33) predicts a linear relationship between oscillation frequency and channel leakage of test device. It is also evident that the oscillation frequency is sensitive only to the parameters of NMOS devices under test which eliminates the uncertainty of channel leakage corresponding to a measured frequency. A simulation test-bench has been set for verifying the validity (2.33). A three-stage NMOS-only ring oscillator is built with core NMOS devices of $L = 0.2 \mu\text{m}$ and $W = 0.5 \mu\text{m}$. The number of segments of test device m is selected as 21. V_{DD} is set to 415 mV using (2.4) assuming one-unit $60 \mu\text{m} \times 100 \mu\text{m}$ photodiode under 1 mW/cm^2 D65 irradiance.

Shown in Fig. 2.16 is the circuit for extracting the node capacitance C . The total capacitance is the sum of the capacitances seen from the drain of MD1, m replicas of ML1, and the capacitance seen from the gate of MD2. Each capacitance has both extrinsic and intrinsic

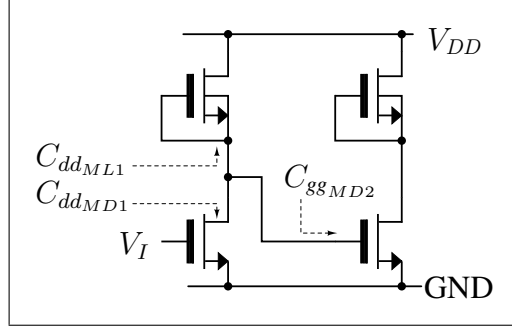


Figure 2.16. Node capacitance extraction.

components. SPICE calculates these components from

$$C_{dd_{MD1}} = C_{ddi_{ML1}} + W \cdot CGDO + \left[\frac{A_D \times CJ}{\left(1 + \frac{|V_{DB}|}{PB}\right)^{MJ}} + \frac{(P_D - W) \times CJ_{SW}}{\left(1 + \frac{|V_{DB}|}{PBSW}\right)^{MJ_{SW}}} + \frac{W \times CJ_{SWG}}{\left(1 + \frac{|V_{DB}|}{PBSWG}\right)^{MJ_{SWG}}} \right] \quad (2.34)$$

$$C_{dd_{ML1}} = C_{ddi_{MP2}} + W \cdot CGDO + \left[\frac{A_D \times CJ}{\left(1 + \frac{|V_{DB}|}{PB}\right)^{MJ}} + \frac{(P_D - W) \times CJ_{SW}}{\left(1 + \frac{|V_{DB}|}{PBSW}\right)^{MJ_{SW}}} + \frac{W \times CJ_{SWG}}{\left(1 + \frac{|V_{DB}|}{PBSWG}\right)^{MJ_{SWG}}} \right] \cdot m \quad (2.35)$$

$$C_{gg_{MD2}} = C_{ggi} + W \cdot (CGSO + CGDO) + L \cdot CGBO \quad (2.36)$$

Input gate voltage V_I is swept between 0 V and V_{DD} to plot the bias dependency of node capacitance C . Taking its average yields $C = 24.4$ fF of capacitance is loading the each node of the ring oscillator.

Sub-threshold slope η_n and the nominal value of I_{offn} are extracted by plotting the transfer characteristics of a core NMOS device of $L = 0.2 \mu\text{m}$ and $W = 0.5 \mu\text{m}$ with $V_{DS} = V_{DD}$. Their values are $\eta_n = 1.41$ and $I_{offn} = 10.14$ pA. Using (2.33), oscillation frequency of the proposed NMOS-only leakage sensor is plotted against two orders of magnitude change in nominal value of I_{offn} and shown in Fig. 2.17. Also plotted is the oscillation frequency which is extracted with simulation.

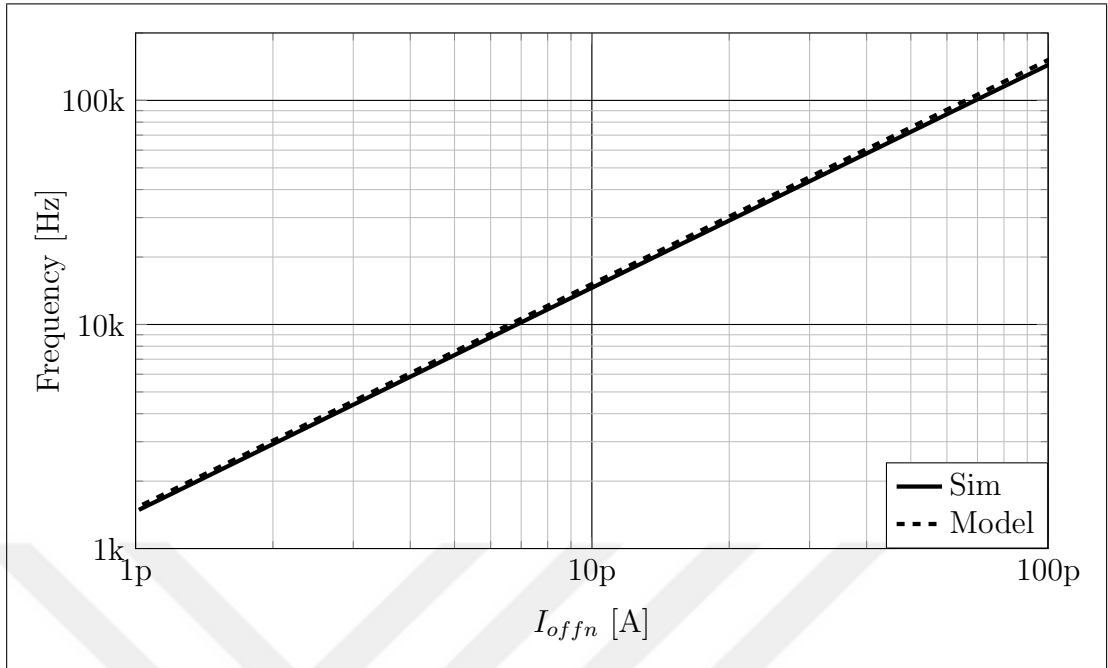


Figure 2.17. Oscillation frequency as a function of channel leakage.

The model presented in (2.33) exhibits good agreement with the simulation against two orders of magnitude change in nominal value of I_{offn} . Sub-threshold slope η_n may exhibit imprecision but its distribution is definitely much narrower than that of channel leakage. The proposed sensor, therefore, eliminates the measurement uncertainty by removing other parameters rather than the MOSFET-under-test.

Another result obtained with the simulation is the improved linearity of the proposed leakage sensor. Regression analysis reveals the correlation between the frequency and leakage as $f \propto I_{offn}^{0.93}$ which is greater than the regression analysis result of the simulated conventional channel leakage sensor.

Sensitivity of f to V_{DD} , hence the irradiance has also been simulated using the proposed leakage sensor built with core NMOS devices of $L = 0.2 \mu\text{m}$ and $W = 0.5 \mu\text{m}$. The number of segments of test device m is selected as 21. V_{DD} is supplied using the model (2.4) between $100 \mu\text{W}/\text{cm}^2$ and $10 \text{ mW}/\text{cm}^2$ of D65 irradiance levels. Shown in Fig. 2.18(a) is the variation of V_{DD} with irradiance. It exhibits 20.7 percent relative sensitivity per decade around $E = 1 \text{ mW}/\text{cm}^2$. Shown in Fig. 2.18(b) is the variation of f with irradiance. It exhibits 4.3 percent

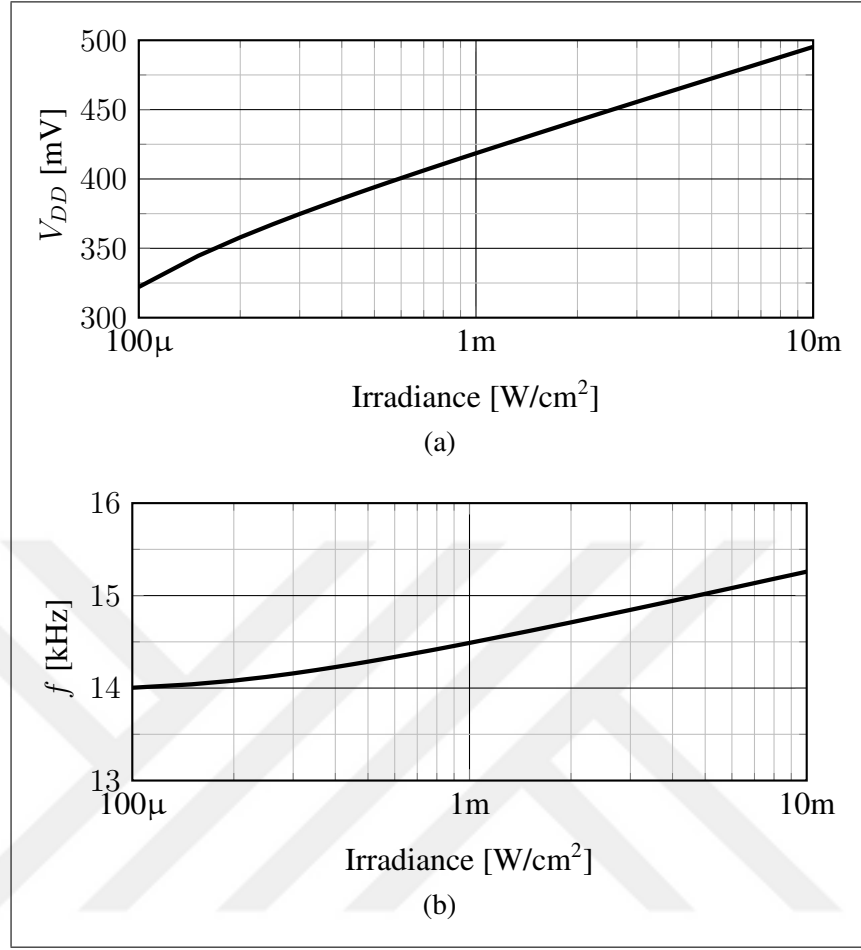


Figure 2.18. Irradiance sensitivity: (a) V_{DD} vs. irradiance. (b) f vs. irradiance.

relative sensitivity per decade around $E = 1 \text{ mW/cm}^2$. Considering the environment where the scribe tests are performed, the variation of irradiance is far below 1 decade. Proposed sensor, therefore, is apparently capable of being powered with photovoltaic converter directly without any regulation.

The linear relationship predicted between f and I_{off} was tested on PMOS and NMOS sensors of different samples of Chip-1. The experimental sensors of Chip-1 are based on core devices of $L = 0.18 \mu\text{m}$, $W = 0.5 \mu\text{m}$, and $m = 21$. Shown in Fig. 2.19(a) is the measurement setup built for NMOS leakage sensor oscillation frequency readout. The output of the sensor is connected to a tapered buffer which is powered from off-chip supply. $V_{DD,ext}$ and $V_{SS,ext}$ are set to 0.4 V and -0.3 V respectively for emulating the photovoltaic level binary signals to be monitored in the chip. The reason for using tapered buffer is to drive

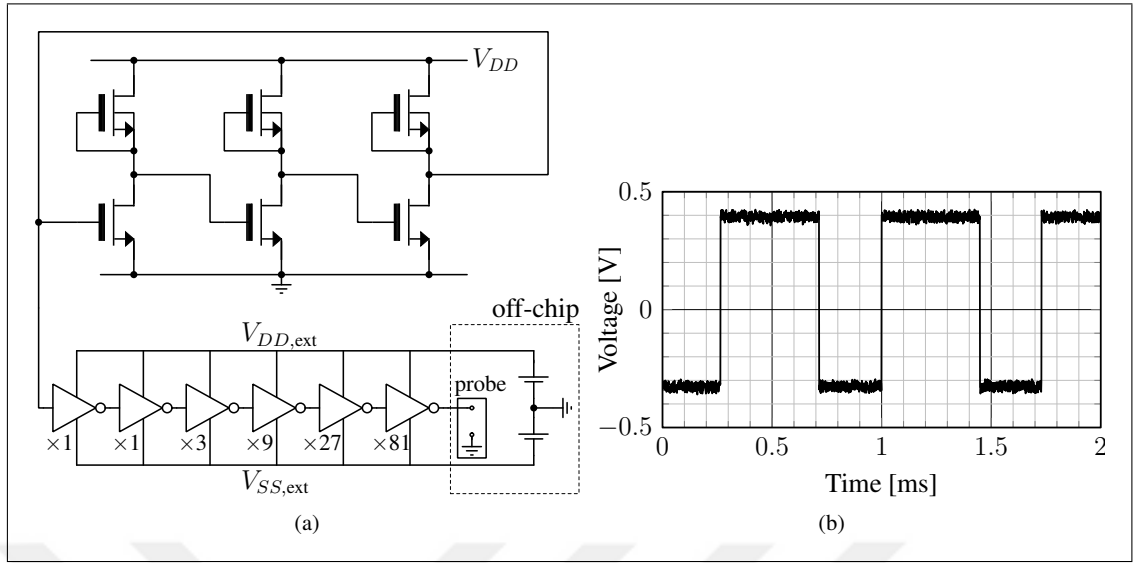


Figure 2.19. (a) Measurement setup for f . (b) Exemplar sensor readout.

the capacitive load which is the summation of the pad capacitance, PCB trace parasitics and the capacitance of probe. The voltage waveforms in Fig. 2.14(b) and Fig. 2.15(b), therefore, have not been visualized during the characterization of Chip-1. Instead, these signals have been monitored as if photovoltaic level binary signals. Fig. 2.19(b) shows the exemplar readout taken from one of the test dies. It measures 1.39 kHz of oscillation frequency.

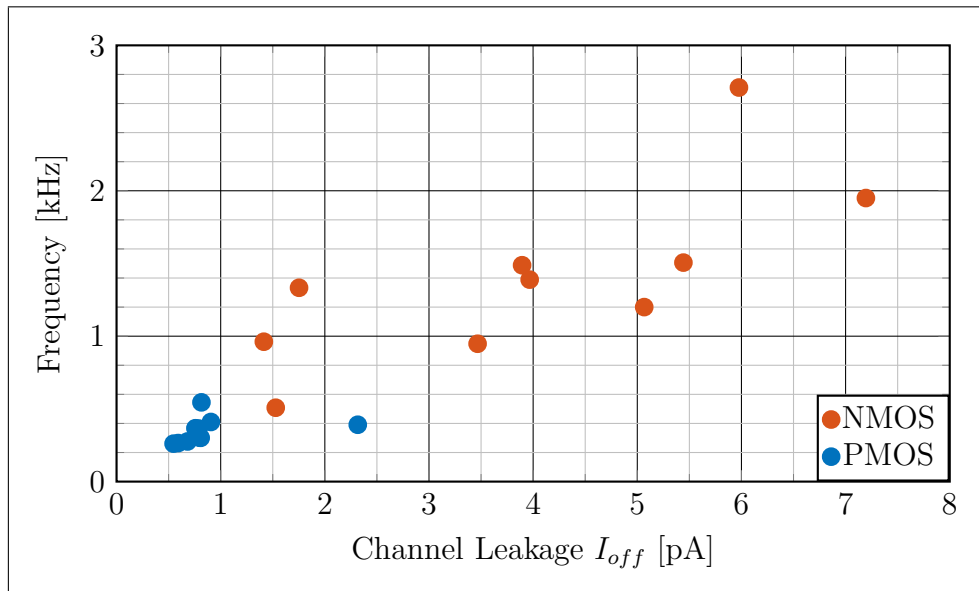


Figure 2.20. Frequency vs. channel-leakage scatter in Chip-1.

In order not to interfere with oscillator operation while performing these tests, $I_{offn,p}$ and

$\eta_{n,p}$ were characterized on 21 additional unit devices being identical to load devices MLx of Fig. 2.14 and Fig. 2.15. The result is shown with a scatter plot in Fig.2.20 and summarized in Table 2.2. Regression analysis applied to Table 2.2 reveals the correlation between the frequency and leakage as $f \propto I_{offn}^{0.74}$ for the NMOS sensor and $f \propto I_{offp}^{0.30}$ for PMOS sensor which are both below $f \propto I_{offn}^{0.80}$, the simulated correlation of the the conventional sensor. A possible reason of such a discrepancy is the physical distance between the sensor and test devices which is $\approx 400 \mu\text{m}$ in horizontal direction and $\approx 300 \mu\text{m}$ in vertical direction leading to a total distance of $\approx 500 \mu\text{m}$ which can be seen in Fig. 2.1. Having such a distance, it is inevitable for the frequency measured from sensor devices to show a weak correlation with the leakage current measured from test devices.

Table 2.2. Chip-1 f vs. I_{off} scatter.

NMOS	I_{off} [pA]	f [kHz]	PMOS	I_{off} [pA]	f [kHz]
Sample #1	3.97	1.39	Sample #1	0.76	0.37
Sample #2	5.07	1.20	Sample #2	0.79	0.36
Sample #3	5.44	1.51	Sample #3	2.32	0.39
Sample #4	3.89	1.49	Sample #4	0.80	0.30
Sample #5	3.47	0.95	Sample #5	0.68	0.28
Sample #6	7.20	1.95	Sample #6	0.91	0.41
Sample #7	5.98	2.71	Sample #7	0.82	0.54
Sample #8	1.53	0.51	Sample #8	0.55	0.26
Sample #9	1.75	1.33	Sample #9	0.81	0.30
Sample #10	1.41	0.96	Sample #10	0.59	0.26

Even though the common-centroid placement of test and sensor devices has been planned before Chip-1 tapeout, this idea has been abandoned since it brings additional parasitic capacitances due to increased number of interconnections. Since the correlation coefficient is lower than expected in core NMOS and PMOS devices, however, the common-centroid placement of test and sensor devices has been adopted in Chip-2 whose details are discussed in Chapter 3.

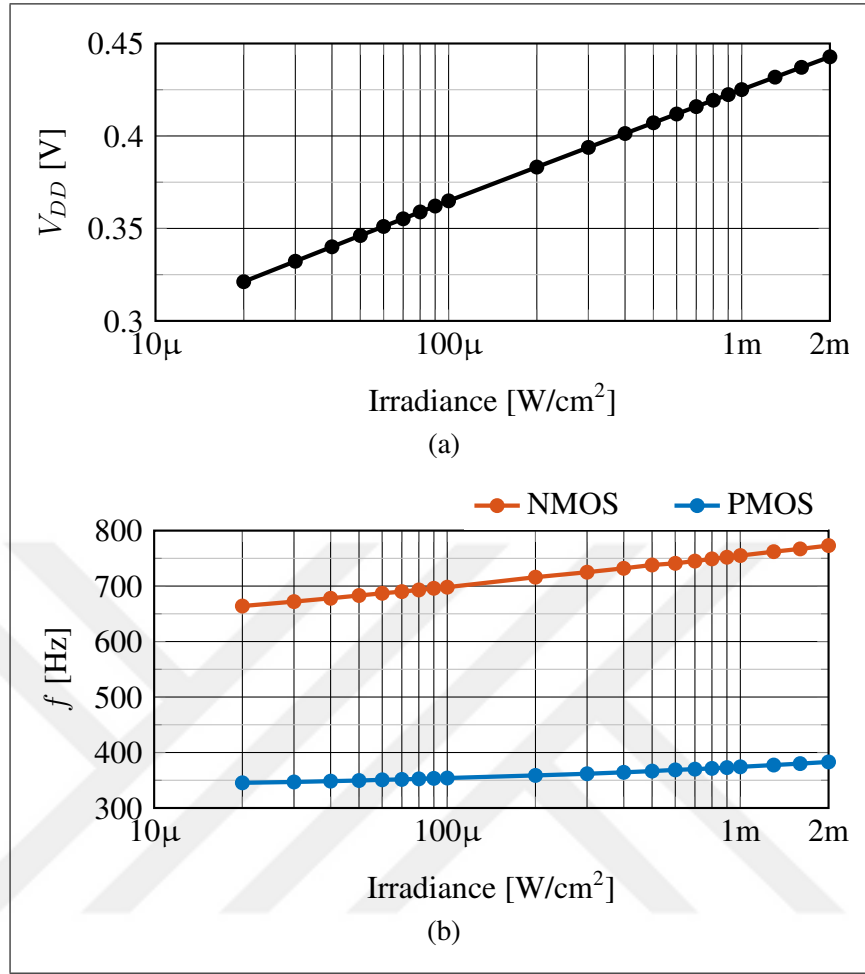


Figure 2.21. Experimental irradiance sensitivity of: (a) V_{DD} . (b) Frequency.

The relationship predicted between f and irradiance was tested on PMOS and NMOS sensors of Chip-1. Shown in Fig. 2.21(a) is the variation of V_{DD} with irradiance. It exhibits $\Delta V = 120$ mV change between $20 \mu\text{W}/\text{cm}^2$ and $2 \text{mW}/\text{cm}^2$ of D65 irradiance levels. Also plotted in Fig. 2.21(b) is the oscillation frequency variation of NMOS and PMOS leakage sensor against the irradiance change. The relative sensitivity per decade around $E = 1 \text{mW}/\text{cm}^2$ of the leakage sensors turn out to be 7.5 percent for NMOS and 5.4 percent for the PMOS sensor respectively.

2.3. VLC RECEIVER BLOCK

As stated in Section 1.2, a visual light communication (VLC) receiver selects either NMOS or PMOS leakage sensor to be integrated with the beacon platform for readout. It is built

with two sub-blocks where photo-detection and rectification take place. Chip-1 includes the design and experimental characterization of a novel photodetector circuit which is introduced and discussed in the following subsection.

2.3.1. Photodetector Block

Shown Fig 2.22 is the electrical schematic of the novel self-biased photodetector circuit proposed in this work. Unlike the conventional trans-impedance amplifier (TIA) topologies, the proposed circuit does not require an OPAMP and resistor which provides a radical decrease in the power consumption and footprint. The circuit comprises identical photodiodes D1 and D2, identical current-mirroring MOSFETs M1 and M2, and a filtering capacitor C3.

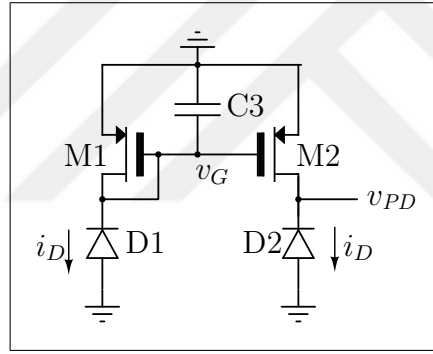


Figure 2.22. Proposed photodetector circuit.

A small fraction of the light is modulated with a certain frequency and applied on the photodetector circuit. The relative change in the illumination is then, converted to a variation in voltage as long as the modulation is maintained. Fig 2.23 helps to visualize how such a conversion takes place. The blue solid curve shows the current-voltage characteristics of negative photodiodes D1 and D2 under a certain irradiance level. Similarly, orange solid curve shows the current-voltage characteristics of MOS devices M1 and M2 under the same irradiance level provided that $V_{GS} = V_G = V_{PD1}$. The output voltage of the photodetector V_{PD} , therefore, is equal to V_{PD1} where the current of photodiodes and MOS devices are equalized. When the irradiance is increased, these characteristics are represented with dashed lines. The new value of the photodetector output voltage equals V_{PD3} .

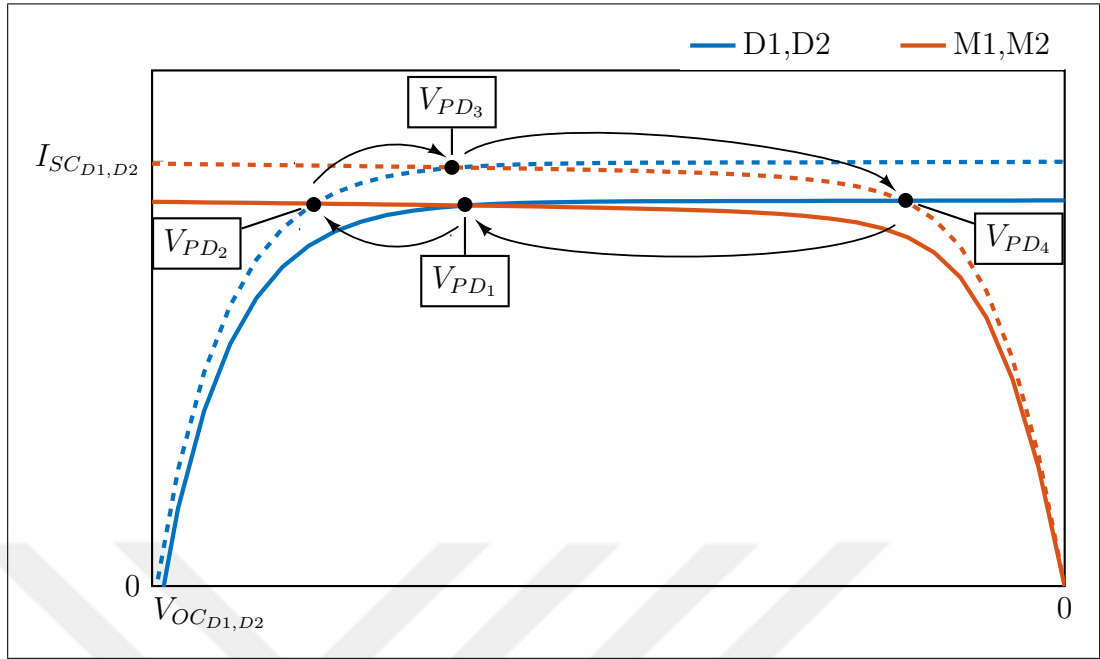


Figure 2.23. Photodetector large signal response.

If the filtering capacitor $C3$ does not exist in the circuit, the output of the photodetector will swing between V_{PD1} and V_{PD3} as long as the irradiance modulation is maintained. The amount of swing, however, is too low to be rectified. When the filtering capacitor $C3$ is added to the circuit, it delays V_G to respond to the increase in irradiance for a short period of time. During this period, MOS devices operate in the regime shown with orange solid line and output of voltage of the photodetector becomes V_{PD2} . As $C3$ keeps charging, photodetector output settles to V_{PD3} . When the irradiance level gets back to its initial value, $C3$ delays V_G to respond to the decrease in irradiance for a short period of time. During this period, MOS devices operate in the regime shown with orange dashed line and output of voltage of the photodetector becomes V_{PD4} . As $C3$ keeps discharging, photodetector output settles to V_{PD1} . Thanks to $C3$ which filters the ripple in v_G , the output of the photodetector now swings between V_{PD2} and V_{PD4} as long as the irradiance modulation is maintained. The amount of swing is more appropriate to be rectified as compared with the swing value $V_{PD1} - V_{PD3}$.

The transfer function relating time varying component v_{pd} to the time varying component i_d of the matching photodiode currents flowing in $D1$ and $D2$ can be extracted from the small-signal equivalent circuit shown in Fig. 2.24, where g_m and r_o represent the trans-conductance

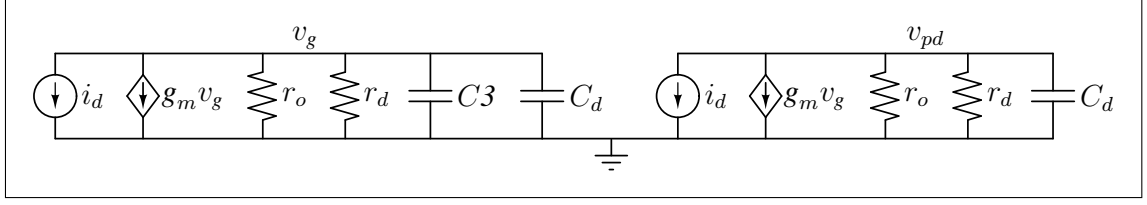


Figure 2.24. Photodetector small-signal equivalent circuit.

and output resistance parameters of M1 and M2. C_d represents the junction capacitance of D1 and D2. As indicated by the outcome

$$\frac{v_{pd}}{i_d} = - \frac{r_o || r_d}{\left[1 + \frac{g_m / (C3 + C_d)}{s} \right] \cdot [1 + s \cdot (r_o || r_d) \cdot C_d]} \quad (2.37)$$

the photodetector section acts on i_d as a band-pass trans-impedance amplifier of corner frequencies $\omega_L = \frac{g_m}{C3 + C_d}$ and $\omega_H = \frac{1}{(r_o || r_d) \cdot C_d}$.

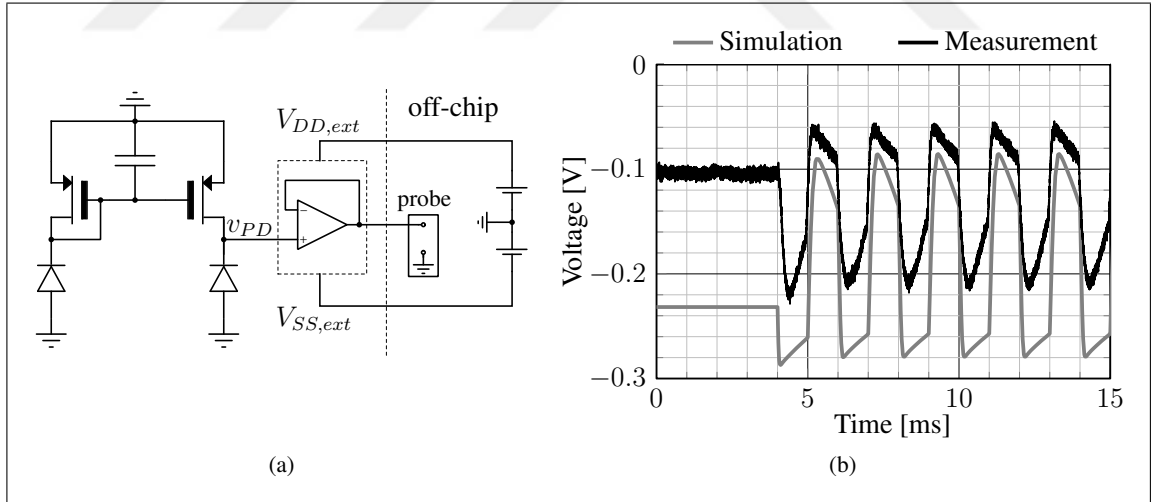


Figure 2.25. (a) Photodetector measurement setup. (b) Simulated and measured waveforms of v_{PD} .

Physical design of the photodetector is based on (a) negative photodiodes D1 and D2 of dimensions $6 \mu\text{m} \times 10 \mu\text{m}$, (b) low- V_T I/O devices M1 and M2 of $L = 2 \mu\text{m}$ and $W = 1 \mu\text{m}$, (c) low- V_T core p-type MOSCAP C3 of $670 \mu\text{m}^2$ gate area. Shown in Fig. 2.25(a) is the photodetector measurement setup where the output voltage v_{PD} is monitored with an integrated unity-gain buffer to prevent loading by the pad capacitance and PCB trace

parasitics. A detailed design flow of the unity-gain buffer is provided in Appendix A. An experimental waveform of v_{PD} is displayed in Fig. 2.25(b). Notice the dc value due to a constant 1 mW/cm^2 irradiance prior to the activation of modulation at $t = 4 \text{ ms}$, and the $500 \text{ Hz}/160 \text{ mV}$ peak-to-peak time-varying signal resulting from 10 percent modulation of the irradiance thereafter. Also plotted in Fig. 2.25 is the simulation result under typical condition for comparison with the measurement. A 130 mV shift in dc value of v_{PD} is observed. This is due to the fact that both MOS devices and photodiodes operate as current source and sink with finite output resistance respectively. Any slight difference in output resistances will move the dc bias point V_{PD1} drastically. Also the experimental peak-to-peak voltage is 20 percent less than what is predicted by the simulation. Assuming that the modulation frequency is selected in the pass-band, the trans-resistance is directly determined by the parallel equivalent of output resistances of MOS devices and photodiodes. Assuming these resistances are the same, a 33 percent difference between simulation and measurement in one of these resistances may cause such a scenario. Considering the scattering range of output resistance of a MOS device, this is such a probable situation.

2.4. RING OSCILLATOR AND CLOCK GENERATOR BLOCKS

The dual-supply shown in Fig. 2.7 generates 760 mV open circuit voltage under 1 mW/cm^2 D65 irradiance. The value of the supply voltage decreases when it is loaded with a circuit. The amount of decrease is determined by the current drawn from the supply. Increasing either the number of photovoltaic converters or the amount of irradiance are two ways to keep the supply voltage fairly constant regardless of the load. Considering the limited space available inside scribe lines, the maximum number of photovoltaic converters is also limited. The second method requires extreme levels of irradiance beyond the indoor illumination levels which degrades the applicability of the scribe test. Also the photo-generated current saturates with the increasing amount of irradiance. Device sizing and appropriate library selection among a variety of threshold voltages, therefore, play a critical role in on-chip photovoltaic conversion with optimum efficiency.

Shown in Fig. 2.26 is the logic schematic of clock generator. It is built with a ring oscillator, two NOR gates for non-overlapping clock generation, and a staged buffer for driving the

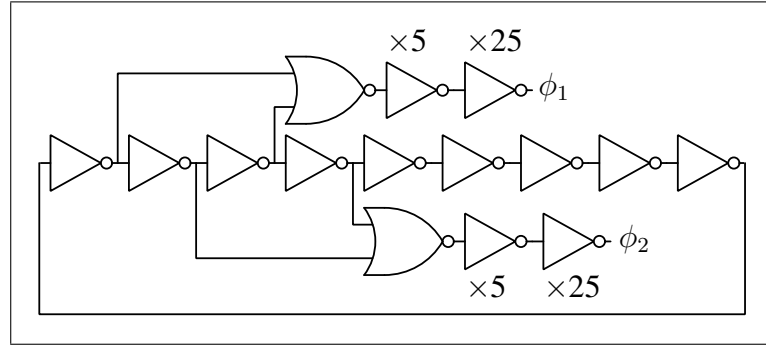


Figure 2.26. Logic schematic of clock generator.

charge pump. As derived in [34], oscillation frequency of the ring oscillator with the assumption of devices operating in sub-threshold regime is given by

$$f = K_1 \cdot \frac{10^{V_{PS}/S_M}}{V_{PS}} \quad (2.38)$$

where V_{PS} is the voltage between positive and negative rails of photovoltaic supply. Assuming identical sub-threshold slope for NMOS and PMOS devices, S_M defines this sub-threshold slope parameter. K_1 is defined as

$$K_1 = \frac{I_{leakP} \parallel I_{leakN}}{C \cdot n} \quad (2.39)$$

where I_{leakN} and I_{leakP} define the off-state leakage current of NMOS and PMOS devices respectively. $C \cdot n$ is the total capacitance loading n -stage oscillator.

Experimental clock generator is realized using a nine stage ring oscillator and two NOR gates whose outputs are connected to a two-staged buffer where each stage has 1:5 tapering factor. The devices are of I/O library. Their channel dimensions are $L = 0.34 \mu\text{m}$ and $W = 0.8 \mu\text{m}$ in PMOS, and $L = 0.5 \mu\text{m}$ and $W = 0.24 \mu\text{m}$ in NMOS. This combination yields closely matching sub-threshold transfer characteristics for the pull-down and pull-up paths, and therefore results in nearly identical rise and fall times for inverter stages. V_{DD1} is supplied via seven copies of unit positive photodiode whereas V_{SS1} is supplied via four copies of unit negative photodiode.

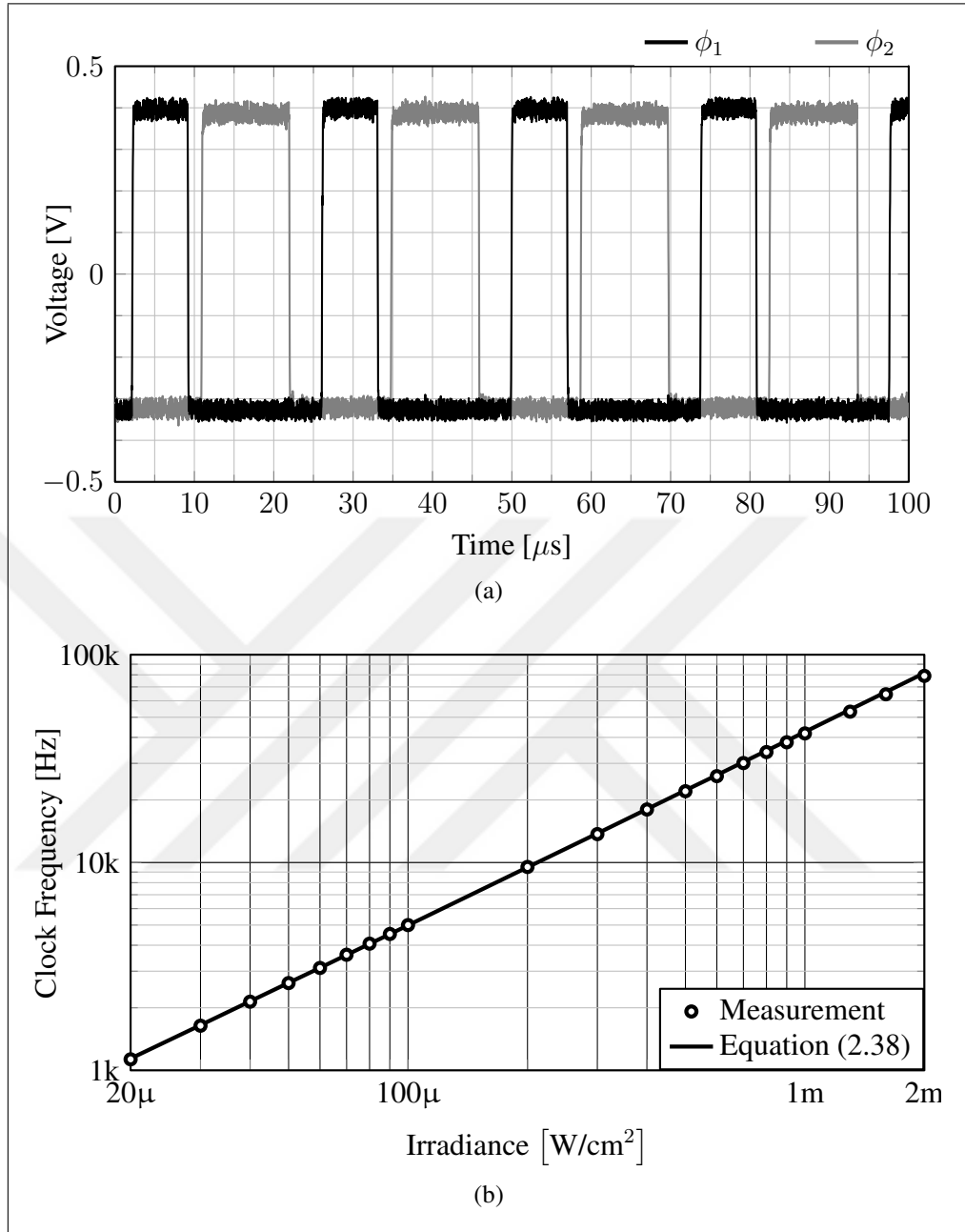


Figure 2.27. (a) Non-overlapping clocks. (b) Frequency vs. irradiance.

The non-overlapping clocks ϕ_1 and ϕ_2 of the experimental clock generator are measured using the tapered buffers similar to the one in Fig 2.19. Shown in Fig. 2.27(a) is the voltage waveforms of ϕ_1 and ϕ_2 under 1 mW/cm^2 D65 irradiance. The oscillation frequency of ϕ_1 and ϕ_2 was measured as 41.9 kHz. The relationship predicted between the clock frequency and irradiance was also tested on clock generator between 20 $\mu\text{W}/\text{cm}^2$ and 2 mW/cm^2 of D65 irradiance levels. Shown in Fig. 2.27(b) is the variation of clock frequency with irradiance.

Also plotted is the equation (2.38) with the extracted parameters of $K_1 = 22$ mV/s and $S_M = 125$ mV/decade.

2.5. CHARGE PUMP BLOCK

The power required by the impulse generator and UWB radio is relatively high compared to the amount of power available from the photovoltaic converters. This is why a charge pump is needed. It generates positive supply voltage across a storage capacitor. Once the sufficient amount of charge is stored on the capacitor, that is, the voltage on the capacitor is enough for the radio transmitter to operate, it begins transmitting the data driven by the level-shifted impulses of the channel-leakage sensor. Dickson charge pump in Fig. 2.28(a) was selected as a candidate topology since it is validated on silicon.[34] Alternatively, voltage doubler in Fig. 2.28(b) was selected as another candidate. Also known as the Nakagome cell, this topology was proposed as a Word-line driver with feedback charge-pump circuit in [36].

One of the differences between the Dickson charge pump in Fig. 2.28(a) and voltage doubler in Fig. 2.28(b) is the number of capacitors per stage. Voltage doubler consists two capacitors per stage in which, one transfers the charge to the next stage while the other is in storage stage. The amount of charge using voltage doubler, therefore, is expected to be greater than Dickson charge pump with the identical device selection. A two-phase version of Dickson charge pump is also introduced in Fig. 2.28(c) which operates in a full clock cycle, not just half. It includes two Dickson charge pumps with flipped clock signals. The number of capacitors per stage, therefore, is doubled.

The output voltage of the charge-pump topologies shown in Fig. 2.28 were compared with a simulation using 100 fF MIM of $10\ \mu\text{m} \times 10\ \mu\text{m}$ footprint, I/O PMOS and deep n-well NMOS with minimum geometry. Each charge-pump has 8 stages. The non-overlapping clock signals were provided by the clock generator which is supplied by the dual supply using (2.14). V_{DD1} is supplied via seven copies of unit positive photodiode whereas V_{SS1} is supplied via four copies of unit negative photodiode. Simulation results under $E = 1$ mW/cm² D65 irradiance is shown in Fig. 2.29. Pumping starts at $t = 0.3$ ms and the output voltage of the charge-pumps reach their maximum at $t = 1.5$ ms. Voltage doubler

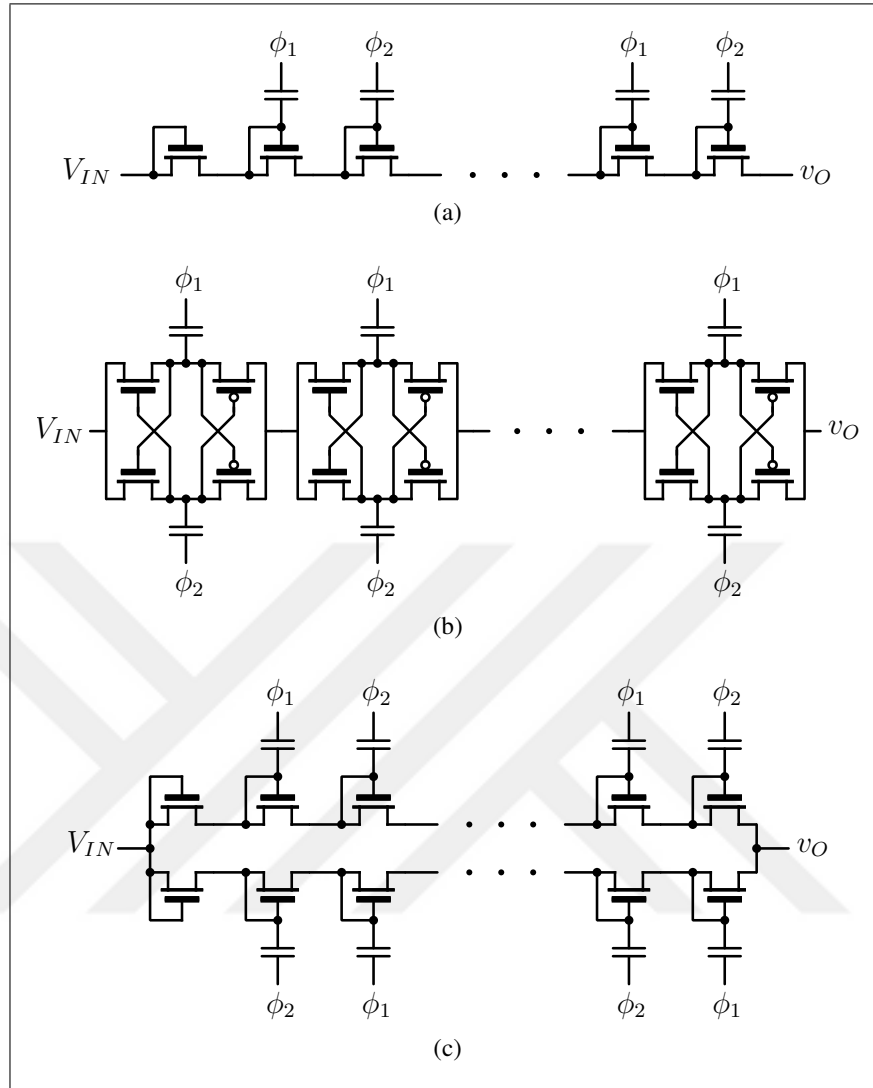


Figure 2.28. (a) Dickson CP. (b) Nakagome cell. (c) Dickson CP (doubled).

and two-phase Dickson charge pump exhibit similar response whereas Dickson charge pump falls behind them as expected. The simulations are repeated under various irradiance levels and with different device geometries. Based on these results, voltage doubler is chosen as the charge pump in the proposed leakage monitor.

Shown in Fig. 2.30(a) is the electrical schematic of one stage of voltage doubler. Black components implement the charge transfer function as described in [36]. Gray components are added for eliminating the body effect of charge transferring devices by establishing an uninterrupted source-bulk short circuit in accordance with the technique proposed in [37]. Experimental eight-stage voltage-doubler was built with core PMOS and deep n-well NMOS

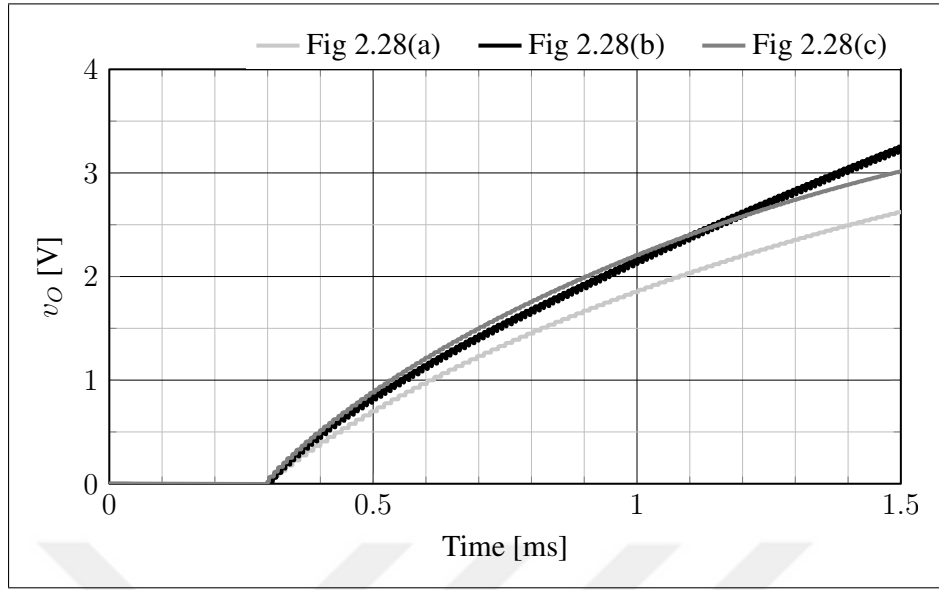


Figure 2.29. Simulated charge-pump comparison.

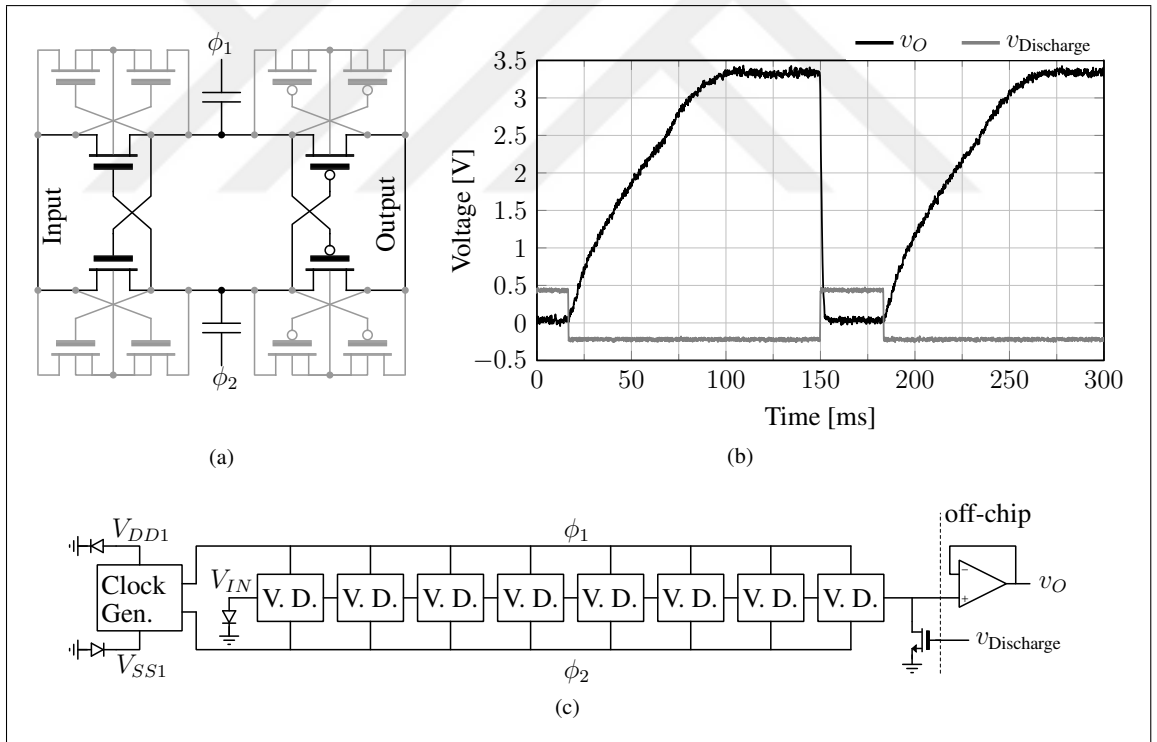


Figure 2.30. Voltage doubler: (a) Schematic. (b) Experimental output voltage v_O . (c) Measurement setup.

devices of $L = 0.18 \mu\text{m}$ and $W = 0.44 \mu\text{m}$. Clock coupling capacitors are 100 fF MIM of $10 \mu\text{m} \times 10 \mu\text{m}$ footprint.

Experimental waveform of the eight-stage voltage doubler output v_O captured under 1 mW/cm^2 D65 irradiance is presented in Fig. 2.30(b) together with the output discharging control signal $v_{\text{Discharge}}$. Discharging of v_O is performed with an NMOS switch which is closed when the applied voltage at its gate equals to positive photovoltaic supply. Similarly, the switch is opened whenever the applied voltage at its gate equals to negative photovoltaic supply thus allowing the charge pump to boost the output voltage v_O . Shown in Fig. 2.30(c) is the measurement setup for the output voltage of the charge-pump. Unlike the ultimate target, output voltage of the charge-pump is monitored with an off-chip analog buffer built with an ultra-low input-current OPAMP. The gate of the discharging switch is also controlled with an off-chip signal. Upon the completing charge-pump characterization, the discharging switch has been removed in subsequent tapeouts.

2.6. STORAGE CAPACITOR BLOCKS

Shown in Fig. 2.31 is the comparison between the capacitance - voltage characteristics of MIM and MOS capacitors occupying the same footprint. MIM provides the lowest capacitance per unit area. The capacitance is around 10 pF as strong inversion sets when $V_{O1} > 0.8 \text{ V}$ for I/O MOSCAP and 17 pF when $V_{O1} > 0.5 \text{ V}$ for core MOSCAP. Even though providing less capacitance per unit area as compared with the core devices, the usage of I/O devices is more favorable due to (a) precaution against the possibility of excessive boosting of the power-supply voltage due to the imprecision of the voltage reference, (b) low oxide leakage compared with core MOSCAPs. [34]. Capacitors C1 and C2, which store the boosted voltage as shown in Fig. 1.1, therefore, were built with multiples of very-low leakage I/O n-type MOSCAP of $55 \mu\text{m} \times 22 \mu\text{m}$ footprint and 10 pF capacitance. Ten and fifteen units are paralleled for constructing C1 and C2, respectively.

2.7. VOLTAGE REFERENCE BLOCK

Recalling Section 1.3, a reference voltage is necessary since it is compared with the scaled down copy of boosted voltage for determining whether or not the voltage on storage capacitors is boosted to a sufficient level. This reference, therefore, is expected to be a constant voltage that is insensitive to environmental variables such as irradiance and

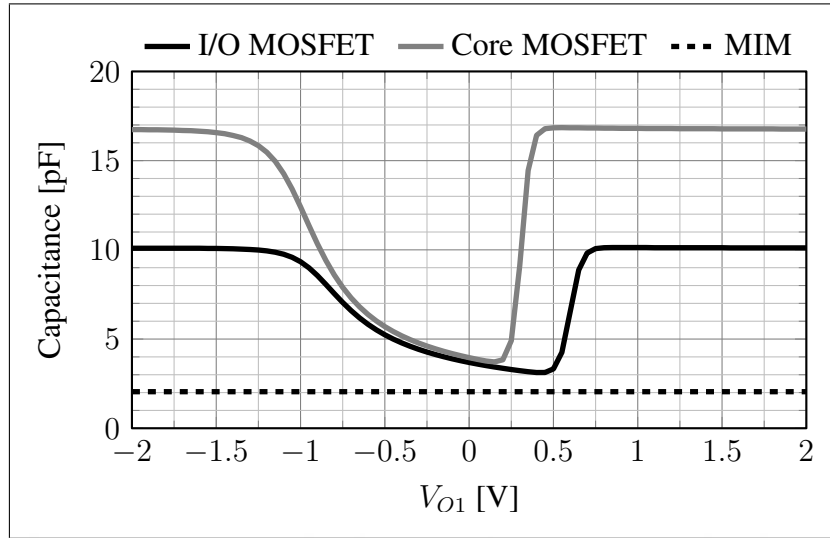


Figure 2.31. Capacitance - Voltage characteristics of MIM and MOS capacitors.

temperature. The relative distribution of the reference should also be low across all process corners and die-to-die variations since the application does not have an option of trimming. The radio, impulse generator and the level-shifters operate with the boosted supply. The rest of the blocks, however, are power supplied directly from the photovoltaic converters which makes impractical to use conventional bandgap voltage reference topologies. Considering the limited space and ultra-low power requirements makes compulsory to use a simpler circuit than the conventional voltage reference topologies.

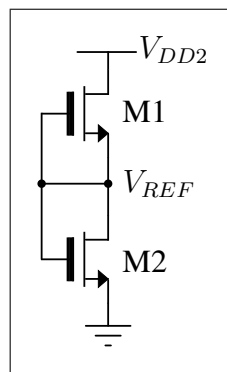


Figure 2.32. Electrical schematic of initially proposed voltage reference.

Shown in Fig 2.32 is a 2-transistor reference circuit used in [38] and selected as a candidate for this work. M1 is a core MOS device with low-threshold option whereas M2 is selected from I/O library with standard threshold option. Assuming $V_{DD2} - V_{REF}$ and V_{REF} itself are

greater than a few $\frac{kT}{q}$, the devices are saturated and operating in sub-threshold condition. The current of each device is given by

$$I = \frac{W}{L} \cdot \mu_N C_{ox} \cdot (A_N - 1) \cdot \left(\frac{kT}{q} \right)^2 \cdot \exp \left(\frac{q}{kT} \cdot \frac{V_{GS} - V_{TN}}{A_N} \right) \quad (2.40)$$

Equating sub-threshold current of the devices and solving for V_{REF} yields

$$V_{REF} = A_{N2} \cdot \frac{kT}{q} \cdot \ln \left[\frac{(W/L)_1}{(W/L)_2} \cdot \frac{(\mu_N C_{ox})_1}{(\mu_N C_{ox})_2} \cdot \frac{(A_{N1} - 1)}{(A_{N2} - 1)} \right] - \left(\frac{A_{N2}}{A_{N1}} \cdot V_{TN1} - V_{TN2} \right) \quad (2.41)$$

Using (2.41), an optimum $\frac{(W/L)_1}{(W/L)_2}$ can be selected for temperature independent V_{REF} since the derivative of $[(A_{N2}/A_{N1}) \cdot V_{TN1} - V_{TN2}]$ with respect to temperature is positive. As observed with simulation, the ratio $\frac{(\mu_N C_{ox})_1}{(\mu_N C_{ox})_2}$ remains nearly constant along the temperature range of interest since the rate of change in effective mobility is near the same for both devices. The value of $\frac{(\mu_N C_{ox})_1}{(\mu_N C_{ox})_2}$ was calculated with simulation as well as the sub-threshold slope terms A_{N1} and A_{N2} . The temperature dependence of threshold voltage is expressed as a linear equation whose coefficients were extracted with a temperature sweep for both devices. The only parameter to be determined, therefore, is the ratio of channel dimensions of devices $\frac{(W/L)_1}{(W/L)_2}$. Its value is found by plotting (2.41) as a function of temperature and $\frac{(W/L)_1}{(W/L)_2}$ with a surface plot as shown in Fig. 2.33(a). Optimum value of $\frac{(W/L)_1}{(W/L)_2}$ is found by Y-Z projection of Fig. 2.33(a) which is also shown in Fig. 2.33(b). The constant voltage along the temperature range is read as 205 mV by selecting $\frac{(W/L)_1}{(W/L)_2} = 2.87$.

Die-to-die variation analysis through process and mismatch conditions for the voltage reference circuit in Fig. 2.32 was performed using Monte-Carlo simulations. M1 was built with $m_1 = 26$ copies of unit devices selected from the core library with the channel dimensions of $L = 1 \mu\text{m}$ and $W = 1 \mu\text{m}$. M2 was built with $m_2 = 9$ copies of unit devices selected from the I/O library with the same channel dimensions as M1. Monte-Carlo simulation result for V_{REF} in Fig. 2.34 shows that the reference voltage has a mean value around 200 mV with 9.3 percent relative standard deviation.

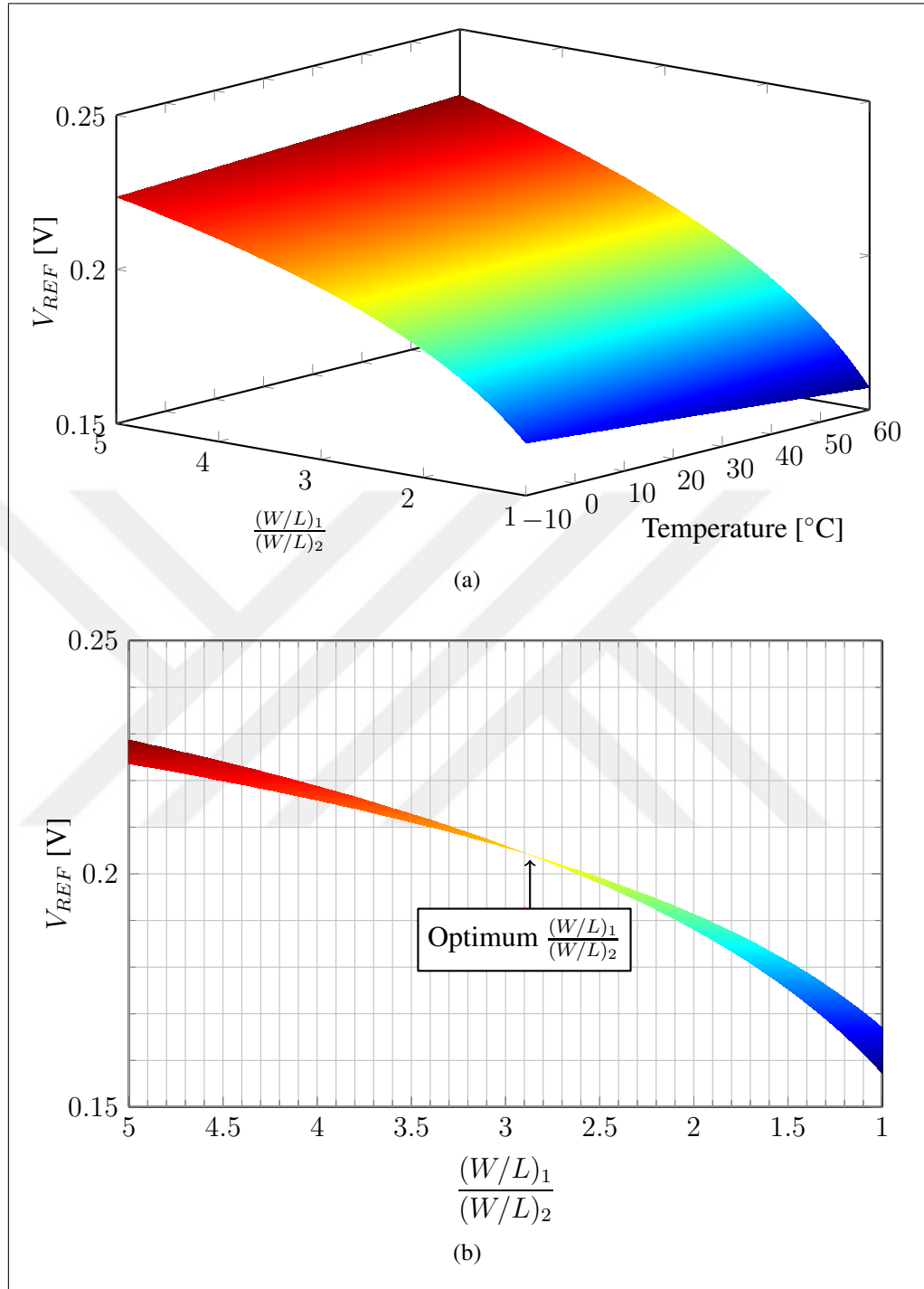


Figure 2.33. V_{REF} as a function of (a) T and $\frac{(W/L)_1}{(W/L)_2}$. (b) Y-Z projection.

The main contribution to standard deviation is due to device selection from different libraries. Considering the environment where the scribe tests are performed, the variation of temperature is nearly zero. Based on this situation, design flow which targets a constant voltage along certain temperature range can be abandoned. Instead, the design may target

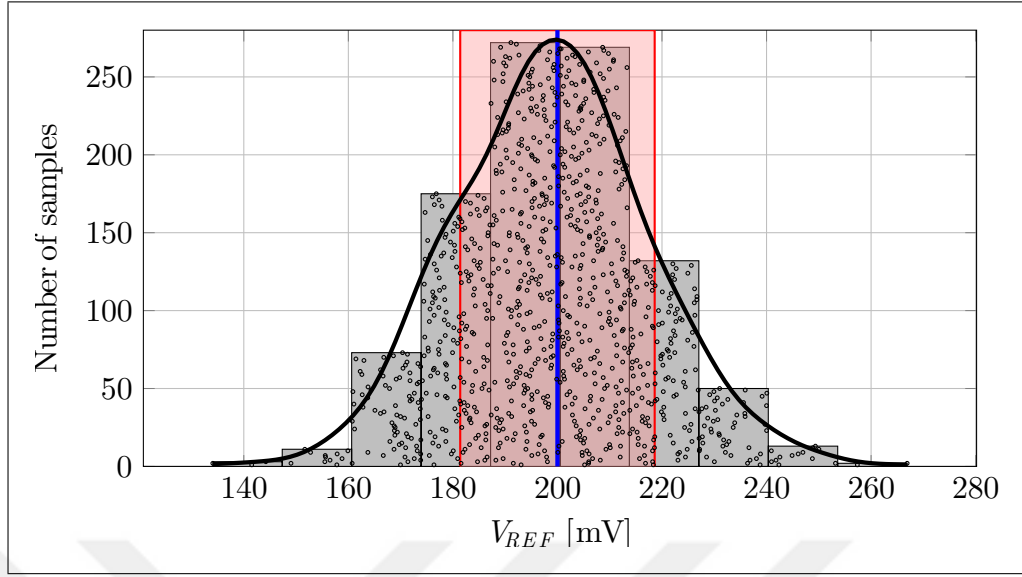


Figure 2.34. Monte-Carlo simulation results of V_{REF} .

improvement in relative standard deviation using the devices of same library. Using (a) unit device of I/O library for M1 and M2 with $L = 1 \mu\text{m}$ and $W = 1 \mu\text{m}$ and (b) setting m_1/m_2 using (2.41) yields 4.7 percent relative standard distribution around the mean value of 200 mV.

An alternative two-transistor voltage reference proposed in [39] and used in [34] was also built and shown in Fig. 2.35(a). It differs from the circuit in Fig. 2.32 with its common-gate terminal which is connected to V_{DD2} rather than the V_{REF} . The current of each device is still given by (2.40) assuming $V_{DD2} - V_{REF}$ and V_{REF} itself are greater than a few $\frac{kT}{q}$. Selecting M1 and M2 from the same library results in identical slope parameter A_N for both devices. Equating sub-threshold current of the devices and solving for V_{REF} yields

$$V_{REF} = A_N \cdot \frac{kT}{q} \cdot \ln \left[\frac{(W/L)_1}{(W/L)_2} \right] - (V_{TN1} - V_{TN2}) \quad (2.42)$$

where the inequality of threshold voltages V_{TN1} and V_{TN2} is due to body effect which can be eliminated by using deep n-well devices. Since M1 and M2 are from the same library, the derivative of $(V_{TN1} - V_{TN2})$ with respect to temperature is practically zero. The voltage reference circuit, therefore, has a proportional-to-absolute-temperature (PTAT) characteristics which can also be used as a temperature sensor.

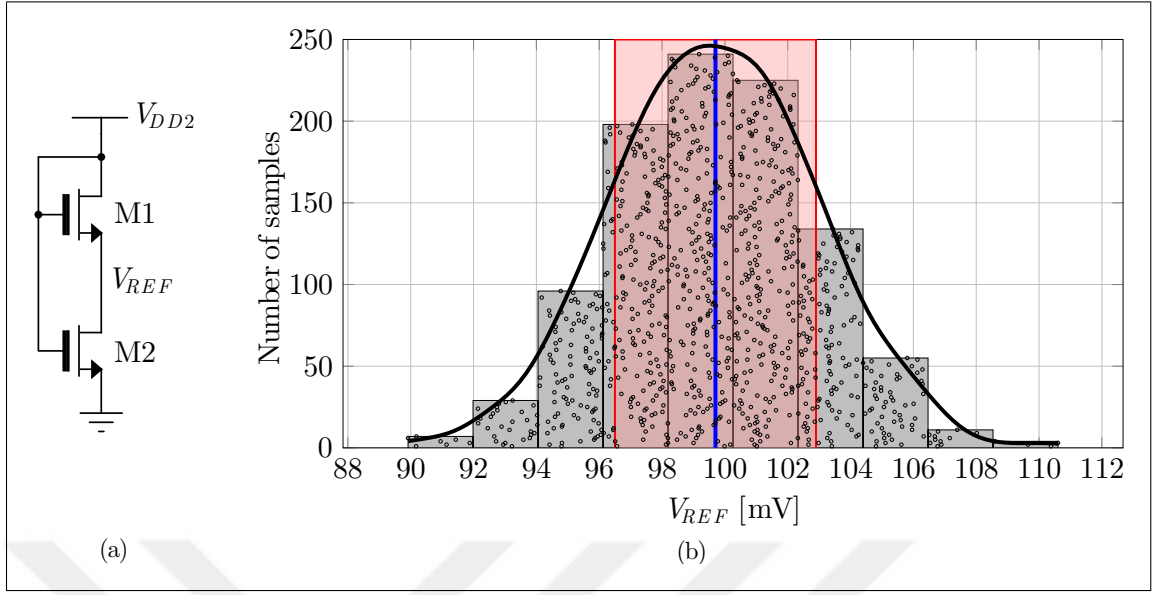


Figure 2.35. Voltage reference: (a) Schematic. (b) Monte-Carlo results.

Die-to-die variation analysis through process and mismatch conditions for the voltage reference circuit in Fig. 2.35(a) was performed using Monte-Carlo simulations. M1 and M2 were built with $m1 = 54$ and $m2 = 1$ copies of a unit MOSFET from I/O library with channel dimensions of $L = 2 \mu\text{m}$ and $W = 2 \mu\text{m}$ respectively. Monte-Carlo simulation result for V_{REF} in Fig. 2.35(b) shows that the reference voltage has a mean value around 99.7 mV with 3.2 percent relative standard deviation.

Based on the comparison between two candidate voltage reference circuits, the circuit in Fig. 2.35(a) which offers lower relative standard deviation was selected for tapeout. Shown in Fig. 2.36(a) is the measurement setup for experimental voltage reference which was built with the same devices and same channel dimensions as the simulation model. V_{DD2} was supplied by one unit $60 \mu\text{m} \times 100 \mu\text{m}$ photodiode. The output of the voltage reference V_{REF} was connected to a source-measure-unit (SMU) probe whose equivalent circuit is also shown in Fig. 2.36(a).[40] The measurement was performed with a Keithley 4200-SCS parametric analyzer by sweeping the voltage V_{SET} and reading its value when I_{SET} is equal to zero since this is the condition where V_{REF} equals V_{SET} . Shown in Fig. 2.36(b) is an example readout under $E = 1 \text{ mW/cm}^2$ D65 irradiance where V_{REF} was measured as 102.8 mV. Irradiance dependence of V_{REF} was also characterized and plotted in Fig. 2.36(c). It exhibits 6 mV change between $20 \mu\text{W/cm}^2$ and 2 mW/cm^2 of D65 irradiance levels. Considering

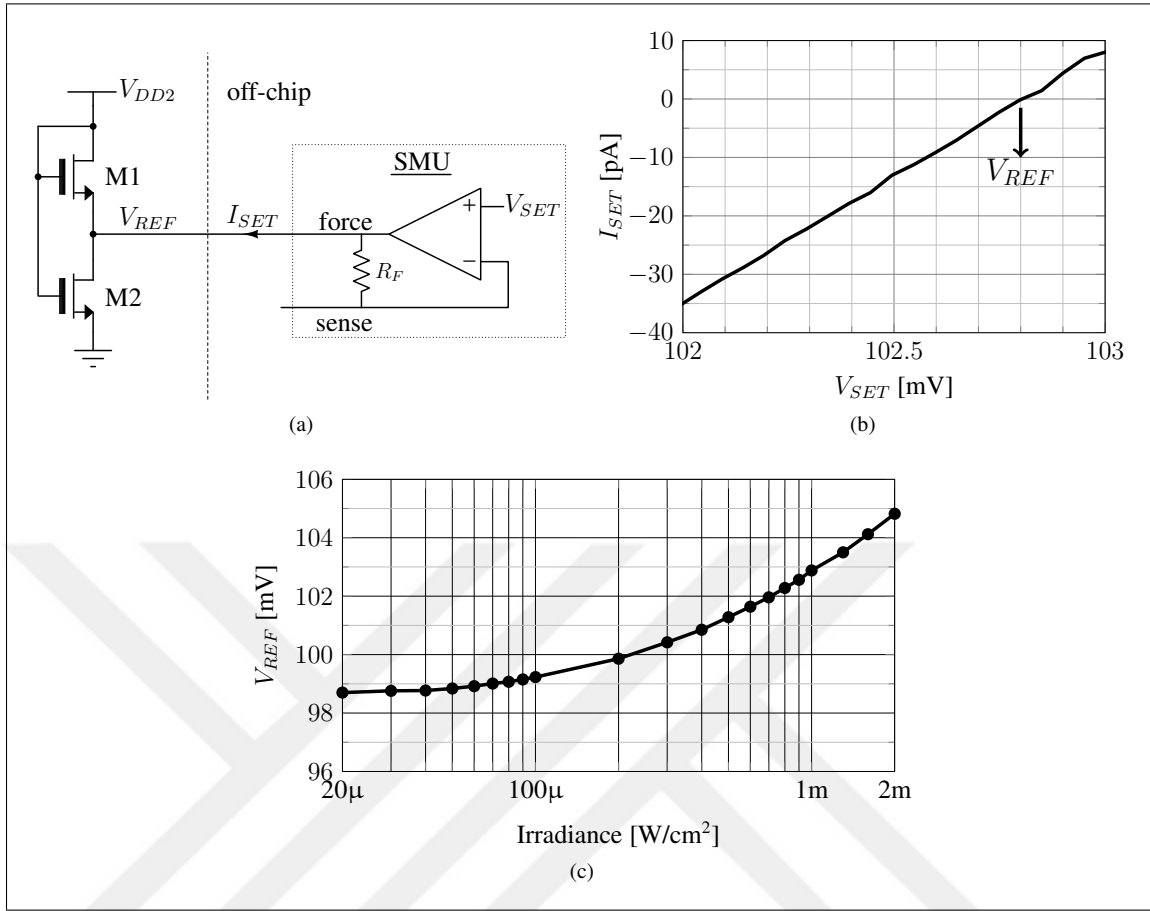


Figure 2.36. Experimental voltage reference: (a) Measurement setup. (b) I_{SET} vs. V_{SET} for V_{REF} readout. (c) V_{REF} vs. irradiance.

the environment where the scribe tests are performed, the variation of irradiance is far below such a range. The voltage reference, therefore, does not require any regulation.

2.8. HYSTERESIS COMPARATOR BLOCK

The reason why a comparator with hysteresis is needed lies in the content of the data generated by the proposed leakage monitor architecture. If only a digital data with finite word length to be transmitted via UWB radio, a transmission-end control logic would terminate the transmission sequence and the charge pump would begin storing energy on storage capacitors. In the channel leakage sensor, however, the situation is different. In this case, the data to be sent is a periodic signal whose frequency is determined by the channel leakage sensor. In other words, there is no transmission ending control logic. In

the proposed architecture, end of transmission is determined with a logic-threshold value. If the voltage on storage capacitors has reached down to that of threshold, transmission is ended and energy-storage phase is initiated. A comparator with hysteresis is needed to serve this purpose. Its upper trip point determines the beginning of transmission phase, whereas the lower trip point determines the ending of transmission and beginning of energy storage phase. Electrical schematic of hysteresis comparator is shown in Fig. 2.37(a).[41]

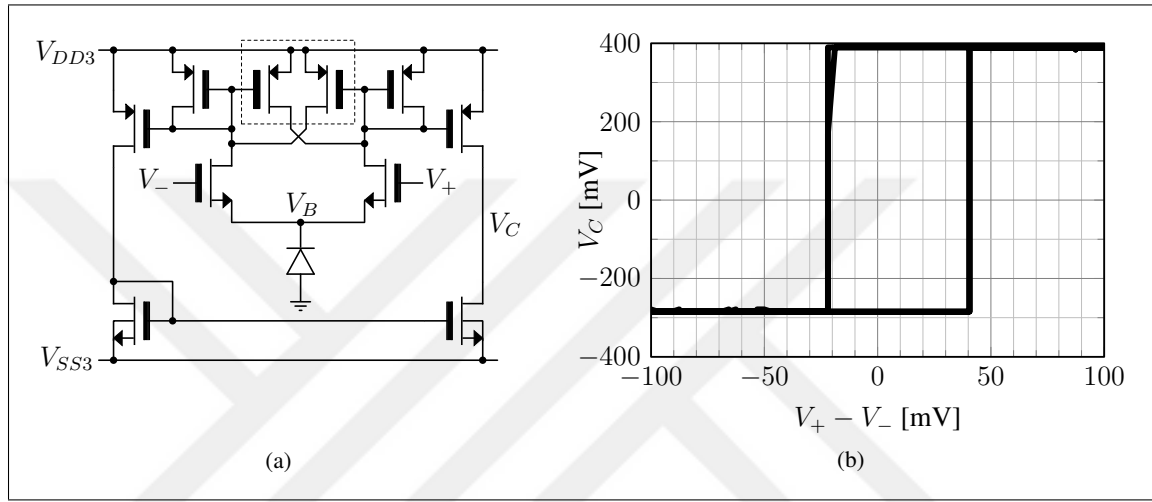


Figure 2.37. Hysteresis comparator: (a) Schematic. (b) Voltage transfer curve.

The NMOS driver devices of the experimental comparator were built with four copies of a unit MOSFET of channel dimensions $W = 2 \mu\text{m}$ and $L = 1 \mu\text{m}$. Each of the two cross-coupled PMOS devices inside dashed rectangle comprises two copies of a unit MOSFET of dimensions $W = 3 \mu\text{m}$ and $L = 1 \mu\text{m}$. All other devices of the comparator, except the diode, are unit MOSFETs. V_{DD3} was supplied via four copies of unit positive photodiode whereas V_{SS3} was supplied via two copies of unit negative photodiode. A unit photodiode supplies the bias current by acting as a current sink.

A sine-wave was applied to the non-inverting input of the comparator where the inverting input was biased with a DC voltage being equal to $V_{REF} = 100 \text{ mV}$. The output of the comparator V_C was measured using the tapered buffer similar to the one in Fig 2.19. Hysteresis curve obtained by plotting V_C as a function of $V_+ - V_-$ under $E = 1 \text{ mW/cm}^2$ D65 irradiance is shown in Fig. 2.37(b). Hysteresis gap at the output of the comparator is measured as $\pm 30 \text{ mV}$ with a 10 mV shift which is believed to be due to an offset either in

signal generator or the probe.

2.9. VOLTAGE DIVIDER BLOCK

Comparing the boosted voltage v_{O2} directly with a threshold value to initiate the radio transmission is not possible since the analog section of the leakage monitor operate with photovoltaic voltage levels. There are two possible techniques to provide a solution to that problem. In the first method, a voltage booster is needed to create a voltage to be compared with v_{O2} . Also a voltage regulator is needed to keep the reference voltage constant and the comparator should be power supplied from the boosted voltage. Considering the limited space available inside scribe lines, the available power is also limited to maximum number of photovoltaic converters. The power requirement of this method is much greater than the available power. For this reason, the second method is much more applicable, since it proposes to create a fraction of the voltage on storage capacitors, and to compare with a reference voltage at photovoltaic levels.

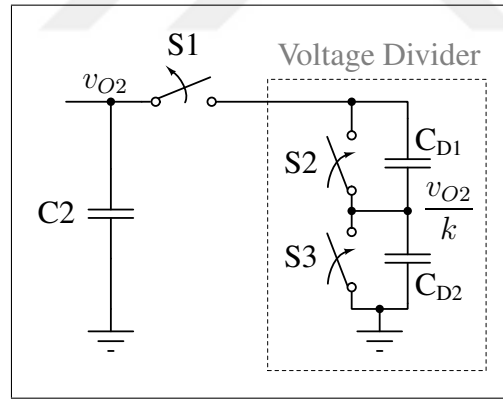


Figure 2.38. Electrical schematic of voltage divider.

Shown in Figure 2.38 is the electrical schematic of a capacitive voltage divider that creates the fraction of voltage v_{O2} . The number of capacitors is equal to k for a fraction ratio of $1/k$. Division is performed by capacitors C_{D1} and C_{D2} , which comprise one and $k - 1$ copies of a unit capacitor, respectively. $\frac{v_{O2}}{k}$ is obtained when S1 is closed, S2 and S3 are open.

C_{D1} and C_{D2} are discharged by the switches S2 and S3 at the end of each transmission period for obtaining accurate fraction. During discharging, the storage capacitor C2 is isolated from

C_{D1} and C_{D2} via S_1 to prevent losing its charge which is stored during the charging phase. The equivalent capacitance of divider is approximately equal to C_{D1} when the switches S_2 and S_3 are open. Selecting the value of unit capacitance at least three orders of magnitude smaller than C_2 prevents the charging rate of charge pump to be affected as well as it occupies a smaller footprint.

Being a high-side switch, S_1 can not be controlled with photovoltaic levels since v_{O2} is greater than photovoltaic levels. If this switch is realized with an NMOS device, a voltage greater than v_{O2} is required for turning it on. Using PMOS device, however, requires a high voltage also, but this voltage does not have to be greater than v_{O2} . This switch, therefore is realized with a PMOS device whereas S_2 and S_3 are realized with an NMOS devices and their gates are connected to the gate of PMOS device for complementary operation. Still, a level shifter is necessary for controlling the PMOS device. If the output of level shifter can not go up to v_{O2} , all switches S_1 , S_2 and S_3 may remain closed causing charge pump to source its current directly to the ground. The voltage on storage capacitors, therefore, can not increase to the required levels. This situation shows that the design of level shifter plays a critical role in the proposed architecture as to be explained further in Chapter 2.

Following properties should be considered for selecting the division ratio k :

- The minimum voltage where the capacitance of I/O MOSCAP in Fig. 2.31 reaches its maximum is 0.8 V.
- The nominal value of the reference voltage equals 100 mV.
- The value of the hysteresis gap generated by the comparator is typically ± 25 mV around the reference voltage.

Based on the considerations above, the lower limit of v_{O2} for radio transmission is specified as 1 V. In the case of using core MOSCAP, the maximum value of v_{O2} is limited to 2 V. The product $k \times (100 \pm 25)$ mV, therefore, is also limited between the minimum and maximum values of v_{O2} . Selecting $k = 16$ defines that the radio transmission starts when $v_{O2} = 16 \times 0.125 = 2$ V and stops when $v_{O2} = 16 \times 0.075 = 1.2$ V. The additional ± 5 mV hysteresis gap observed in Fig. 2.37(b) shifts these limits by 80 mV. Such an addition does

not cause any problem in the proposed design since the storage capacitors were built with I/O MOSCAPs. In the case of using core MOSCAPs, however, voltage reference design should be revisited to set the reference voltage to a lower value. Physical design of the voltage divider is based on (a) one and fifteen copies of a 100 fF MIM of $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ unit capacitor for CD1 and CD2 respectively (b) minimum-geometry I/O NMOS devices for S2 and S3 and (c) I/O PMOS device of $L = 1\text{ }\mu\text{m}$ and $W = 0.24\text{ }\mu\text{m}$ for S1.



3. DESIGN AND CHARACTERIZATION OF CHIP-2

This chapter discusses the design and characterization of level shifter, impulse generator, transmitter and antenna unit which have been taped out in Chip-2. Also the design of leakage sensor and the VLC receiver were revisited for properly integration with the proposed architecture. A preliminary version of the entire system was also built to perform the system level tests. The chapter is organized as follows: Sections 3.1 and 3.2 describe the refinements in the design of leakage sensor and VLC receiver respectively. Following four sections 3.3, 3.4, 3.5 and 3.6 cover the design of level shifter, antenna unit, transmitter and impulse generator respectively. Finally, system level tests and experimental verification results are discussed in Section 3.7.

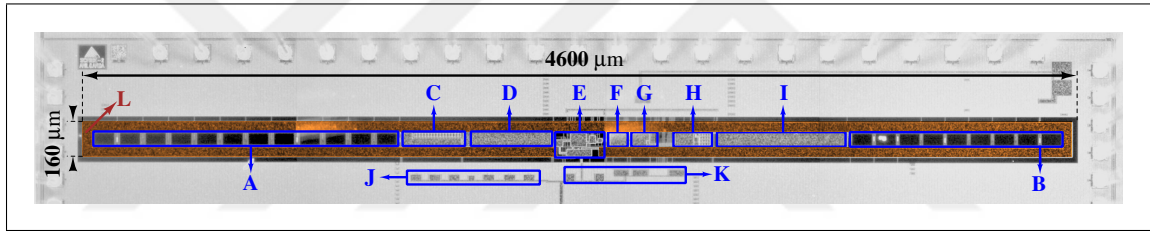


Figure 3.1. Photomicrograph of Chip-2.

Table 3.1. List of blocks in Chip-2.

A: Positive photodiodes.	B: Negative photodiodes.
C: Ring oscillator and charge pump.	D & I: Storage capacitors.
E: Impulse generator and radio transmitter.	F: Channel leakage sensors.
G: Sensor selecting block.	L: Antenna.
J: Digital buffers.	K: Analog buffers.
H: Voltage ref., voltage divider, comparator.	

Shown in Fig 3.1 is the photomicrograph of Chip-2 fabricated in UMC 0.18 μm CMOS with a footprint of $4960 \times 1525 \mu\text{m}$. The geometry of the prototype equals three mini-asic blocks wide since it contains the antenna to be used in the proposed architecture. All

blocks were designed with a footprint having less than 160 μm which is suitable for scribe-line placement. Whole system has, therefore, a very small aspect ratio. Table 3.1 lists the functional blocks which are marked in Fig 3.1.

3.1. CHANNEL LEAKAGE SENSOR BLOCKS

Having already derived the mathematical model and experimentally characterized the channel leakage sensors of Chip-1, measurement results show that, channel leakage sensor built with core NMOS devices exhibits a correlation coefficient $f \propto I_{offn}^{0.74}$ whereas the core PMOS sensor has $f \propto I_{offn}^{0.30}$ both of which are below the expectations. As stated in Chapter 2, one potential cause of such a situation is the separation between test and sensor devices. Common-centroid placement of test and sensor devices has been adopted in Chip-2 for improving the correlation between f and I_{off} .

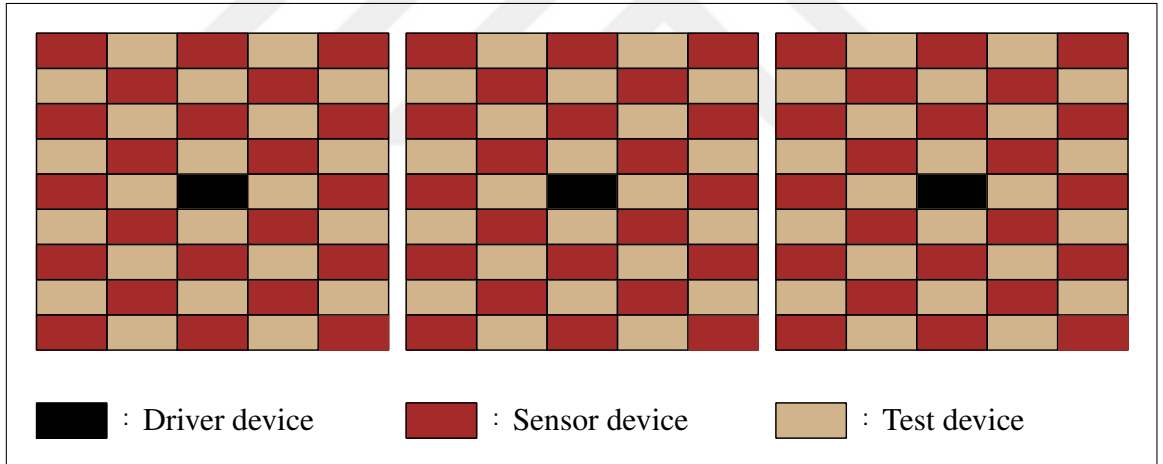


Figure 3.2. Common-centroid placement of sensor and test devices.

Fig. 3.2 shows the abstract view of three-stage leakage sensor built with $m = 22$ segments of sensor devices and one driver device in the center of each stage. Also, a 66-unit supplementary MOSFET sharing a common centroid with the driver and load devices of all ring-oscillator stages was also integrated for independently determining I_{off} and η from MOSFET sub-threshold characteristics. f was extracted by monitoring the voltage waveform with an on-chip analog unity-gain buffer attached to one of the stages of the ring oscillators.

Shown in Fig. 3.3 are the voltage waveforms monitored on one of the test dies. They

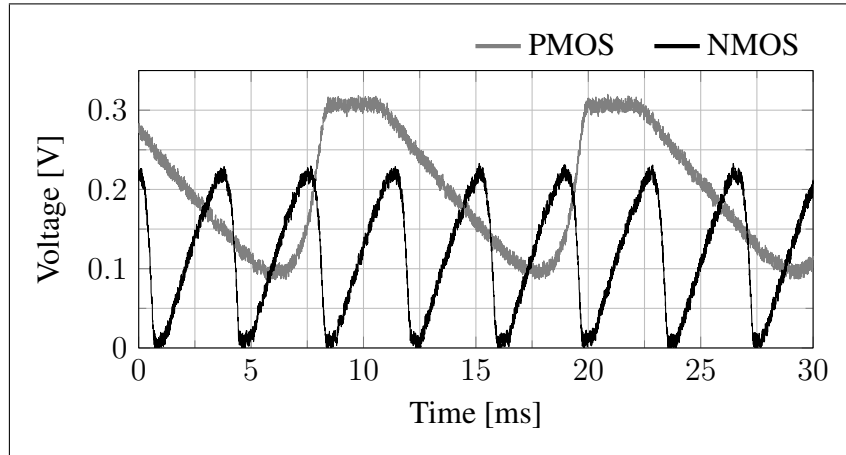


Figure 3.3. Measured leakage-sensor waveforms.

obviously match the simulated waveforms shown in Fig. 2.14(b) and Fig. 2.15(b). Sensitivity of f to V_{DD} was also experimentally evaluated. Relative sensitivity per 100 mV variation in V_{DD} was 10.6 percent in NMOS and 6.6 percent in PMOS. Independent tests on I_{off} indicate that this mild sensitivity is mainly due to the dependence of I_{off} itself on V_{DD} .

The linear relationship predicted between f and I_{off} was tested on the PMOS and NMOS sensors of different test dies. In order not to interfere with oscillator operation while performing these tests, I_{off} was characterized on additional unit devices having a common centroid with the sensor devices. The result is presented with a scatter plot in Fig.3.4 and summarized in Table 3.2. The conversion rate f/I_{off} had a mean value 194 Hz/pA in NMOS and 224 Hz/pA in PMOS. Since the measured values of f and I_{off} were associated with different devices, the precision of the conversion rate was not perfect. Still, the relative standard deviation of its die-to-die distribution was only 16.6 percent in NMOS, and 16.4 percent in PMOS.¹

The correlation between f and I_{off} is calculated as $f \propto I_{offn}^{0.62}$ in PMOS sensors and $f \propto I_{offn}^{0.95}$ in NMOS sensors. Comparing with the results of Chip-1, it is obvious that common centroid placement of sensor and test devices helps to improve the correlation between f and I_{off} . Since the correlation between f and I_{off} in PMOS sensors is still lower compared to that of NMOS sensors, sub-threshold transfer characteristics of NMOS and PMOS devices

¹One outlier (Sample #3) beyond 2σ was excluded from the PMOS range.

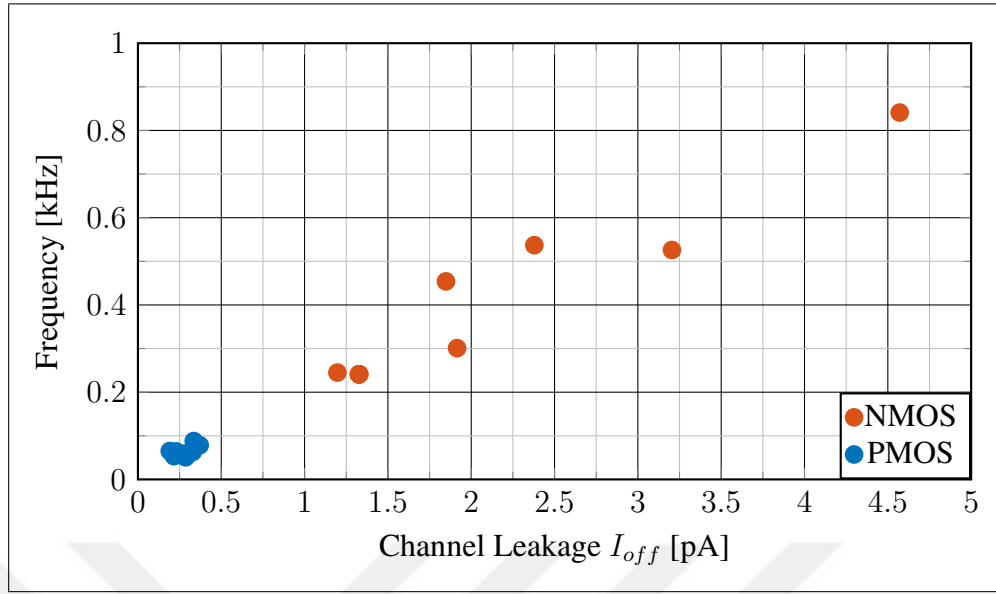


Figure 3.4. Frequency vs. channel-leakage scatter in Chip-2.

Table 3.2. Chip-2 f vs. I_{off} scatter.

NMOS	I_{off} [pA]	f [Hz]	PMOS	I_{off} [pA]	f [Hz]
Sample #1	1.20	245	Sample #1	0.23	64.3
Sample #2	1.85	454	Sample #2	0.37	78.4
Sample #3	2.38	537	Sample #3	0.19	65.1
Sample #4	4.57	841	Sample #4	0.31	58.6
Sample #5	1.92	301	Sample #5	0.33	88.1
Sample #6	3.20	526	Sample #6	0.22	53.3
Sample #7	1.33	241	Sample #7	0.23	57.1
Sample #8			Sample #8	0.28	59.3
Sample #9			Sample #9	0.33	63.2
Sample #10			Sample #10	0.29	50.8

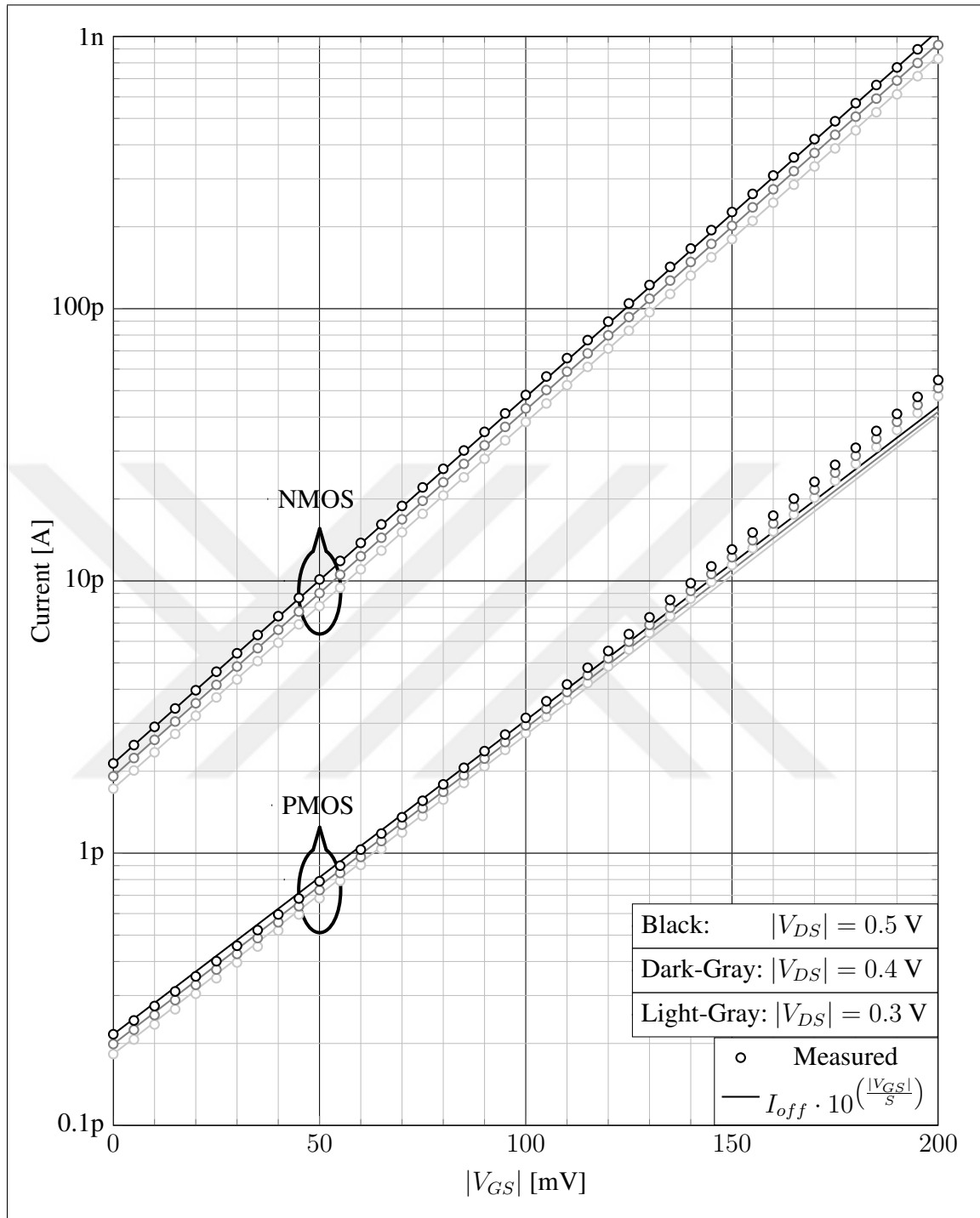


Figure 3.5. Experimental I_D vs. V_{GS} of MOS devices.

are measured with different drain to source voltages. The result is plotted in Fig. 3.5.

It can be clearly seen from Fig. 3.5 that NMOS device current - voltage characteristics perfectly fits into the equation defined by sub-threshold regime. PMOS devices, on the other

hand, exhibits a slight deviation from the equation as the gate-source voltage exceeds 100 mV in magnitude. In other words, if the equation is fitted using the data where $|V_{GS}| > 0.1$ V, the measured data at $|V_{GS}| = 0$ V would be greater than the value predicted by the sub-threshold equation. This shows that there is an additional leakage current which is comparable with channel-leakage when $|V_{GS}| < 0.1$ V. This term is the junction leakage which defines the current that is injected from bulk to drain of PMOS device. Since the same junction leakage in NMOS devices is smaller compared to channel-leakage, NMOS sensor does not suffer from this effect.

Stage capacitance C , as estimated from (2.33) for $m = 22$ and the measured values of η and f/I_{off} , was 255 fF for NMOS and 196 fF for PMOS. These rather large capacitances are attributable to the common centroid placement of unit devices inside individual wells.

3.2. VLC RECEIVER BLOCK

Experimental results of Chip-1 show that the voltage swing of the photodetector output is not sufficient to be rectified. Fig. 3.6(a) shows the proposed solution together with the peak-detector rectifier. The source-bulk terminals of PMOS devices are connected to a positive photovoltaic converter rather than the ground. The small-signal trans-resistance parameter is still given by (2.37) with a greater value of $r_o || r_d$ due to PMOS devices operating now with higher overdrive voltage at the operating point. The swing of v_{PD} , therefore, increases at the pass-band.

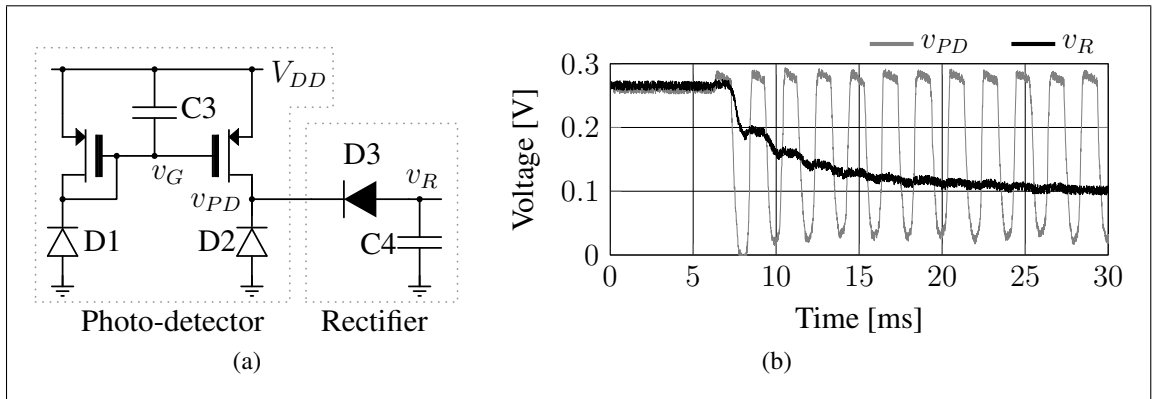


Figure 3.6. (a) Proposed VLC receiver. (b) Experimental waveforms v_{PD} and v_R .

An experimental waveform of v_{PD} is displayed in Fig. 3.6(b). Notice the dc value due to a constant 1 mW/cm^2 irradiance prior to the activation of downlink at $t = 6 \text{ ms}$, and the $500 \text{ Hz}/265 \text{ mV}$ peak-to-peak time-varying signal resulting from 35 percent modulation of the irradiance thereafter. Fig. 3.6(b) also includes the binary signal v_R generated from v_{PD} by the rectifier section built with the combination of diode D3 and capacitor C4. The binary levels of this signal are expanded to the photovoltaic supply voltages V_{DD} and V_{SS} , and the outcome v_{SEL} is used for controlling a multiplexer which makes a selection between NMOS and PMOS leakage sensor.

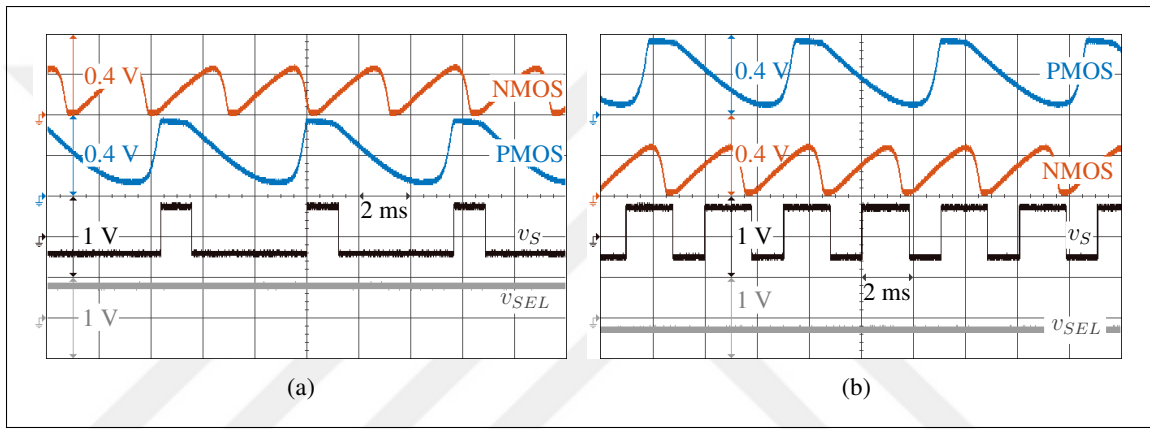


Figure 3.7. VLC receiver results: (a) PMOS selection. (b) NMOS selection.

Shown in Fig. 3.7(a) and (b) are experimental waveforms of the multiplexer control signal v_{SEL} , multiplexer output signal v_S and the output signals of NMOS and PMOS leakage sensors. Notice the shifting of the repetition frequency from 177 Hz to 330 Hz as the PMOS sensor is replaced by the NMOS sensor followed by the transition of v_{SEL} from photovoltaic-high to photovoltaic-low.

3.3. LEVEL SHIFTER BLOCK

Level shifters in the proposed leakage monitor architecture are used to (a) elevate the photovoltaic signal created by the channel leakage sensor to the boosted voltage level for driving the UWB radio (b) elevate the photovoltaic signal created by the comparator to the boosted voltage to control the switch used for separating the two storage capacitors during transmission and connecting them back during charging phase (c) elevate the photovoltaic

signal created by the analog chain to the boosted voltage for discharging the capacitors of the voltage divider in the beginning of each charging phase. Based on these considerations, level shifters play a critical role in leakage monitor for proper operation of analog chain and radio. These blocks become dysfunctional if the level shifters do not operate properly.

When the charge pump in Chip-1 is monitored alone, it was observed that its output can reach to a maximum voltage of 3.4 V. When the preliminary version of the level shifters were powered by the charge pump, however, the same output was stuck at 0.6 V. In the most possible scenario, the level shifter that controls a load which emulates the radio has created an incorrect output. This causes continuous connection between load and charge pump, which prevents the voltage on storage capacitor to increase.

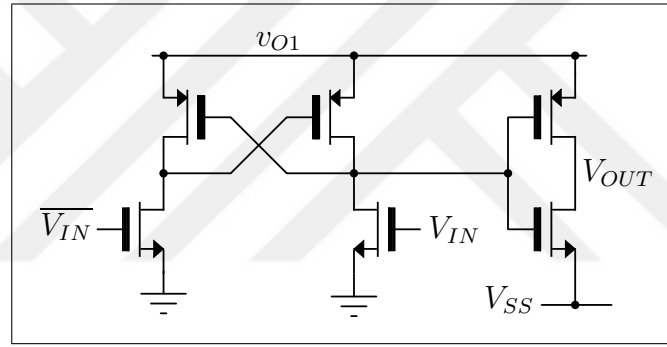


Figure 3.8. Electrical schematic of level shifter.

Also the capacitive divider in Chip-1 has exhibited dysfunctionality. Since the level shifters can not discharge the capacitors of the divider, the output of charge pump is therefore can not be controlled. This causes the transmission phase of monitor not to start, leading to operate in charging phase only. Due to the limited number of pins, there were no discrete replica of level shifter in Chip-1. But the incorrect functionalities of voltage divider and radio emulator point a common element, that is, the level shifter. With these findings in hand, electrical schematic of level shifter has been reviewed and its functionality was simulated under different process corners.

Shown in Fig. 3.8 is the electrical schematic of cross-coupled level shifter which provides lower-power consumption compared with the current mirror structure. One disadvantage of the cross-coupled structure is the weak pull-down devices as the supply voltage reaches

down to one threshold voltage. [42]. This problem can be solved by using low-threshold devices for the pull-down devices which comes at a cost of increasing power consumption.

Photovoltaic binary-high signal V_{IN} applied at the input is elevated to binary-high at boosted voltage level v_{O1} and appears as V_{OUT} . If the input signal is photovoltaic binary-low, it is not converted to any voltage level and is used directly as it is. The key factor here is the unregulated voltage level v_{O1} created by the charge pump. As the photovoltaic converters get illuminated, this voltage starts from 0 V to a defined high level where the radio transmission begins. As the transmission starts, same voltage begins to decrease until it reaches down to a defined low level that ends the transmission phase. As long as the sufficient amount of illumination exists, the voltage v_{O1} changes between the high and low levels that control the radio transmission.

The preliminary version of the level shifter with a photovoltaic binary-low signal at the input was simulated as the charge pump increases the voltage v_{O1} . The waveforms, v_{O1} and V_{OUT} are plotted as a function of time and shown in Fig. 3.9(a).

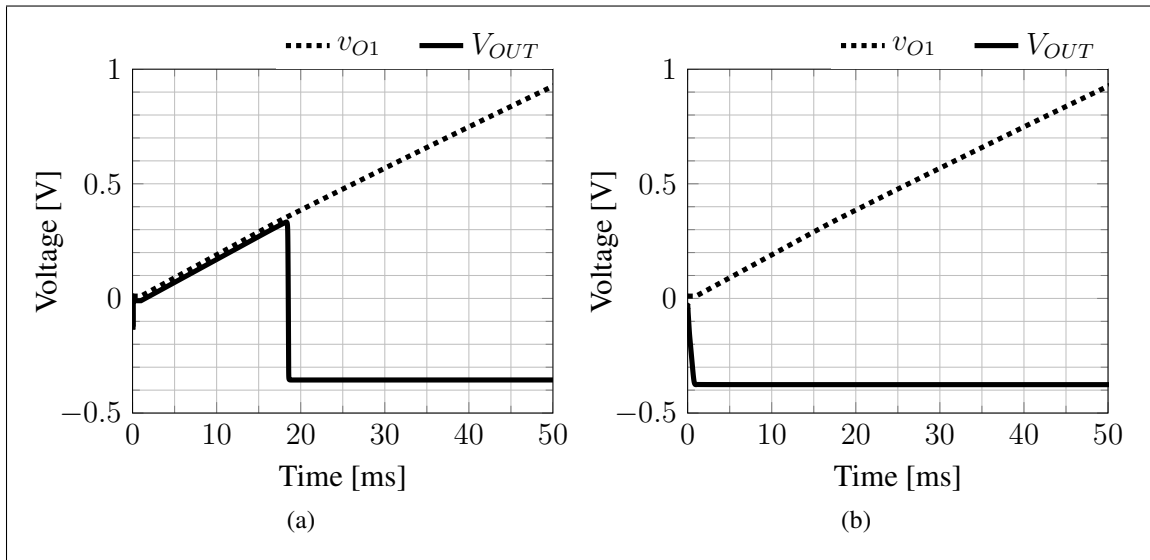


Figure 3.9. v_{O1} and V_{OUT} in (a) Chip-1. (b) Chip-2.

The level shifter generates incorrect output until v_{O1} reaches 0.35 V. As v_{O1} exceeds that value, the level shifter generates correct value at its output. Considering the threshold voltages of core devices in the process library, a gate to source voltage of 0.4 V is considered

as a near-threshold region. This causes any pull-down device driven with V_{OUT} to leak more current than its off-state leakage. This causes the switches which are assumed as open to be closed, leading a complete failure of the system.

This problem was observed in Chip-1 tests, with the failure of capacitive divider. This suspicious situation has nearly become absolute with the failure of charge pump which exhibits an excellent performance when unloaded with the level shifter and radio emulator. To overcome the problem in Chip-2, the devices in the level shifter have been resized so that, such a problem never exists in all process corners which is verified with simulations. Physical design of the level shifter is based on low- V_T I/O devices of $W = 3 \mu\text{m}$ and $L = 0.5 \mu\text{m}$ for pull-down devices, and regular- V_T I/O devices of $W = 0.24 \mu\text{m}$ and $L = 3 \mu\text{m}$ for pull-up devices. The output of the newer version of level shifter is plotted in Fig. 3.9(b). As the simulation begins, the output settles down to binary-low value just as expected.

Two precautions have been taken against the possibility of failure in the second version of level shifter. First, the supply pin of level shifter was detached from v_{O1} and tied to a dedicated pin. The reason for the separation is to spare the charge pump output from a power-hungry circuit which consumes much more energy than expected. If the level shifter operates just as expected, its supply pin is connected to v_{O1} with off-chip connection.

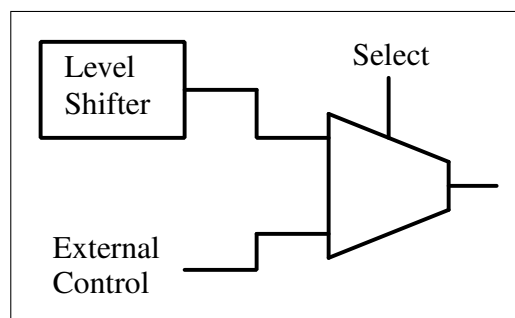


Figure 3.10. Level shifter integrated with a multiplexer.

Second precaution taken against the possibility of complete failure in level shifter even with the dedicated supply pin, is a multiplexer whose select pin is controlled via off-chip. In the case of a failure, the multiplexer deactivates the level shifter and an external control signal takes over the job.

of the width of the antenna is based on (a) 160 μm of maximum scribe width specification and (b) 80 μm of spare for the photovoltaic converter placement. The length of the antenna is 4600 μm which is the all available area in a three-chips wide footprint. As observed in Fig. 3.1 with the colored region, all circuits of the monitor are physically enclosed by this antenna. Also, all units other than photodiodes and MIM capacitors are covered by a three-layer metal shield for preventing light penetration, and are encircled with multiple guard rings to prevent photo-generation. The effect of metal shield is also included in the 3D-EM model whose closer view is shown in Fig. 3.11(b).

3D-EM model of the antenna was simulated using a commercially available 3D-EM simulator for obtaining the variation of inductance and Q-factor with frequency. Shown in Fig. 3.11(c) is the equivalent lumped model of the antenna used for co-simulation with the UWB radio unit.[43]. Lumped element values of Fig. 3.11(c) were calculated with an optimization routine to find an accurate representation of 3D-EM model. Fig. 3.11(c) and (d) show the comparison between EM and lumped model by plotting the inductance and Q-factor respectively. These plots indicate that the lumped model obviously match the EM model and can be used for co-simulation with the UWB radio.

3.5. UWB RADIO BLOCK

UWB Radio consists of an LC tank and a cross-coupled pair (XCP). Since the inductor and capacitor of the tank is not ideal, a negative resistance unit is necessary to cancel out the resistive terms of the tank.

Shown in Fig. 3.12(a) is an LC oscillator built with an inductor, capacitor, cross-coupled of pairs of NMOS and PMOS devices and a current sink. It is also possible not to include a capacitor where the necessary capacitance is supplied from the parasitic components of inductor and XCP.[44]. A capacitor bank with digital inputs may also be added for accurately trimming the oscillation frequency. [45]

Fig. 3.12(b) shows the small-signal equivalent circuit of the XCP to derive its input

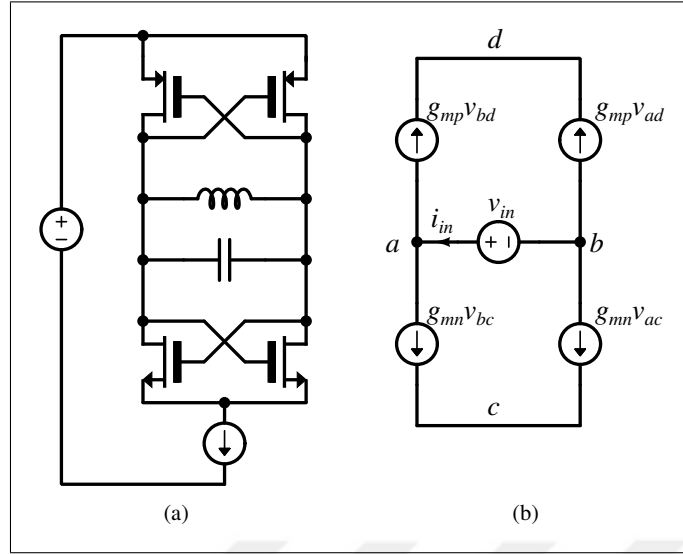


Figure 3.12. (a) LC-tank with XCP. (b) XCP small-signal equivalent circuit.

impedance. Input current i_{in} is written as

$$i_{in} = g_{mn}v_{bc} + g_{mp}v_{bd} \quad (3.1)$$

Defining the input impedance as the impedance between the nodes a and b yields

$$Z_{in} = \frac{v_{ab} + v_{cb}}{g_{mn}v_{bc} + g_{mp}v_{bd}} \quad (3.2)$$

Using (a) identical devices in NMOS XCP and (b) identical devices in PMOS XCP enables to write the equality between node voltages as

$$v_{ac} = v_{cb} = v_{ad} = v_{db} = v_{in}/2 \quad (3.3)$$

Using (3.2) and (3.3), the input impedance is written as

$$Z_{in} = \frac{v_{in}/2}{-v_{in}/2 \cdot (g_{mn} + g_{mp})} + \frac{v_{in}/2}{-v_{in}/2 \cdot (g_{mn} + g_{mp})} = -\frac{2}{g_{mn} + g_{mp}} \quad (3.4)$$

The circuit oscillates at $f = 1/2\pi\sqrt{LC}$ if the negative impedance found in (3.4) is sufficient to cancel out the losses included by the resistive terms which can be achieved by properly

sizing the XCPs and setting the appropriate value for the tail current.

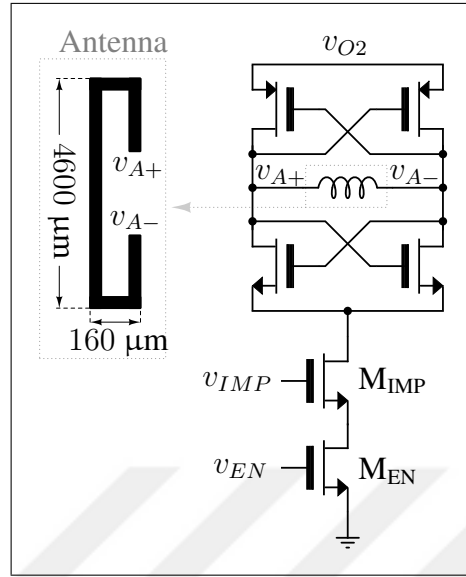


Figure 3.13. Electrical schematic of UWB radio.

Shown in Fig. 3.13 is the electrical schematic of the UWB radio unit. The thick line demonstrates the inductor-antenna unit of the radio. Its parasitic capacitance terms combined with the parasitics of the XCPs form an equivalent capacitance that is necessary for the circuit to oscillate. Physical design of UWB radio is based on I/O devices. Each cross-coupled PMOS device comprises ten copies of a low- V_T unit MOSFET of $W = 10 \mu\text{m}$ and $L = 0.34 \mu\text{m}$. As to NMOS cross-coupled devices, five and ten copies of a zero- V_T unit MOSFET of $W = 10 \mu\text{m}$ and $L = 0.5 \mu\text{m}$ were paralleled. While zero or low threshold option improves the trans-conductance of these devices, the intentional mismatch of the NMOS pair helps improve the start-up performance. Tail switches M5 and M6 were built with twenty copies of a regular- V_T unit device of $W = 10 \mu\text{m}$ and $L = 0.34 \mu\text{m}$.

Thanks to the negative gate-source voltage thus imposed on M_{EN} during boosting, the otherwise highly conductive path of the radio is prevented from leaking any significant current during the charging phase. Same gate-source voltage is equal to v_{O1} during the radio transmission. M_{IMP} drives the radio with level-shifted pulses of the sensor signal after being converted into nanosecond-wide pulses switching between ground and v_{O1} . The radio, therefore, transmits one UWB impulse for each sensor pulse it receives. The value of the oscillation frequency is important for determining the width of the impulses. Simulation

results show that the oscillation frequency of the radio is 2.7 GHz.

3.6. IMPULSE GENERATOR BLOCK

Shown in Fig. 3.14 is the electrical schematic of the impulse generator. It is built with odd-number of inverter stages as a delay-line, an AND gate, and a stage buffer for edge sharpening.

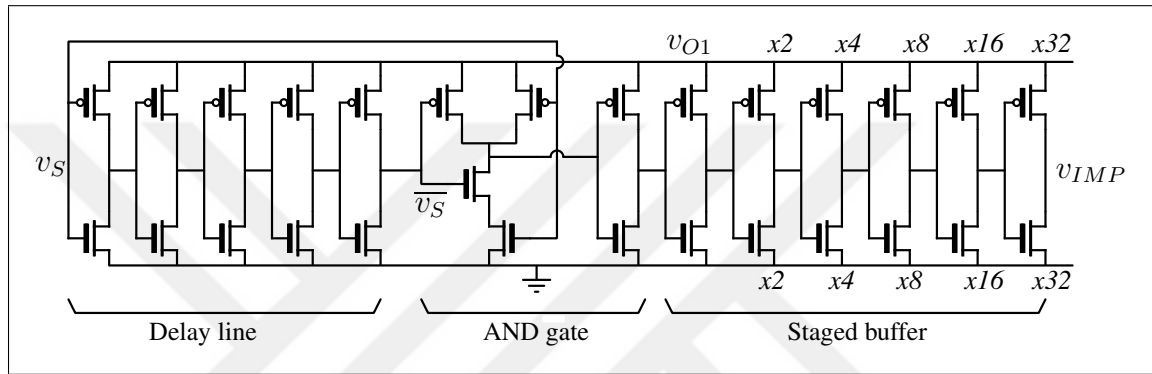


Figure 3.14. Electrical schematic of impulse generator.

Binary-high voltage applied to v_S input of the AND gate is inverted and applied to $\overline{v_S}$ input of the same gate after passing through a delay line. The logic complement of v_S is appeared at $\overline{v_S}$ after a certain amount of time due to the latency of delay line. During this time, however, both inputs v_S and $\overline{v_S}$ stay at binary-high. The output of the AND gate, therefore is binary-high during that interval. It is passed through a staged buffer to drive the capacitive input of the radio with fast edge transitions. At the end of duration determined by the delay line, $\overline{v_S}$ and therefore, v_{IMP} fall down to binary-low. With each low-to-high transition of v_S , the impulse generator, therefore, generates impulses whose width is determined by the delay line and having an amplitude of v_{O1} .

As the frequency of the UWB radio is found as 2.7 GHz, it is assumed as 2.5 GHz which is the result of a ten percent probable shift due to unforeseen inaccuracy of EM modeling of the antenna. The time interval where the radio is active was selected as ten periods which is equal to 4ns. Using this specification, physical design of the impulse generator is based on I/O devices with $W = 3 \mu\text{m}$ and $L = 0.34 \mu\text{m}$ for PMOS devices and $W = 1 \mu\text{m}$ and

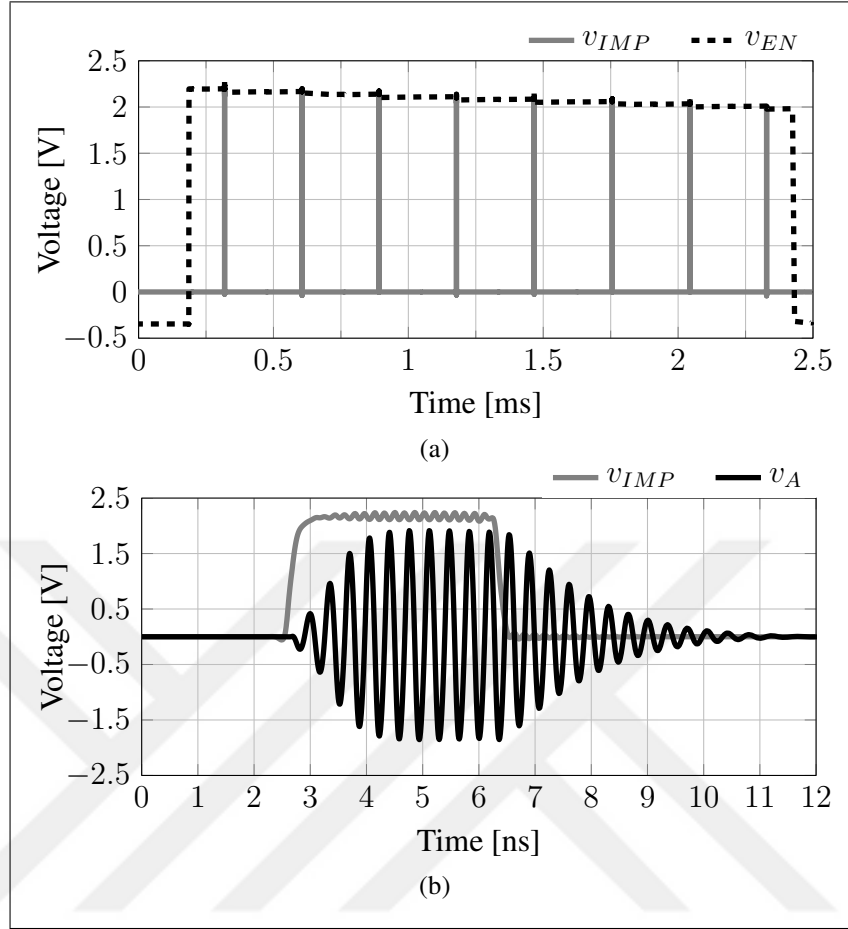


Figure 3.15. IR-UWB simulation results: (a) v_{IMP} and v_{EN} . (b) v_{IMP} and v_A .

$L = 0.34 \mu\text{m}$ for NMOS devices

Typical simulation results of impulse generator and UWB radio is shown in Fig.3.15. The gate voltage of M_{EN} that activates the radio is denoted as v_{EN} . v_{IMP} is the gate voltage of M_{IMP} which drives the radio with nanosecond-wide pulses whose repetition rate is determined by the channel leakage sensor. v_A is the voltage across the terminals of the antenna unit. As can be seen in Fig. 3.15(a), v_{EN} is binary-high with an amplitude of v_{O1} during the transmission period. Also seen is v_{IMP} , the output of the impulse generator being triggered with level-shifted pulses of channel-leakage sensor. The amplitude of the impulses are also equal to v_{O1} . A closer view of one impulse is shown in Fig. 3.15(b). The width of the impulse is approximately 4 ns. Also plotted is the voltage across the terminals of the antenna. It oscillates at 2.7 GHz with ± 2 V maximum amplitude.

3.7. SYSTEM CHARACTERIZATION TESTS

Shown in Fig. 3.16 is the architecture built in Chip-2. As compared with the initially proposed architecture in Fig. 1.1, the system in Chip-2 uses a single photovoltaic supply for positive and negative rails which are defined as V_{DD} and V_{SS} respectively. Light-gray blocks are power supplied directly by positive and/or negative photovoltaic converters. Dark-gray blocks use the supply voltage generated by a voltage booster. The dashed lines show the supply rails connected to these blocks. Considering the limited space inside scribe-lines, this modification offers improved charging rate at the expense of supply noise appeared at critical nodes. The power-supply converters of the experimental monitor comprise seven negative and sixteen positive units.^{2 3} Under full-load, these converters generate $V_{DD} = 310$ mV and $V_{SS} = -305$ mV.

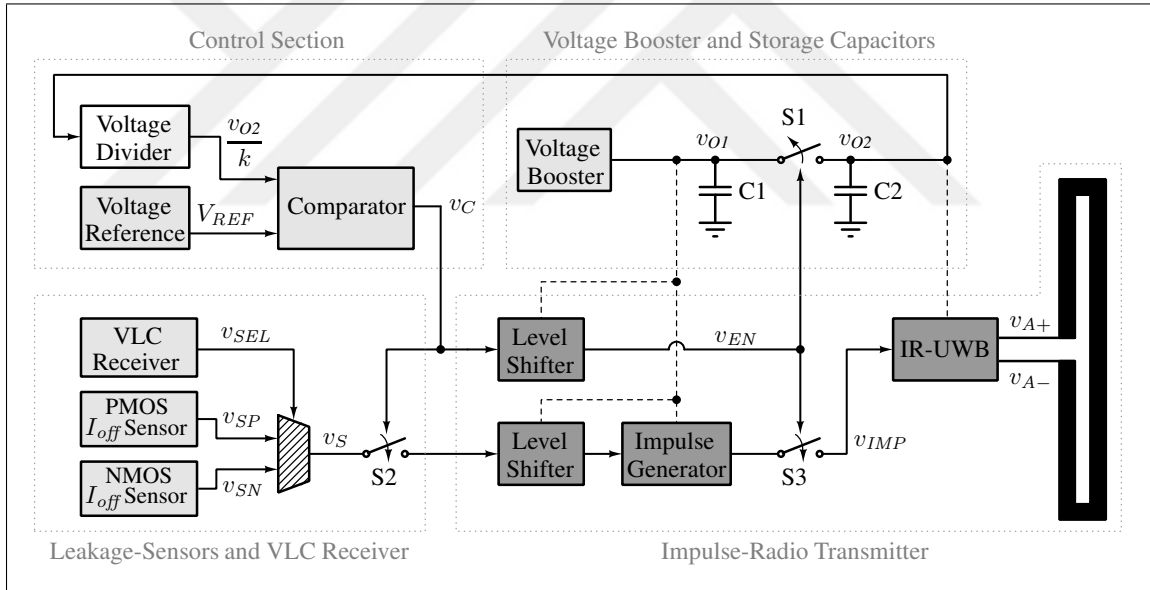


Figure 3.16. Leakage-monitor architecture in Chip-2.

The charge pump and the clock generator with its ring oscillator base are shown as a single block named “Voltage Booster”. The complementary switches SN and SN in Fig. 1.1 are realized with a CMOS multiplexer as shown in Fig. 3.16. Similar to initially proposed architecture, light-gray blocks are power supplied directly by positive and/or negative photovoltaic converters. Dark-gray blocks use the supply voltage generated by a voltage

²The negative converter bank displayed in Fig. 3.1 contains two additional units deployed as current sinks.

³Four additional positive photovoltaic converter not shown in Fig. 3.1 were also used.

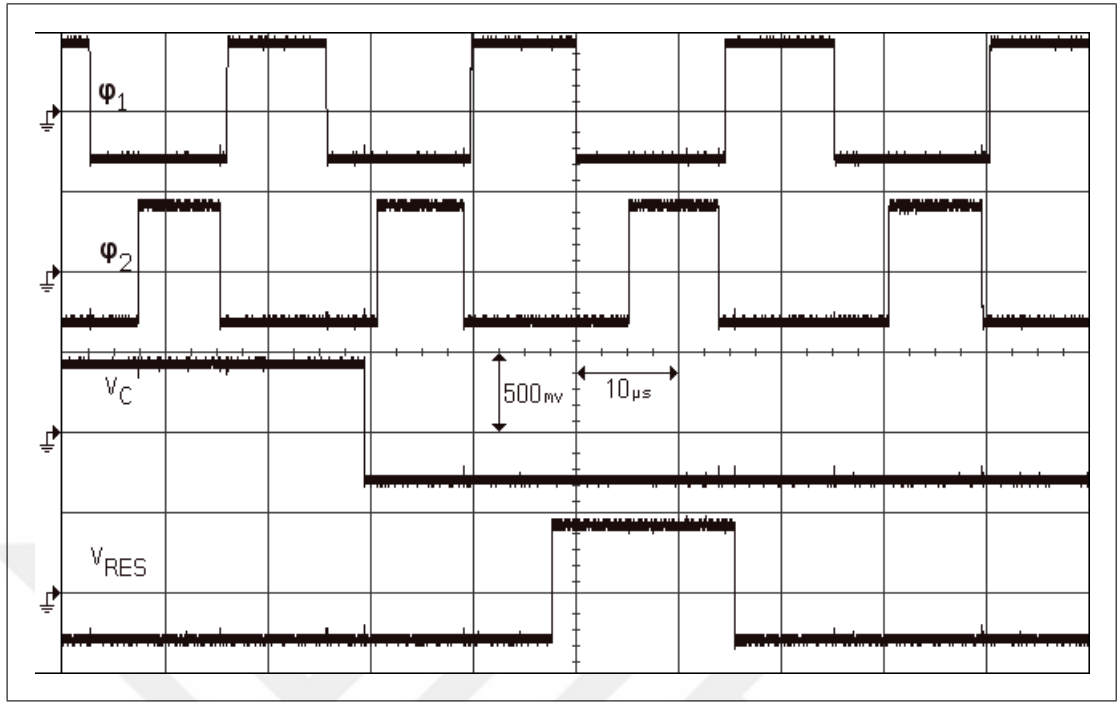


Figure 3.18. Experimental reset block waveform.

block. This block feeds a sample of v_C to a two-stage shift register built with C²MOS gates at each clock period. The non-overlapping clocks ϕ_1 and ϕ_2 are provided from the same clock generator which is used charge pumping. Two successive samples are compared by a NOR gate. The latter generates a single clock-period long binary-high pulse only if the present sample is a binary low and the previous sample is a binary high. This is how the falling edge of v_C is recognized. The pulse generated by the NOR gate is level shifted from V_{SS} and V_{DD} to ground and v_{OI} , respectively. As denoted by v_{RES} in Fig. 3.17, this level-shifted pulse opens S6 and closes the pair S4 and S5 for discharging CD1 and CD2. v_{RES} returns to ground at the end of the resetting clock period, and thus initiates a new division process by opening S4 and S5, and closing S6.

Shown in Fig. 3.18 is the experimental waveform of the reset block before being elevated with a level shifter. Also plotted are the transmission control signal v_C and the non-overlapping clocks ϕ_1 and ϕ_2 . These waveforms were read by using a staged-buffer with an external supply, similar to the technique described in Fig. 2.19. The width of the reset signal is less than a clock period which is due to jitter observed in clock signals.

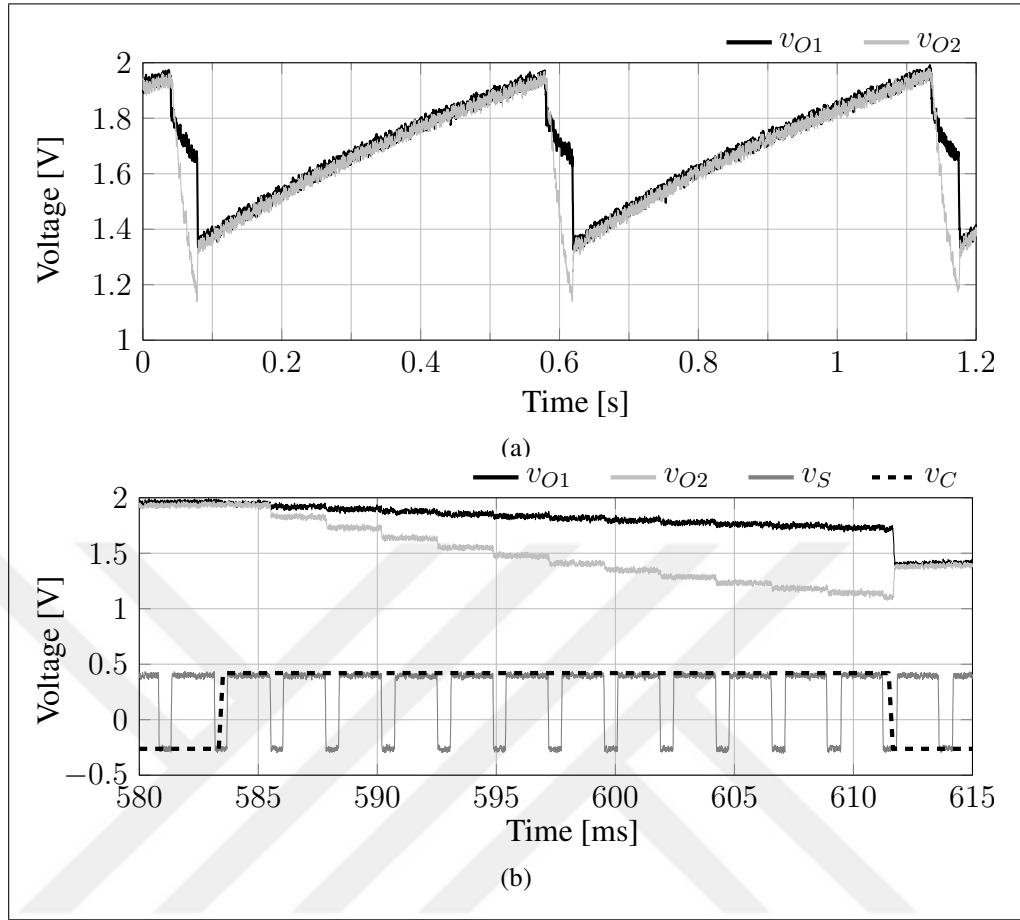


Figure 3.19. (a) Measured booster and control section waveforms. (b) Closer view together with the sensor output.

Experimental waveforms of the boosted supply voltages v_{O1} and v_{O2} are presented in Fig.3.19(a) for two successive boosting and transmission cycles captured under $700 \mu\text{W}/\text{cm}^2$ indoor irradiance. Each cycle takes 0.55 s to complete. Notice the equality of the two voltages while boosting, and their separation during transmission as v_{O1} remains relatively constant while v_{O2} declines rapidly. A closer view of the supply-voltage waveforms during the 28.1 ms long transmission event is presented in Fig.3.19(b) together with the experimental waveforms of the digitized sensor signal v_S and the control signal v_C . Since UWB radio is a power-hungry device compared to level shifters and impulse generator, v_{O1} remains relatively constant while v_{O2} declines rapidly. It is therefore important to separate the capacitors C1 and C2 during transmission for preventing level shifters and impulse generator to operate with lower voltages since the width of the pulses driving the UWB radio depends strongly on this supply voltage. Notice the passage of 12 sensor pulses and

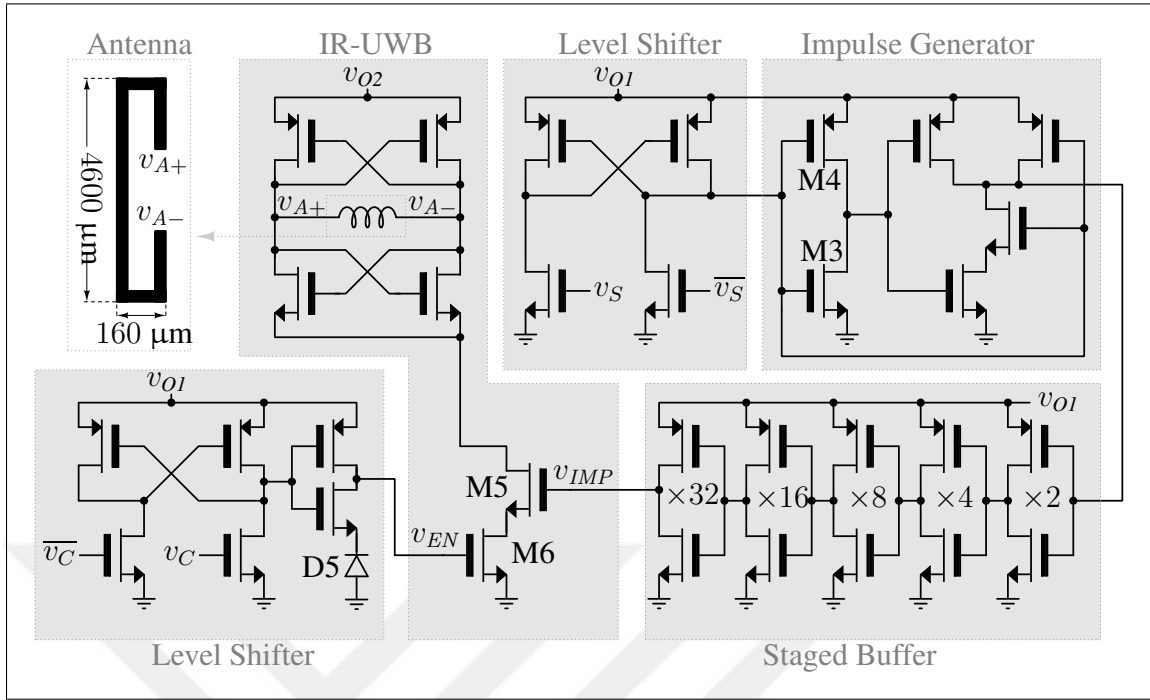


Figure 3.20. Transmitter schematic.

the step-wise decline of v_{O2} during this event. Based on the results above, it is possible to conclude that not only the control section, but also the level shifters, impulse generator and even UWB radio exhibits proper operation as predicted by the simulations. To make sure that the transmitting unit works properly, it is imperative to capture the signal that is transmitted by the radio whose experimental characterization results are discussed in section 3.7.2.

3.7.2. Transmitter and External Receiver Tests

As shown in Fig. 3.20, the transmitter section includes an impulse generator, which converts the level-shifted pulses of the sensor signal v_S into 4 ns wide pulses switching between ground and v_{O1} . The combination of M3 and M4 is a simplified representation of a delay line built with 25 cascaded inverters. Pulses formed by the impulse generator pass through a staged buffer for edge sharpening, and subsequently drive an impulse radio through a tail switching MOSFET M5. A second MOSFET, M6, implements the switch marked as S3 in Fig. 3.16. This switch is placed in series with M5 and is controlled by a level-shifted version of the comparator output signal v_C swinging between the boosted voltage v_{O1} and the negative voltage supplied by a dedicated unit photovoltaic converter D5. Thanks to

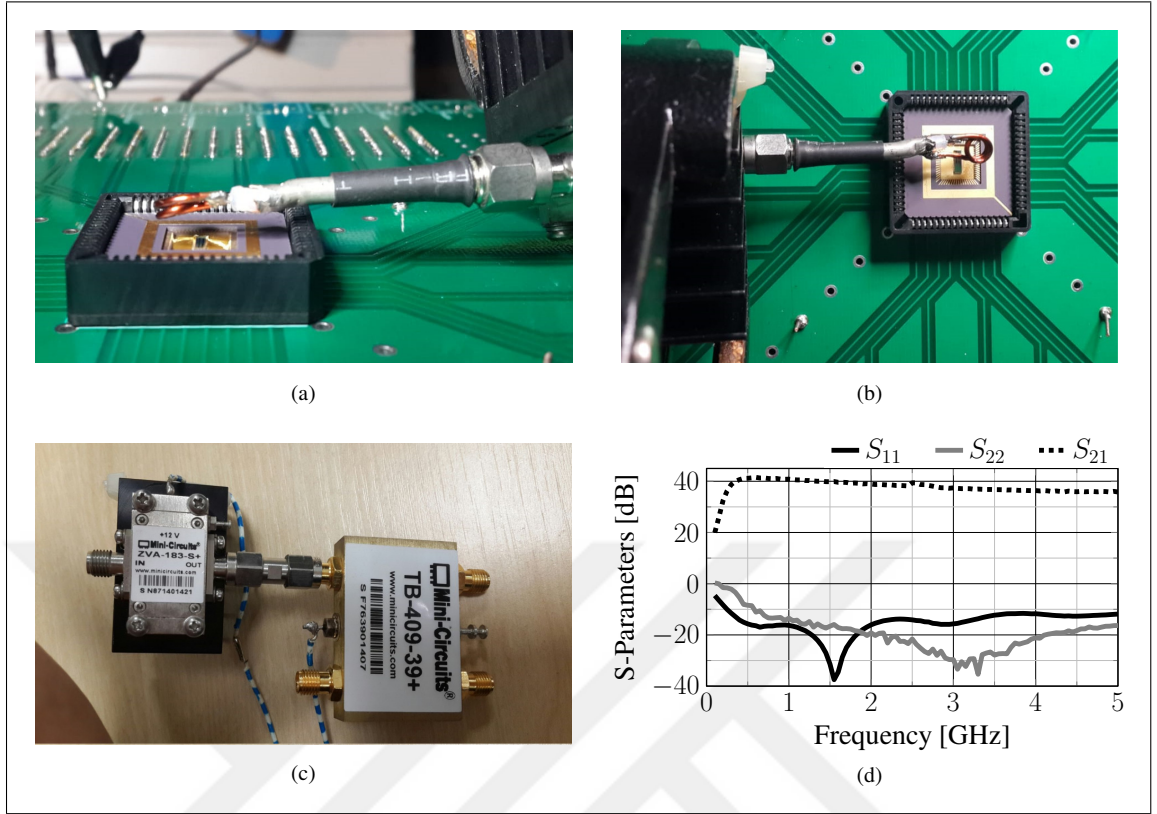


Figure 3.21. (a) RX antenna and monitor side view. (b) RX antenna and monitor top view. (c) LNAs of RX unit. (d) LNA S-parameters.

the negative gate-source voltage thus imposed on M6 during boosting, the otherwise highly conductive pull-down path of the radio is prevented from leaking any significant current. The radio differentially drives an inductive loop antenna with UWB impulses, whose repetition rate is identical to the frequency of the pulse train generated by the selected leakage-current sensor.

Since the measured voltage of C2 that feeds the UWB radio exhibits exact behavior predicted by the simulations, UWB radio is strongly believed to dissipate nanosecond-wide energy with the each pulse it receives. To make sure that the dissipated energy is used for the radiation from the antenna, a receiver unit is needed which includes an off-chip antenna followed by an amplifier stage with sufficient gain.

Shown in Fig. 3.21(a)-(b) are the side and top view of a 5 mm diameter two-turn loop antenna loosely aligned on the test chip. Two cascaded low-noise amplifiers, deployed for detecting

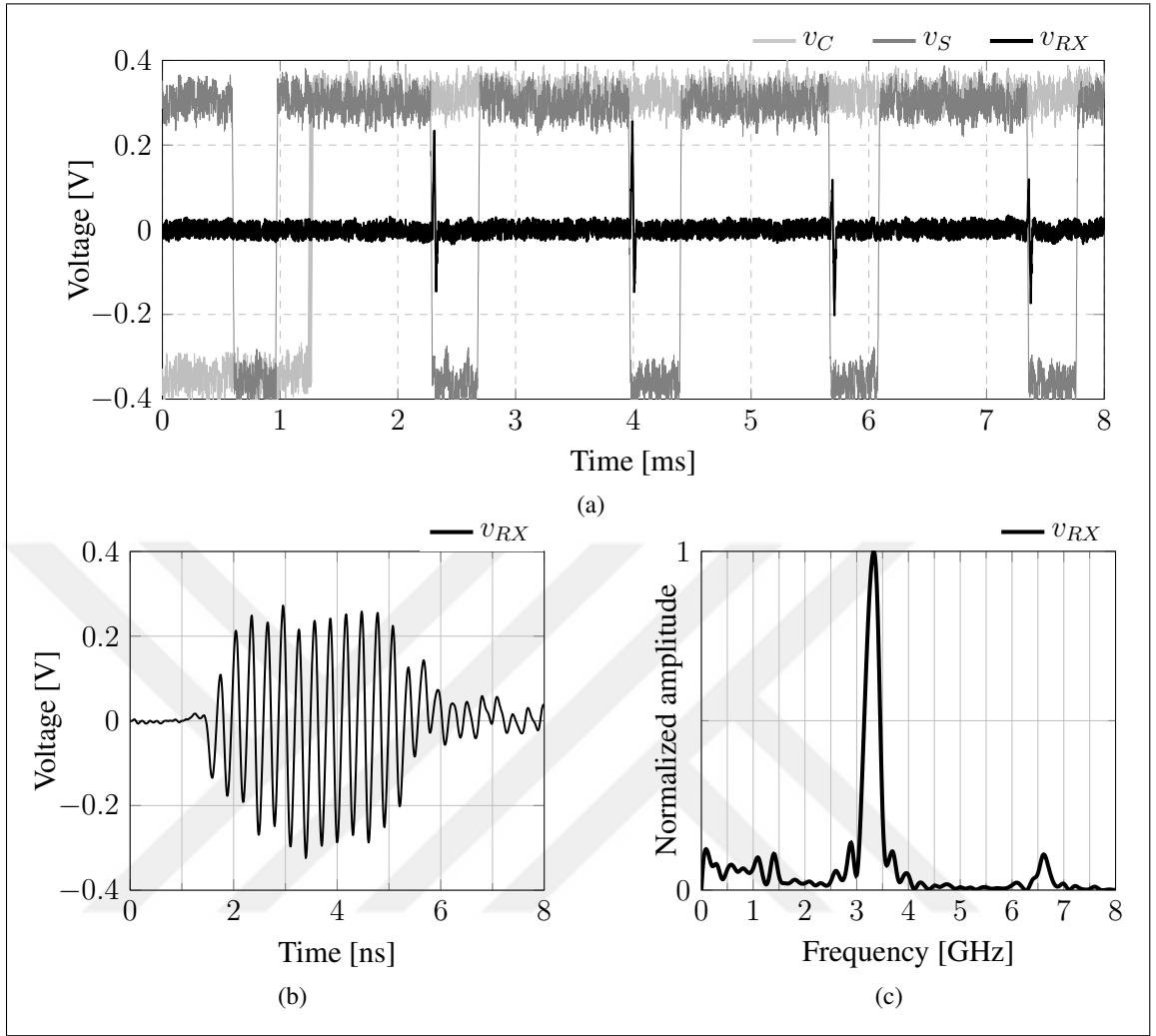


Figure 3.22. (a) Transmission control signals together with received impulses. (b) Closer view of one impulse. (c) Impulse frequency spectrum.

the UWB signal transmitted by the experimental monitor and the scattering parameters of the overall amplifier unit are shown in Fig. 3.21(c) and (d) respectively. The reverse isolation of the amplifier is not plotted since it is below -40 dB. The input and output impedance of the amplifier is near 50Ω between 1-5 GHz. Also it exhibits more than 35 dB gain over the frequency of interest.

Fig. 3.22(a) shows the received impulses waveform v_{RX} together with transmission control signals v_C and v_S . The output of the comparator v_C and the digitized sensor output v_S are at photovoltaic levels. The amplitude of the received impulses, however, depends on the distance between experimental monitor and uplink reader antenna. There is no received

impulse as long as the comparator output v_C remains binary-low. It carries one UWB impulse aligned with the falling edge of each sensor pulse v_S after the transmission enabling control signal v_C goes high.

Nanosecond-wide impulses in Fig. 3.22(a) is not shown clearly since it is plotted with the sensor output v_S that has millisecond-wide periods. Therefore, the measurement is repeated to capture one impulse by increasing the sampling rate and decreasing the time scale on the scope. A closer view of one UWB impulse thus received is shown in Fig. 3.22(b). It exhibits 4 ns-wide pulses during transmission. Fig. 3.22(c) shows the normalized frequency spectrum of one impulse. A center frequency of 3.3 GHz with 1.5 GHz bandwidth of the signal can be clearly identified in the spectrum. Considering the expectation of 2.7 GHz center frequency predicted by the simulations, obtaining a higher value of the center frequency reveals the double-counting of the parasitics when simulating the transmitter circuit.

As the test results of Chip-2 show that, the radio in the experimental monitor transmits UWB pulses at a rate of repetition frequency of the leakage sensor. Also the consecutive operation of charging and transmission phases are properly controlled with a base-band unit by accurately monitoring the voltage across the storage capacitor C2. Receiving the UWB impulses with a loosely aligned antenna removes the contacting and micro-metric alignment issues of a wafer acceptance test. Whole system including the UWB radio together with the antenna, occupies an area of $4600 \mu\text{m} \times 160 \mu\text{m}$ which is convenient to be used in scribe-line tests.

Total power consumption of the experimental monitor is calculated using (a) the power-supply port characteristics of dual-supply scheme derived in (2.14), (b) the voltage on positive and negative photovoltaic converters under full load and (c) number of photodiode units paralleled for building positive and negative photovoltaic converters. Shown in Fig. 3.23(a) is the equivalent circuit representing the channel-leakage monitor for power consumption calculation. I_{Load1} represents the total current flowing between the terminals V_{DD} and V_{SS} whereas I_{Load2} represents the current drawn from V_{DD} terminal only. This current is the summation of currents flowing through the leakage sensors, voltage reference and the tail current of the comparator.

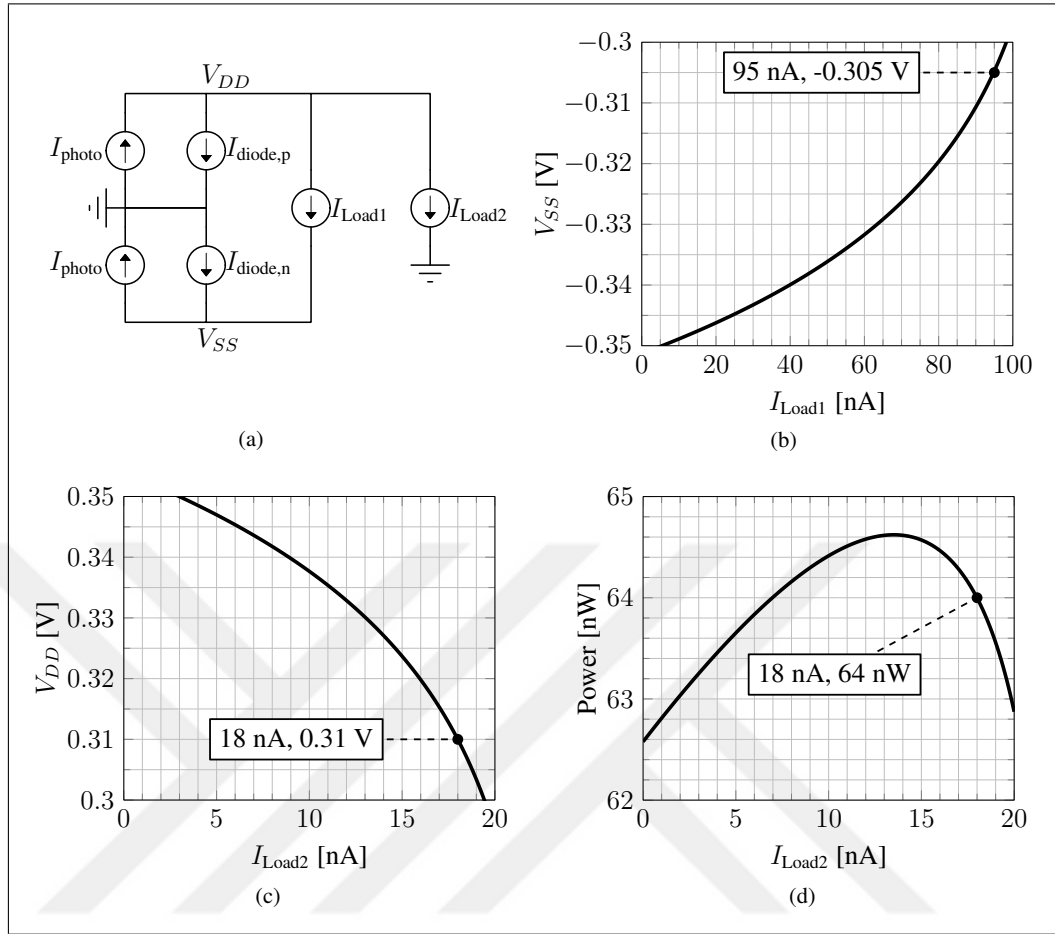


Figure 3.23. (a) Equivalent circuit for power consumption analysis. (b) V_{SS} vs. I_{Load1} . (c) V_{DD} vs. I_{Load2} . (d) P vs. I_{Load2} .

The calculation begins by setting I_{Load2} to zero and sweeping I_{Load1} . The current where V_{SS} equals -0.305 V is the equivalent current flowing between V_{DD} and V_{SS} . Using Fig. 3.23(b), I_{Load1} is read as 95 nA. Similar procedure is applied to I_{Load2} after setting $I_{Load1} = 95$ nA. The current where V_{DD} equals 0.31 V is the equivalent current flowing between V_{DD} and ground. Using Fig. 3.23(c), I_{Load2} is read as 18 nA. The total power is found as

$$P_{total} = [0.31 - (-0.305)] \times 95 + (0.31 \times 18) = 64 \text{ nW} \quad (3.5)$$

Same result can also be obtained by sweeping I_{Load2} after setting $I_{Load1} = 95$ nA. The total power where I_{Load2} equals 18 nA is read as 64 nW as can be read from Fig. 3.23(d).

4. DESIGN AND CHARACTERIZATION OF CHIP-3

Chip-2 was designed to examine the functionality of each block when connected together and powered with the photovoltaic converters only. The only block powered with an external supply in Fig. 3.1 is the multiplexer shown with hatched fill. The reason why external supply was used for the multiplexer is the low amplitude of the leakage sensor outputs. In a real application, the multiplexer is supposed to be operated with positive and negative photovoltaic converters to have a split supply configuration. Logic threshold of the multiplexer falls around 0 V if the minimum geometry devices are used. This threshold voltage may be shifted by approximately ± 0.1 V with selecting the proper device dimensions. Nevertheless, power pins of the multiplexer are connected to external supply pins in case of a situation where the amplitude of the leakage sensor output is not enough to turn on and off the switches in the multiplexer causing a complete failure of the monitor. In this case, logic threshold of the multiplexer may be slightly changed by adjusting the value of positive and negative supply voltages. During Chip-2 tests, it was observed that, when the supply voltages of the multiplexer are set equal to the voltage of photovoltaic converters which are under full load, the amplitude of leakage sensor output is enough to turn on and off the switches in the multiplexer, that is, conversion from analog to digital is properly achieved.

Another issue to be mentioned about Chip-2 is the bridged connections of photovoltaic converters and power pins. In Chip-2, power pins of all blocks operating with photovoltaic converters were connected to separate pins for off-chip access, where the photovoltaic converters were connected to their dedicated pins for the same purpose. When the tests begin, these pins were shorted with an off-chip connection and the monitor was powered if there is sufficient amount of incident light in the environment. Considering the real application where the experimental monitor is aimed to be used, there will be no external power supply and bridged connection. The routing between the blocks including the photovoltaic converters should be completed inside the chip and prototyped on silicon. When the sufficient amount of light falls into the design, the system automatically should begin to operate. This specification is the motivation of designing a fully integrated form of the monitor in Chip-3.

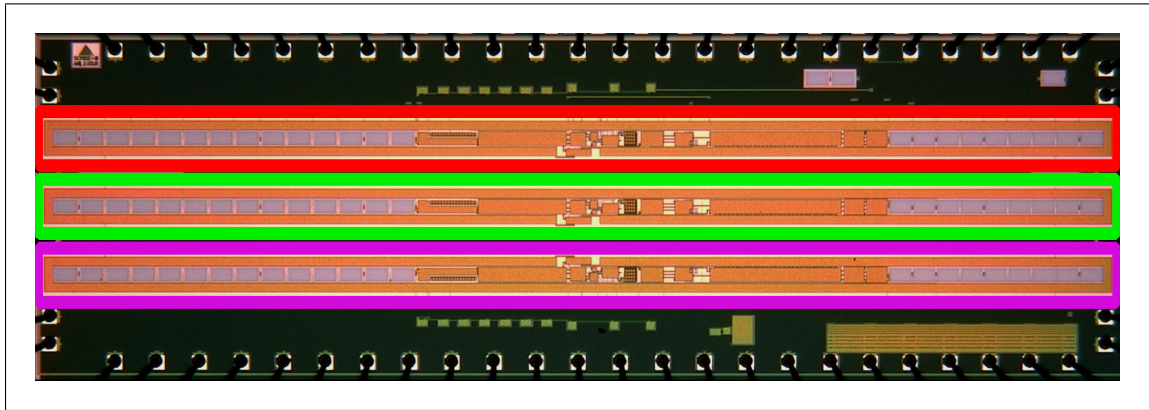


Figure 4.1. Photomicrograph of Chip-3.

Shown in Fig. 4.1 is the layout of Chip-3 fabricated in UMC 0.18 μm CMOS with a footprint of $4960 \times 1525 \mu\text{m}$. Adopting the same blocks used in Chip-2, the layout is nearly identical to Chip-2 layout with a few exceptions. In this design, all blocks including the photovoltaic converters were connected from the inside of the chip, that is, none of the blocks in Figure 3.16 used any external power supply. The length of the monitor was extended as the length of the chip to include additional photovoltaic converters. In its final form, the power-supply converters of the experimental monitor comprise fourteen positive and nine negative units two of which was deployed as current sinks. The design, therefore has a footprint of $4960 \mu\text{m} \times 160 \mu\text{m}$.

Since the chip size is $4960 \mu\text{m} \times 1525 \mu\text{m}$ which is wider than the experimental monitor, the design was laid out in 3 variants. The variants with red and magenta frame were placed in such a way that their power nets are accessible for reinforcement with additional photovoltaic converters in case of an unexpected power need. Also the critical nets of the system were buffered and connected to separate pins for monitoring in case of an unexpected failure. Another advantage of the accessibility of power nets in red and magenta-framed variants is their disabling option. They can be deactivated by shorting their power nets to the ground from the outside of the chip. The only difference between red-framed and yellow-framed variants is the connection of their power nets. In red-framed design, each block is supplied with their dedicated positive and negative photovoltaic converters. In other words, there are multiple positive and negative power rails as proposed in Fig. 1.1. In magenta-framed variant, however, all positive rails are connected in parallel and power supplied from the total number

of positive photovoltaic converters. Same is also applied for the negative supply counterpart.

Similar to magenta-framed monitor, the variant with the green frame uses only one positive and one negative supply rail, that is, all positive photovoltaic converters are connected in parallel and all negative photovoltaic converters are connected in parallel. But the variant with green frame has no physical connection with the outside world which is aimed to be the final product. Neither its critical nodes are traceable, nor the power pins are accessible from the outside of the chip. While the other (red-framed and magenta-framed) monitors are deactivated by shorting their power nets to the ground, if an UWB impulse similar to Figure 3.22 (a) is obtained with the receiver unit, the green-framed variant has been proved to operate properly. This fact will conclude that the fully autonomous channel leakage monitor which can fit into a scribe line can function properly as long as the sufficient amount of ambient light is available in the environment.

This chapter discusses the measurement results of experimental monitor prototyped in Chip-3 by presenting the measurement results of its sub-blocks which are VLC receiver, voltage booster with control section and transmitter with modified architecture of external receiver.

4.1. SYSTEM CHARACTERIZATION TESTS

The block diagram of the system architecture in Chip-3 is the same as the architecture of Chip-2 which is shown in Fig. 3.16. The only difference between the architectures of Chip-2 and Chip-3 is that the multiplexer which selects either NMOS or PMOS channel-leakage sensor is powered by the photovoltaic converters. Following three sections discuss the experimental results of VLC receiver, voltage booster with control section and transmitter with modified architecture of external receiver respectively.

4.1.1. VLC Receiver Tests

The VLC receiver keeps the PMOS sensor online by default, and replaces it with the NMOS sensor when the downlink is activated by modulating the light with a square wave. The frequency of modulation is 500 pulses per second, which is sufficiently high to distinguish

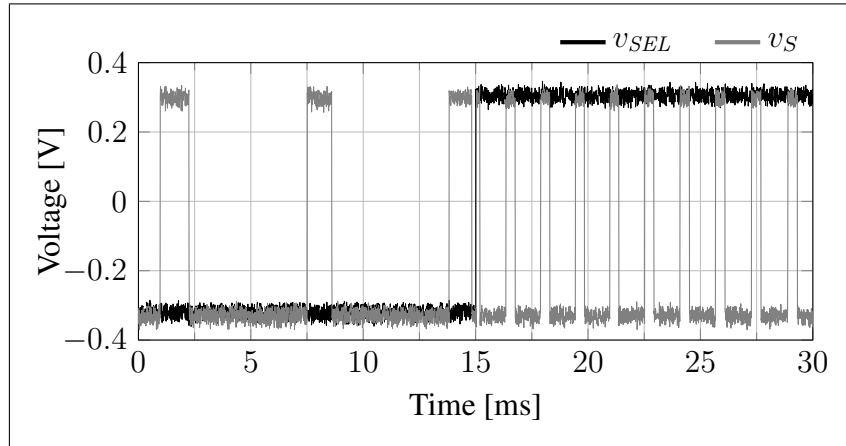


Figure 4.2. Experimental multiplexer control signal v_{SEL} and output signal v_S .

the signal from mains flicker, yet low enough to permit a low-power VLC construction.

Shown in Fig. 3.6(d) is an experimental waveforms of the multiplexer control signal v_{SEL} and multiplexer output signal v_S extracted from a test monitor accessible by wire resulting from 35 percent modulation of the irradiance. Notice the shifting of the repetition frequency from 152 Hz to 641 Hz as the PMOS sensor is replaced by the NMOS sensor.

4.1.2. Voltage Booster and Control Section Tests

Experimental waveforms of the boosted supply voltages v_{O1} and v_{O2} are presented in Fig. 4.3(a) together with the control signal v_C . These waveforms were extracted on the very same Chip-3 test monitor whose v_S -waveform is displayed in Fig. 4.2. They exhibit two successive boosting and transmission cycles captured under 1 mW/cm² indoor irradiance. The period of each cycle is 216 ms long. Notice the equality of v_{O1} and v_{O2} during boosting, and their separation during transmission as v_{O1} remains almost constant while v_{O2} declines rapidly. A closer view of the these two waveforms during a 21.6 ms long transmission cycle is presented in Fig. 4.3(b) together with the experimental waveforms of sensor signal v_S and control signal v_C . The cycle comprises 14 sensor pulses, each of which causes a step-wise 50 mV drop in v_{O2} as a result of IR-UWB activation. Note that the transmission from this monitor is terminated when v_{O2} drops to 1.1 V instead of the target 1.2 V. The difference is due to the limited precision of the hysteretic comparator and voltage reference.

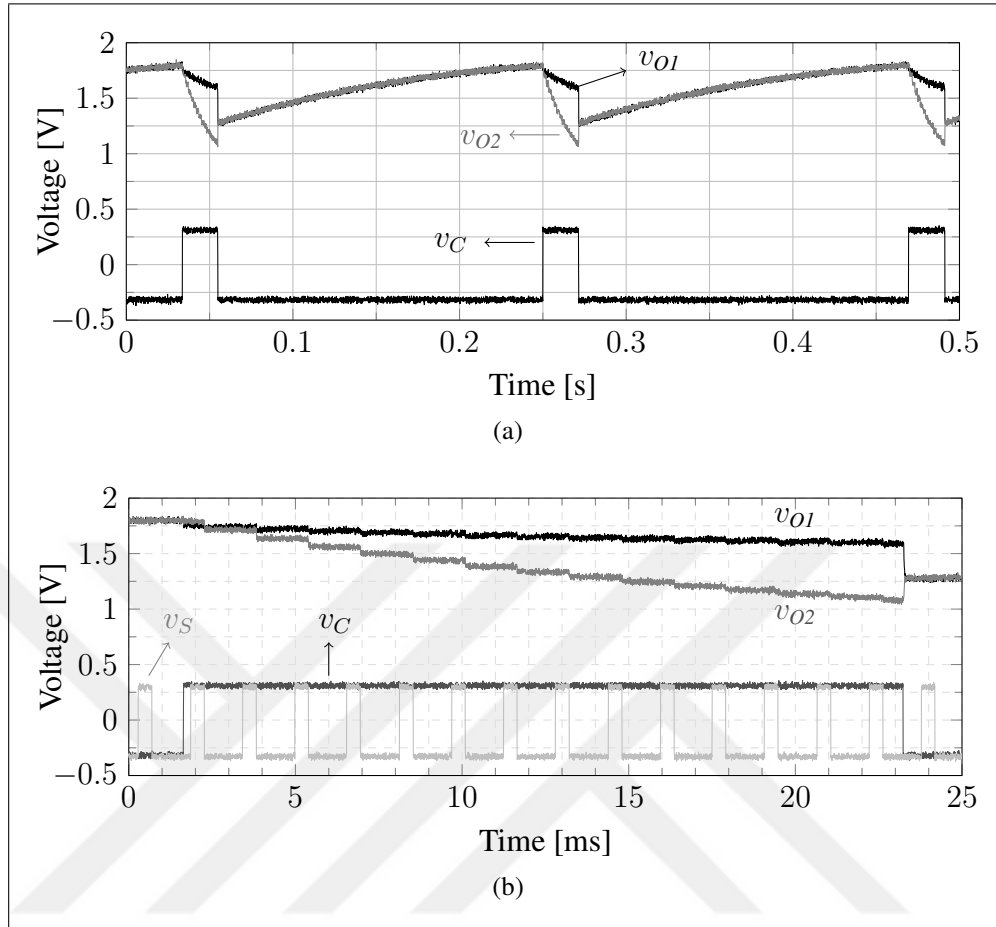


Figure 4.3. (a) Measured booster and control section waveforms. (b) Closer view together with the sensor output.

4.1.3. Transmitter and External Receiver Tests

The experimental results of Chip-2 has revealed that the received UWB impulses has 3.3 GHz center frequency. The receiver unit, therefore, was improved in such a way that the low-noise amplifiers in Fig. 3.21(c) were replaced by the low-noise amplifiers tuned to 3.3 GHz with lower noise figure.

Shown in Fig. 4.4 is one of the low-noise amplifiers utilized in this work. A detailed design flow of the low-noise amplifier of Fig. 4.4 is provided in Appendix B.

The second improvement is to place a matching network between antenna and the amplifier. Shown in Fig. 4.5(a) is the matching network which is connected at the end of the receiver

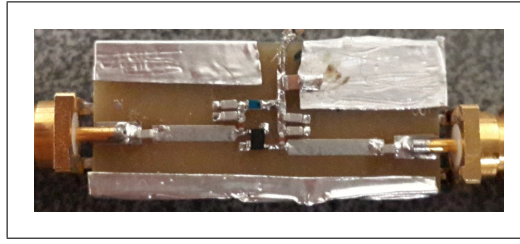


Figure 4.4. Purpose-built low-noise amplifier.

antenna unit. It is built with microstrip transmission lines and stubs for transforming the input impedance of the antenna to 50Ω at 3.3 GHz. Fig. 4.5(b) shows the input impedance measurement results of the antenna unit with and without the matching network. The input impedance of the antenna with the matching network is measured as $46.7 + j3.4 \Omega$ at 3.3 GHz which can be quite assumed to be matched to the amplifier.

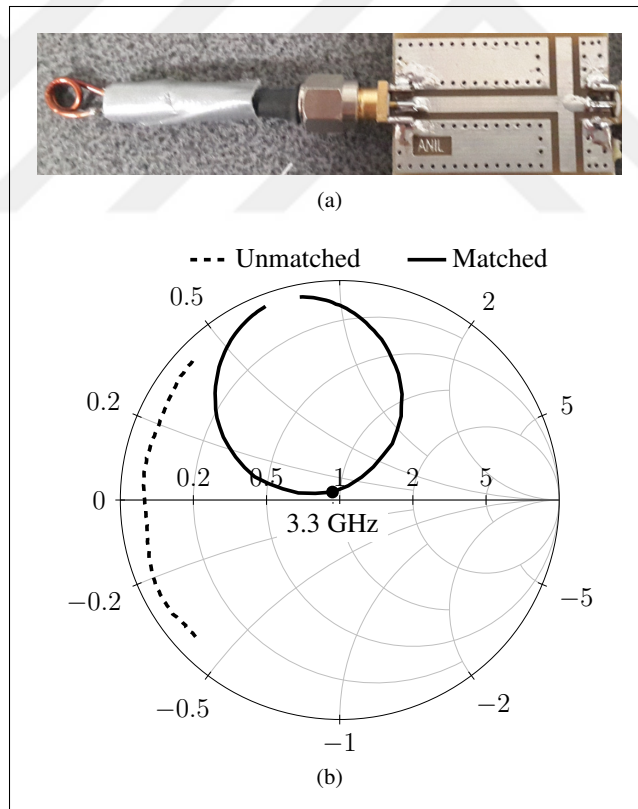


Figure 4.5. (a) Matched RX antenna. (b) Experimental input impedance.

During Chip-2 tests, a clean measurement setup for receiving UWB impulses was only obtained by performing the measurements in an anechoic chamber due to using broadband

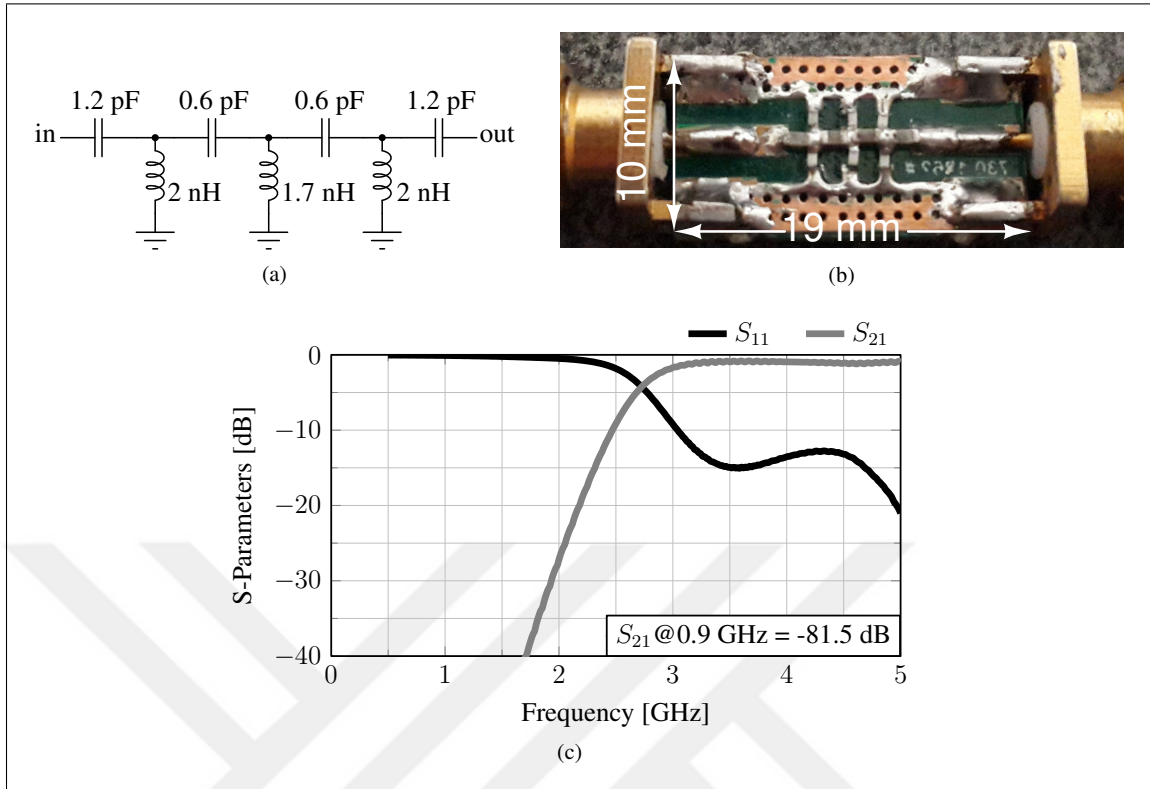


Figure 4.6. Filter: (a) Schematic. (b) Prototype. (c) Measurement results.

matched amplifiers with wideband gain which also amplify the signals from GSM, Wi-Fi and Bluetooth. This problem was mostly eliminated by designing low-noise amplifiers tuned to 3.3 GHz. As a reinforcement, a high-pass filter was designed to filter out the signals from GSM and Wi-Fi.

Shown in Fig. 4.6(a) is the electrical schematic of a 7th order Chebyshev high-pass filter utilized in this work. It was prototyped using 0603 SMD components on an FR4 substrate of 1.6mm height. As can be seen in Fig. 4.6(b), it occupies a footprint of 10 mm $\times$ 19 mm. Experimental scattering parameters of the filter is shown in Fig. 4.6(c). Practically, it suppresses the entire GSM band and exhibits 10dB attenuation at 2.45 GHz. Considering the most of the interference while performing UWB impulse reception tests is due to GSM and Wi-Fi, using such an high-pass filter enables these measurements to be performed outside the anechoic chamber.

Shown in Fig. 4.7(a) is the complete prototype of the receiver unit. It is built with the

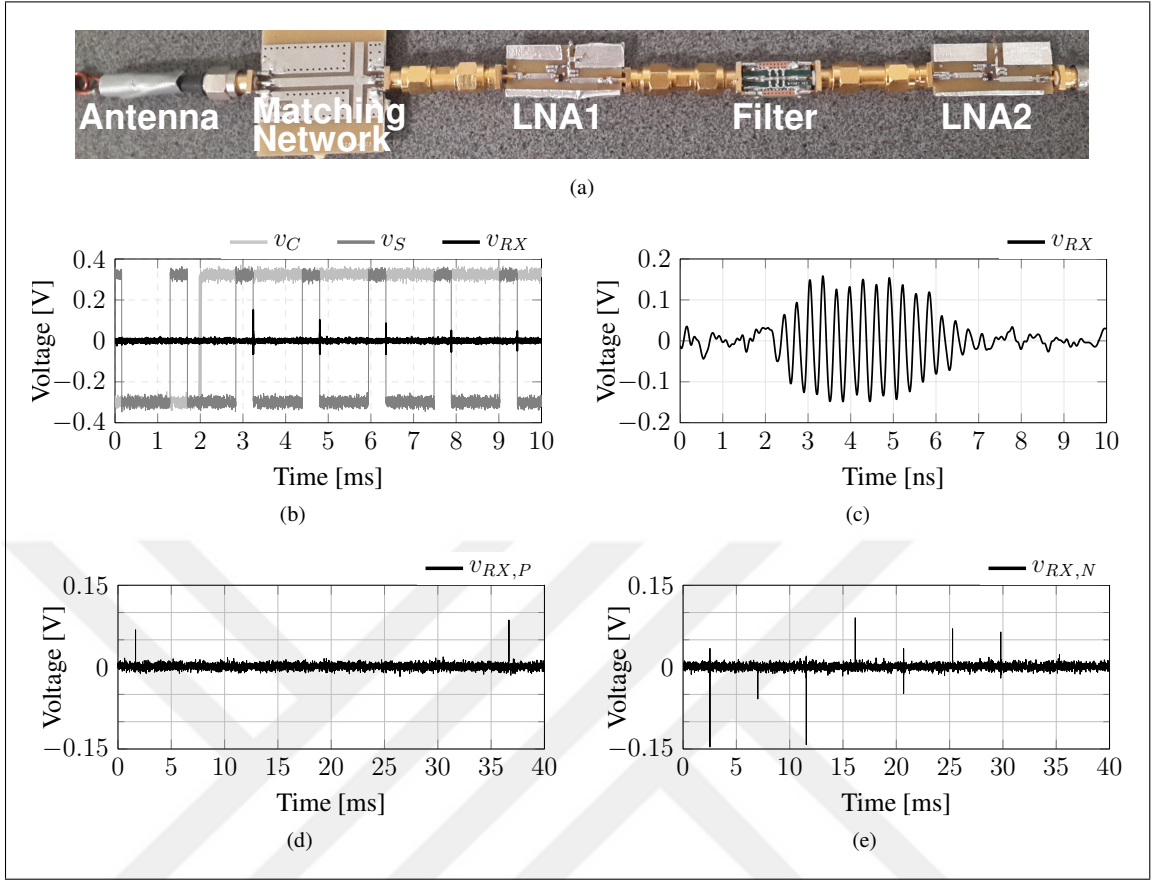


Figure 4.7. (a) Experimental RX unit. (b) TX control signals and received impulses. (c) Closer view of one impulse. (d) PMOS sensor signal received from the standalone monitor. (e) NMOS sensor signal received from the standalone monitor.

same antenna used in Chip-2 tests followed by an impedance matching network, and a two-stage low-noise amplifier with high pass filter. An experimental waveform read out with this receiver is presented in Fig. 4.7(b) as v_{RX} . It was transmitted by the very same monitor that generated the waveforms displayed in Fig. 4.2 and Fig. 4.3. It is obvious that the monitor transmits one UWB impulse aligned with the falling edge of each sensor pulse v_S after the transmission enabling control signal v_C goes high. A closer view of one UWB impulse of 3.3 GHz center frequency thus received is presented in Fig. 4.7(c).

Except for v_{RX} , all experimental waveforms displayed in Fig. 4.2, Fig. 4.3(a–b), and Fig. 4.7(b–c) were extracted by wire from analog and digital buffers integrated with a Chip-3 test monitor. The v_{RX} waveforms displayed in Fig. 3.21(b–c) belong to the same test monitor but were extracted wirelessly by the external receiver. For an ultimate indicator of

proper functionality, however, the reader is referred to Fig. 3.21(d) and (e), which display IR-UWB waveforms received from a completely wireless standalone version of the monitor integrated on Chip-3. Part-d belongs to the case of unmodulated illumination corresponding to PMOS sensor selection. Modulating the illumination switches the online sensor from PMOS to NMOS as evidenced in part-e by the 7.6 fold shift in repetition frequency.



5. CONCLUSION

The test structures placed in either scribe lines or dedicated test chips are experimentally characterized at the end of manufacturing process in a semiconductor foundry. Also measured are the critical MOSFET parameters such as channel-leakage (I_{off}), saturation current (I_{sat}) and threshold voltage (V_T). Based on the results provided by these measurements, the wafer is qualified for sorting and dicing.

Main problem of these tests is the usage of metallic probe needles which necessitate micrometric alignment and contacting which comes as an expensive practice. Cost is even higher if the parameter under test is the channel-leakage current parameter I_{off} because in that case the probe card must be built on a very high resistivity substrate in order not to distort the measurement with inadequate isolation. In most cases, a controlled environment is also necessary because alignment precision and contact pressure are sensitive to ambient temperature and environmental vibration. Precision additionally calls for periodic cleaning of probe needles from the debris accumulated as a result of repeated touchdowns. This abrasive process consumes time and limits the lifespan of the probe card

A summary of the features of the existing wafer testing techniques is presented in Table 5.1 together with the proposed architecture. Except for [8] which uses focused laser beam, all existing techniques use contacting for power transfer. Also, inductive and capacitive coupling for data transfer and focused beam for power transfer still need micrometric alignment.

This work demonstrates the viability of fully contactless scribe-line testing of channel-leakage current on wafer without any tight alignment requirement. Photovoltaic power transfer from indoor illumination, VLC downlink for sensor selection and IR-UWB uplink for readout are the instruments of this achievement. Readout is based on converting the measured leakage current into the impulse repetition frequency of IR-UWB. The processing blocks of this conversion must be designed for small footprint and low power in order to comply with the constraint of photovoltaic power generation from indoor lighting in a

very restricted area. A novel leakage-current sensor was designed in accordance with these restrictions. It offers a constant conversion rate with respect to the channel-leakage current under test, and is fundamentally insensitive to power-supply voltage and any potentially imprecise device parameter other than the channel-leakage current under test. Another novel unit is the photodetector circuit in VLC block that fullfills the ultra-low power consumption in a very restricted area.

Table 5.1. Comparison with the existing wafer testing techniques.

Feature	Steinbrueck [8]	Kim [9]	Park [10]	Yoshida [11]	Scarselli [15]	This work
Power link	Focused laser beam	Microbumps	Inductive coupling or probe needles	Probe needles	Probe needles	Ambient light
Downlink	None	Capacitive coupling	None	Inductive coupling	Capacitive coupling	Visual light communication
Uplink	Capacitive coupling	Capacitive coupling	Image rejection transmitter	Inductive coupling	Capacitive coupling	Ultra wideband impulse radio
Technology	45-nm, 65-nm, 90-nm CMOS	0.18- μ m CMOS	InGaP/GaAs HBT	90-nm CMOS	40-nm CMOS	0.18- μ m CMOS
Size	Not declared	80 μ m $\times$ 80 μ m	1.1 mm $\times$ 1.7 mm	100 μ m $\times$ 100 μ m	40 μ m $\times$ 90 μ m	160 μ m $\times$ 4960 μ m
Link distance	Large	4 μ m	25 cm	100 μ m	10 μ m	Millimeters
Horizontal Alignment	Tight due to focusing	Tight due to power link	Tight due to power link	Tight due to power link	Tight due to power link	Millimeters
Power consumption	65 μ W	TX: 4.87 μ W RX: 1.63 μ W	300 mW	TX: 1 mW RX: 4.6 mW	320 μ W	64 nW

The proposed architecture took its final form at the end of three successive chip design and verification processes. Chip-1 includes the design and characterization of individual blocks of the architecture which are photovoltaic converters, channel-leakage sensors, VLC receiver unit, ring oscillator, clock generator, storage capacitors, voltage reference, comparator and voltage divider. Based on the experimental results of Chip-1, channel-leakage sensors and VLC receiver are redesigned and placed in Chip-2. Also designed blocks in Chip-2 are the level shifter, antenna, UWB radio and impulse generator which are the elements of transmitter unit. Chip-2, therefore, includes all of the blocks of the proposed architecture. The experimental characterization of Chip-2, contains not only block level, but also system level characterization tests. Upon the validation of functionality of Chip-2, the final version of the monitor was designed in Chip-3 in a fully integrated form and its functionality was validated with the system-level tests.

Thanks to their minimalist design, all baseband blocks and VLC of the 0.18 μm CMOS implementation consume 64 nW power supplied directly by photovoltaic converters without voltage regulation. Only the impulse-radio transmitter is powered by boosting the photovoltaic voltage. Direct powering of the majority of the components also helps keep the footprint small for scribe-line integration of the entire monitor.



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APPENDIX A: CASCODED SYMMETRICAL OTA DESIGN

This appendix describes the OTA Design flow provided in [46]. The specs are listed as:

- Technology: UMC 0.18 μm
- Substrate connection: Circuit ground
- Maximum rail-to-rail voltage: 3.3 V
- Closed-loop application: Unity-gain buffer
- Maximum DC output voltage error due to gain: 1 mV
- Input signal: Sine wave of maximum amplitude $V_i = 1$ V, biased around 1 V
- Full-power bandwidth: 1 MHz when loaded with 25 pF capacitance

A.1. TOPOLOGY AND SUPPLY VALUE ESTIMATION

Since the input signal to be tracked varies between 0 V and 2 V, some devices will be subject to terminal voltages higher than 1.8 V. This situation limits to use core devices. Therefore, I/O devices are necessary. Although the devices closest to supply rails usually have smaller terminal voltages, it is beneficial to use devices with the same threshold option since it makes the design easier if common-mode and output range specs are met properly. Using I/O devices, however, brings a difficulty due to having higher threshold voltage. This problem can be minimized by using low-threshold I/O devices. Also, there must be a negative supply since the minimum input signal reaches down to 0 V. This requires to use deep n-well (DNW) NMOS devices with source-bulk short to prevent any forward biasing since the substrate is connected to 0 V.

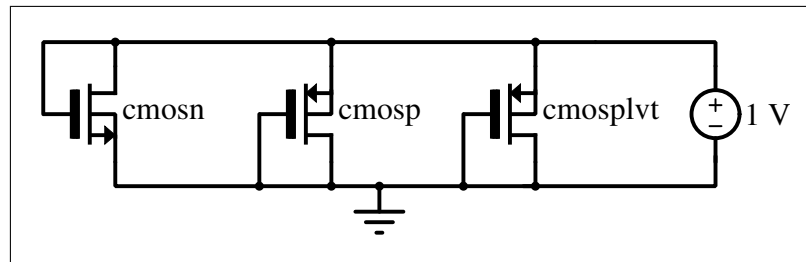


Figure A.1. Threshold voltage extraction.

UMC 0.18 μm Technology has low-threshold I/O devices but its low-threshold NMOS devices do not have deep n-well option. Three devices, namely I/O NMOS (cmosn), I/O PMOS (cmosp) and low-threshold I/O PMOS (cmosplvt) have been compared as a candidate for being the drivers of the OTA. Electrical schematic for extracting threshold voltage of each device is shown in Fig. A.1. Each device is diode-connected, source-bulk shorted and biased with 1 V DC supply. Channel widths are fixed to 5 μm which is a typical value in practice. Threshold voltage is extracted as a function of channel length and shown in Fig. A.2.

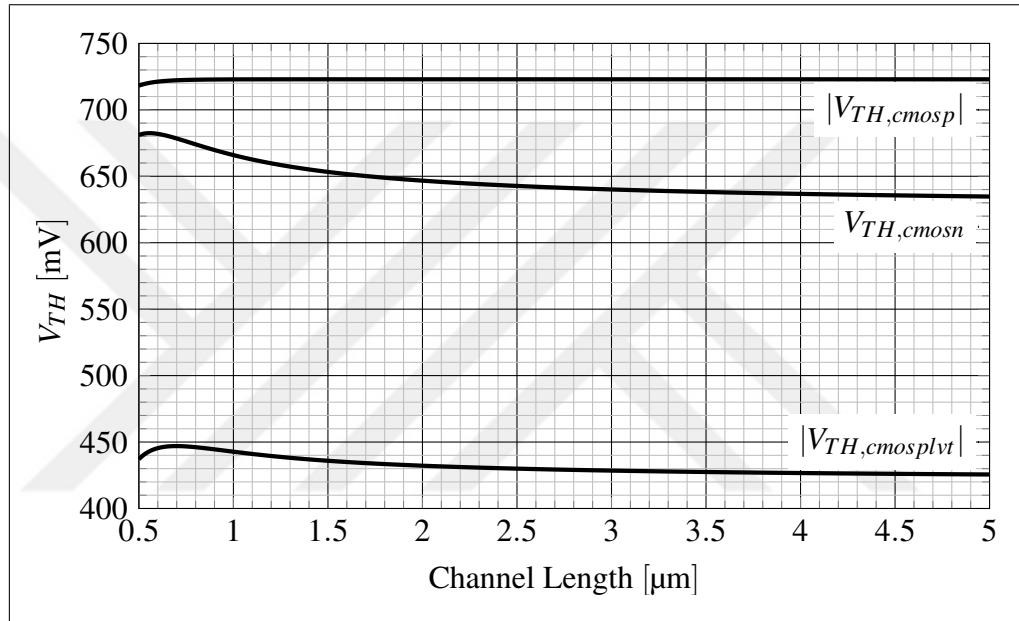


Figure A.2. Threshold voltage comparison of I/O devices.

As can be seen in Fig. A.2, it is wise to select low-threshold I/O PMOS device as the driver instead of I/O NMOS since the former has smaller threshold in magnitude roughly by $|200 \text{ mV}|$. This additional $|200 \text{ mV}|$ headroom relaxes the compliance limit of the current source. Saturation condition of drivers can be met by properly sizing drivers and cascoded sink network. Pull-up cascode network is to be realized with either low-threshold I/O PMOS or I/O PMOS devices depending on the performance of the OTA which will be explained in next section. Finally, cascoded sink network will be designed by using I/O NMOS devices with deep n-well option. Electrical schematic of PMOS-Drive Cascoded Symmetrical OTA is given in Fig. A.3.

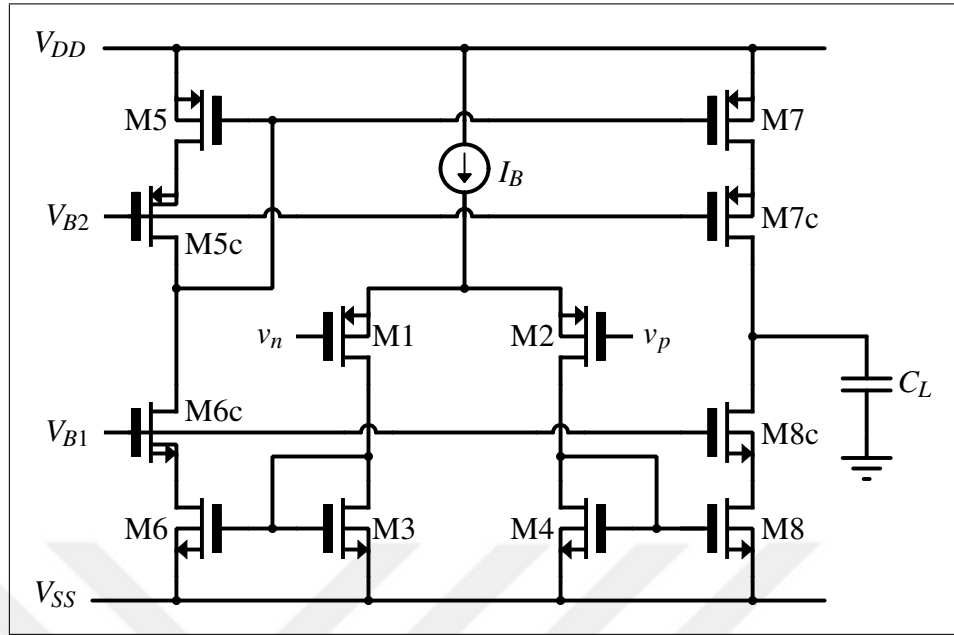


Figure A.3. PMOS-drive cascoded SOTA schematic.

A.1.1. Estimating Positive Supply Voltage

Input signal is biased around 1 V with 1 V amplitude. This much input signal makes impractical to design an OTA without slewing. As a result, Differential input range (V_{DIR}) will be smaller than the amplitude of the input. Maximum common-mode voltage will be 2 V since the closed loop application is non-inverting amplifier with a gain of 1. Common-source of driver devices will be one-gate-source-voltage higher than the maximum common-mode signal. The magnitude of driver threshold voltage is approximately $|0.4 \text{ V}|$ as can be seen in Fig. A.2. From the analytical point of view, V_{DIR} can be approximated as the overdrive voltage of drivers. Since the gate-source voltage equals to the sum of overdrive and threshold voltages, common-source voltage of drivers will have a maximum voltage of $\approx 2.6 \text{ V}$ if the OTA has $0.2 \text{ V } V_{DIR}$. Allowing 0.1 V compliance limit for the current source and 0.1 V safety margin results in at least $2.8 \text{ V } V_{DD}$. Increasing V_{DIR} will cause less negative supply voltage for a given maximum rail-to-rail voltage, hence smaller headroom for the cascoded sink devices.

A.1.2. Estimating Negative Supply Voltage

Maximum Rail-to-Rail Voltage and estimated value of V_{DD} have left -0.5 V margin for the negative supply. Such a value is enough for keeping drivers and cascoded current sink network in saturation. To see why, let us analyze common-mode input. Minimum common-mode input voltage is 0 V. As analyzed in previous section, common-source of drivers will follow the common-mode input by ≈ 0.6 V behind if V_{DIR} is selected as 0.2 V. Selecting 0.2 V V_{DIR} also means that the drain of each driver must be at least ≈ 0.2 V smaller than its source to operate in saturation. Therefore, drain of a driver is allowed to have a maximum voltage of 0.4 V. Since this node also belongs to gate of diode-connected NMOS current sink, this device will operate in $0.4 - (-0.5) = 0.9$ V gate-source voltage. As can be seen in Fig. A.2, threshold voltage of I/O NMOS devices is around 0.65 V. Such a gate-source voltage corresponds to ≈ 0.25 V overdrive voltage and ≈ 0.2 V drain-source saturation voltage. Selecting identical devices for the current sink network consumes $2 \times (0.2) = 0.4$ V headroom and there is still 0.1 V margin left. Therefore selecting $V_{SS} = -0.5$ V is suitable.

A.2. DESIGN FLOW

In order to size each device properly, performance metrics of the amplifier should be related to device parameters.

A.2.1. Output Voltage Error

1 mV output voltage error will be observed when the output voltage is supposed to be 2 V peak. The actual output voltage will be $2 \text{ V} - 0.001 \text{ V} = 1.999 \text{ V}$. Closed-loop gain of unity-gain buffer is, therefore $1.999 \text{ V} / 2 \text{ V} = 0.9995 \text{ V} / \text{V}$. Gain error is expressed as:

$$E_{gain} = \frac{1 - 0.9995}{1} = 5 \times 10^{-4} \quad (\text{A.1})$$

For a unity-gain buffer, Open-Loop Gain is therefore expressed as:

$$A_{d(0)} = \frac{1}{E_{gain}} = \frac{1}{5 \times 10^{-4}} = 2000 \text{ V/V} \quad (\text{A.2})$$

DC open-loop gain found in (A.2) is increased 50 percent for safety margin. Since the OTA is built with cascoded devices, meeting such a spec is not that hard. Increasing the gain from 2000 V/V to 3000 V/V can be realized by a small amount of increase in channel length. Therefore; $A_{d(0)}$ is selected as 3000 V/V.

A.2.2. Differential Input Range (V_{DIR})

Electrical Schematic of a PMOS-drive differential pair with source-bulk short, its small-signal equivalent circuit and trans-conductance characteristics are shown in Fig. A.4 (a), (b) and (c) respectively. When the gate voltage v_{I2} is held constant, the sensitivity of i_{d1} to gate voltage v_{I1} is defined as the trans-conductance of differential pair and using Fig. A.4 (b), derived as follows:

$$\frac{i_{d1}}{v_{i1}} = \frac{\frac{-v_s}{1/g_{m2}}}{\frac{1/g_{m2}}{(1/g_{m2}) + (1/g_{m1})}} \quad (\text{A.3})$$

Around the common-mode operation point, where $V_{I1} = V_{I2}$, trans-conductance of devices are equal. Therefore, equation (A.3) is simplified as:

$$\frac{i_{d1}}{v_{i1}} = \frac{g_{m(1-2)}}{2} \quad (\text{A.4})$$

Differential input range (V_{DIR}) is defined as a range where trans-conductance characteristic of differential pair shows a nearly-linear behavior and denoted as the difference between common-mode voltage and the intercept point on x-axis, created by the tangential line drawn at the common-mode operating point as can be shown in Fig. A.4 (c). Since the current through each device is $I_B/2$ and the slope is defined by (A.4), differential input range is

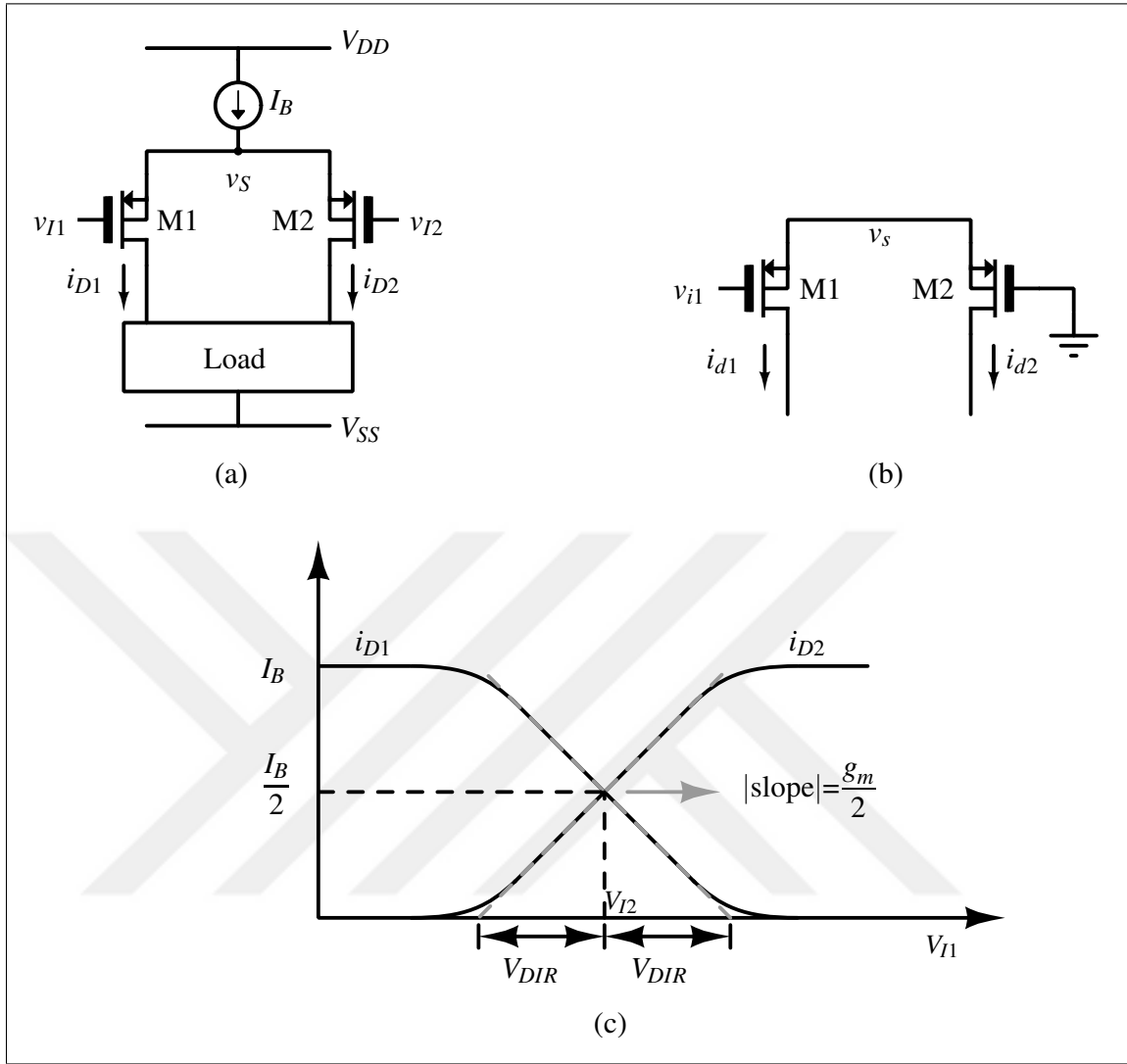


Figure A.4. a) PMOS-drive differential pair. b) Small-signal equivalent circuit. c) Trans-conductance characteristics.

defined as:

$$V_{DIR} = \frac{I_B/2}{g_{m(1-2)}/2} = \frac{2}{g_{moverid(1-2)}} \approx |V_{GS} - V_T| \quad (\text{A.5})$$

A.2.3. Full-Power Bandwidth (f_{fp})

Since the amplitude of the input signal is larger than any selected V_{DIR} within a reasonable range, OTA will inevitably slew. Its bandwidth, therefore, will be limited due to slewing.

The relation between full-power bandwidth and closed-loop bandwidth is defined as:

$$f_{cl} = f_{fp} \times \sqrt{\left(\frac{V_i}{V_{DIR}}\right)^2 - 1} \quad (\text{A.6})$$

Since the term in square-root is greater than 1, closed-loop bandwidth should be greater than the desired bandwidth.

A.2.4. Gain-Bandwidth Product

DC differential gain of cascoded symmetrical OTA is defined as:

$$A_{d(0)} = g_{m(1-2)}(R_{out1} || R_{out2}) \quad (\text{A.7})$$

where R_{out1} and R_{out2} are the output resistances of cascoded PMOS and NMOS networks respectively. Bandwidth of the OTA is defined as:

$$f_p = \frac{1}{2\pi(R_{out1} || R_{out2})C_L} \quad (\text{A.8})$$

Using (A.7) and (A.8), gain-bandwidth product is defined as the multiplication of open-loop gain and bandwidth. Since the closed-loop application is unity-gain amplification, gain-bandwidth product also equals closed loop bandwidth. Therefore, closed-loop bandwidth is defined in terms of device operating variables as follows:

$$f_{cl} = \text{GBW} = g_{m(1-2)}(R_{out1} || R_{out2}) \times \frac{1}{2\pi(R_{out1} || R_{out2})C_L} = \frac{g_{m(1-2)}}{2\pi C_L} \quad (\text{A.9})$$

Equation (A.9) can be modified in order for f_{cl} to be expressed as a function of bias current I_B . The result is as follows:

$$f_{cl} = \frac{g_{m(1-2)}/\frac{I_B}{2}}{2\pi C_L} = \frac{g_{moverid(1-2)} I_B}{2\pi C_L} \frac{I_B}{2} \quad (\text{A.10})$$

By using (A.10), bias current is expressed as follows:

$$I_B = \frac{4\pi C_L f_{cl}}{gm_{overid(1-2)}} \quad (A.11)$$

Using (A.7) with expressing $g_{m(1-2)} = \frac{gm_{overid(1-2)} \cdot I_B}{2}$, and selecting $R_{out1} = R_{out2} = R_{out}$, the output resistance of a cascoded network is defined as:

$$R_{out} = \frac{4A_{d(0)}}{gm_{overid(1-2)} \cdot I_B} \quad (A.12)$$

A.2.5. Device Sizing

A.2.5.1. Driver Devices

As can be seen in (A.5),(A.6),(A.11) and (A.12), $gm_{overid(1-2)}$ is the main determinant among the design variables. Since it is a function of overdrive voltage, electrical schematic shown in Fig. A.5 is used for extracting the design variables as a function of overdrive voltage $V_{GS} - V_{TP}$ with a single DC-sweep. As determined in Section A.1, low-threshold

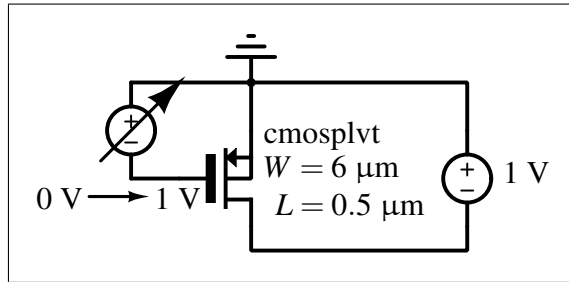


Figure A.5. Driver parameter extraction.

I/O PMOS (cmosplvt) is selected with minimum channel length and channel width of $6 \mu\text{m}$ which is far beyond the minimum limit. Gate voltage is swept between 0 V and 1 V to plot the design variables $f_{cl}, I_B, R_{out}, W_{DR(1-2)}$ and $V_{DSSAT(1-2)}$ as a function of overdrive voltage $V_{GS} - V_{TP}$ and shown in Fig. A.6 (a)-(b)-(c)-(d) and (e) respectively. Operating driver devices with more overdrive voltage is useful for lowering closed-loop bandwidth f_{cl} , hence bias current I_B as shown in Fig. A.6. Also driver geometry is and the parasitic capacitances

associated with the drivers are reduced. On the other hand, the magnitude of drain-source saturation voltage $|V_{DSSAT}|$ and the necessary output resistance R_{out} increase with negatively increasing overdrive voltage. This causes cascoded sink network to be operated at lower terminal voltages with higher device geometries which is undesirable as far as footprint and the dynamic response is concerned. A reasonable choice is $V_{GS} - V_{TP} = -0.2$ V as estimated in section A.1. With the selection of overdrive voltage and using Fig. A.6, closed-loop bandwidth f_{cl} , bias current I_B , output resistance of each cascoded network R_{out} , driver channel width $W_{DR(1-2)}$ and driver drain-source saturation voltage $V_{DSSAT(1-2)}$ is summarized as follows:

Table A.1. Design variable summary.

Parameter	Value
$V_{GS} - V_{TP}$	-0.2 V
f_{cl}	4.33 MHz
I_B	153 μ A
R_{out}	8.81 M Ω
$W_{DR(1-2)}$	26.1 μ m
$V_{DSSAT(1-2)}$	-0.216 V

As can be seen in Table A.1, channel width of driver devices is found as $W_{DR(1-2)} = 26.1$ μ m for minimum channel length $L_{DR(1-2)} = 0.5$ μ m

A.2.5.2. Cascoded Sink Network

Before sizing and biasing cascoded sink network, electrical schematic shown in Fig. A.7 is built for extracting the relation between $V_{GS} - V_{TN}$, V_{DSSAT} and sheet current $I/(\frac{W}{L})$. Gate voltage of I/O NMOS device operating with source-bulk short is swept between 0.6 V and 1.2 V. Drawn channel length is selected as $3L_{DR(min)}$ to avoid short-channel effects and the channel width is selected as 5 μ m which is a typical value in practice. When sizing cascoded

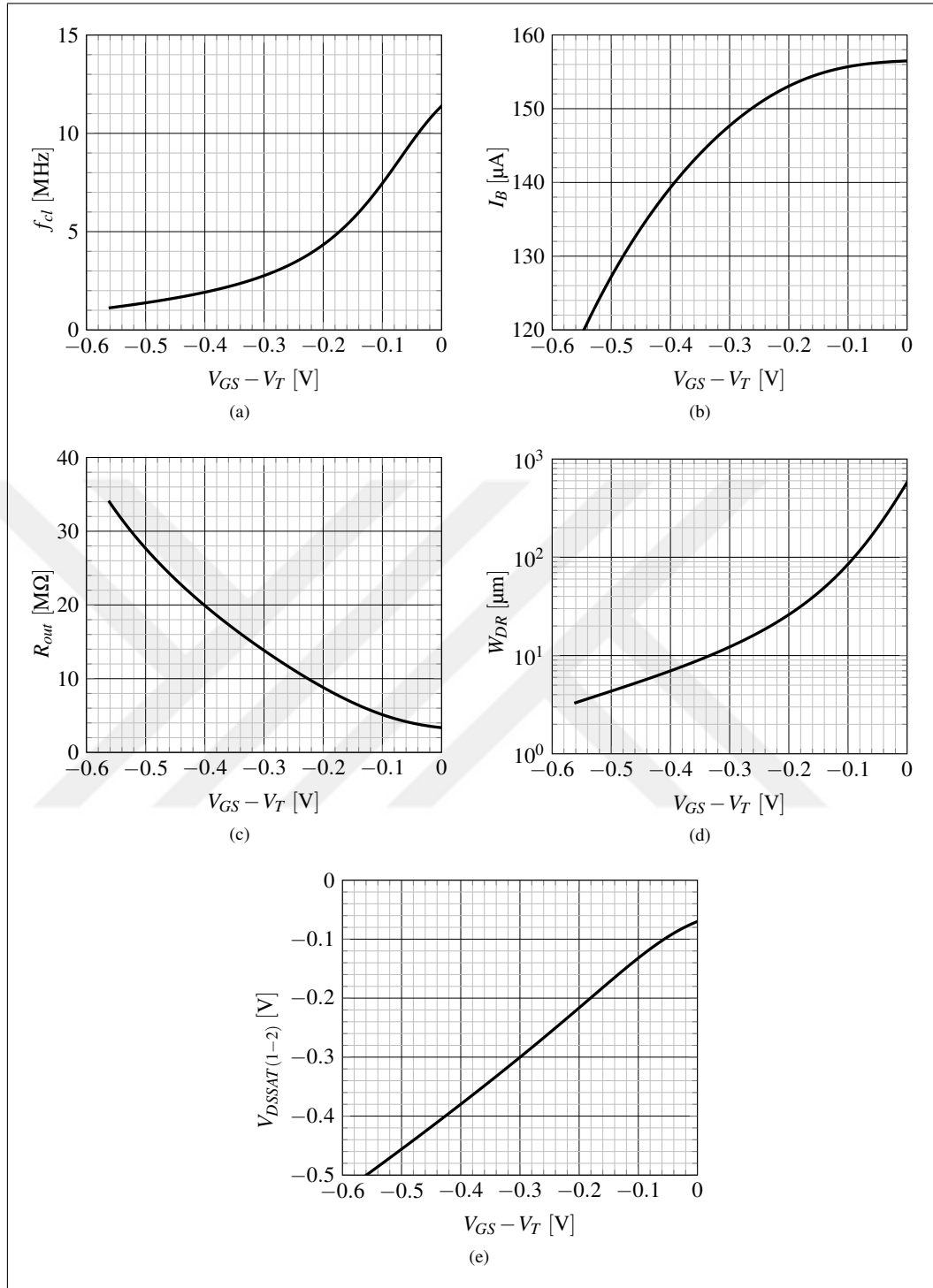


Figure A.6. (a) f_{cl} vs. $V_{GS} - V_{TP}$. (b) I_B vs. $V_{GS} - V_{TP}$. (c) R_{out} vs. $V_{GS} - V_{TP}$. (d) W_{DR} vs. $V_{GS} - V_{TP}$. (e) $V_{DSSAT(1-2)}$ vs. $V_{GS} - V_{TP}$.

sink network devices, two considerations must be taken into account. These are the saturation condition of drivers within the common-mode range, and saturation condition of cascoded sink network devices within the output range. Both of them specify a maximum gate-source

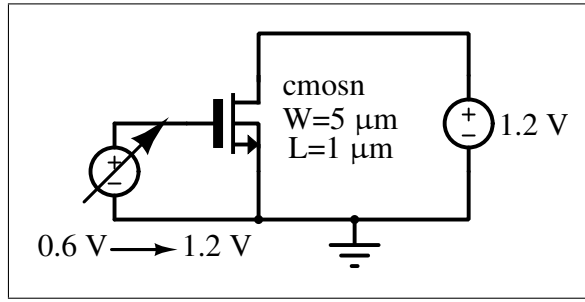
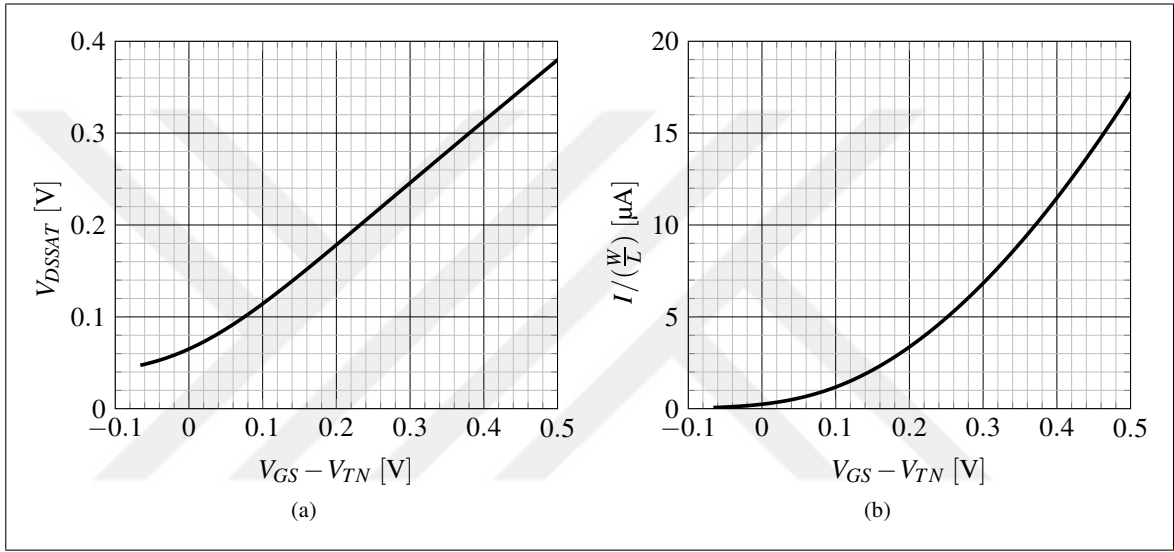


Figure A.7. Cascoded sink network device parameter extraction.

Figure A.8. I/O NMOS characteristics: (a) V_{DSSAT} vs. $V_{GS} - V_{TN}$. (b) $I/(W/L)$ vs. $V_{GS} - V_{TN}$.

voltage and an aspect ratio for sink network devices. Beginning with the saturation condition of M1 and M2 yields:

$$V_{DS(1-2)} \leq V_{DSSAT(1-2)} \quad (A.13)$$

$$V_{SS} + V_{GT(3-4)} + V_{TN(3-4)} + V_{GT(1-2)} - V_{CM(min)} + V_{TP(1-2)} \leq V_{DSSAT(1-2)} \quad (A.14)$$

Since $V_{GT(1-2)}$ is selected as -0.2 V in previous section, corresponding $V_{DSSAT(1-2)}$ is found as -0.216 V as can be seen in Table A.1. Threshold voltage of drivers $V_{TP(1-2)}$ is found as -0.44 V as can be seen from Fig. A.2. Even though the threshold voltage of cascoded devices $V_{TN(3-4)}$ is not specified without a given channel length, its maximum value is selected for worst-case analysis. Its value is, therefore, selected as 0.68 V from Fig. A.2. Using (A.14)

with the values found in previous section, overdrive voltage of M3 & M4 is found as:

$$V_{GT(3-4)} \leq \underbrace{\underbrace{V_{DSSAT(1-2)}}_{-0.22} - \underbrace{V_{SS}}_{-0.5} - \underbrace{V_{TN(3-4)}}_{0.68} - \underbrace{V_{GT(1-2)}}_{-0.2} + \underbrace{V_{CM(min)}}_0 - \underbrace{V_{TP(1-2)}}_{-0.44}}_{0.24 \text{ V}} \quad (\text{A.15})$$

Considering the output range with identical sink network devices, following equation can be written for saturation condition of cascoded sink network devices:

$$V_{SS} + 2V_{DSSAT(3-4-6-6c-8-8c)} + \Delta V_{DS} \leq V_{O(min)} \quad (\text{A.16})$$

Assigning 0.1 V saturation safety margin ΔV_{DS} , (A.16) is rewritten as:

$$V_{DSSAT(3-4-6-6c-8-8c)} \leq \underbrace{\frac{\overbrace{V_{O(min)}}^0 - \overbrace{\Delta V_{DS}}^{0.1} - \overbrace{V_{SS}}^{-0.5}}{2}}_{0.2 \text{ V}} \quad (\text{A.17})$$

When equations (A.15) and (A.17) are analyzed carefully together with Fig. A.8, it can be seen that once (A.17) is satisfied, (A.15) is automatically met. Therefore, (A.17) is determining factor for sizing cascoded sink network. Selecting $V_{DSSAT(3-4-6-6c-8-8c)} = 0.15 \text{ V}$ corresponds to 0.157 V overdrive voltage and 2.265 μA sheet current as can be seen in Fig. A.8. This choice lefts $\Delta V_{DS} = 0.2 \text{ V}$ safety margin. Since the cascoded sink network devices are operating with bias current $\frac{I_B}{2} = 76.5 \mu\text{A}$, aspect ratio of devices is found as $76.5/2.265 = 33.77$. Electrical schematic for sizing cascoded sink network is given Fig. A.9. Since all devices have identical drain-source saturation voltage and identical current, they also have identical aspect ratios and overdrive voltages.

Therefore, bias voltage V_{B1} is calculated as:

$$V_{B1} = V_{SS} + V_{DSSAT} + \Delta V_{DS} + V_{GS} \quad (\text{A.18})$$

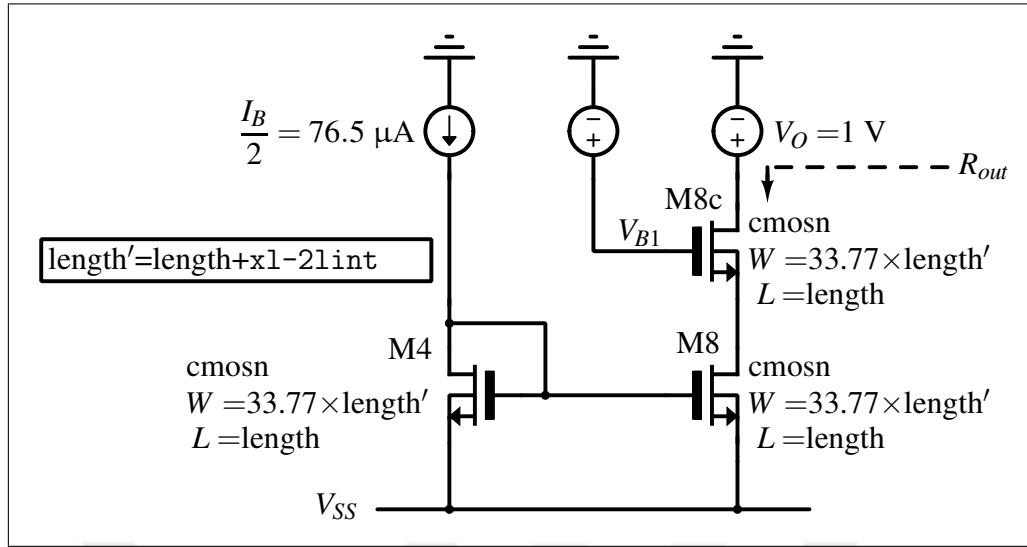


Figure A.9. Cascoded sink network device sizing.

Assuming threshold voltage has its maximum value (This value will be trimmed after selecting proper channel length), equation (A.18) can be rewritten as:

$$V_{B1} = \underbrace{V_{SS}}_{-0.5} + \underbrace{V_{DSSAT}}_{0.15} + \underbrace{\Delta V_{DS}}_{0.2} + \underbrace{V_{GT}}_{0.157} + \underbrace{V_{TN}}_{0.68} = 0.687 \text{ V} \quad (\text{A.19})$$

For the sake of simplicity, it is practical to select same channel geometry for all devices. DC operating point and transfer function analysis have been performed to find the output resistance R_{out} as a function of parameter “length”. Using Fig. A.10, channel length $L_{(3-4-6-6c-8-8c)}$ is selected as $0.49 \mu\text{m}$ for cascoded sink network devices to have a output resistance $R_{out} = 9.4 \text{ M}\Omega$. Since the aspect ratio is found as 33.77, channel width of the devices $W_{(3-4-6-6c-8-8c)}$ is calculated as $17.3 \mu\text{m}$. There is no need to re-trim the bias voltage V_{B1} since the maximum threshold voltage falls somewhere very close to selected channel length. Channel geometry and bias voltage for the cascoded sink network devices are summarized and shown in Table A.2.

Output voltage V_O in Fig. A.9 is swept with a voltage source between -0.2 V and 1.1 V with channel dimensions and bias voltage in Table A.2 is shown in Fig. A.11. Output current at the common-mode operating point ($V_O = 1 \text{ V}$) is read as $72.6 \mu\text{A}$ which is not equal to the

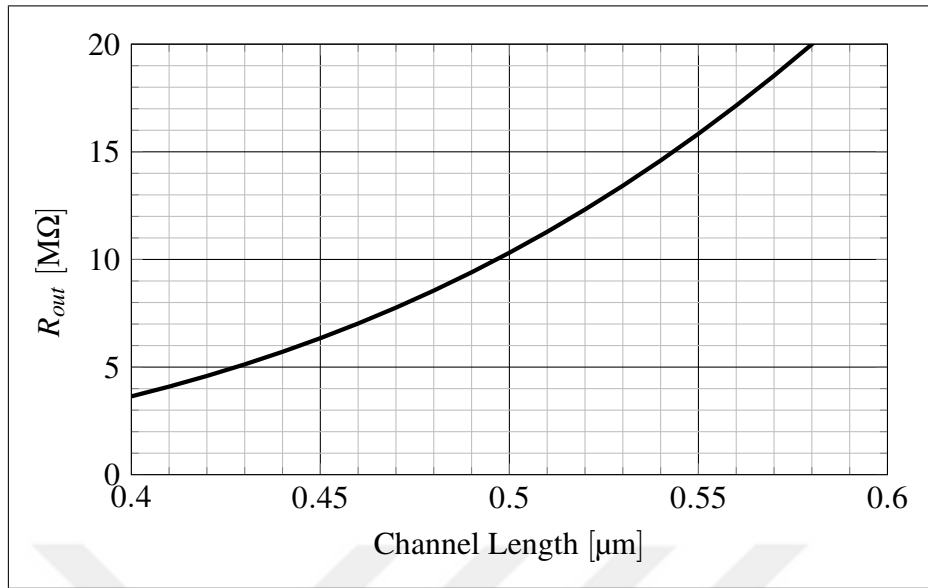


Figure A.10. R_{out} vs. channel length.

Table A.2. Cascoded sink network design summary.

Device	W[μm]	L[μm]	V_{B1} [V]	R_{out} [M Ω]
cmosn	17.3	0.49	0.687	9.4

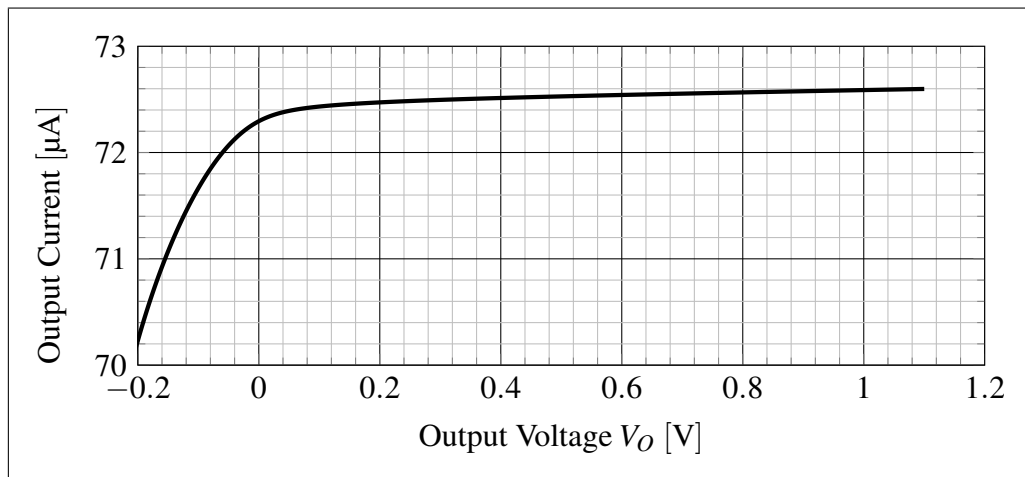


Figure A.11. Output current vs. output voltage.

half of bias current I_B . This is due to the mirroring devices M4, and M8 which are operating with different drain voltages.

A.2.5.3. Cascoded Source Network

Before sizing and biasing cascoded source network, electrical schematic shown in Fig. A.12 is built for extracting the relation between $V_{GS} - V_{TP}$, V_{DSSAT} and sheet current $I/(\frac{W}{L})$ of two candidates I/O PMOS device (cmosp) and low-threshold I/O PMOS device (cmosplvt). Each device is biased with appropriate terminal voltages to obtain its characteristics within

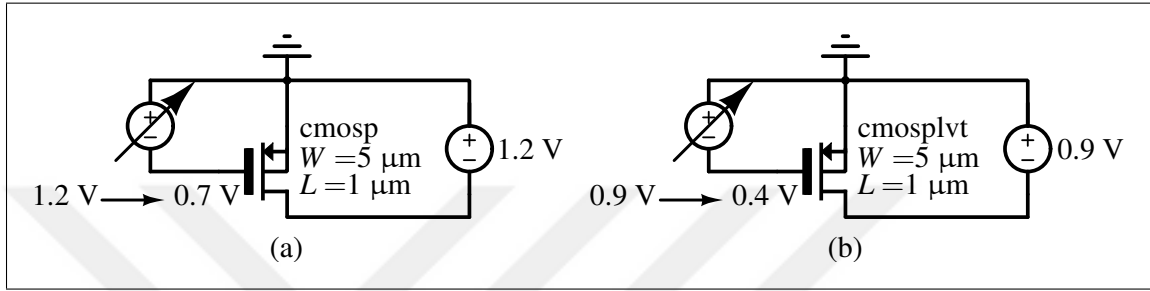


Figure A.12. Cascoded source network device parameter extraction.

a similar overdrive voltage range. Channel dimensions are selected as $W=5 \mu\text{m}$, $L=1 \mu\text{m}$ for avoiding short channel effects. Two DC-sweep analysis one of which for cmosp and

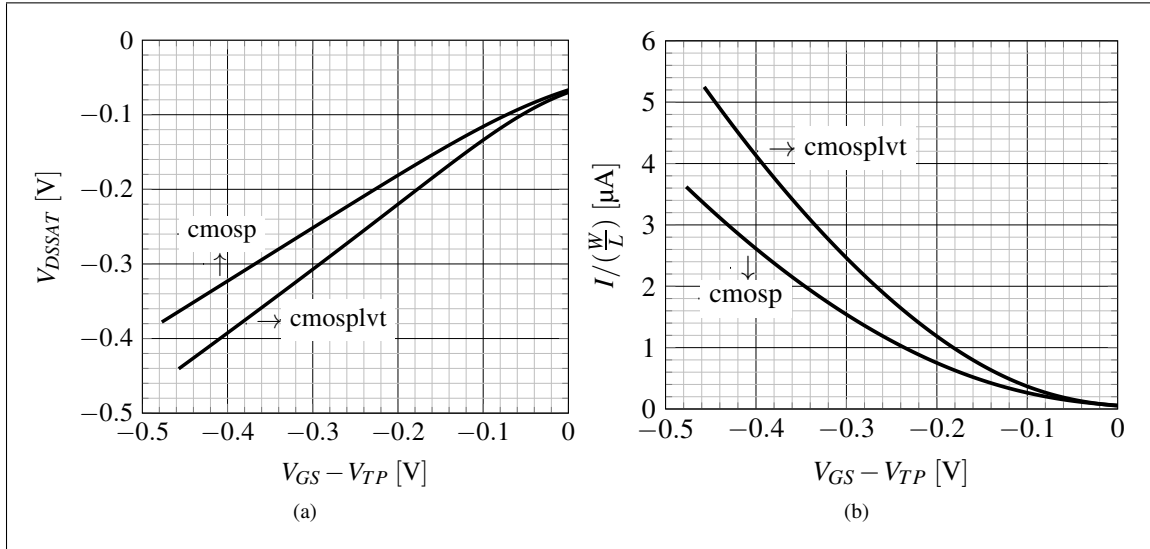


Figure A.13. I/O PMOS (cmosp) and low-threshold I/O PMOS (cmosplvt) characteristics: (a) V_{DSSAT} vs. $V_{GS} - V_{TP}$. (b) $I/(\frac{W}{L})$ vs. $V_{GS} - V_{TP}$.

the other one is cmosplvt have been performed to plot drain-source saturation voltage and sheet current as a function of overdrive voltage. As shown in Fig. A.13(a) and (b), I/O PMOS (cmosp) requires more overdrive voltage for a given V_{DSSAT} and low-threshold I/O

PMOS (cmosplvt) has more sheet current for a given overdrive voltage. Using Fig. A.13(a) and (b), sheet current as a function of drain-source saturation voltage of each device is plotted and shown in Fig. A.14. For a given V_{DSSAT} , sheet current of PMOS devices are

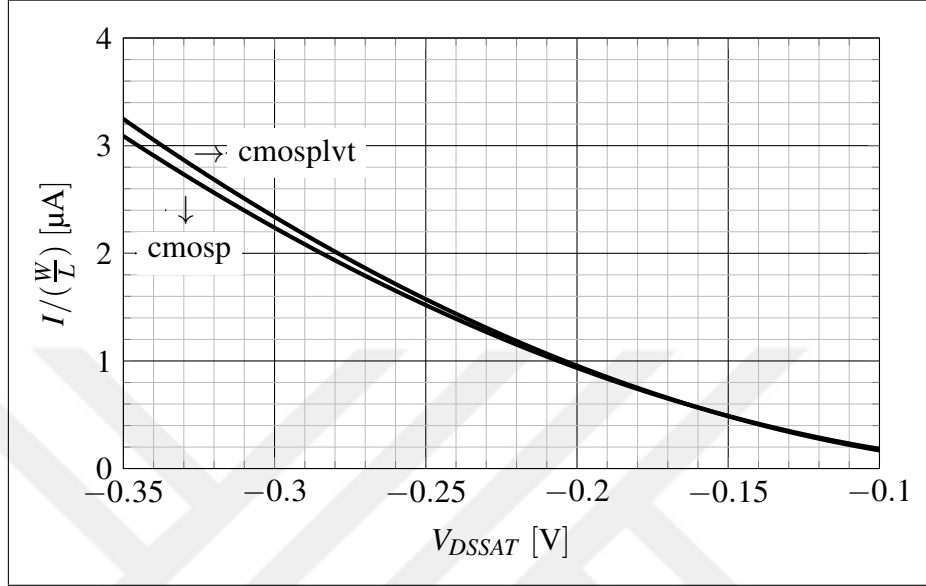


Figure A.14. I/O PMOS (cmosp) and low-threshold I/O PMOS (cmosplvt) characteristics: $I/(W/L)$ vs. V_{DSSAT} .

nearly identical especially in drain source saturation voltages close to zero. Their channel dimensions will, therefore be the same for a given channel length. Since the pull-up network consist of cascoded devices, and the desired output resistance R_{out} in Table A.1 is relatively low for a cascoded topology, channel dimension of a PMOS device will be nearly the same whether the selected device is cmosp or cmosplvt. Therefore, neither cmosp nor cmosplvt has no superiority on each other as the footprint is concerned. Since I/O PMOS has higher threshold voltage, M5 and M7 in Fig. A.3 will operate with higher gate-source voltage in magnitude for a given overdrive voltage. This will bring drain voltages of M5c and M7c closer to each other at the common-mode operating point hence improve mirroring from M5 to M7. With the improved mirroring, OTA will have less offset voltage. To show this effect, two cascoded source network, hence two OTA with different cascoded network will be designed and compared.

When sizing cascoded source network, output range of the OTA must be taken into account. Saturation condition of cascoded source network with the maximum value of output is

written as:

$$V_{DD} + 2V_{DSSAT(7-7c)} + \Delta V_{DS} \geq V_{O(max)} \quad (A.20)$$

Allowing $\Delta V_{DS} = -0.2$ V safety margin yields $V_{DSSAT} = -0.3$ V for each device. Using Fig. A.14, sheet current is read as $2.24 \mu\text{A}$ for cmosp and $2.34 \mu\text{A}$ for cmosplvt. For calculating aspect ratio, output current of cascoded sink network at common-mode operating point is taken ($72.6 \mu\text{A}$) rather than $I_B/2$ to take into account poor mismatch caused by cascoded sink network. Therefore aspect ratio is calculated as $72.6/2.24 = 32.44$ for cmosp and $72.6/2.34 = 31.04$ for cmosplvt. Bias voltage V_{B2} is calculated as:

$$V_{B2} = V_{DD} + V_{DSSAT(7-7c)} + \Delta V_{DS} + V_{GT(7-7c)} + V_{TP} \quad (A.21)$$

$$V_{B2} = 2.8 - 0.3 - 0.2 - 0.368 - \underbrace{0.723}_{V_{TH,cmosp(max)}} = 1.209 \text{ V for cmosp}, \quad (A.22)$$

$$V_{B2} = 2.8 - 0.3 - 0.2 - 0.292 - \underbrace{0.447}_{V_{TH,cmosplvt(max)}} = 1.561 \text{ V for cmosplvt}, \quad (A.23)$$

The threshold voltages used in (A.22) and (A.23) are the maximum values used for estimating the value of bias voltage V_{B2} . The actual threshold voltage will be determined after iterating channel length for desired output resistance R_{out} . With the new value of threshold voltage, bias voltage V_{B2} will take its final value. For device sizing, electrical schematic shown in Fig. A.15 is built. For the sake of simplicity, it is practical to select same channel geometry for all devices. DC operating point and transfer function analysis have been performed to find the output resistance R_{out} as a function of parameter “length”. Using Fig. A.16, $L = 0.46 \mu\text{m}$ for cmosp and $L = 0.68 \mu\text{m}$ for cmosplvt is selected to provide output resistance $R_{out} = 9 \text{ M}\Omega$ which is slightly greater than the necessary output resistance shown in Table A.1. Selected channel length $L = 0.46 \mu\text{m}$ for cmosp corresponds to the threshold voltage which is 9 mV less than the value used in (A.22). Therefore the bias voltage V_{B2} is trimmed down to 1.2 V. DC operating point and transfer function analysis yields $R_{out} = 9.15 \text{ M}\Omega$ with the new bias voltage $V_{B2} = 1.2$ V. As for cmosplvt, there is no need to trim since the selected channel length corresponds to approximately the same

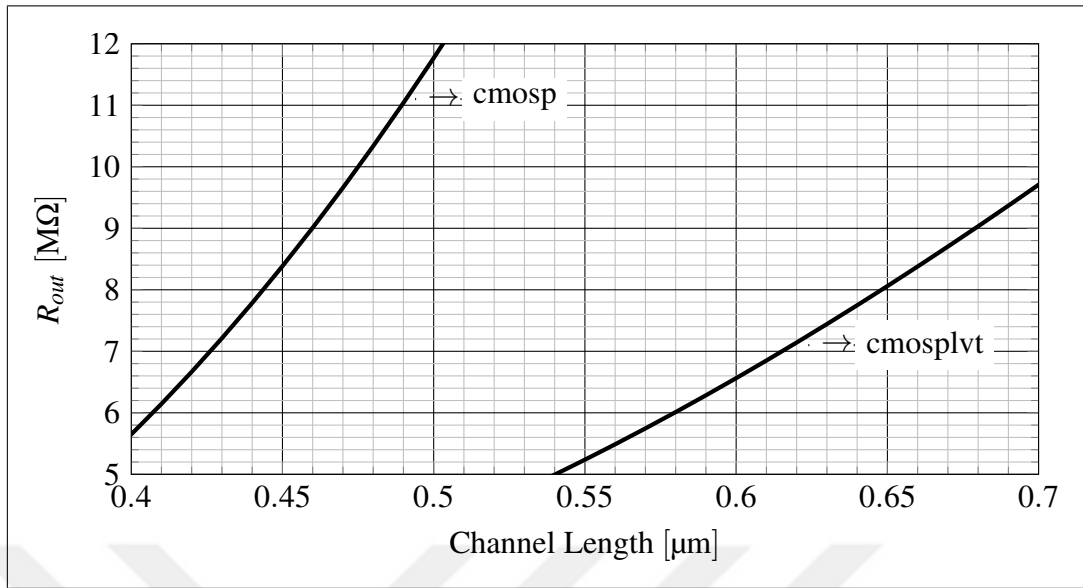


Figure A.16. R_{out} vs. channel length.

I/O PMOS (cmosp) offers more accurate mirrored current hence less offset of the OTA. Offset comparison of OTAs with different cascoded network will be made in next section.

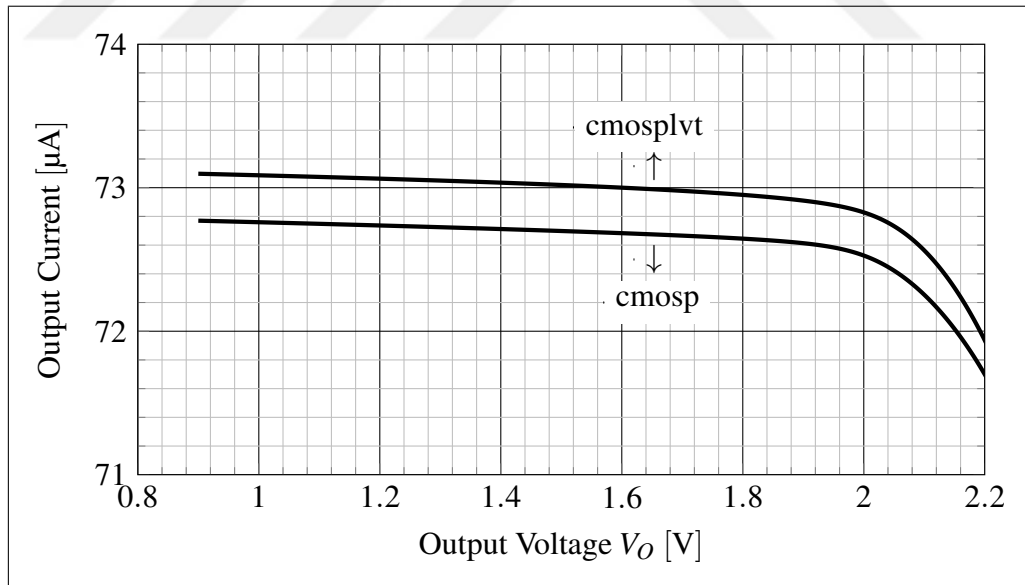


Figure A.17. Output current vs. output voltage V_O .

A.2.5.4. Current Source

Maximum common-mode input voltage defines the saturation condition of the current source, built with a single PMOS device. Therefore compliance limit is defined as:

$$\underbrace{V_{DD}}_{2.8} + V_{DSSAT(I_B)} \geq \underbrace{V_{CM(max)}}_2 - \underbrace{V_{GT(1-2)}}_{-0.2} - \underbrace{V_{TP(1-2)}}_{-0.45} \quad (A.24)$$

$$V_{DSSAT(I_B)} \geq -0.15 \text{ V} \quad (A.25)$$

Using (A.25), $V_{DSSAT(I_B)}$ is selected as -0.15 V. Using, Fig. A.13, $V_{GT(I_B)}$ and sheet current is found as -0.158 V and 0.49 μA respectively. Calculated sheet current corresponds to an aspect ratio of $153/0.49 = 312$. Allowing $L = 1 \text{ }\mu\text{m}$ for the channel length for a relatively high output resistance yields a wide channel width. Therefore, device is built with ten segments. At the common-mode operating point common-source voltage of the drivers M1 and M2 is calculated as

$$V_{S(1-2)} = \underbrace{V_{CM}}_1 - \underbrace{V_{GT(1-2)}}_{-0.2} - \underbrace{V_{TP(1-2)}}_{-0.45} = 1.65 \text{ V} \quad (A.26)$$

The common-source voltage calculated in (A.26) is also the drain voltage of the current source. Therefore the current source operates with $1.65 \text{ V} - 2.8 \text{ V} = -1.15 \text{ V}$ drain-source voltage. Necessary bias voltage for the current source is calculated as follows:

$$V_{GS(I_B)} = \underbrace{V_{GT(I_B)}}_{-0.158 \text{ V}} + \underbrace{V_{TP(I_B)}}_{-0.722 \text{ V for } L=1 \text{ }\mu\text{m}} \quad (A.27)$$

$$V_{B3} - \underbrace{V_{DD}}_{2.8 \text{ V}} = \underbrace{V_{GT(I_B)}}_{-0.158 \text{ V}} + \underbrace{V_{TP(I_B)}}_{-0.722 \text{ V for } L=1 \text{ }\mu\text{m}} \quad (A.28)$$

$$V_{B3} = 1.92 \text{ V} \quad (A.29)$$

Exact dimensions and bias voltages are trimmed with DC-operating point analysis whose electrical schematic is shown in Fig. A.18 and summarized in Table A.4.

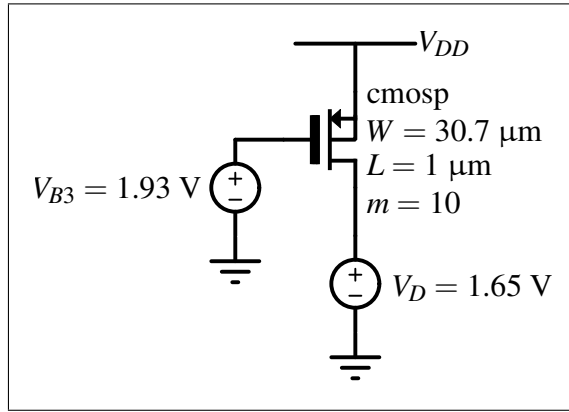


Figure A.18. Current source sizing.

Table A.4. Current source design summary.

Device	W[μm]	L[μm]	m	$V_{B3}[\text{V}]$	$V_{DSSAT(I_B)}[\text{V}]$	$I_B[\mu\text{A}]$
cmosp	30.7	1	10	1.93	-0.15	153

A.3. VERIFICATION

A.3.1. DC Open-Loop Test

Electrical schematic for DC Open-Loop simulation is given in Fig. A.19. Input voltage V_p is swept between 999 mV and 1001 mV. Output voltage V_O is plotted as a function of input voltage V_p and DC open-loop gain $A_{d(0)}$ is plotted as function of output voltage V_O and both graphs were shown in Fig. A.20 a and b respectively.

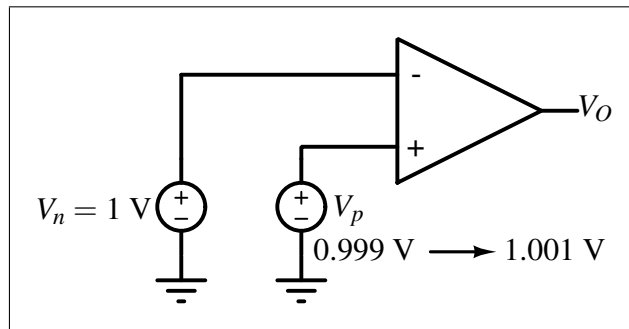


Figure A.19. DC open-loop simulation.

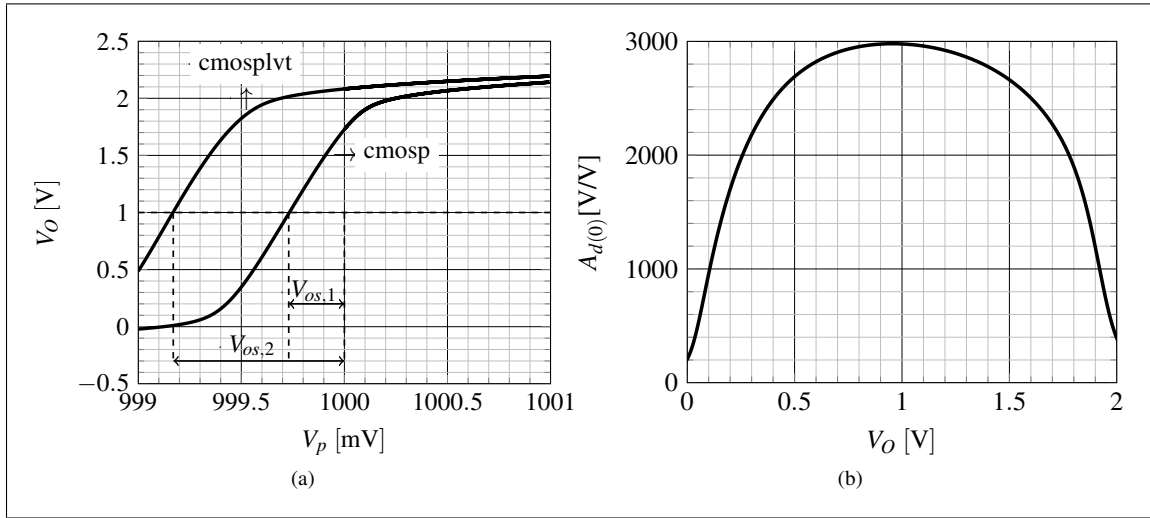


Figure A.20. (a) Open-loop transfer characteristics. (b) $A_{d(0)}$ vs. V_O .

Fig. A.20 a shows that building cascoded source network with I/O PMOS devices provides less input offset. As explained in previous section, the reason is closer drain-source voltages of M5c and M7c due to high threshold voltages. Input offset is $267 \mu\text{V}$ with I/O PMOS cascoded source network while the OTA with I/O low-threshold PMOS cascoded source network provides $831 \mu\text{V}$ offset. DC Open-Loop gain $A_{d(0)}$ in Fig. A.19(b) is read as 2975 V/V when $V_O = 1$ V which slightly smaller than the expected value.

A.3.2. DC Closed-Loop Test

Input voltage V_p is swept from 0 V to 2 V and the error between output and input voltage $V_O - V_p$ is plotted as a function of input voltage V_p . A comparison between output voltage errors with and without offset is given in Fig. A.21. Maximum DC output voltage error is still very close to 1 mV even with input offset.

A.3.3. AC Closed-Loop Test

Electrical schematic for AC Closed-Loop simulation is given in Fig. A.22. Magnitude and phase of the AC transfer function is plotted and shown in Fig. A.23. Closed-loop bandwidth f_{cl} is read as 4.08 MHz which is slightly smaller than target f_{cl} . Closed-loop bandwidth can be increased by lowering load capacitance (roughly by 2 pF) or re-designing the whole OTA

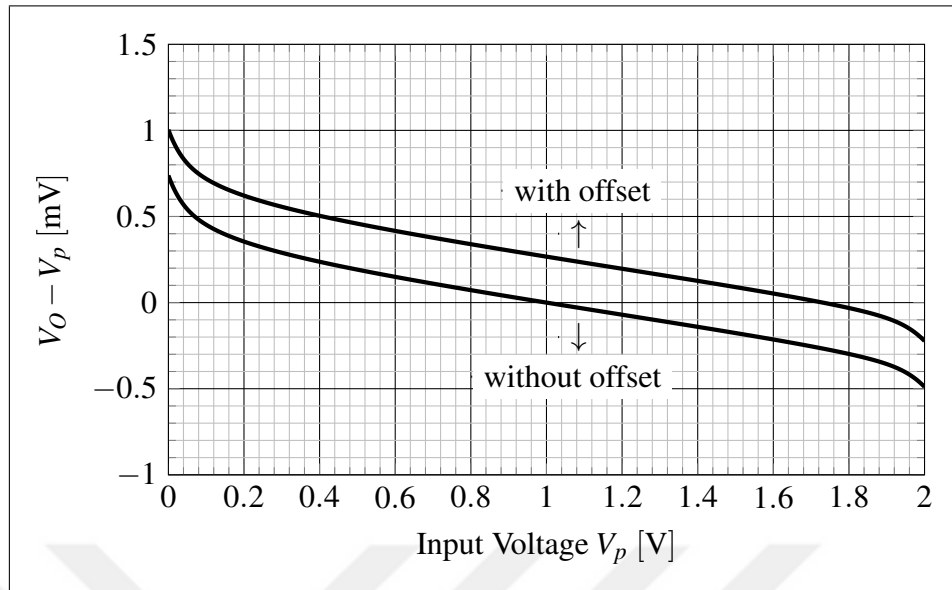
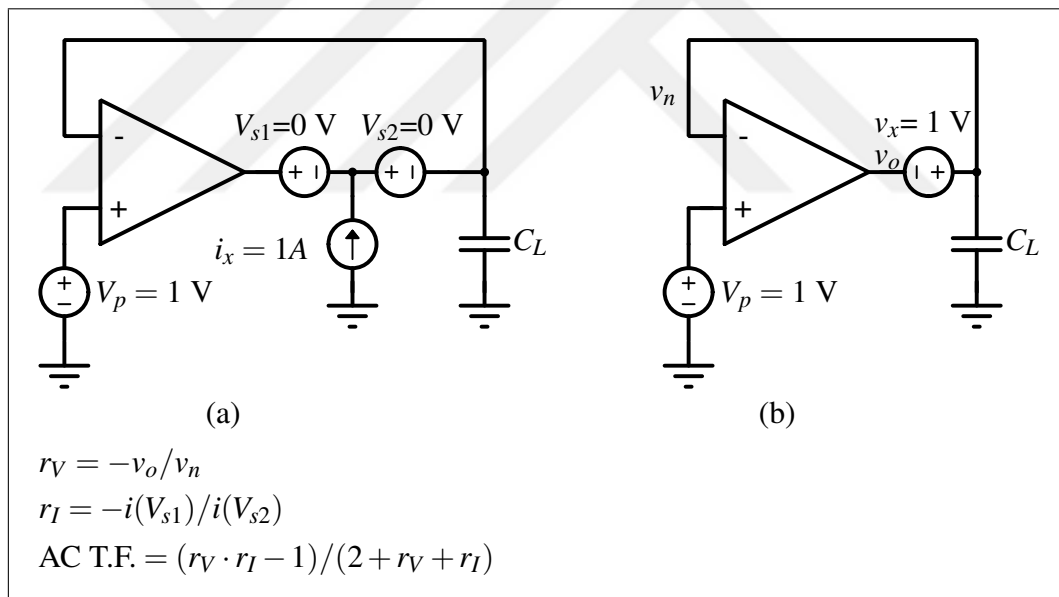
Figure A.21. Output voltage error vs. input voltage V_p 

Figure A.22. AC closed-loop simulation.

by assuming 2 pF additional load capacitance. Phase margin is read as 89.4°.

A.3.4. Transient Closed-Loop Test

Electrical schematic for transient closed-loop simulation is given in Fig. A.24(a). Input voltage sinusoidal signal with 1 V offset, 1 V amplitude and 1 MHz frequency. Input voltage

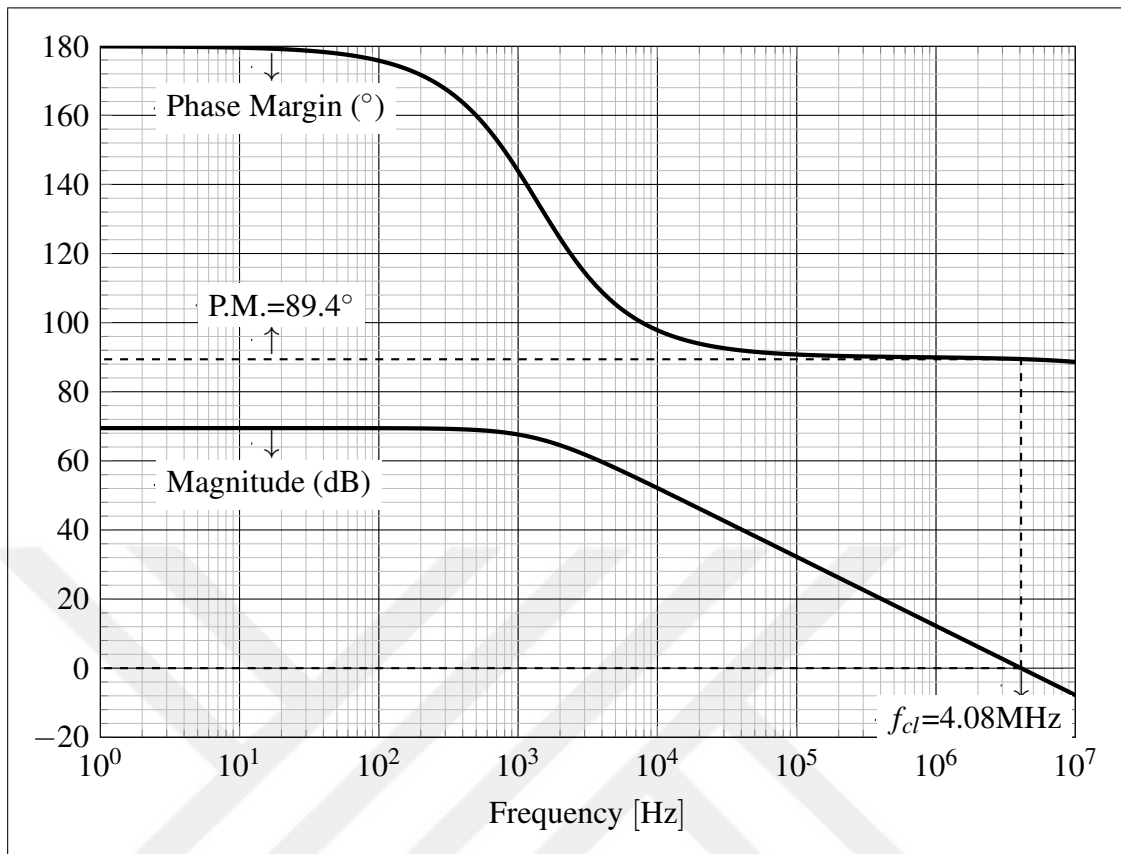


Figure A.23. Closed-loop transfer function AC response.

V_p and output voltage V_O is plotted with a five periods transient analysis and shown in Fig. A.24(b). Output voltage has 0.964 V amplitude and 2.2 percent THD performed with a fourier analysis.

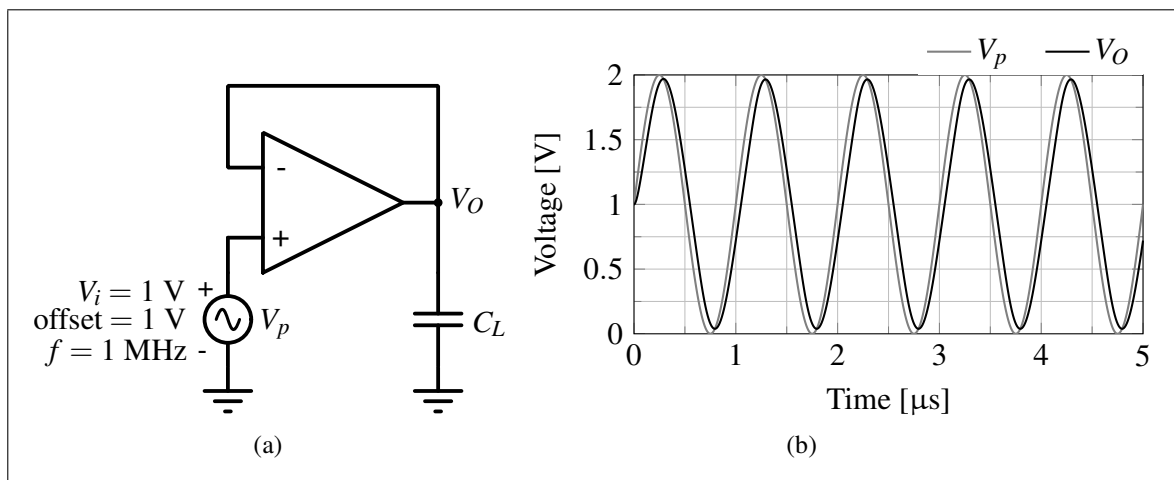


Figure A.24. Transient closed-loop simulation.

A.4. SUMMARY

Performance metrics of cascoded symmetrical-OTA are summarized and shown in Table A.5

Table A.5. Design summary.

Technology	UMC 0.18 μm
V_{DD}	2.8 V
V_{SS}	-0.5 V
Load Capacitance	25 pF
Tail Current	153 μA
Input Offset	267 μV
DC Gain @ $V_O = 1\text{ V}$	2975 V/V
Maximum DC Output Voltage Error	1.005 mV (with offset)
Maximum DC Output Voltage Error	738 μV (without offset)
Closed-Loop Bandwidth	4.08 MHz
Phase Margin	89.4°
Amplitude of V_O @ 1 MHz	0.964 V
THD @ 1 MHz	2.2 percent

APPENDIX B: LOW-NOISE AMPLIFIER DESIGN

B.1. INTRODUCTION

Electrical schematic of a common-emitter low-noise amplifier is given in Fig. B.1. Input matching network provides the required value of source reflection coefficient Γ_S that is compliant with the input reflection coefficient Γ_{IN} . Similarly, output matching network provides the required value of load reflection coefficient Γ_L that is compliant with the output reflection coefficient Γ_{OUT} . Together with the Bias Tee networks, coupling capacitors C_1 and C_2 provide isolation between AC and DC parts of the circuit. These capacitors can be removed if the matching networks include a series capacitor. The resistor R_B is used to adjust the Q-point of the transistor. It is the most primitive DC biasing circuit, since the amplifier is assumed to operate in a constant temperature environment. In this study, a similar design flow in [47] is adopted.

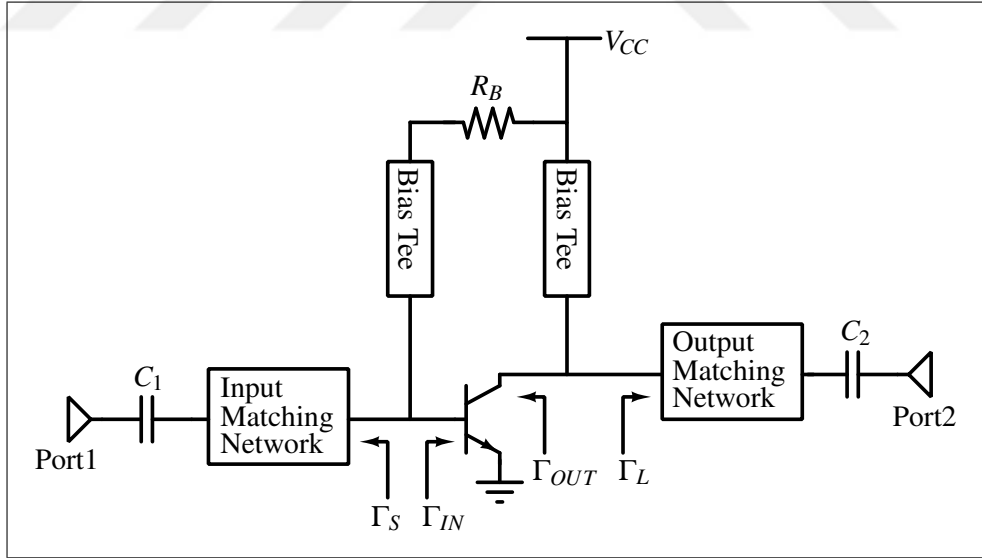


Figure B.1. Electrical schematic of common-emitter low-noise amplifier.

Design specifications are listed in Table B.1.

Table B.1. Specifications.

Item	Value
f	3.3 GHz
G_A	≥ 14 dB
$VSWR_{IN}$	≤ 2
$VSWR_{OUT}$	≤ 2
NF	≤ 1 dB
Transistor	BFP842ESD
Capacitors	Johanson (0603 package)
Inductors	Johanson (0402 package)
Resistors	Vishay (0603 package)

B.2. DESIGN

B.2.1. Bias Tee

Performance of bias tee network is critical since it provides an isolation between DC and AC parts of the circuit. It should therefore behave like a short circuit at DC and nearly open circuit at the frequency of operation. This circuit can be designed with a simple inductor but, when package parasitics are included, each inductor has a self resonance frequency above which it behaves like a capacitor. Similarly a capacitor with the package parasitics behaves like an inductor at the frequencies greater than self resonance frequency. Adopting the same analysis in [48], first procedure is to find to maximum allowable values of inductors and capacitors at the frequency of operation.

As specified in Table B.1, Johanson inductors in a 0402 package and capacitors in a 0603 package are used for characterization. Simulated input impedance of the lumped elements at the frequency of operation is shown in Fig. B.2. Even though 10 nH inductor and 3 pF capacitor behave like ideal open and ideal short respectively, it is wise to select smaller values considering the component tolerances. Therefore 8.2 nH and 2.7 pF are chosen as the

limits for the operation frequency. If desired, connecting two 2.7 pF capacitors in parallel will decrease input impedance close to zero. This option can also be considered for better performance.

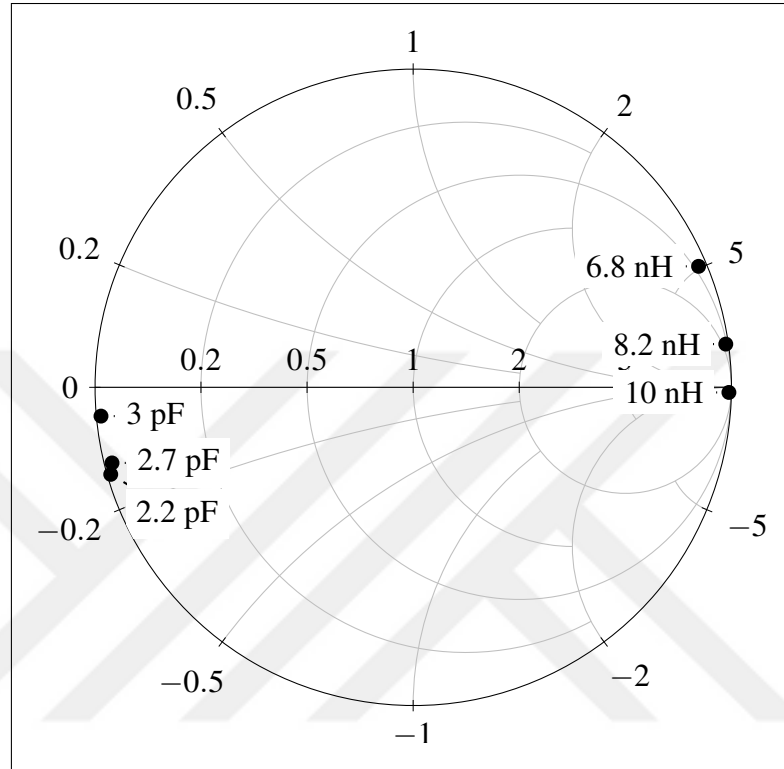


Figure B.2. Input impedance of lumped components with package parasitics.

Electrical schematic of bias-tee network is shown in Fig. B.3. Bottom plates of the capacitors are connected to ground with a microstrip via. These vias, together with the microstrip lines and junctions are simulated with EM simulation for all parasitic and coupling effects to be taken into account. Two ports have been placed for simulating the forward transmission along the network.

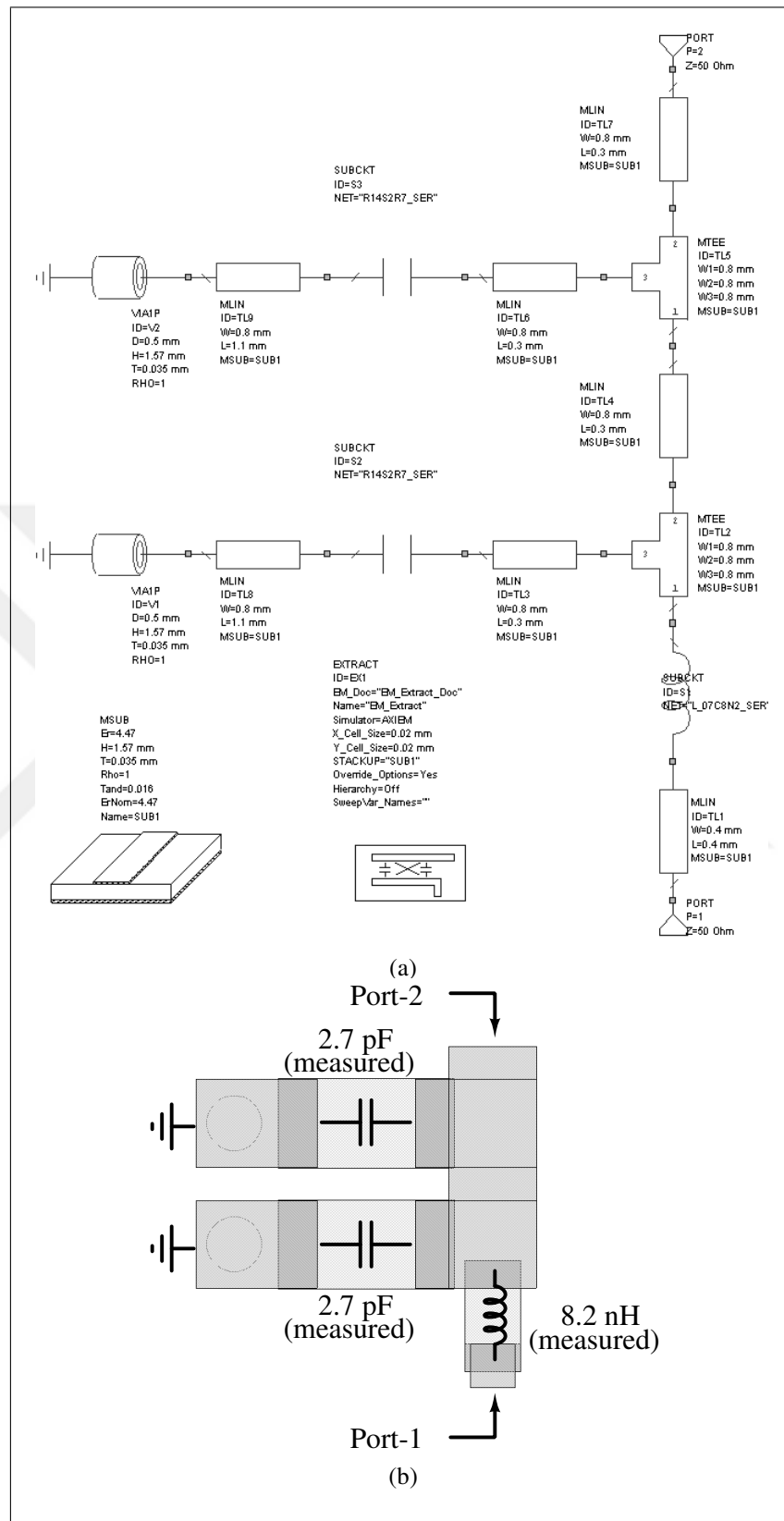


Figure B.3. Bias tee network: (a) Schematic. (b) Layout.

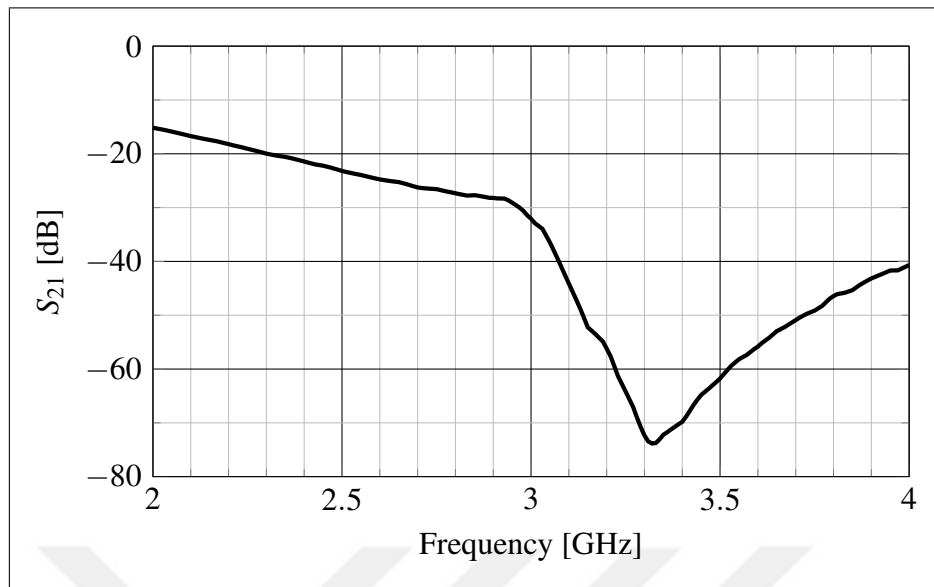


Figure B.4. Bias tee frequency response.

Simulated frequency response of Bias tee network is shown in Fig. B.4. It can be clearly seen that, practically there is no transmission through the network at the frequency of operation. This concludes that the circuit behaves like an open circuit at the frequency of operation.

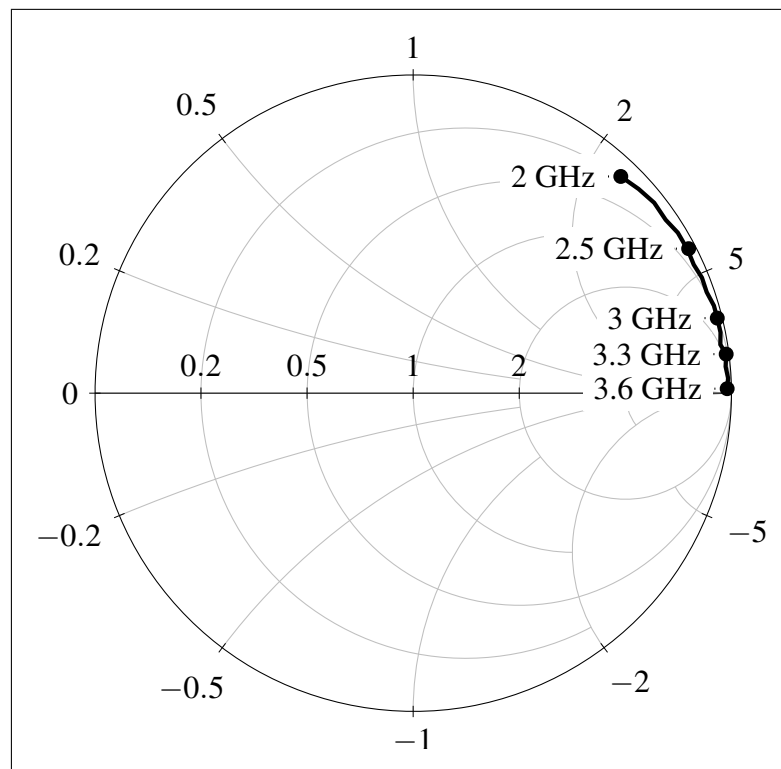


Figure B.5. Bias tee input impedance seen from port-1.

Same response can be also obtained by simulating the input impedance seen from port 1. As can be seen from Fig. B.5, input impedance at the frequency of operation shows quite high reactance. In other words, the network behaves like an open circuit.

B.2.2. Biasing

Design does not target the value of supply voltage. Since the maximum collector emitter voltage is defined as 3.25 V in datasheet, supply voltage is selected as 1 V which is below absolute maximum ratings. Therefore, output characteristics of the device is extracted with maximum collector to emitter voltage of 1 V. Increasing the collector current will degrade the noise performance of the amplifier where operating with lower currents will require additional precautions against instability. Three parameters, namely K , B_1 and $NF_{\min}$ is plotted as a function of collector current and is shown in Fig. B.6.

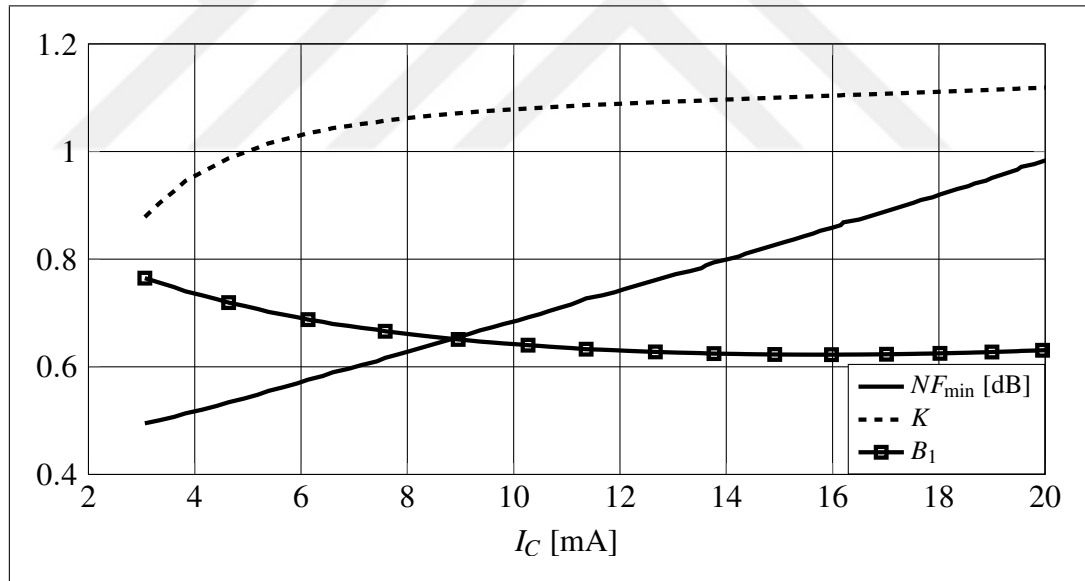


Figure B.6. Stability and minimum noise figure as a function of I_C .

As can be seen in Fig. B.6, transistor becomes potentially unstable below 5 mA of collector current since the parameter K becomes less than 1. This requires additional stabilization methods to avoid instability and increases complexity of the design. Selecting higher collector current, however, increases the minimum noise figure of the transistor. The amplifier will exhibit higher noise figure than the minimum if the source termination is

different than the optimum noise termination. All the lumped components together with the microstrip lines will bring additional noise terms. Considering the additional noise terms coming from each component and inappropriate termination of source port, it is wise to select a collector current whose minimum noise figure is below the limit and that choice does not cause instability. Based on the considerations above, collector current is selected as $I_C = 10$ mA.

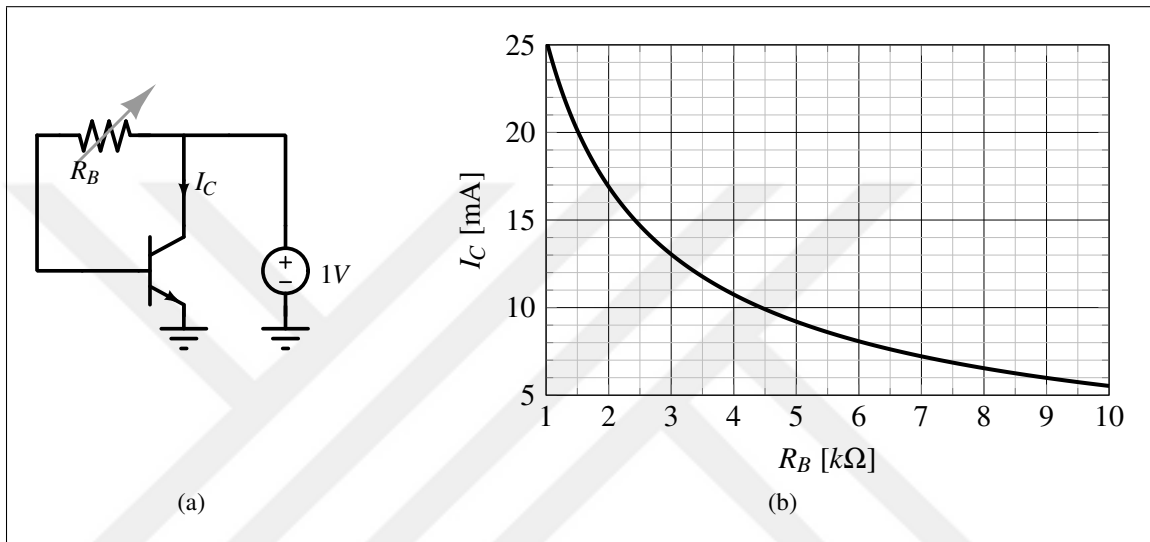


Figure B.7. Test setup for finding R_B : (a)Electrical schematic. (b) Collector current vs. base resistance.

To avoid using second voltage source for biasing the base, a resistor R_B is trimmed such that it is connected between the base and the supply voltage as shown Fig. B.7 (a). Its value is read as 4.4 kΩ from Fig. B.7 (b) for conducting a collector current of 10 mA.

B.2.3. S-Parameters Calculation

After the biasing is complete, next step is to obtain S-parameters of the unmatched amplifier which consists bias tee networks and biasing resistor only. Shown in Fig. B.8 is the S-parameter measurement setup. Notice the presence of decoupling capacitors denoted by C_∞ . If the simulator consists an “RF-short” element, it is also applicable to use that component to make an isolation between DC and AC parts of the circuit. In this case, they are replaced with 1 F ideal capacitors. The collector of the transistor is connected to supply voltage via

bias tee network whereas the base of the transistor is connected to another identical bias tee network. This network is tied to supply voltage through series connection of two $2.2\text{ k}\Omega$ resistors.

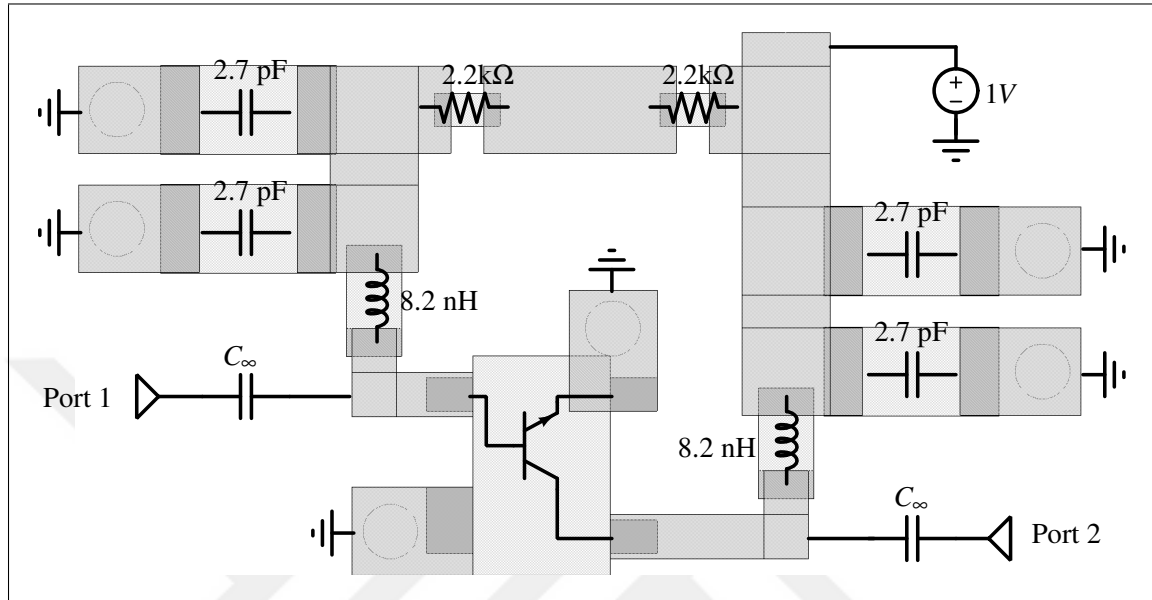


Figure B.8. S-parameter extraction setup.

Before performing the analysis, two important issues must be checked. These are listed as follows:

- There are more than one method to perform S-parameter simulation such as small signal analysis, harmonic balance and transient analysis with steady state shooting methods. These analyses are performed around a bias point. Therefore DC solution (0 Hz) should be added to the requested frequencies. This is also necessary for the accurate extraction of microstrip lines through EM analysis.
- If the measured model is used instead of ideal one for the inductors and capacitors, make sure that they are defined at DC (0 Hz.). One such example is given Fig. B.9. Johanson inductors with 0402 package does not contain measured data at DC. Using this component in DC calculation may cause erroneous results regarding the bias point of the circuit. To solve the problem, a line in black box is added to define the two port network at DC.

```
#      mhz      s      ma      r      50
# Freq MagS11 AngS11 AngS21 AngS22 MagS12 AngS12 MagS22 AngS22
0      0      0      1      0      1      0      0      0
50     0.03 53.20      0.99 0.10 0.99 0.10 0.03 53.20
100    0.05 62.90      0.99 -1.30      0.99 -1.30      0.05 62.90
```

Figure B.9. Top section of the S-parameter file for the inductor with added line for DC.

Just like in bias tee network design, bottom plates of the capacitors are connected to ground with a microstrip via. These vias, together with the microstrip lines and junctions are simulated with EM simulation for all parasitic and coupling effects to be taken into account.

Scattering and noise parameters of the circuit in Fig. B.8 are extracted with the EM simulation at 3.3 GHz whose results are listed in Table B.2.

Table B.2. Port and noise parameters of unmatched amplifier at 3.3 GHz.

S_{11}	S_{21}	S_{12}	S_{22}	$NF_{\min}$ (dB)	Γ_{opt}	r_n
0.140/ -122°	6.02/ 41.9°	0.0897/ 36.6°	0.214/ -104°	0.689	0.17/ 157°	0.0575

B.2.4. Matching Networks

Designing matching networks includes the proper selection of source and load reflection coefficients Γ_S and Γ_L respectively. These choices are determined with a set of trade-offs between maximum gain and minimum noise figure. Before designing a matching network, this trade-offs should be clarified.

Analysis begins with the stability check. If the amplifier is stable, then the optimum source reflection coefficient for maximum available gain falls into the smith chart, otherwise; source and load reflection coefficients are determined with input and output stability circles. Two parameters K and B_1 quickly determine whether the amplifier is stable or not. These

parameters are calculated as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} = 1.119 \quad (\text{B.1})$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 = 0.6995 \quad (\text{B.2})$$

Since $K > 1$ and $B_1 > 0$, the amplifier is stable. Maximum available gain ($G_{A,max}$) and optimum source reflection coefficient (Γ_{MS}) are calculated as:

$$G_{A,max} = \frac{|S_{21}|}{|S_{12}|} (K - \sqrt{K^2 - 1}) = 41.4 = 16.2 \text{ dB} \quad (\text{B.3})$$

$$C_1 = S_{11} - \Delta S_{22}^* = 0.2212 / -147^\circ \quad (\text{B.4})$$

$$g_{a,max} = \frac{G_{A,max}}{|S_{21}|^2} = 1.1426 \quad (\text{B.5})$$

$$\Gamma_{MS} = \frac{g_{a,max} C_1^*}{1 + g_{a,max} (|S_{11}|^2 - |\Delta|^2)} = 0.356 / 147^\circ \quad (\text{B.6})$$

NF, VSWR_{IN} , VSWR_{OUT} are defined as:

$$NF = NF_{\min} + \frac{4r_n |\Gamma_S - \Gamma_{\text{opt}}|^2}{(1 - |\Gamma_S|^2) |1 + \Gamma_{\text{opt}}|^2} \quad (\text{B.7})$$

$$\Gamma_{\text{OUT}} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}, \Gamma_{\text{IN}} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (\text{B.8})$$

$$|\Gamma_a| = \left| \frac{\Gamma_{\text{IN}} - \Gamma_S^*}{1 - \Gamma_{\text{IN}}\Gamma_S} \right|, |\Gamma_b| = \left| \frac{\Gamma_{\text{OUT}} - \Gamma_L^*}{1 - \Gamma_{\text{OUT}}\Gamma_L} \right| \quad (\text{B.9})$$

$$\text{VSWR}_{\text{IN}} = \frac{1 + |\Gamma_a|}{1 - |\Gamma_a|}, \text{VSWR}_{\text{OUT}} = \frac{1 + |\Gamma_b|}{1 - |\Gamma_b|} \quad (\text{B.10})$$

Shown in Fig. B.10 is the optimum Γ_S selection trade-off between maximum gain and minimum noise figure. A line connects two points for selecting additional candidate Γ_S locations if the extends do not meet the requirements. Two ends of the line is analyzed for Γ_S selection and their results are summarized in Table B.3.

As can be seen from Table B.3 each Γ_S selection satisfies all the constraints depicted in Table B.1. This is due to the fact that the locations of Γ_{MS} and Γ_{opt} are very close to each other. In other words, a design which targets maximum gain by matching input and output simultaneously; also gets a near-minimum noise figure which is smaller than the maximum allowable noise figure dictated by the specifications. The same is also valid for a design

Table B.3. Γ_S selection trade-off summary.

Γ_S	Γ_{OUT}	$\Gamma_L = \Gamma_{OUT}^*$	VSWR _{OUT}	Γ_{IN}	VSWR _{IN}	G_A	NF
$\Gamma_{S_1} = \Gamma_{MS}$	0.403/ $\underline{118^\circ}$	0.403/ $\underline{-118^\circ}$	1	0.357/ $\underline{-147^\circ}$	1	$G_{A,max}$	0.74 dB
$\Gamma_{S_2} = \Gamma_{opt}$	0.304/ $\underline{-110^\circ}$	0.304/ $\underline{110^\circ}$	1	0.288/ $\underline{-149^\circ}$	1.29	16.1 dB	NF_{min}

which targets a minimum noise figure. When Γ_S is selected equal to Γ_{opt} , available gain G_A and matching specs for input and output ports are still satisfied. This is actually a very rare case for an RF designer to encounter such that; he/she must get a ticket at the end of the day to win the lottery. Since all selections comply with the specs, we select the first selection which targets maximum gain with input and output ports are matched.

Before moving into matching network design, following considerations must be examined properly. These rules must be checked and verified before prototyping; otherwise the circuit may encounter with a failure. Here, the instructions are listed as follows:

- It is a practical way to include a series capacitor in the matching network since it is going to be used for both matching and isolation between AC and DC parts of the circuit at the same time. If the target reflection coefficient is not suitable for such an implementation, a coupling capacitor which act nearly as a short circuit at the target frequency must be inserted. If no series capacitor is inserted, then the DC and AC parts of the circuit can not be isolated from each other which will cause a complete failure of the amplifier.
- If the matching circuit consists a shunt inductor or a shunt shorted-stub before the series capacitor is inserted, this will cause the short that node to the ground. The amplifier will not work since it is not biased properly. These shunt components must be at the AC part of the circuit which is isolated from the DC side. If the target impedance does not allow such a configuration, inserting a decoupling capacitor in series with the shunt component will prevent any DC current to flow to the ground and will act as a short circuit at the target frequency.
- There must be sufficient amount of copper pads at the input and output of the circuit

to provide soldering area for SMA connectors. Typically, these pads are built with microstrip lines having $50\ \Omega$ characteristic impedance. If the input and output impedances of the circuit are close to $50\ \Omega$, the length of the soldering pads does not affect the circuit if it has a characteristic impedance of $50\ \Omega$ according to transmission line theory. Same theory also indicates that the impedance seen into a transmission line with an electrical length of $0.5\ \lambda$ is equal to the load impedance that is connected to the end of the transmission line. In other words, one other way to insert a copper trace without affecting the amplifier is to select its electrical length equal to $0.5\ \lambda$ regardless from its characteristic impedance. A third possible way is to design a matching network with soldering pad is taken into account in the beginning of the design.

- If the transistor is potentially unstable at the frequency of operation either series or shunt connection of a resistor at the input or output port may help the transistor to become stable. Shunt resistor connections must be blocked by a capacitor to prevent any DC current to flow through the ground.

B.2.4.1. Input Matching Network

Electrical schematic of input matching network is given in Fig. B.11 (a). Referring Table B.3, source reflection coefficient is selected as $\Gamma_{MS} = 0.356/\underline{147^\circ}$ in the previous section. In other words, port impedance of $50\ \Omega$ is to be transformed into another impedance whose reflection coefficient is equal to Γ_{MS} .

As can be seen in Fig. B.11 (b), location of Γ_{MS} is suitable for the matching network to be designed with a series capacitor and series transmission line with proper characteristic impedance. The capacitor is represented with the measured model which is taken directly from vendor libraries and the microstrip line dimensions are tuned with the EM simulation to have the required characteristic impedance and the electrical length.

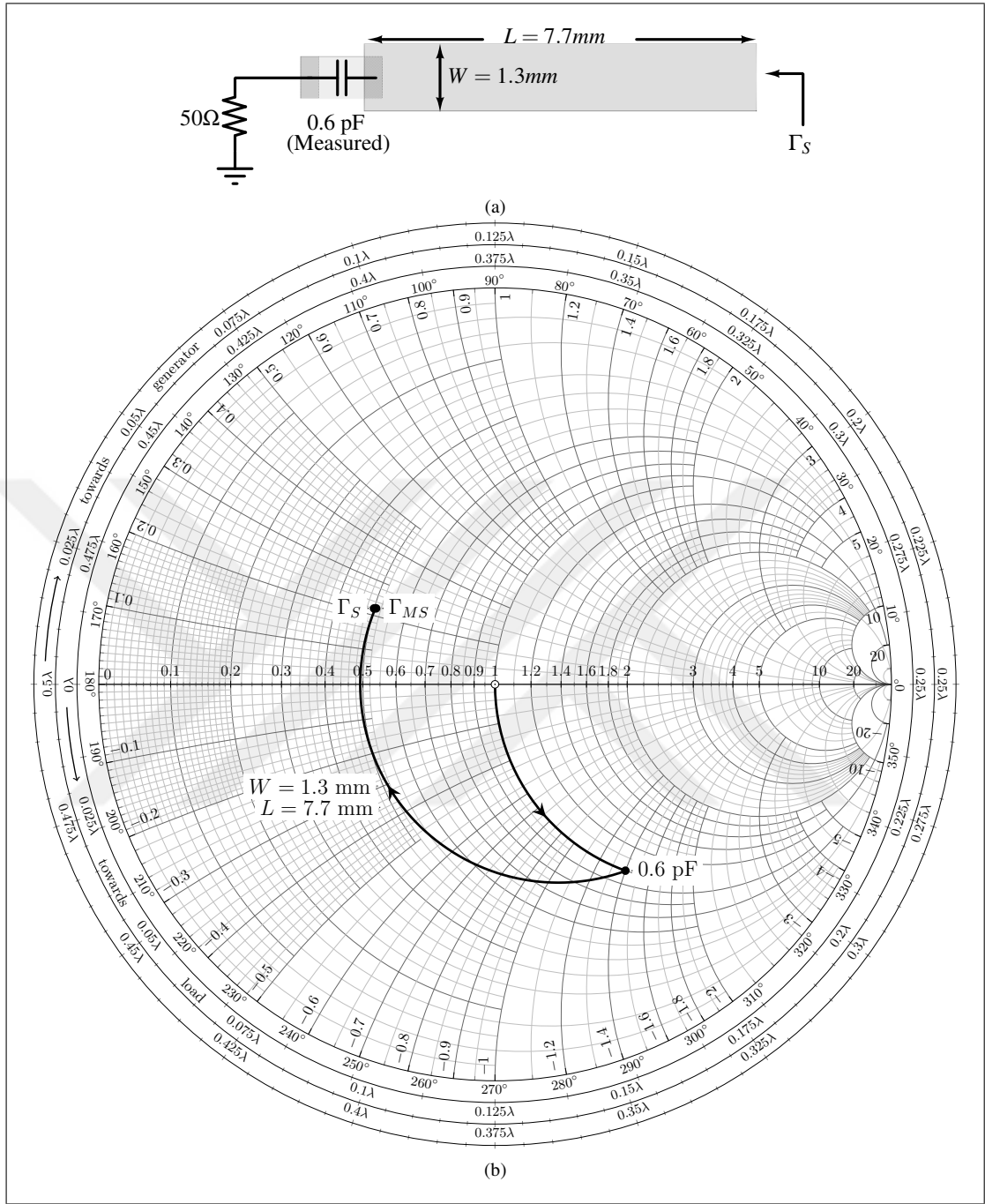


Figure B.11. Input matching network: (a) Schematic. (b) Design on smithchart.

B.2.4.2. Output Matching Network

Referring Table B.3, Γ_{OUT} is calculated as $0.403/118^\circ$ and the load reflection coefficient is selected as the complex conjugate of Γ_{OUT} to match the output properly, that is $VSWR_{OUT} = 1$. Location of Γ_L is close to Γ_{MS} , therefore same topology with input matching network can

be applied with proper tuning. Electrical schematic and design on smithchart is illustrated in Fig. B.12 (a) and (b) respectively.

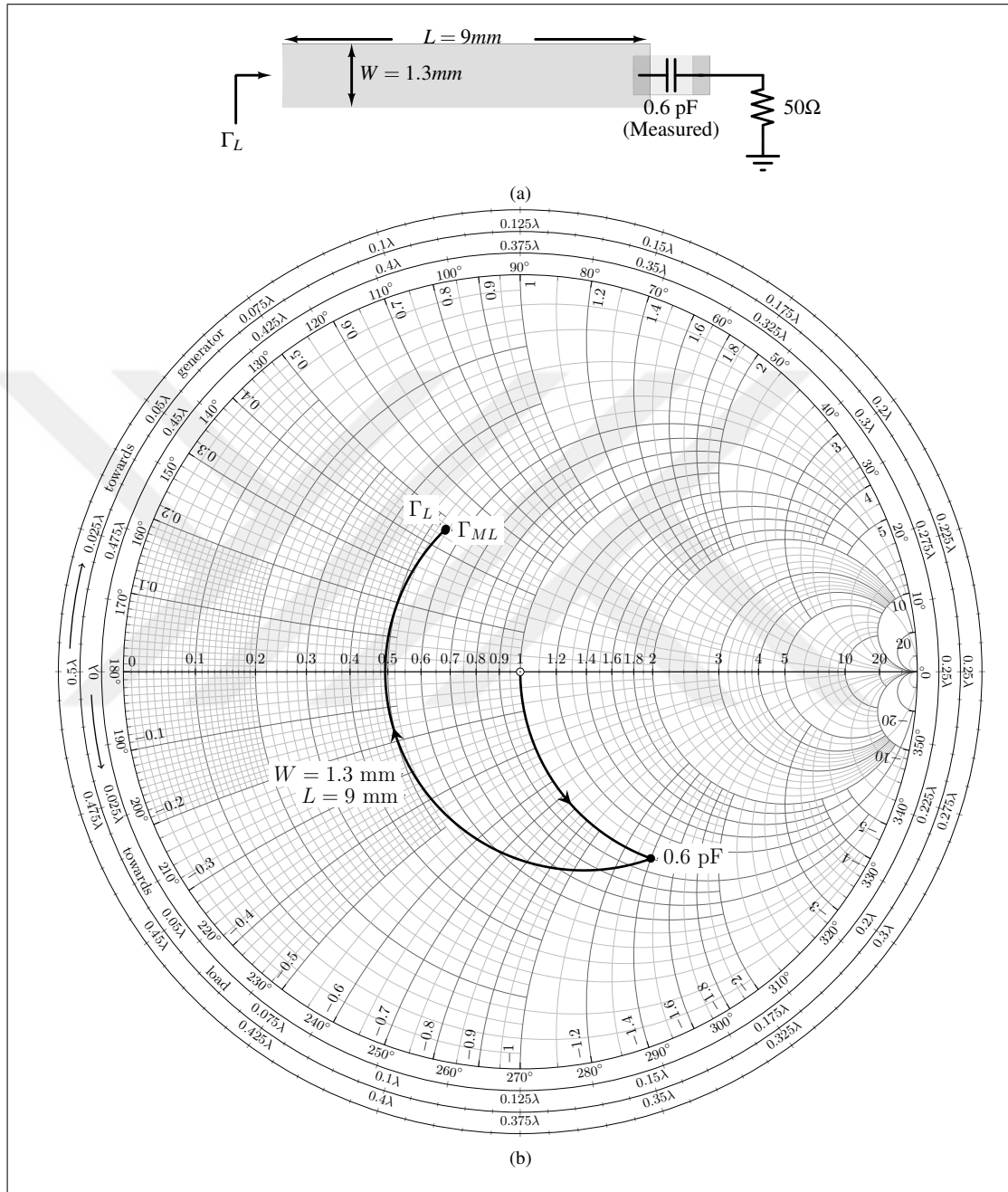


Figure B.12. Output matching network: (a) Schematic. (b) Design on smithchart.

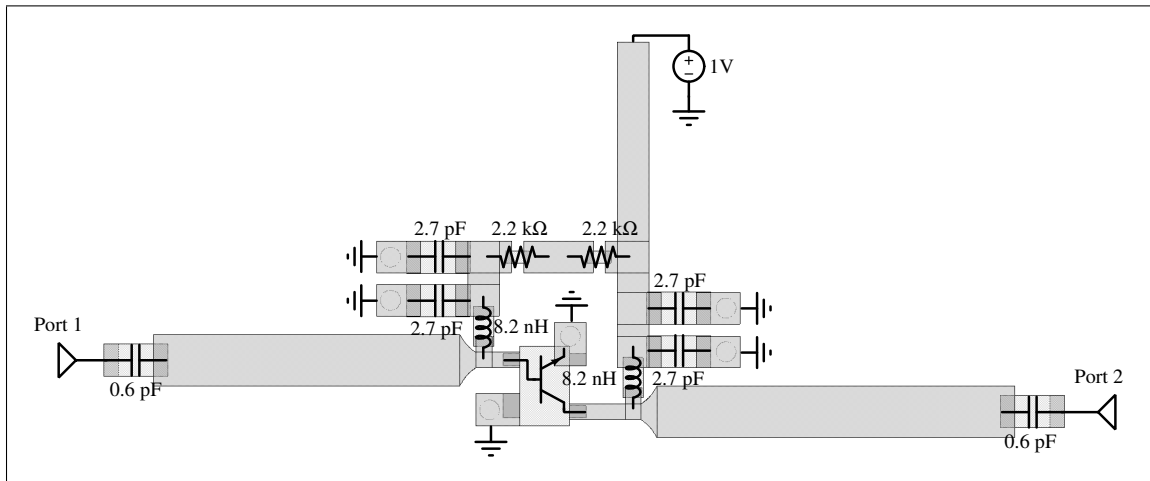


Figure B.13. Electrical schematic of matched amplifier.

B.3. VERIFICATION

B.3.1. Matched Amplifier

Electrical schematic of matched amplifier is given in Fig. B.13. It is the combination of S-parameter extraction circuit in Fig. B.8, input and output matching networks in Fig. B.11 (a) and Fig. B.12 (a) respectively. The reader may notice the absence of copper pads to be added for SMA connectors soldering. The reason why they are not shown in Fig. B.13 is that in the design of matching networks, their presence has not been taken into account. Once the verification of the circuit in Fig. B.13 is completed, a second analysis is going to be run to show the effects of adding the pads. As mentioned earlier, it is possible to design the matching network with soldering pad that is taken into account in the beginning of the design. In this respect, we choose the other way around and decided to give it a shot without taking into account of soldering pads.

Another difference is the presence of tapering lines attached at the base and collector of the transistor. Their presence is due to (a) make a smooth transition between matching network and base/collector of the transistor (b) provide a spacing between the bias tee and matching network. Since the electrical length of these lines are relatively small, their effect on amplifier performance is negligibly small.

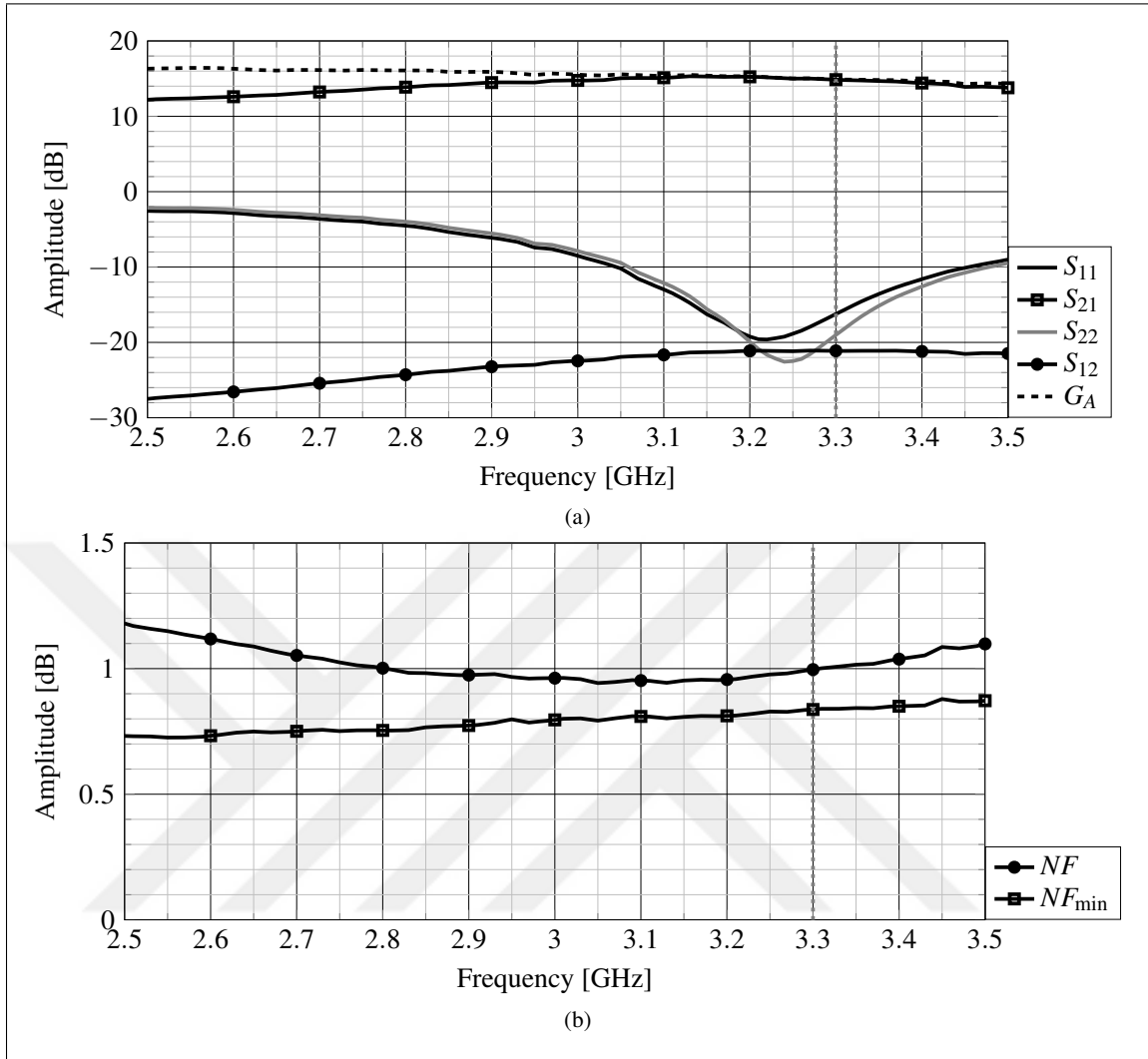


Figure B.14. LNA simulation results: (a) S-parameter. (b) Noise figure.

S-parameter and noise analysis results of the matched amplifier is given in Fig. B.14 (a) and (b) respectively. Magnitude of input and output reflection coefficients are read as -16 dB and -19 dB respectively. These values correspond to a voltage standing wave ratio of 1.37 for the input and 1.25 for the output which are quite below the maximums dictated by the specs. Also S_{21} is read as 14.9 dB which is nearly equal to the available gain G_A due to having a low mismatch at the input and output.

One unexpected result comes from the noise figure measurement of the amplifier. Based on the analysis summarized in Table B.3, selecting source reflection coefficient equal to Γ_{MS} would yield a noise figure of 0.74 dB. This holds true if the matching networks are replaced

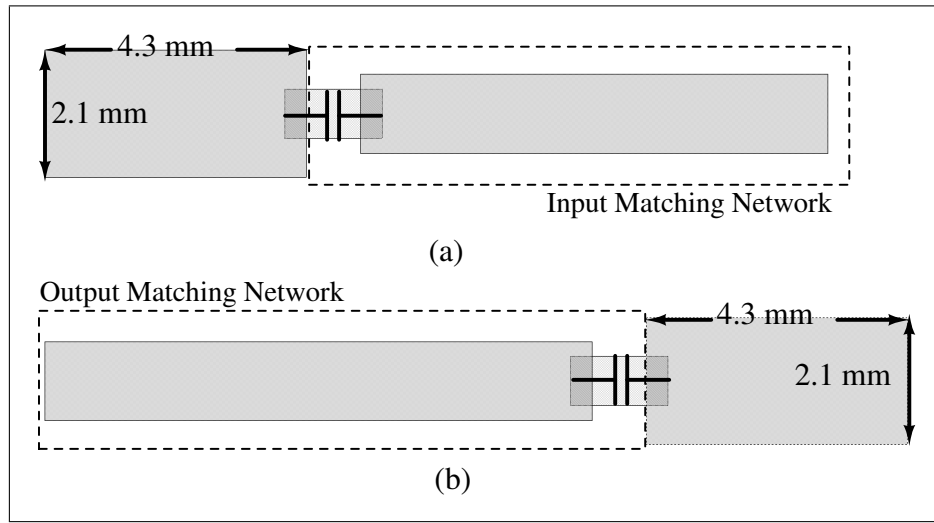


Figure B.15. Additional copper pads attached to: (a) Input matching network (b) Output matching network.

with a properly-set gamma-port which have no noise contribution on the circuit. Matching network components, however bring additional noise due to their inevitable resistive parts. One another reason is the coupling between bias tee and matching networks due to proximity. This causes the transistor to see an “effective Γ_S and Γ_L ” at its input and output which are slightly different than the pre-calculated values of Γ_S and Γ_L . That’s why EM simulation is pretty important when designing a high frequency circuit. Next comes the effect of adding soldering traces to see whether the situation is getting worse or not.

B.3.2. Matched Amplifier with Soldering Pads

The additional copper pads for soldering are merged with the matching networks as shown in Fig. B.15 (a) and (b) respectively. Dimensions of the pads are selected based on the physical dimensions of SMA connector. Similar to the other microstrip components of the circuit, these elements are also included in EM simulation. With these modifications, S-parameter and noise analysis of the amplifier is re-run and the results are plotted in Fig. B.16.

As can be seen in Fig. B.16 (a), S_{21} and S_{12} are not affected too much whereas the input and output reflection coefficients approaches to zero in magnitude roughly at 3.15 GHz. Noise figure shown in Fig. B.16 (b) is reduced by 0.1 dB compared with the circuit with no pads.

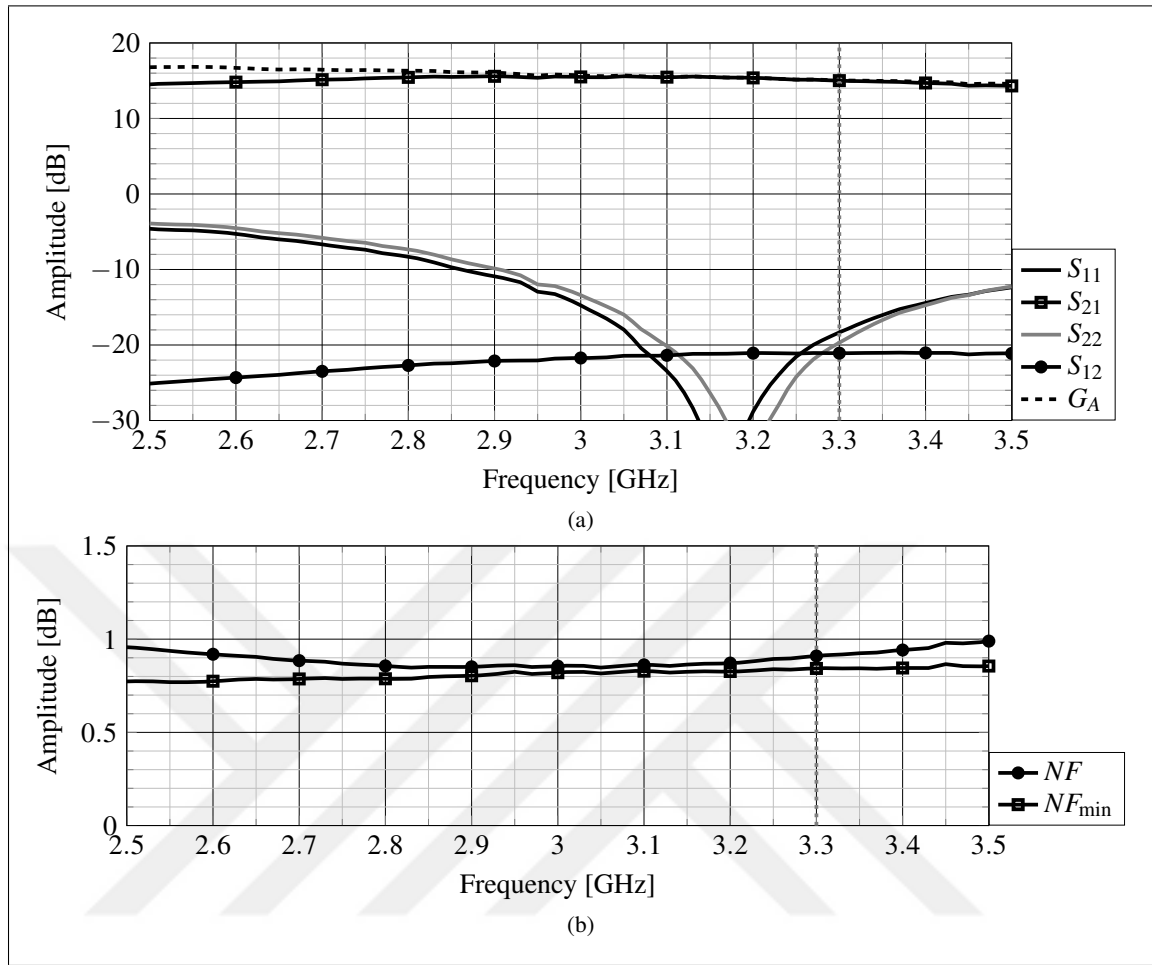


Figure B.16. Simulation results of LNA with soldering pads : (a) S-parameter. (b) Noise figure.

Before finding an answer how possible it is, let's try to tune the circuit so that the frequency where input and output reflection coefficients are minimum is shifted to 3.3 GHz.

B.3.3. Matched Amplifier with Final Tuning

Since matching networks contain only two elements namely, a capacitor and a microstrip line, the tuning options are limited. Possible options are (a) changing the value of capacitance (b) changing the dimensions of microstrip line. This procedure is not mandatory; since it is only for checking if a better result is available or not. At the end of trial-and-error effort, the width of microstrip lines are increased from 1.3 mm to 1.5 mm as shown in Fig. B.17.

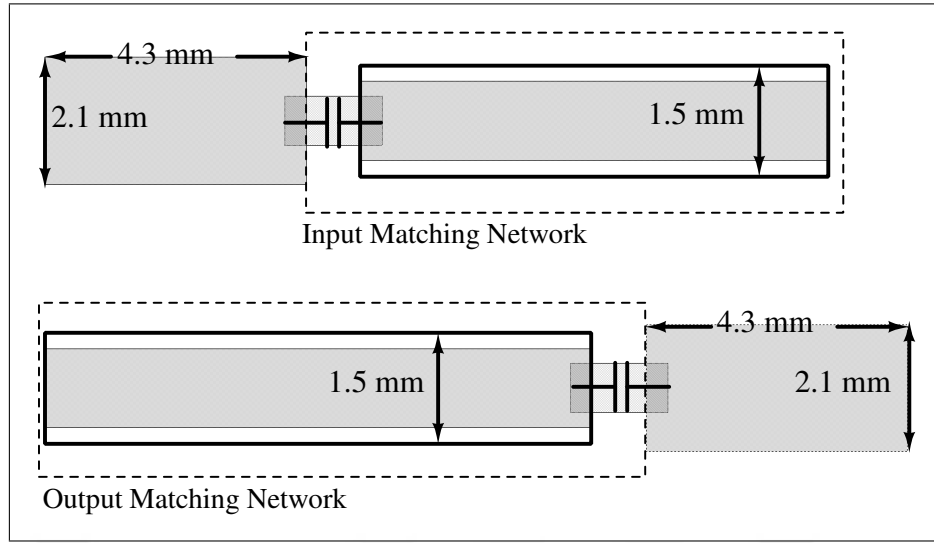


Figure B.17. Tuning the microstrip width in input and output matching networks.

With these modifications, S-parameter and noise analysis of the amplifier is re-run and the results are plotted in Fig. B.18. Port parameters S_{21} and S_{12} and noise figure are virtually remain the same whereas S_{11} and S_{22} have reached their minimum approximately at 3.3 GHz. Before proceeding into measurement results, it is important to explain how these modifications affected the amplifier in a positive way. Because if we are lucky, we need to know where this luck comes from. If are changing something in a systematic way, we should express its effect via some analytical or graphical methods.

B.3.4. Modified Matching Network Analysis

Additional copper pads and the tuning the microstrip widths have moved source and load reflection coefficients to the new pair of points denoted by $\Gamma_{S_{\text{new}}}$ and $\Gamma_{L_{\text{new}}}$ respectively. The circuit shown in Fig. B.19 is built and the impedance seen into each network is simulated to find their location on smith chart. The locations of $\Gamma_{S_{\text{new}}}$ and $\Gamma_{L_{\text{new}}}$ together with their older locations denoted by $\Gamma_{S_{\text{old}}}$ and $\Gamma_{L_{\text{old}}}$, and optimum noise termination denoted by Γ_{opt} are shown in Fig. B.20.

Before adding copper pads and changing the microstrip widths in the matching network, source reflection coefficient was located on the point denoted by $\Gamma_{S_{\text{old}}}$. This allows us to find

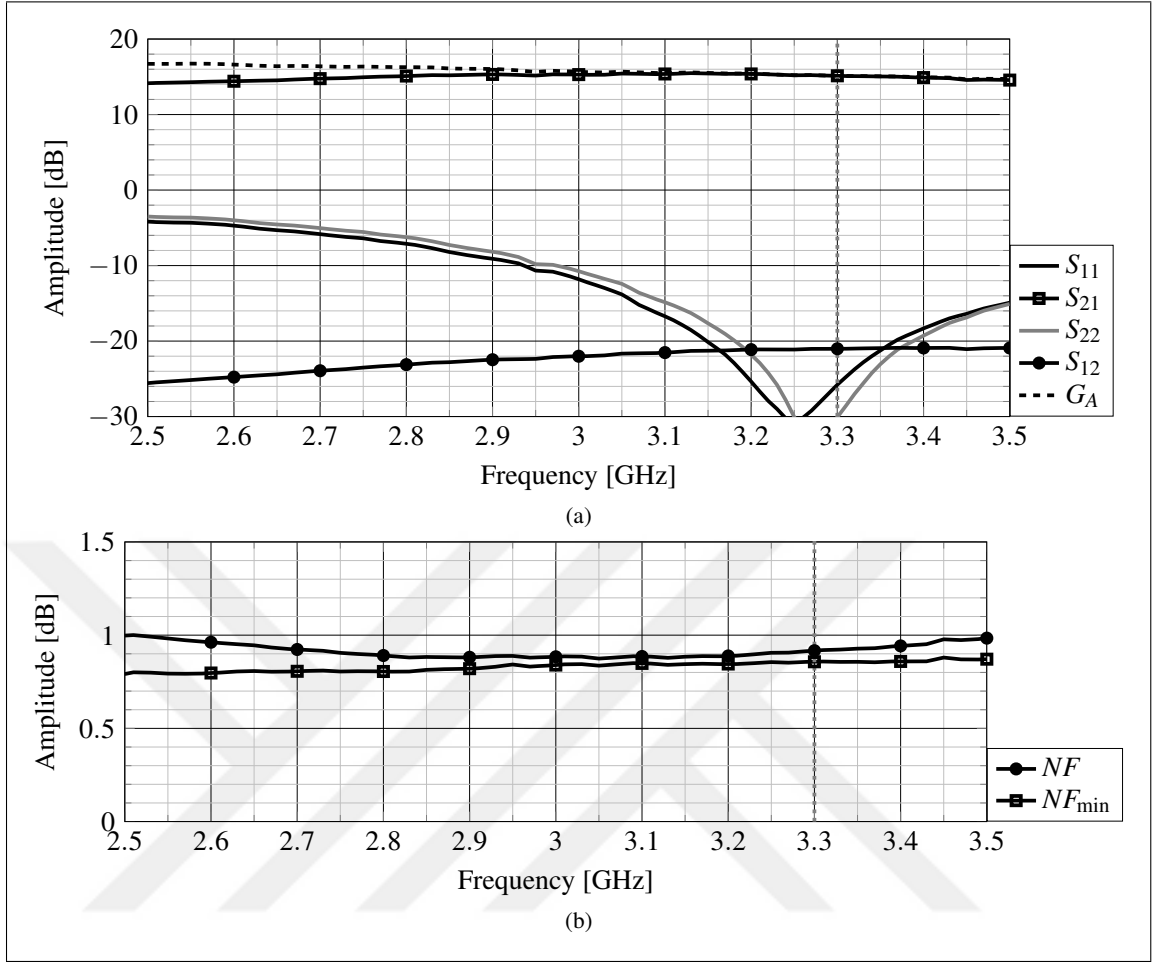


Figure B.18. Simulation results of LNA with modified matching networks : (a) S-parameter. (b) Noise figure.

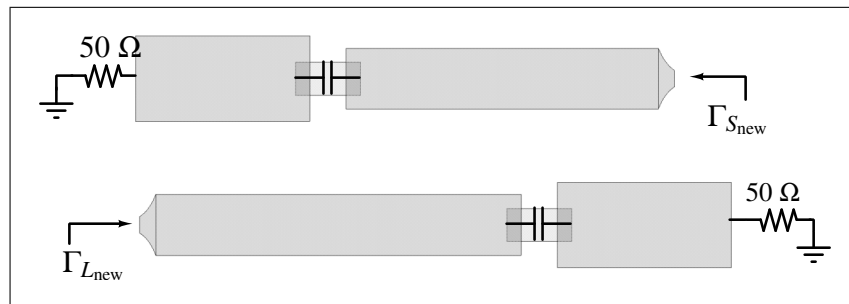


Figure B.19. Finding the new location of Γ_S and Γ_L in input and output matching network.

the value of Γ_{OUT} whose complex conjugate is selected as the load reflection coefficient denoted by $\Gamma_{L_{old}}$. Since the load reflection coefficient is equal to complex conjugate of Γ_{OUT} , $VSWR_{OUT}$ is equal to 1. With the modifications depicted above, source reflection coefficient has moved to a point denoted by $\Gamma_{S_{new}}$. This causes Γ_{OUT} to move a new location

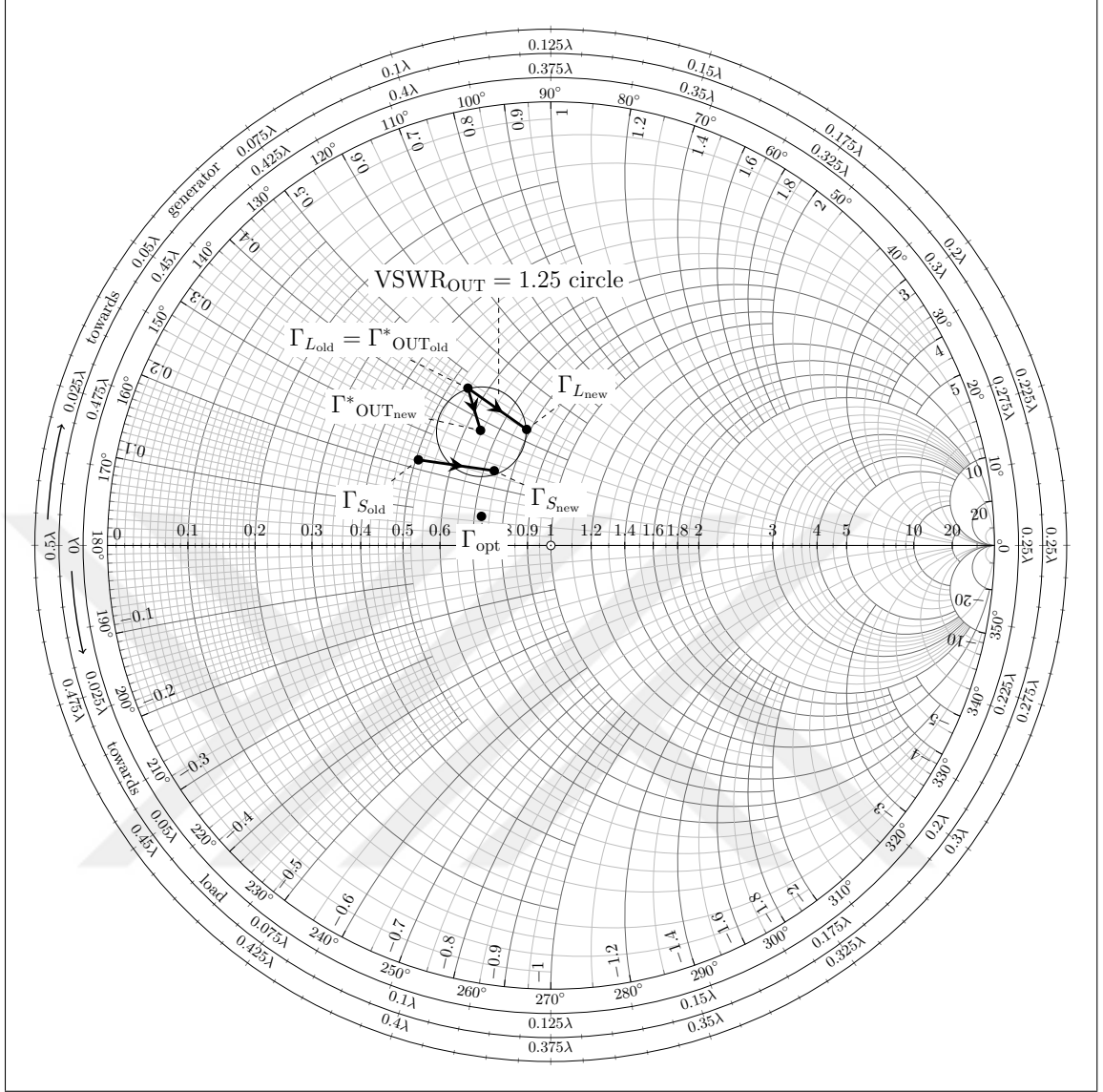


Figure B.20. Variation of source and load reflection coefficients.

whose complex conjugate is denoted by $\Gamma^{*}_{OUT_new}$. Same modifications has led load reflection coefficient to move a new point denoted by Γ_{L_new} . Even though the two points $\Gamma^{*}_{OUT_new}$ and Γ_{L_new} may seem separated, they are still close enough to each other as Γ_{L_new} lies on a circle that creates only a slight mismatch at the output, that is $VSWR_{OUT} = 1.25$. Since Γ_{S_new} is closer to Γ_{opt} than Γ_{S_old} , noise figure is lowered as can be compared by the plots in Fig. B.14 (b) and Fig. B.18 (b) respectively. In summary, we are lucky for a few reasons which are listed below.

- Γ_{MS} and Γ_{opt} are so close such that, a noise figure closer to minimum can be obtained

by targeting maximum gain. This proximity also helps us in such a way that, even though the additional modifications have moved us to a new point, amplifier noise figure is not affected; even got better.

- Source and load reflection coefficients are also close to each other. This helps us to design similar matching networks at the input and output. Their locations are also suitable for designing simple and robust networks that is, each network is built with only a capacitor and microstrip line. The near-identical values of reflection coefficients and their matching networks has led same amount of shift with the modifications depicted above. The new pair $\Gamma_{S_{new}}$ and $\Gamma_{L_{new}}$ have created a “near-simultaneous-conjugate match” that still satisfies the matching conditions dictated by $VSWR_{IN} \leq 2$ and $VSWR_{OUT} \leq 2$.
- The new location of source reflection coefficient is closer to Γ_{opt} which results to obtain lower noise figure. Since Γ_{MS} and Γ_{opt} close to each other, obtaining a lower noise figure, did not create a considerable change in the match conditions.

Final version of the amplifier with the modifications depicted above is given in Fig. B.21.

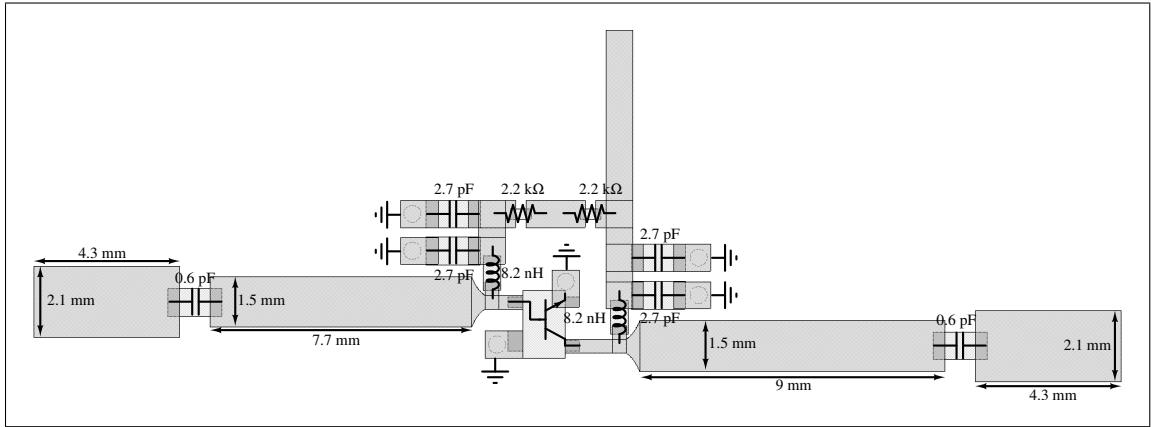


Figure B.21. Final version of LNA.

B.4. MEASUREMENTS

A prototyped version of the LNA is shown in Fig. B.22. There are a few changes in the prototype. Biasing resistor R_B is realized with a single resistor having a value of 10 kΩ,

leading a collector current of $I_C = 8$ mA drawn from the supply. Second change is the capacitor replacement. Capacitors in the matching networks have been replaced with 0.8 pF capacitors due to missing components in the Johanson capacitor kit.

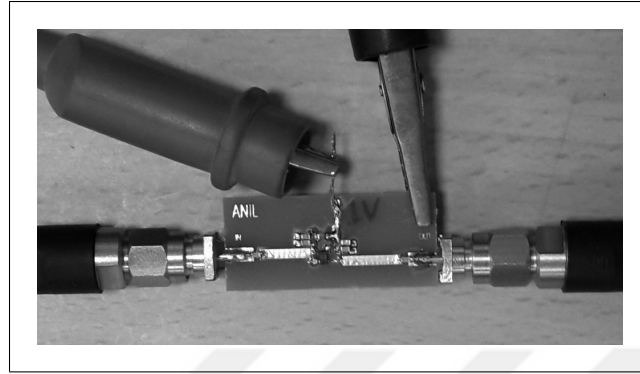


Figure B.22. Prototype of LNA.

Measured scattering and stability parameters are plotted in Fig. B.23. Noise figure measurements have not been performed due to lack of noise figure meter. The values read at 3.3 GHz are listed in Table B.4.

Table B.4. Measurement results summary.

S_{11}	S_{21}	S_{22}	S_{12}	G_A	K	B_1
-16.9 dB	14 dB	-20 dB	-22 dB	14.1 dB	1.48	0.85

As can be seen in Table B.4 input and output matching of the amplifier exhibits similarity with the simulation. Corresponding voltage-standing-wave-ratio for the input and output are calculated as $VSWR_{IN}=1.33$ and $VSWR_{OUT}=1.22$ which are below the limits dictated by the specs. Available gain is 1 dB lower than the predictions, but this is acceptable as long as the specs are satisfied. If a slight increase in gain is needed, collector current I_C can be slightly increased by selecting a lower value of R_B but it should be kept in mind that; this increase may lead to increase in noise figure. The amplifier is stable since $K > 1$ and $B_1 > 0$.

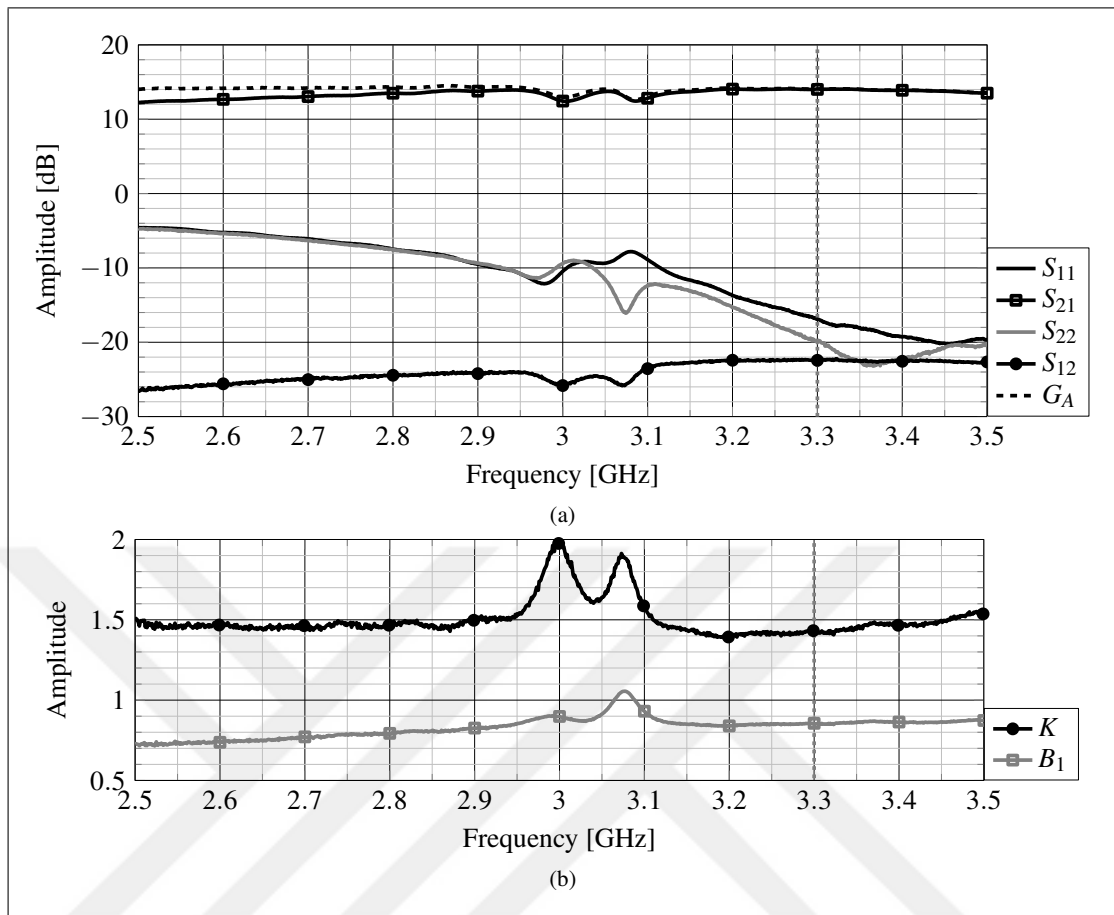


Figure B.23. LNA measurement results: (a) S-parameter. (b) Stability.