

FABRICATION OF ALN/GAN MIS-HEMT WITH SIN AS GATE DIELECTRIC AND PERFORMANCE ENHANCEMENT WITH ALD DEPOSITED ALUMINA

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Sağnak Sağkal
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Fabrication of AlN/GaN MIS-HEMT with SiN as gate dielectric and
performance enhancement with ALD Deposited Alumina

By Saęnak Saękal

October, 2016

We certify that we have read this thesis and that in our opinion it is fully adequate,
in scope and in quality, as a thesis for the degree of Master of Science.

Talip Serkan Kasıręa(Advisor)

Necmi Bıyıklı(Co-Advisor)

Selim Hanay

Emre Taşçı

Approved for the Graduate School of Engineering and Science:

Prof.Dr. Ezhan Karaşan
Director of the Graduate School

ABSTRACT

FABRICATION OF ALN/GaN MIS-HEMT WITH SiN AS GATE DIELECTRIC AND PERFORMANCE ENHANCEMENT WITH ALD DEPOSITED ALUMINA

Sağnak Sağkal

M.S. in Materials Science and Nanotechnology

Advisor: Talip Serkan Kasırga

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Silicon based transistors reached a limit, especially for high power and high frequency applications due to their relatively low bandgap and breakdown voltage. With its higher bandgap and breakdown voltage, GaN based transistors are promising devices for high power and high frequency applications. In particular with its high mobility due to the 2D Electron Gas at its interface, AlN/GaN heterostructure is a promising option to be used for such applications. High Electron Mobility Transistors (HEMT) fabricated on this heterostructure can work under higher voltages and higher frequencies when compared with standard silicon based transistors due to these superior properties. Also, as current electronics technology is mostly depend on Silicon based circuits, fabrication of these AlN/GaN HEMTs on Silicon substrates will provide easiness to integrate this technology to current systems. However, these transistors can suffer from high leakage currents, which can cause a high power consumption problem. One solution to this problem is depositing a dielectric under gate area and such kind of transistors are called as MIS-HEMTs.

In this thesis, MOCVD grown AlN/GaN on Silicon samples are used for fabrication of MIS-HEMTs. Before the fabrication of the transistors, a study on formation of ohmic contacts on these samples is performed. Then, two different AlN/GaN MIS-HEMTs with different gate dielectrics are fabricated and characterized. First type of samples have MOCVD grown SiN as gate dielectric and for second type of transistors, an alumina layer is deposited with ALD on top of SiN under gate area to decrease the gate leakage. Both of the transistors can remain gate control up to +2V gate bias. At least a three order of magnitude of decrease in gate leakage current is observed for high negative gate biases after deposition

of alumina. Also, a gate leakage current in the order of $10^{-10} - 10^{-11} A$ is observed for lower negative biases. A peak transconductance of $2.57 mS$ is obtained for the transistors with gate length of $2 \mu m$, which is decreased to $1.71 mS$ after alumina deposition.



Keywords: AlN, GaN, HEMT, gate leakage current, atomic layer deposition, alumina.

ÖZET

SiN KATMANININ KAPI DİELEKTİĞİ OLARAK KULLANILDIĞI ALN/GAN MIS-HEMT YAPILARININ ÜRETİMİ VE ALD İLE KAPLANAN ALUMİNA İLE PERFORMANSININ ARTIRILMASI

Sağnak Sağkal

Malzeme Bilimi ve Nanoteknoloji, Yüksek Lisans

Tez Danışmanı: Talip Serkan Kasırga

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Silikon bazlı transistörler, bant genişliği ve kırılma geriliminden kaynaklı olarak, özellikle yüksek güç ve yüksek frekans uygulamaları konusunda bir limite ulaşmışlardır. Daha yüksek bant genişliği ve kırılma gerilimine sahip olması sebebiyle, GaN temelli transistörler, yüksek güç ve yüksek frekans uygulamaları için uygun malzemeler olarak görülmektedirler. Özellikle AlN/GaN heteroyapıları, arayüzeyindeki 2D Elektron Gazı kaynaklı yüksek elektron mobilitesi sayesinde bu tip uygulamalar için uygun bir aday haline gelmektedir. Bu özellikleri sayesinde, bu yapılar üzerine geliştirilen yüksek elektron mobiliteli transistörler(HEMT), Silikon temelli transistörlere göre daha yüksek gerilim ve frekans altında çalışabilirler. Ayrıca, günümüz elektronik teknolojisinin Silikon temelli olması sebebiyle, AlN/GaN HEMT yapılarının Silikon örnekler üzerine büyütülmesi, bu teknolojinin günümüz sistemlerine entegrasyonunu kolaylaştıracaktır. Fakat, bu transistörler, daha fazla enerji tüketimine sebep olacak şekilde yüksek kap kaçak akımı problemine sahiptirler. Bu sorun için geliştirilen çözümlerden biri, MIS-HEMT adı verilen, kapı kontağı altında bir dielektrik malzeme bulunan transistörlerdir.

Bu çalışmada, Silikon üzerine MOCVD tekniği ile büyütülen AlN/GaN örnekler kullanılmıştır. Transistörlerin üretimine başlamadan önce, bu örnekler üzerine ohmik kontakların yapılabilmesi için çalışmalar gerçekleştirilmiştir. Sonra farklı dielektrikler kullanarak iki farklı MIS-HEMT yapısı üretilmiş ve karakterize edilmiştir. İlk tip transistörlerde MOCVD ile büyütülen SiN, kapı dielektriği olarak kullanılırken, ikinci tip transistörlerde, kapı kaçak akımını düşürmek amacıyla kapı kontağı altında, SiN üzerine ALD tekniği ile alumina

büyütülmüştür. Her iki transistörde de $+2V$ kapı gerilimine kadar kapı üzerinden kontrol özelliği korunmuştur. Alumina büyüülmesinden sonra, yüksek negatif gerilim altındaki kapı kaçak akımında en az üç derecelik bir düşüş gözlenmiştir. Ayrıca, düşük negatif gerilim altında $10^{-10} - 10^{-11}A$ aralığında kapı kaçak akımı gözlenmiştir. Bunların dışında, $2\mu m$ kapı uzunluğuna sahip örneklerde, $2.57mS$ lik transkondüktans değeri elde edilmiş ve bu değeri, alumina kaplanması ile $1.71mS$ 'e düşmüştür.



Anahtar sözcükler: AlN, GaN, HEMT, kapı kaçak akımı, atomik katman kaplama, alumina.

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Contents

1	Introduction	1
1.1	Introduction to Transistors	1
1.2	AlN/GaN HEMT Structure	3
1.3	Research Objectives	5
1.4	Thesis Overview	6
2	Theoretical Background for AlN/GaN HEMTs	8
2.1	Spontaneous and Piezoelectric Polarization in AlGaN/GaN Het- erostructures	8
2.2	Theoretical Information about HEMT Operation	13
2.3	Background Information on Contact Materials	17
3	Fabrication of AlN/GaN MIS-HEMTs	20
3.1	Introduction	20
3.2	Mask Writing for Fabrication	20

3.3	Sample Preparation	22
3.4	Optical Lithography	23
3.5	Metal Deposition	27
3.6	Lift-off	29
3.7	Annealing	29
3.8	Dry Etching	31
3.9	Atomic Layer Deposition	36
3.10	Fabrication Steps	38
4	Ohmic Contact Formation	42
4.1	Introduction	42
4.2	Transmission Line Method	42
4.3	Electrical Characterization of Ohmic Contacts	44
4.4	Van Der Pauw Structures	49
5	Electrical Characterization of AlN/GaN MIS-HEMTs	54
5.1	Introduction	54
5.2	Characterization of s-MIS-HEMTs	55
5.3	Characterization of a-MIS-HEMTs	59
5.4	Gate Leakage Currents for s-MIS-HEMTs and a-MIS-HEMTs . . .	62



List of Figures

1.1	Growth of GaN on Silicon with and without buffer layer[15]	3
1.2	A representative figure for HEMT structure	5
2.1	Crystal structure of Ga and N-Face GaN crystal [40]	9
2.2	Polarization vectors and corresponding induced charge densities on AlGaIn/GaN heterostructure [44]	11
2.3	Band diagram of AlGaIn/GaN heterostructure before and after reaching t_{CR} [17]	12
2.4	3D illustration of AlN/GaN HEMT	13
2.5	I_D vs V_{DS} graphs at different gate voltages [48]	16
2.6	Ti/Al/Ni/Au metal stack with alloys formed after annealing	18
3.1	Screen shot of mask from L-Edit	21
3.2	AZ5214E as positive and negative photoresist[57]	24
3.3	Examples for alignmentmarks used in this project	25
3.4	EVG 620 Mask Aligner System	26

3.5	Pictures of E-beam evaporator(left) and Thermal evaporator(right)	28
3.6	Lift-off process	30
3.7	Rapid thermal annealing system	31
3.8	STS-615(left) and STS-616(right) ICP systems	32
3.9	SEM picture of surface after CF_4/O_2 ICP treatment	33
3.10	AFM images for CF_4/O_2 etch recipe	34
3.11	XPS results for CF_4/O_2 recipe	35
3.12	1 cycle of an ALD process [63]	37
3.13	ALD Savannah 100 system	38
3.14	Steps of ohmic metallization steps	39
3.15	Mesa etching process	40
3.16	Deposition of gate metal	41
4.1	TLM structure	43
4.2	An example for R_T vs distance graph[65]	44
4.3	SEM image of TLM structures	45
4.4	Current vs voltage graph for the sample without native oxide removal	46
4.5	I-V results before(a) and after(b) annealing	47
4.6	R_T vs distance graph for annealing temperatures of 800(a),850(b) and 900°C(c)	48

4.7	van der pauw structure used in this project	50
5.1	SEM(a) and optical microscope(b) image of fabricated HEMTs . .	55
5.2	I_D vs V_{DS} characteristics of s-MIS-HEMTs with gate length of 2(a),3(b) and 5(c) μm	56
5.3	G_m vs V_{GS} characteristics of s-MIS-HEMTs with gate length of 2(a),3(b) and 5(c) μm	58
5.4	I_D vs V_{DS} characteristics of a-MIS-HEMTs with gate length of 2(a),3(b) and 5(c) μm	60
5.5	G_m vs V_{GS} characteristics of a-MIS-HEMTs with gate length of 2(a),3(b) and 5(c) μm	61
5.6	I_G vs V_{GS} characteristics of s-MIS-HEMTs(black line) and a-MIS- HEMTs(red line) with gate length of 2(a),3(b) and 5(c) μm . . .	63

List of Tables

3.1	Parameters used in metal deposition	29
3.2	Ar/Cl_2 ICP etch recipe parameters	36
4.1	R_C and R_{SH} values at different annealing temperatures	49
4.2	eZHEMS measurement results for different applied current	53
5.1	Transistor dimensions	55

Chapter 1

Introduction

1.1 Introduction to Transistors

Transistors are one of the key elements that are used in most of today's technological devices such as computers, televisions, sound systems, power amplifiers etc. They are based on semiconductor materials such as Silicon, Germanium and III-V compounds and used as amplifier or switch in electronic circuits. They generally have three terminals and in a circuit, a voltage is applied between two terminals to control the voltage or obtain an amplified signal at the output.

The first transistor is made in Bell Laboratories by using Germanium as semiconductor material in 1947 [1]. Later, Silicon become the most preferred semiconductor material that is used for transistor fabrication due to its low cost. Today, in most of the devices, Silicon based transistors are used with its native oxide(SiO_2), which is an excellent dielectric. Moreover, Complementary Metal Oxide Semiconductor(CMOS) transistors are the basis of today's digital circuits, which are based on Silicon as semiconductor material. Therefore, further development in transistor technology should be compatible with this Silicon based technology. In other words, it must be possible to fabricate newly developed devices on Silicon substrates in order to easily unite this new technology with

current devices.

The most popular Silicon based transistor types in the industry are Bipolar Junction Transistors(BJT) and Metal Oxide Semiconductor Field Effect Transistors(MOSFET). BJTs consist of combination of two p-n junction diodes. By applying forward or reverse bias to these junctions, one can modify the depletion region that is caused by the junctions, therefore control the signal or obtain an amplified signal at the output. On the other hand, MOSFETs consist of two highly doped area, which are called source and drain. Third terminal, which is called as gate, is placed on the less doped area between those two highly doped area and it is placed on an oxide layer. By applying a voltage between gate and source, one can modify the conductivity between source and drain and control the current flowing through these terminals by this way.

Silicon transistors served well in electronics industry, however, researchers work on different materials that will be superior to Silicon, especially for high frequency applications. [2] Moreover, using a semiconductor with a higher breakdown electric field will be beneficial, especially devices that works at high voltage such as power electronics area. One solution found to this situation is High Electron Mobility Transistors(HEMT) and the first HEMT transistor is designed and fabricated in 1979 by Mimura by using GaAs. [2] Later, in early 90's, first GaN based HEMTs are fabricated. [3]

In a different way from Silicon based transistors, HEMTs are fabricated on a heterostructure of two semiconductors, in this case $Al_xGa_{1-x}N/GaN$ heterostructure. [3] By this way, no extra doping process is required to fabricate these transistors. In addition to this, HEMTs requires a substrate at the bottom, where this substrate provides the surface to start GaN growth. Today, it is possible to fabricate GaN based HEMTs on different substrates such as Sapphire [4–6], Al_2O_3 [7], Silicon Carbide [8,9] and Silicon [10,11].

1.2 AlN/GaN HEMT Structure

GaN is a wide bandgap semiconductor material with a bandgap value of 3.4eV, [12] which makes it superior to Silicon for high power-high frequency applications. For example, mobile base stations are devices from 100W class and to reach that power, parallel configuration of multiple Silicon transistors are required. Instead of it, a single GaN HEMT can reach the same power level. [13] Also, GaN based transistors can have higher breakdown voltages as GaN has a higher breakdown electric field(E_c) value. ($E_c = 3.3 \times 10^6 V/cm$ for GaN, where $E_c = 0.3 \times 10^6 V/cm$ for Silicon) [14].

Fabrication of GaN HEMTs on Silicon substrates will make them easily suit in current technology. However, growth of GaN on Silicon is challenging as there is a lattice mismatch between GaN and Silicon over 14%. [15] Also, as GaN growth is a high temperature process, due to the difference between thermal expansion coefficients of GaN and Silicon, some cracks may occur on GaN film. [15] To avoid these cracks, stress on the GaN film should be reduced. For this purpose and successfully grow GaN on Silicon, a nucleation and buffer layer, which consist of $Al_xGa_{1-x}N$ with variable Al composition, or sequentially grown multiple AlN/GaN layers, is required. This situation is explained in Figure 1.1.

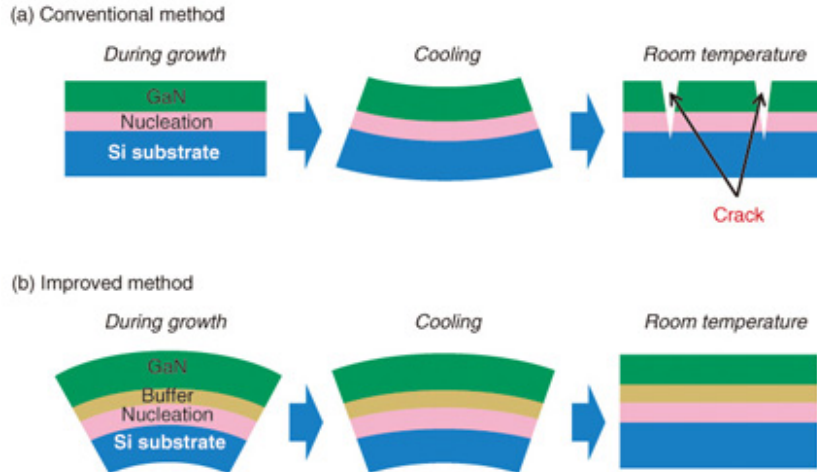


Figure 1.1: Growth of GaN on Silicon with and without buffer layer[15]

Epitaxial growth of GaN on Silicon is mostly done by using Metal-organic Chemical Vapor Deposition [10], but there are also examples of epitaxial growth done by Molecular Beam Epitaxy [16]. For fabrication of HEMTs, GaN is not used alone, but its heterostructure with $Al_xGa_{1-x}N$ is used. AlGa_xN/GaN heterostructure consists a 2D Electron Gas(2DEG) at its interface, which provides high electron mobility to the substrate. This 2DEG forms due to spontaneous and piezoelectric polarizations. [17] This situation will be explained detailed in Chapter 2.

In fabrication of GaN based HEMTs on Silicon, after nucleation and buffer layers, a channel layer, which is formed by the material with lower bandgap (in this case GaN) is grown. On top of it, a thin barrier layer, which is formed by material with higher bandgap (in this case AlGa_xN), is grown. Thickness of the barrier layer in this heterostructure is an important parameter and decided carefully for high performance transistors. Decreasing the thickness of barrier layer will result with lower gate leakage, which is a desired result for power applications. [18] On the other hand, decreasing the thickness of barrier layer also cause a decrease in 2DEG density, which is a drawback for high frequency applications. [19]

One solution to this dilemma is using AlN as a barrier layer. Piezoelectric and spontaneous polarization difference can be maximized by using AlN as barrier, thus, higher 2DEG density can be obtained with even thinner films. A 2DEG density of $5.5 \times 10^{13}/cm^2$ can be obtained with only 7nm thick AlN layer [20], whereas 2DEG density for 25nm $Al_{0.26}Ga_{0.74}N$ layer is $6.2 \times 10^{12}/cm^2$ [21].

Another solution for gate leakage problem is placing an insulator under gate area, in other words, fabrication of Metal Insulator Semiconductor HEMTs (MIS-HEMT).Deposition of insulator material can be realized by many method such as thermally grow method [22], Chemical Vapor Deposition (CVD) [23,24] or Atomic Layer Deposition (ALD) [25]. Also, there are many choices that can be used for this purpose such as SiO_2 [26], SiN [21, 27] and Al_2O_3 [28, 29]. The deposited insulator material can also used as a passivation layer and it can suppress current collapse [30] In addition to this, a thin SiN layer can help to reduce stress on AlN layer and therefore, increase surface quality. [31] This thin SiN layer can

also be used as a protection layer for AlN layer during fabrication process. The photoresist developer AZ400K etches AlN, which may cause a problem in device performance as it may weaken or completely remove 2DEG channel. [32] By putting a thin SiN at top, AlN layer can be protected against etchant effect of AZ400K during process.

A representative figure of a HEMT structure with AlN as barrier layer can be observed in 1.2. There is also an insulator layer, which is an optional layer in such kind of structures.

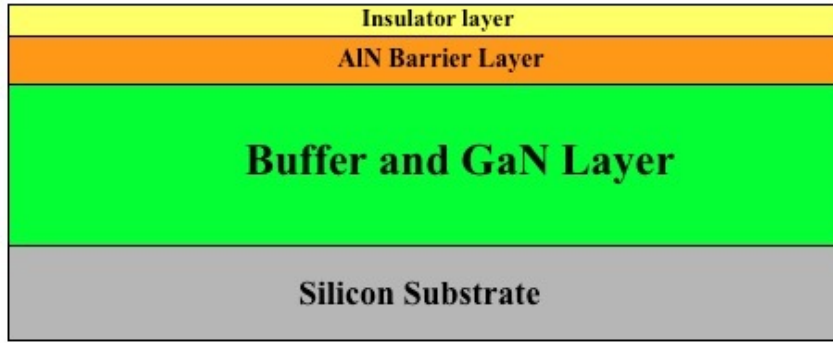


Figure 1.2: A representative figure for HEMT structure

1.3 Research Objectives

Gate leakage is one of the main problems that GaN based HEMTs are dealing with. Mechanism of this leakage is still being researched [33], but it is known that leakage current is caused by traps based on dislocations and N-vacancies [34,35]. Also, it is found that one of the dominant mechanism for this gate leakage is through vertical tunneling, which occurs between barrier and channel layer and there is a significant contribution from lateral tunneling, which occurs between gate and drain contacts [36]. By putting a dielectric under gate area, one can decrease the gate leakage current [37]. Putting a dielectric material can remove the traps due to N-vacancy, therefore lessens the sources of gate leakage [34].

In this research, MOCVD grown AlN/GaN heterostructure grown on Silicon samples that are bought from EpiGaN is used to fabricate and characterize MIS-HEMTs. Effects of deposition of different dielectrics on gate leakage current is investigated. For this purpose, steps that are followed can be seen below:

1. Fabrication of ohmic contacts on AlN is a challenging situation, therefore, a study for ohmic contact fabrication is realized. Results at different annealing temperatures are compared.
2. The samples have a thin in-situ grown SiN layer on top of them. This layer is used as gate dielectric to fabricate MIS-HEMTs and electrical characterization of them are made.
3. Effect of adding another dielectric on in-situ grown SiN as gate dielectric is investigated. For this purpose, thin film of Al_2O_3 is deposited with ALD on SiN as gate dielectric to fabricate MIS-HEMTs. Electrical characterizations are made and gate leakage of samples are compared.

1.4 Thesis Overview

This thesis consists of six chapters. Chapter 1 (this chapter) is the introduction chapter, which gives some background information about history of transistors, a brief introduction for GaN based HEMTs and objectives of this research.

Chapter 2 will give detailed information about polarization in material, operation of HEMTs and materials used to form contacts.

Chapter 3 will define the fabrication techniques used in this research and give the fabrication steps that are followed for HEMT fabrication.

Chapter 4 will be about ohmic contact formation on AlN and experimental results of this process

Chapter 5 will have experimental results of MIS-HEMTs with different gate dielectrics and a comparison of gate leakage performances of them.

Chapter 6 will conclude the thesis with a brief summary.



Chapter 2

Theoretical Background for AlN/GaN HEMTs

2.1 Spontaneous and Piezoelectric Polarization in AlGaN/GaN Heterostructures

GaN, like other III-V nitrides, has a wurtzite crystal structure, which has 4 tetrahedrally coordinated atoms with a Bravais lattice in its unit cell [38]. Crystal structure of wurtzite can be defined by three parameters, which are edge length a of hexagon, the height c of the prism and length u of the anion-cation bond along (0001) axis. Due to the nonideality in their structure, III-V nitrides contain very large spontaneous polarization, in other words, polarization in zero strain, and this spontaneous polarization strength increases while going from GaN to InN and AlN, due to the increased nonideality (u increases and c/a decreases). Moreover, spontaneous polarization in AlN is only 3-5 times smaller than ferroelectric perovskites [39]

For GaN structure, there are two possible polar faces that can be used to define the material. The material becomes Ga-face, if Gallium is on the top position and materials with opposite situation are called as N-faced. These structures can be

observed in Figure 2.1 [40]. In this project, Ga-face samples are used.

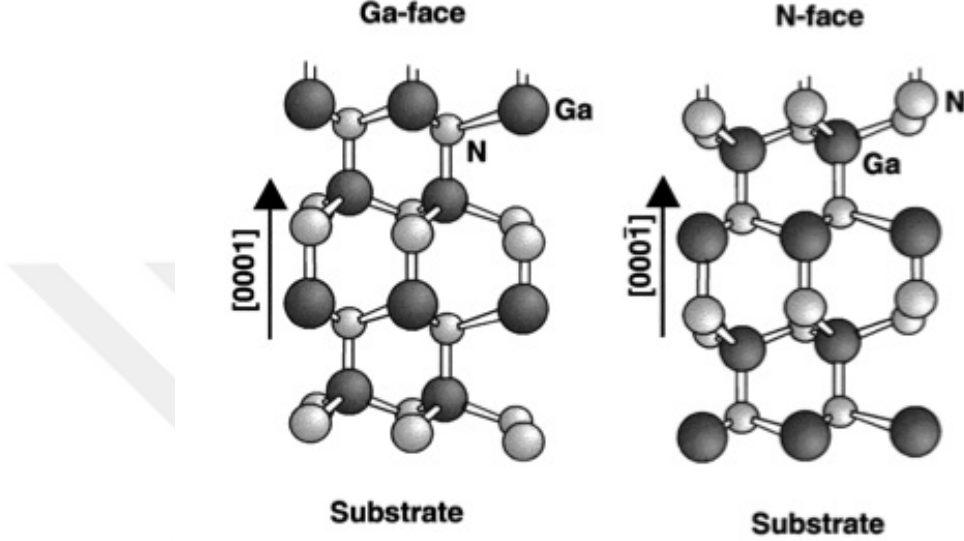


Figure 2.1: Crystal structure of Ga and N-Face GaN crystal [40]

For a Ga-face sample, the direction of spontaneous polarization is negative, which means that direction of polarization is through the substrate [41]. Opposite situation is valid for N-face samples. In addition to this, growth of AlGaN film on top of a GaN layer ends up with a strain on these materials due to the lattice mismatch between them. Because of this strain, a piezoelectric polarization exists in such kind of heterostructures in c axis and this piezoelectric polarization can be calculated by the formula [42]

$$P_{PE} = 2 \frac{a - a_0}{a_0} (e_{31} - e_{33} \frac{C_{13}}{C_{33}}), \quad (2.1)$$

where C_{13} and C_{33} are elastic constants, e_{33} and e_{31} are piezoelectric coefficients. For AlGaN,

$$(e_{31} - e_{33} \frac{C_{13}}{C_{33}})$$

is negative for any Al composition so, under tensile strain ($a > a_0$), piezoelectric polarization is negative. [42] In order to maximize total magnitude of polarization, piezoelectric and spontaneous polarization should be on the same direction. Therefore, as spontaneous polarization is negative for Ga-face GaN, piezoelectric

polarization should be negative, which means, tensile strain should be applied on AlGa_N. It is found that growth of AlGa_N layer on Ga_N ends up with a tensile strain and reverse of it causes a compressive strain [42]. Therefore a configuration such as in Figure 1.2 is ideal for a Ga-face sample in order to maximize total polarization.

The gradient of polarization gives the polarization induced charge density. Therefore, in an AlGa_N/Ga_N heterostructure, polarization induced sheet charge density at the interface can be calculated by [42]

$$\begin{aligned}\sigma &= P(\text{GaN}) - P(\text{AlGaN}) \\ &= P_{SP}(\text{GaN}) - P_{SP}(\text{AlGaN}) - P_{PE}(\text{AlGaN})\end{aligned}\tag{2.2}$$

where P_{SP} is used for spontaneous polarization and P_{PE} is used for piezoelectric polarization. Note that piezoelectric polarization for Ga_N is neglected as Ga_N layer is a thick layer and it is almost relaxed. It is also known that P_{SP} of AlGa_N has a higher magnitude than P_{SP} of Ga_N. Therefore, polarization induced charge density at the interface is positive(+ σ) for AlGa_N/Ga_N heterostructure. Also, as there is no externally applied field, a negative induced charge density(- σ) must exist at the surface of AlGa_N layer for charge neutrality in the material [43]. The resultant structure can be observed in Figure 2.2 [44].

There exists a surface donor state 1.65eV below AlGa_N conduction band [17]. During the growth of AlGa_N on top of Ga_N, these donor states are initially below fermi level. Therefore these levels are occupied by electrons and behaves as a trap as these electrons cannot leave these states. As the thickness of AlGa_N on top of Ga_N increases, the difference between donor states and fermi level decreases. When the thickness of AlGa_N layer reaches a specific height, donor state and fermi level meets with each other, therefore electrons at donor states can jump to conduction band and become free electrons. This specific height is called as

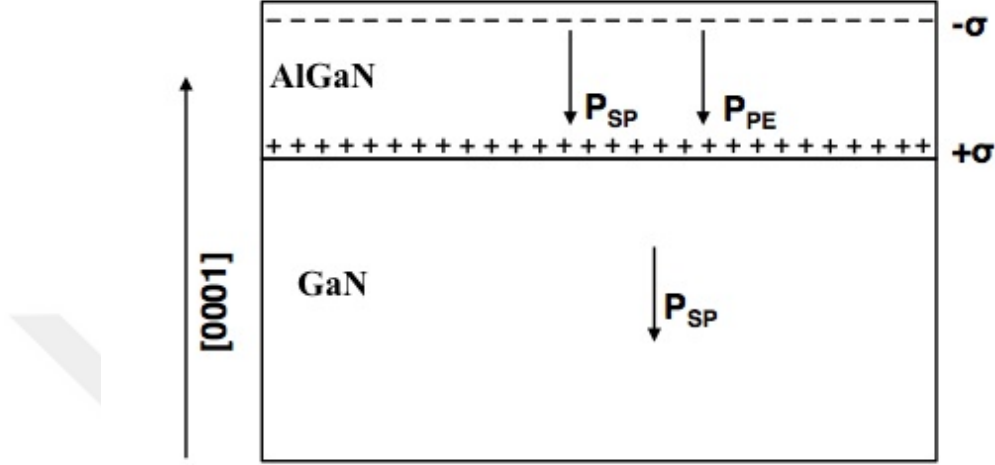


Figure 2.2: Polarization vectors and corresponding induced charge densities on AlGaN/GaN heterostructure [44]

critical thickness and can be calculated by [17]

$$t_{CR} = (E_D - \Delta E_C) \frac{\epsilon}{q\sigma_{PZ}} \quad (2.3)$$

where ϵ is relative AlGaN dielectric constant, ΔE_c is AlGaN/GaN conduction band offset, E_D is donor energy level and σ_{PZ} is polarization induced charge density. By increasing the thickness beyond t_{CR} , fermi level and donor state stays at same energy level but more electrons move to conduction band and become free electrons. Change in band diagram of AlGaN/GaN heterostructure before and after reaching critical thickness can be observed in Figure 2.3

These generated free electrons moves to the AlGaN/GaN interface, in order to compensate polarization induced positive charge during the cooling process after growth [40]. These electrons form a 2DEG at the AlGaN/GaN interface of the substrate and in an undoped sample, the carrier concentration can be calculated

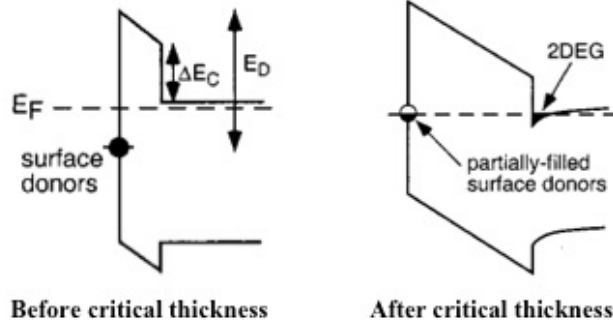


Figure 2.3: Band diagram of AlGaIn/GaN heterostructure before and after reaching t_{CR} [17]

by the equation [45]

$$n_s(x) = \frac{\sigma(x)}{e} - \frac{\epsilon_0 \epsilon(x)}{d_{AlGaIn} e^2} - [e\phi_b(x) + E_F(x) - \Delta E_c(x)], \quad (2.4)$$

where e is charge of an electron, d_{AlGaIn} is width of AlGaIn layer, $E_F(x)$ is fermi level with respect to GaN conduction band edge energy, ϵ_0 and $\epsilon(x)$ are vacuum permittivity and relative permittivity of AlGaIn and $e\phi_b(x)$ is Schottky barrier of gate contact on AlGaIn layer. After reaching t_{CR} value, n_s will increase rapidly at first but with more increase in t_{CR} , n_s will increase more slowly and it will saturate at a point when $t \gg t_{CR}$ [17]. Also, increasing the Al concentration in barrier layer will end up with an increase in n_s [40], due to the increased ΔE_c .

Electrons that form 2DEG are confined in a quantum well, which exists as a triangle below E_F at the AlGaIn/GaN interface, therefore, they have an enhanced mobility. The maximum mobility of the electrons in this 2DEG is limited by polar optical phonon scattering [40]. However there are other factors that can effect the mobility in these materials. First of all, high roughness at AlGaIn/GaN interface and gradient in alloy composition in the places that are close to the interface can cause a decrease in 2DEG mobility as they bring more scattering locations to the electrons [42]. Increasing the Al content more than 40% will end up with high density defects at the interface due to the high lattice mismatch [40]. In addition to this, presence of Ga and N-faces in same sample can also cause a decrease in

2DEG mobility [42].

2.2 Theoretical Information about HEMT Operation

Fabrication of a transistor on a AlGaIn/GaN (or AlN/GaN) heterostructure is a very convenient process. HEMT transistors consists of three terminals that are used to connect the device to the external circuits. Drain and source terminals are fabricated by deposition of metals as ohmic contacts. On the other hand, gate terminal, which is located between drain and source, is made by deposition of metals as Schottky contact. A 3D illustration of a simple AlN/GaN HEMT can be observed in Figure 2.4.

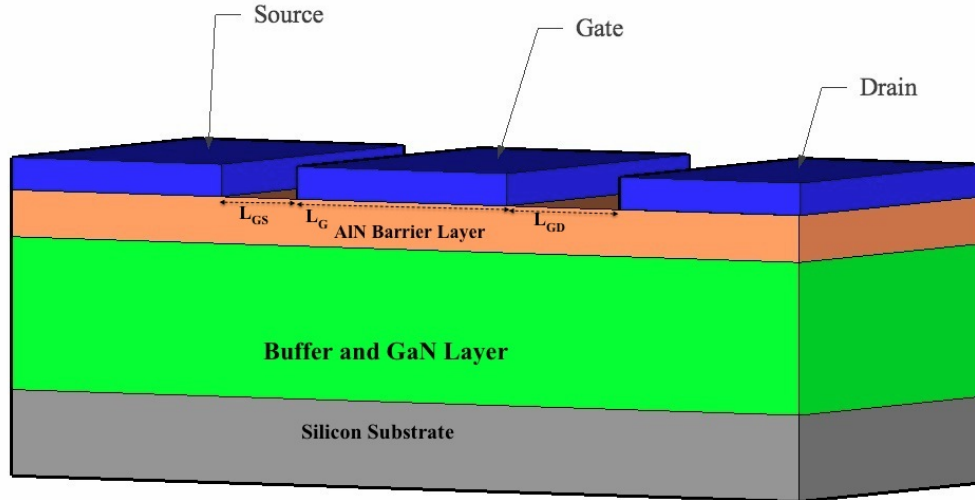


Figure 2.4: 3D illustration of AlN/GaN HEMT

On Figure 2.4, the horizontal distance L_G represents gate length, L_{GD} represents the distance between gate and drain and L_{GS} represents the distance between gate and source. By adjusting these distances, performance of transistors can be enhanced. First of all, it is always beneficial to pick these distances as short

as possible, in order to have more transistors on the same chip and effectively use the substrate area. On the other hand, an experiment made by Egawa revealed that an increase in L_{GD} ends up with an increase in breakdown voltage [26]. In that work, for samples with $L_G = 1.5\mu m$, an increase in breakdown voltage is observed till the saturation at $L_{GD} = 15\mu m$, with the increase in L_{GD} . In addition to these L_G has an effect on RF performance of the device. By decreasing L_G , it is possible to fabricate transistors that can operate at higher frequencies. In a comparative study, it is observed that unity gain frequency of devices jumps from 20GHz to 32GHz and maximum oscillation frequency of devices jumps from 22GHz to 27GHz when L_G is decreased from $0.7\mu m$ to $0.5\mu m$ [46]. However, it should be noted that due to the low aspect ratio between gate length and barrier layer thickness, decreasing the gate length alone will not be effective at some point [19]. Therefore, barrier layer thickness and gate length should be decreased at the same time.

Generally, these transistors are used in common source configuration. In this configuration source terminal is grounded, gate terminal is used as input terminal and drain terminal is used as output terminal. By applying a voltage at gate terminal, which is a Schottky contact, 2DEG region under gate area can be depleted by applying a negative bias or electron density can be increased by applying a positive bias, therefore 2DEG density can be modified. By this way, conductivity of the channel between ohmic source and drain contacts can be adjusted. This mechanism is similar to MOSFETs so they can be used to amplify a signal or as a switch in a circuit such as a MOSFET.

There is a direct proportionality between 2DEG density and drain current. So, the relationship between 2DEG density and drain current can be defined with the equation

$$I_D = qn_s v_{eff} W_G, \quad (2.5)$$

where q is electron charge, n_s is 2DEG electron density, v_{eff} is the effective velocity of the electrons in 2DEG channel and W_G is gate width.

Generally, HEMTs have a high electron density at their interface, even at zero bias at gate terminal. Therefore, these devices are normally on devices, or in other words, they are called as depletion mode transistors. In order to deplete the 2DEG channel at the interface, a negative bias should be applied to the gate terminal. After reaching some point, 2DEG channel is completely depleted, which means transistor is in off state. That voltage is called as threshold voltage, V_{th} . Therefore, in theory, for gate voltages that are smaller than V_{th} , drain current I_D is zero. For the case where gate voltage V_{GS} is greater than V_{th} , n_s starts to increase and a current starts to flow between source and drain. For $V_{GS} > V_{th}$, n_s can be defined with the equation [47]

$$n_s = \frac{\epsilon_{AlGaN}}{q(d_{AlGaN} + \Delta d)}(V_{GS} - V_{th}), \quad (2.6)$$

where d_{AlGaN} is the thickness of barrier layer and Δd is the effective distance of the 2DEG channel from the AlGaIn/GaN interface.

By applying a bias V_{DS} to the drain terminal, a current starts to flow between source and drain terminal, if $V_{GS} > V_{th}$. For the case $V_{DS} < V_{GS} - V_{th}$, drain current I_D increases linearly with increased V_{DS} , due to the increase in electron velocity with the increase in applied electric field. Therefore this region is called as linear region. On the other hand, when drain voltage is increased enough, so that $V_{DS} > V_{GS} - V_{th}$, drain current saturates at a point as velocity of electrons saturates at a point due to scattering with the semiconductor lattice [47]. This region of operation is called as saturation region. In theory, this current is independent of V_{DS} and has a constant value for constant V_{GS} . This constant value can be calculated with the formula

$$I_D = \frac{\epsilon_{AlGaN} v_{sat} W_G}{(d_{AlGaN} + \Delta d)}(V_{GS} - V_{th}), \quad (2.7)$$

where v_{sat} is the saturated electron velocity. As it can be noticed, I_D can be increased by increasing the V_{GS} value. This makes sense, as n_s can be increased by increasing V_{GS} . An example family of curves for I_D vs V_{DS} that shows linear

and saturation regions and relationship between I_D and V_{GS} can be observed in Figure 2.5 [48].

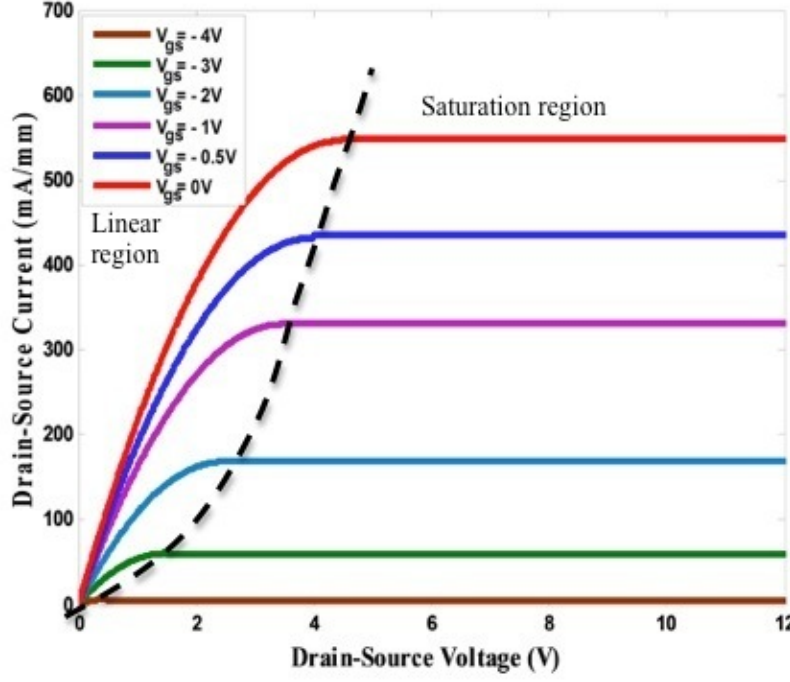


Figure 2.5: I_D vs V_{DS} graphs at different gate voltages [48]

Another important parameter for the transistors is the transconductance, g_m . It is a parameter that defines the effectiveness of the gate in modulating the drain current, and higher g_m means higher gate control on drain current. It can also be defined as instantaneous change in drain current with a change in gate voltage therefore it can be defined with the equation

$$g_m = \frac{\delta I_D}{\delta V_{GS}}. \quad (2.8)$$

In saturation region, by putting equation 2.7 into equation 2.8, g_m can be defined with the equation

$$g_m = \frac{\epsilon_{AlGaIn} v_{sat} W_G}{(d_{AlGaIn} + \Delta d)}. \quad (2.9)$$

As it is previously indicated in this chapter, most of the HEMTs are normally on devices. However, it is possible to fabricate normally off devices, which are called as enhancement mode(E-mode) devices by weakening the 2DEG under gate area. One way to do this is, recess etching of barrier layer under gate area. By this way, 2DEG density can be decreased, so that threshold voltage can be moved to a positive value [49,50]. Another method to fabricate E-mode HEMTs is fluorine ion doping of the gate area to move the threshold voltage to positive values. By fluorine doping of the gate area, conduction band of barrier layer is increased therefore, threshold voltage shifts to a positive value. [51, 52] As an example a D-mode HEMT with $V_{th} = -3.3V$ can be converted a E-mode HEMT with $V_{th} = 0.5V$ by fluorine doping method [51].

2.3 Background Information on Contact Materials

In this project, two types of contacts are used to fabrication of HEMTs. Ohmic contacts are used in source and drain areas, and a Schottky contact is formed as a gate contact. For source and drain contacts, ohmic contacts are preferred because resistivity of these contacts should be as low as possible, in order to avoid power losses at these contacts and have high drain current. On the other hand, a Schottky gate contact is preferred, because a rectifying contact with high resistance is required, therefore 2DEG density can be modified and gate leakage can be minimized to decrease power loss.

In this project, for ohmic contact formation Ti/Al/Ni/Au (20nm /60nm /40nm /50nm) metal stack is deposited and annealed at high temperatures. This is an optimized stack in order to have low contact resistances.

- Titanium is a metal with great adhesion and low work function. After annealing, it creates TiN, which has even lower work function. At this process, nitrogen atoms come from the barrier layer and leaves N-vacancies behind

them, which makes the area under the contact highly n-doped therefore, tunneling between semiconductor barrier layer and metal contact is enhanced [53,54]

- Aluminum is used to prevent oxidation of Ti by forming highly conductive Al_3Ti alloy. Also, by forming this alloy, the rate of aggressive Ti-GaN reaction is decreased, so that formation of voids at barrier layer is avoided [55]. In addition to this, it should be noted that Al/Ti ratio should be higher than 2.82, in order to have good ohmic contacts [56].
- Nickel is used as a diffusion barrier layer between Aluminum and Gold in order to prevent the formation an highly resistive alloy between these two metals, which is called as purple plague [56].
- Gold is used to prevent oxidation of underlying layers. It also improves the conductivity of ohmic contacts.

The defined metal stack with alloys formed after annealing is represented in Figure 2.6.

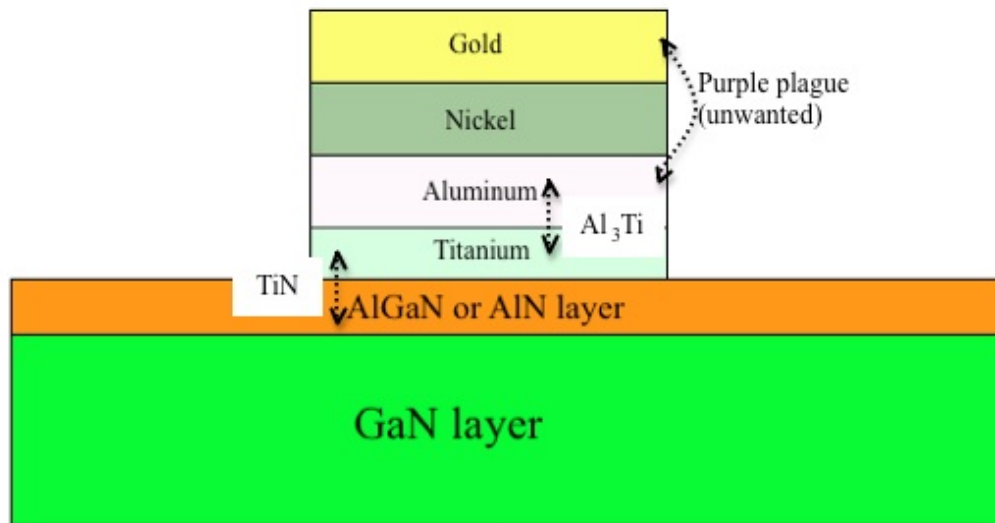


Figure 2.6: Ti/Al/Ni/Au metal stack with alloys formed after annealing

For formation of Schottky contacts, again, adhesion of the metal to the semiconductor surface is important as in ohmic contacts. However, this time, work function of the metal should be high, in order to minimize tunneling of electrons to the metal and leakage current. For this purpose, Nickel is picked to form Schottky contacts. Also, a Gold layer should be coated on top of Nickel, in order to prevent oxidation of this layer. Therefore, in this project, Ni/Au (20nm/100nm) metal stack is deposited as Schottky gate contact.



Chapter 3

Fabrication of AlN/GaN MIS-HEMTs

3.1 Introduction

This chapter will give information about the equipment that are used in this project, in order to fabricate HEMTs. Also, recipes that are used in these equipment will also be given. Finally, fabrication steps of HEMTs will be explained.

3.2 Mask Writing for Fabrication

For fabrication of small sized features, a mask is required, in order to transfer the small patterns on the substrate. For this purpose, L-edit software is used to design a mask that can be used in fabrication process of HEMTs. After design of the mask, mask file that is designed in L-Edit is converted into GDSII format and sent to a mask writer, which is an e-beam lithography system. Mask writer system is used to print these patterns on a chrome film, which is deposited on a quartz substrate with a square shape. In this thesis, fabrication of HEMTs

requires 3 mask levels. First mask level is for deposition of source and drain contacts, second mask level is for mesa isolation of transistors and third mask level is for deposition of gate contact. The screen shot of designed mask for this project can be seen in Figure 3.1.

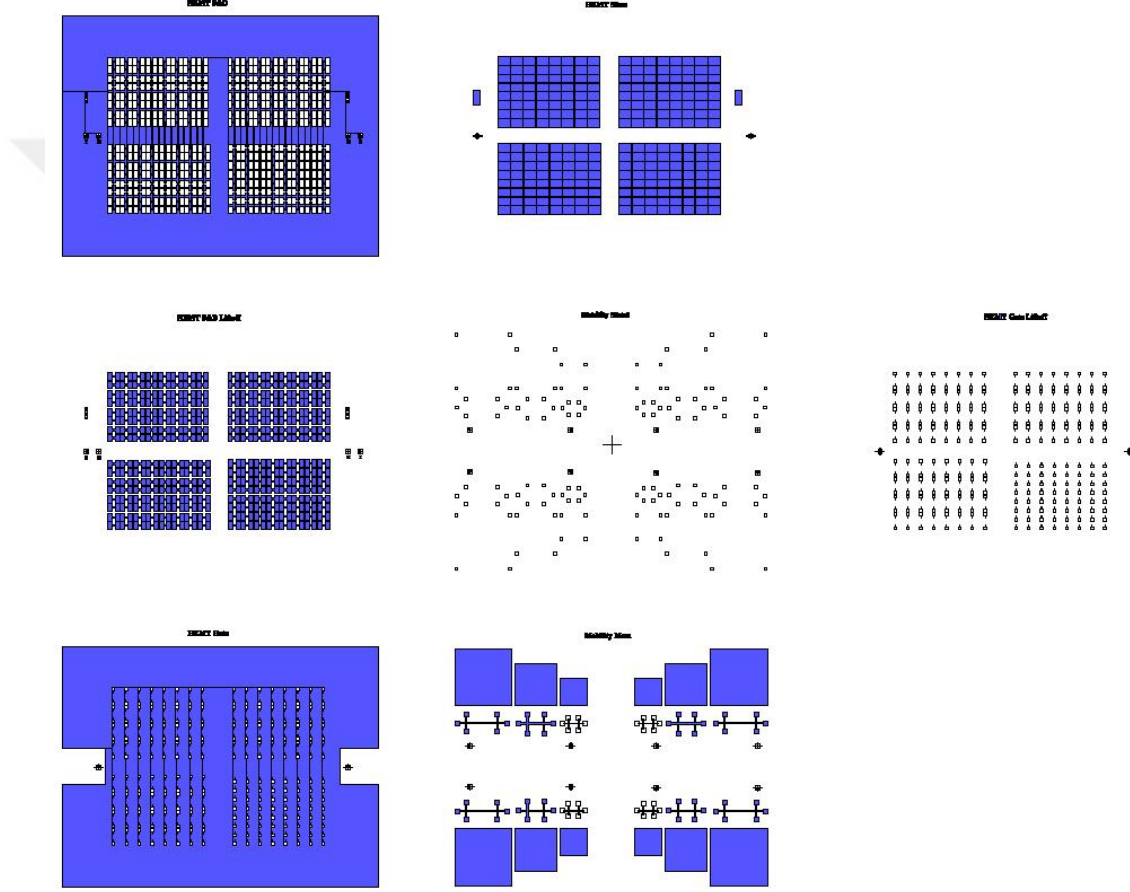


Figure 3.1: Screen shot of mask from L-Edit

On the mask shown in Figure 3.1, there are 7 sub-masks for different purposes. On the top row, from left to right, first mask is for deposition of source and drain contacts with positive lithography and second mask is for mesa isolation of transistors. On the row at the middle, from left to right, first mask is for deposition of source and drain contacts with negative lithography, second mask is for deposition of contacts for van der pauw structures with negative lithography and third mask is for deposition of gate metal with negative lithography. Finally, on the bottom row, from left to right, first mask is for deposition of gate metal with positive lithography and second mask is for mesa isolation of van der pauw

structures.

3.3 Sample Preparation

In this project, a 4-inch sample with configuration defined in Figure 1.2 with AlN barrier layer thickness of 6nm and SiN layer thickness of 6nm is used. In order to experiment different HEMT structures, this sample is diced into smaller samples with sizes $2.5cm \times 2cm$.

Before starting the fabrication of transistors, a sample cleaning process should be applied in order to remove the contaminants on the surface of samples. This is critical because small features are fabricated, therefore contaminants can effect device performance significantly. Also, contaminants can be harmful to the devices in cleanroom, so, samples should not be placed in the equipment before a cleaning step.

The SiN layer on top can be used as a protection layer for thin AlN layer during the process, therefore a standard wafer cleaning can be applied to the samples. For sample cleaning, first, samples are placed in a glass beaker that is filled with acetone and this beaker is placed in a sonicator for 4 minutes. Then, this step is repeated with isopropanol to remove acetone and finally, samples are rinsed with DI water to remove isopropanol and dried with Nitrogen blow. By this process, any organic contaminants on the surface can be removed. Also, after cleaning, samples are placed on a hot plate, which is at $110^{\circ}C$, for at least 5 minutes, in order to evaporate remaining water after rinsing and drying.

3.4 Optical Lithography

In fabrication process of micro or nano structures, lithography is the key step, as it is used to transfer small patterns on the samples. There are two types of lithography, which are optical lithography and e-beam lithography. In optical lithography, the patterns on a mask plate is transferred on a photoresist, which is a light sensitive material that is coated on top of the sample. On the mask, some parts are coated with Chrome to block the incoming light and some parts are just bare glass, which lets the light pass to that part of photoresist. By this way, patterns are transferred on the substrate. Optical lithography is a simple and cheap process, however, it can be problematic for the features that are smaller than $1\mu m$. On the other hand, in e-beam lithography, mask is not required and patterns can directly be written on the sample. E-beam lithography is an expensive and slow process, but it is used especially for fabrication of sub-micron features. In this project, optical lithography is used for patterning.

There are two types of photoresists that are used for optical lithography, which are positive photoresist and negative photoresist. In order to develop the patterns on photoresist, sample is placed in a developer solution. According to the type of the photoresist, some part of the resist is removed in the developer, therefore patterns are formed on the sample. For positive photoresists, light exposed areas are removed in developer solution, therefore Chrome parts of the mask is the remaining photoresist on the sample. On the other hand, for negative photoresists, light exposed areas are not soluble in developer solution. In this case, patterns in Chrome part of the mask is removed from the resist.

In this project, AZ5214E image reversal photoresist is used. This is a special type of photoresist, which can be used as both positive and negative photoresist, by following different processes. In order to use AZ5214E as a positive photoresist, sample is baked in a hotplate after resist coating, then it is exposed with UV-light and finally, put into the developer solution. If another baking process is applied to the sample after exposure, which is called as reversal bake, and then sample is exposed with UV-light again, AZ5214E behaves as a negative photoresist. The

behaviour of AZ5214E with different processes can also be seen in Figure 3.2 [57].

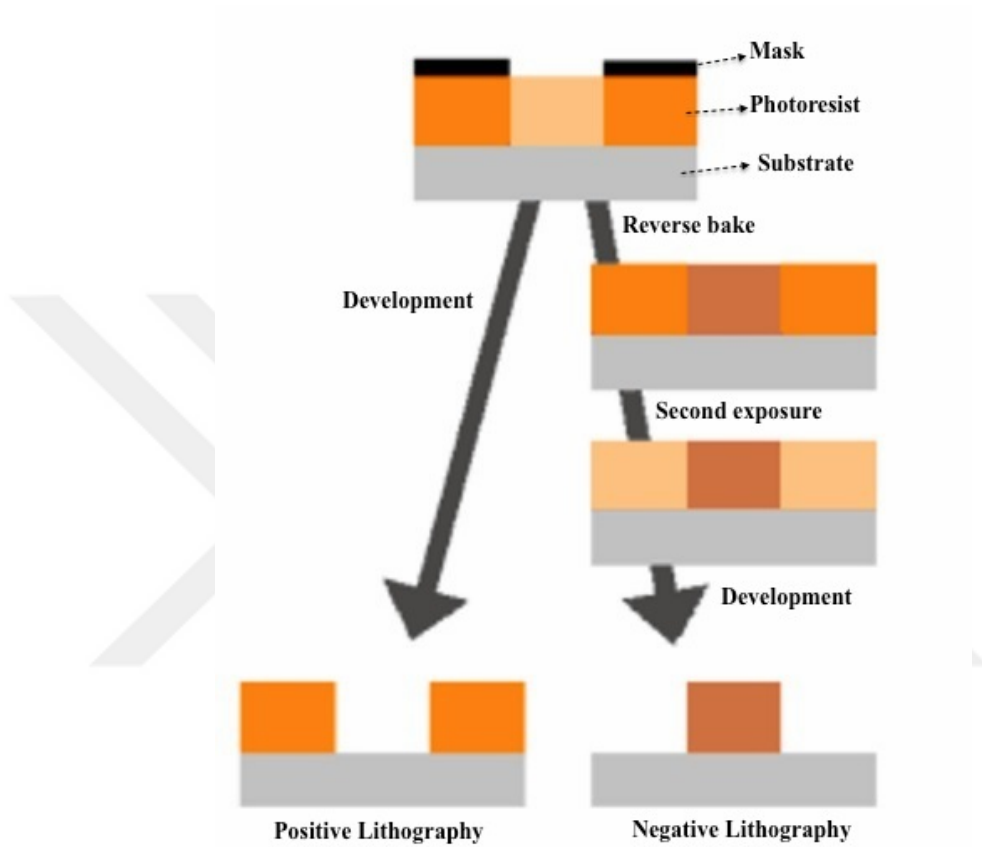


Figure 3.2: AZ5214E as positive and negative photoresist[57]

In a fabrication process, which requires multiple mask stages, alignment marks should be put in each mask level. Mask aligners are useful tools in the processes that require multiple lithography steps, as they are used to place the features that are fabricated in different mask levels in correct places. In different mask levels, different alignment marks with the geometries matching with each other is used. An example of mask aligners that are used in this project can be observed in Figure 3.3.

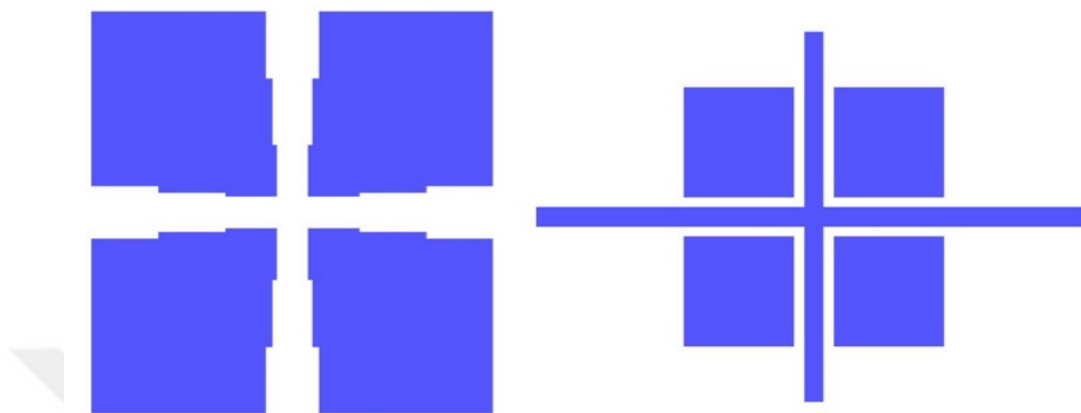


Figure 3.3: Examples for alignment marks used in this project

The mask aligner on the left in Figure 3.3 is placed on the first mask level and the mask aligner on the right is placed on other mask steps. By adjusting the cross that is in the middle of the mask aligner on the right to the space in the middle of the mask aligner on the left, features on different mask levels can be successfully placed on correct locations. In this project, for mask alignment and UV illumination of samples, EVG 620 Mask Aligner is used, which can be observed in Figure 3.4.

In this project, the steps that are followed for lithography is explained below:

- Sample is cleaned as in sample preparation section
- The adhesion layer, hexamethyldisilazane (HMDS) is coated on the sample with spin coating technique. In this technique, material in liquid form is dropped on the sample with a pipette, and then sample is rotated by a spin coater. In this step, HMDS is spin coated at 4000rpm for 50 seconds.
- AZ5214E image reversal photoresist is spin coated at 4000rpm for 50 seconds. The thickness of the photoresist at the end of this process is $1.4\mu m$.
- As a prebake step, sample is baked on hotplate at $110^{\circ}C$ for 50 seconds.

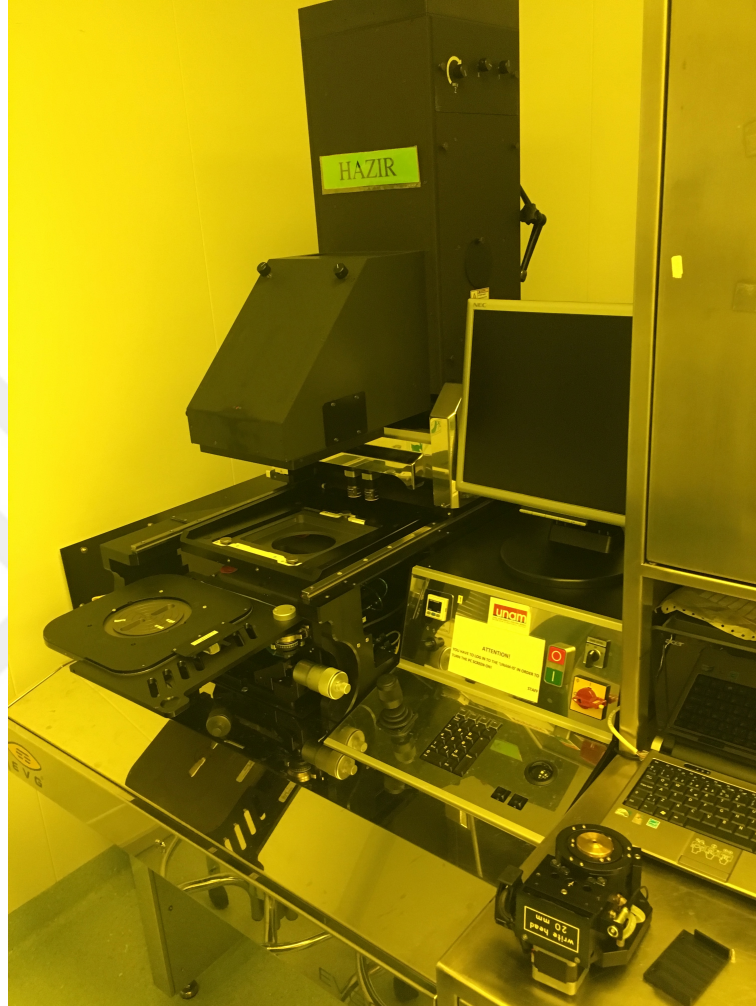


Figure 3.4: EVG 620 Mask Aligner System

After this step, different processes should be followed, in order to use AZ5214E as positive or negative photoresist. To use AZ5214E as positive photoresist, following steps should be performed:

- $40mJ/cm^2$ UV light exposure is applied on the photoresist with mask aligner system. Also, an alignment between mask and sample is performed if necessary.
- Photoresist is developed by AZ400K developer solution with water with a ratio of $AZ400K : H_2O(1 : 4)$ until all the photoresist at the exposed area is removed.

On the other hand, for using AZ5214E as negative photoresist, following steps should be performed:

- $20mJ/cm^2$ UV light exposure is applied on the photoresist with mask aligner system. Also, an alignment between mask and sample is performed if necessary.
- As a reversal bake step, sample is baked on hotplate at 120°C for 2 minutes.
- $75mJ/cm^2$ UV light exposure is applied on the photoresist with mask aligner system. This time, an empty mask is placed to the mask aligner system, therefore the whole sample surface is exposed by UV light.
- Photoresist is developed by AZ400K developer solution with water with a ratio of $AZ400K : H_2O(1 : 4)$ until all the photoresist at the unexposed area in the first UV exposure is removed.

After both positive and negative lithography, samples are placed on Asher system to remove the residue photoresist in developed area. In this step, samples are kept in a plasma, which is formed by 30sccm Oxygen and 5sccm Nitrogen flow under 300W RF power for 30 seconds.

3.5 Metal Deposition

Metal deposition on substrates in fabrication of micro or nano sized features is generally handled with Physical Vapor Deposition(PVD) techniques. In PVD techniques, the target material is heated so that a vapor of that material is formed. Then, this vapor goes up and when it reaches to the substrate, which is placed at the top of the system, it solidifies again due to the low temperature at the surface of the sample. Also, it should be noted that these techniques is performed under high vacuum conditions, in order to avoid contamination or oxidation of coated metals. In this project, Thermal Evaporation and E-beam

Evaporation is used for metal deposition. In Thermal Evaporator system, target material is placed on a metallic boat, and by heating the boat resistively, target can be evaporated. On the other hand, in E-beam evaporation, target material is placed in a crucible and an electron bombardment is applied to it for evaporation. Also, in both techniques, sample should be rotated for obtaining more uniform films. Pictures of thermal evaporator and e-beam evaporator used can be seen in Figure 3.5.



Figure 3.5: Pictures of E-beam evaporator(left) and Thermal evaporator(right)

In this thesis, these two PVD systems are used for deposition of Ti/Al/Ni/Au (20nm/ 60nm/ 40nm/ 50nm) metal stack for source and drain ohmic contacts and Ni/Au (20nm/ 100nm) Schottky gate contact. For deposition of Titanium, Nickel and Gold, E-beam evaporator is used and for deposition of Aluminum, Thermal evaporator is used. Parameters that are used during the deposition of these materials can be observed in Table 3.1.

Material	Density(g/cm^3)	Acoustic Impedance	PVD System
Titanium	4.5	14.06	E-beam
Aluminum	2.7	8.17	Thermal
Nickel	8.91	26.68	E-beam
Gold	19.3	23.18	E-beam

Table 3.1: Parameters used in metal deposition

3.6 Lift-off

Lift-off technique is a common method in nanofabrication that is used to deposit patterned films on substrates. In this technique, first, a photoresist layer is coated as sacrificial layer and patterns are developed on top of this layer. After the development, the remaining resist should just be left on the areas that are not supposed to be coated with desired material. Then, material is coated on top of this sacrificial layer. The process up to this step is defined in Sections 3.4 and 3.5 of this thesis.

After metal deposition, sample is put into acetone. Acetone can remove the photoresist with the unwanted metal on top of it, therefore, metal only remains in desired areas and patterns can successfully transferred on the sample. This process can also be observed in Figure 3.6.

3.7 Annealing

Annealing is a necessary step to fabricate ohmic contacts on GaN substrate. Especially for annealing temperatures above 600 °C, a significant decrease in resistance of Titanium based contacts on GaN substrates is observed [58]. At high temperatures, Ti reacts with GaN and forms, highly conductive alloy TiN. As a result of this reaction, N-vacancies forms in GaN, which makes that area highly n-doped GaN [59]. In this project, for ohmic contact formation of HEMTs, an annealing treatment at 850 °C under N_2 environment is applied for 30 seconds.

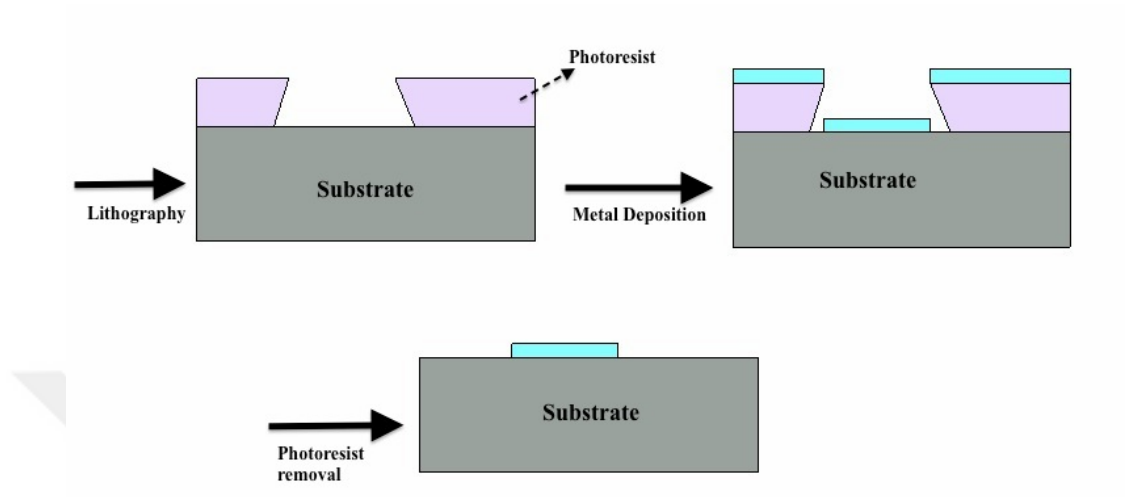


Figure 3.6: Lift-off process

Also, effects of annealing temperature on ohmic contact resistance is observed under three different annealing temperatures, which is explained in detail in Section 4. Rapid Thermal Annealing system used in this project can be seen in Figure 3.7.



Figure 3.7: Rapid thermal annealing system

3.8 Dry Etching

Inductively Coupled Plasma (ICP) is a dry etching system, which is a combination of physical and chemical etching. In this dry etching technique, etchant gases are energized with plasma created by RF power under low pressure, and energized ions are sent to the surface, where they will react with atoms on the surface and remove them from there. ICP etching is a low damage process with high anisotropy, which makes it a good choice for etching in fabrication of HEMTs.

In this project, two ICP systems are used for etching. STS-615 ICP system is used for application of Fluorine based etch recipes and STS-616 ICP system is used for application of Chlorine based etch recipes. Picture of these two systems can be observed in Figure 3.8.



Figure 3.8: STS-615(left) and STS-616(right) ICP systems

The samples used in this project, which can be observed in Figure 1.2, have a thin SiN cap layer on top. Before the deposition of ohmic contacts for source and drain, SiN layer at these areas should be removed for better contacts, as SiN is an insulator material.

In order to remove this SiN at source and drain areas, a Fluorine based ICP recipe is developed and experimented. The following parameters are used in this experiment, which are taken from elsewhere, and modified for use [60]:

- **Gases used:** CF_4/O_2 (1sccm/4sccm)
- **Power:** 20W
- **Pressure:** 2mTorr

- **Temperature:** 18.5 °C

To observe the effects of this recipe on the sample, first, interdigitated finger patterns are printed on sample with optical lithography. The process defined in Section 3.4 is used for this purpose. Then, the sample is treated with this recipe for 20 seconds. Finally, photoresist on top is removed by putting the sample in acetone. The SEM picture of resultant structure can be seen in Figure 3.9.

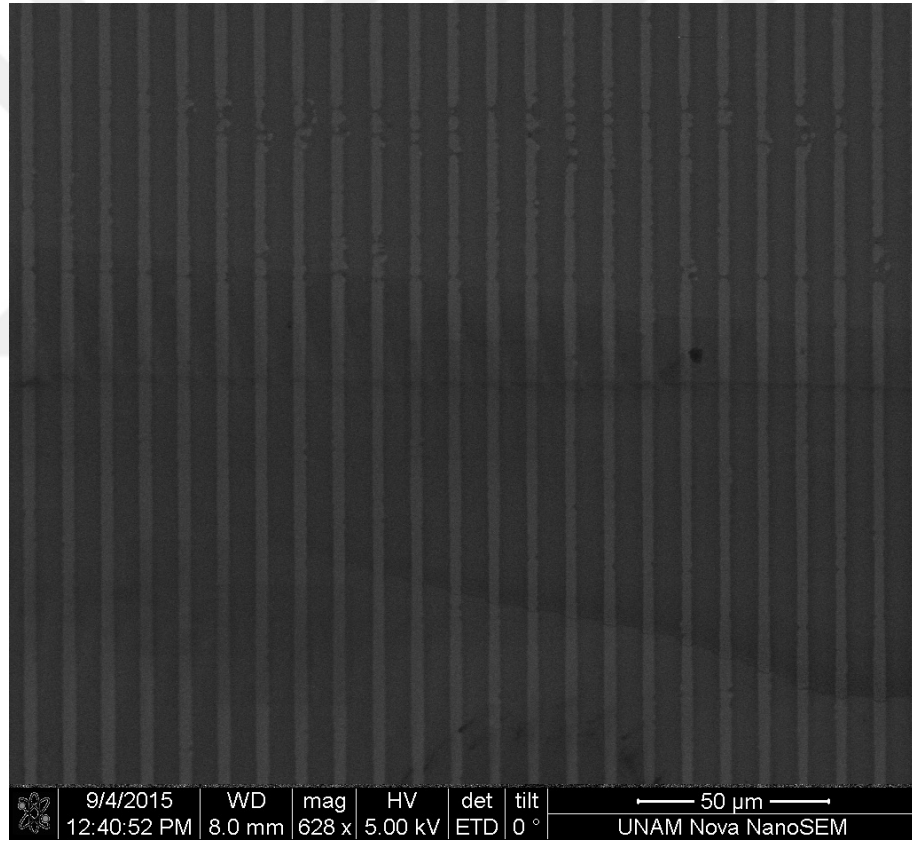


Figure 3.9: SEM picture of surface after CF_4/O_2 ICP treatment

This etching treatment is used for just removal of 6nm thick SiN layer, therefore, an advanced characterization of the surface should be performed to observe the etch depth. For this purpose, surface of the sample is characterized by using Atomic Force Microscopy (AFM) system. The AFM result after ICP treatment can be observed in Figure 3.10.a. An etch depth around 9nm is obtained from AFM results, which is a close value to SiN layer thickness. Then, in order to observe the selectivity of the recipe between AlN and SiN, a blank etch of the

same sample for 1 minutes is performed. AFM result of that experiment can be seen in Figure 3.10.b. This time a smoother surface is observed and as the finger-like structures on the surface is disappeared, it is possible to say that this recipe has a high selectivity between AlN and SiN.

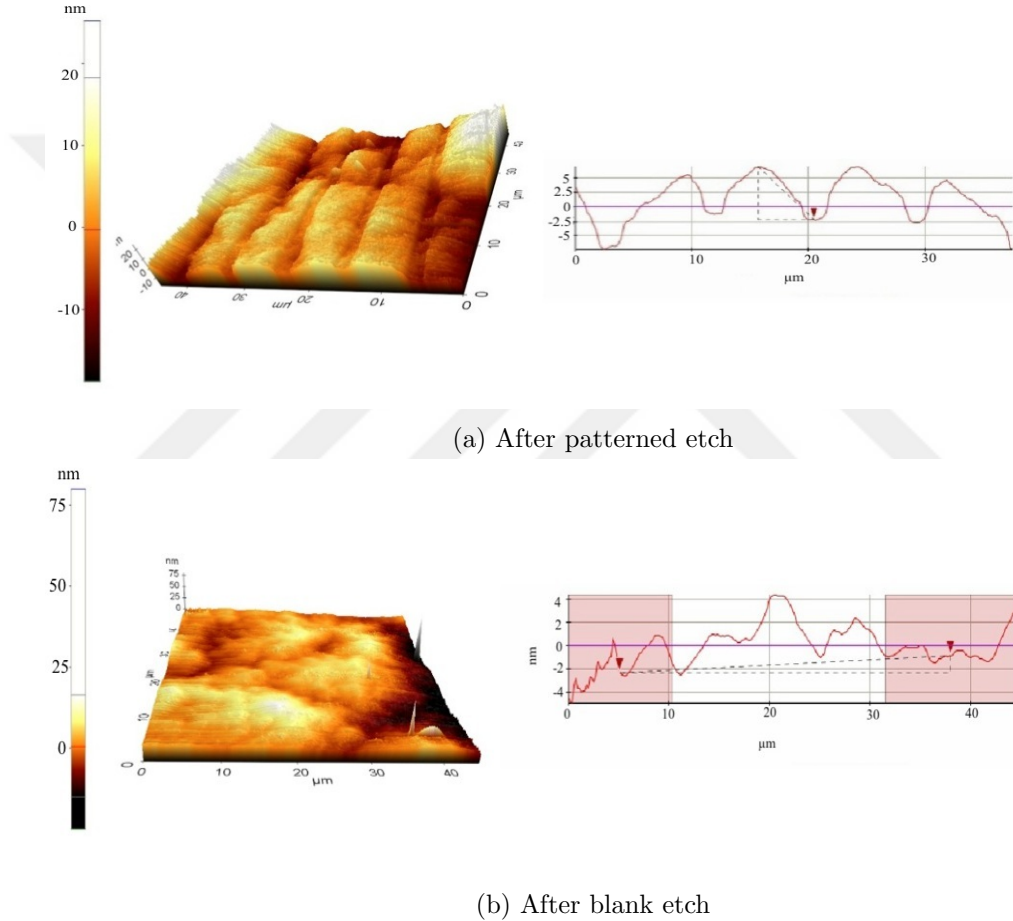


Figure 3.10: AFM images for CF_4/O_2 etch recipe

In order to verify this selectivity and existence of AlN after CF_4/O_2 ICP treatment, XPS measurements are taken for samples with no treatment, 20 seconds treatment and 1 minute treatment. The results of this measurement can be observed in Figure 3.11.

From the XPS results, it is observed that Si2s and Si2p peaks in not etched sample are disappeared for 20 seconds etched sample, therefore, it is verified that SiN layer is completely removed after 20 seconds CF_4/O_2 treatment. Also, Al2p

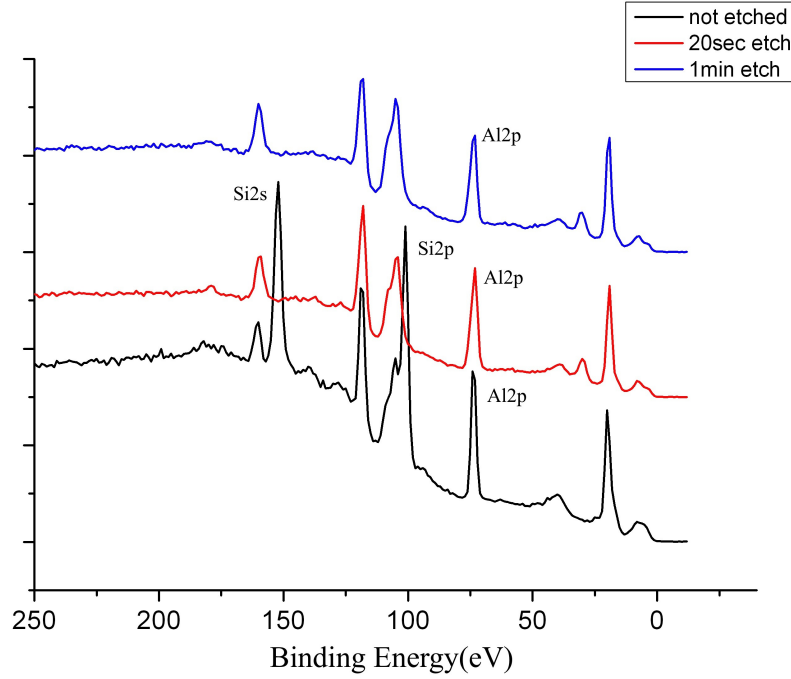


Figure 3.11: XPS results for CF_4/O_2 recipe

peak can be observed for both 20 seconds and 1 minute etched samples, and atomic composition of Aluminum is close for these two samples(%34.06 for 20 sec etch and %30.86 for 1min etch). This result also verifies the high selectivity of this etch recipe between SiN and AlN.

Another etch recipe is needed to isolate individual transistors from each other. In order to isolate individual transistors from each other, an etch depth around at least 150nm is needed for the areas between transistors. To accomplish such an etch depth, a Chlorine based etch recipe is optimized in this project, which is taken from another work [61]. Again, interdigitated finger patterns are printed on sample with optical lithography prior to the ICP treatment. Also, it should be noted that, due to the damage in photoresist, Acetone was not enough to remove the photoresist after etching and an oxygen plasma treatment with 99sccm and 400W RF power should be applied for 15 minutes, in order to remove the resist completely. This time, etching process with different parameters are tried, in order to decide the optimum parameters for this process. Stylus profilometer is

used to measure etch depth of each recipe, as recipes with high etch rates are tried. The result of these experiments can be observed in Table 3.2. Note that temperature is 20 °C for all of these recipes.

<i>Ar/Cl₂</i> flow	RF power	ICP power	Pressure	Etch rate
20/60 sccm	600W	250W	5mTorr	738.2nm/min
10/60 sccm	600W	250W	5mTorr	697.8nm/min
5/20 sccm	600W	250W	10mTorr	590.1nm/min
5/20sccm	300W	150W	10mTorr	290.1nm/min

Table 3.2: *Ar/Cl₂* ICP etch recipe parameters

In the HEMT fabrication process, the recipe with parameters *Ar/Cl₂* (5sccm /20sccm), 600W RF power, 250W ICP power and pressure of 10mTorr with an etch rate of 290.1nm is used.

3.9 Atomic Layer Deposition

Atomic Layer Deposition (ALD) can be considered as an improved CVD technique, which can be used for deposition of ultra-thin films. As in other CVD techniques, ALD is based on sending reactant gases on a reaction chamber, where these materials react with each other and solidifies on the substrate. However, unlike other CVD techniques, these reactants are sent alternatively to the reaction chamber and the pulses of reactants are separated by purge steps. This mechanism provides an advantage of self-limiting growth, as it is possible to deposit only one layer in a cycle. [62] By using ALD, one can deposit very thin films with excellent conformality. One cycle of an ALD process includes the following steps:

1. Exposure of the first precursor
2. Purge step, which includes the removal of precursor from the chamber
3. Exposure of the second precursor

4. Another purge step to remove the precursor

Such an ALD cycle can also be observed in Figure 3.12 [63].

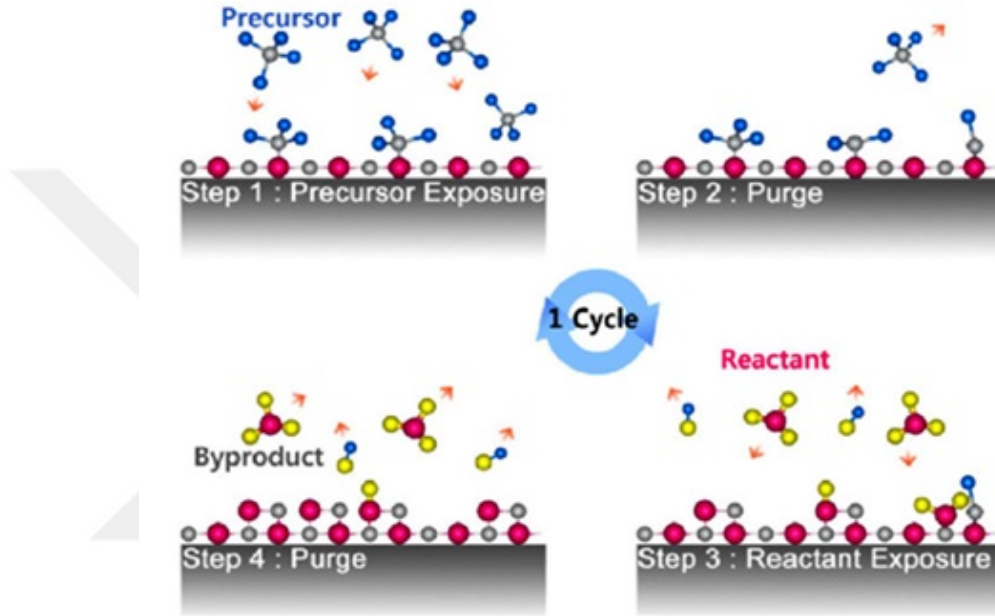


Figure 3.12: 1 cycle of an ALD process [63]

In this project, ALD is required to deposit thin dielectrics as gate dielectric layer. For this purpose, 4nm of Al_2O_3 is deposited by ALD Savannah 100 system, which can be observed in Figure 3.13.

The precursors used for deposition of alumina(Al_2O_3) are trimethylaluminum ($Al(CH_3)_3$) and water(H_2O). First, $Al(CH_3)_3$ is sent as first precursor and it is held by the surface till there is no point left without it. This can be realized due to the hydroxyl group(OH^-) that already exists on the surface, which reacts with $Al(CH_3)_3$ to hold it on surface and exposes methane gas(CH_4) as a result of this reactant. Then excess $Al(CH_3)_3$ and CH_4 is removed in purge step. After that, H_2O is sent as second precursor, which reacts with $Al(CH_3)_3$ to form Al_2O_3 . CH_4 is also produced during this reaction, which is taken out during the purge step. This mechanism provides an ultimate control on deposition thickness as there is a linear relationship between number of cycles performed and film thickness.



Figure 3.13: ALD Savannah 100 system

3.10 Fabrication Steps

In this section, fabrication steps of HEMTs will be explained. Fabrication of standard MIS-HEMTs include three steps. First step is deposition of source and drain ohmic contacts, second step is device isolation with mesa etching and third step is deposition of Schottky gate contact.

Source and drain ohmic contacts are deposited by the following steps:

1. Sample cleaning is done as defined in Section 3.3.

2. Negative lithography is done as defined in Section 3.4, for defining source and drain areas.
3. SiN at source and gate area is etched with CF_4/O_2 recipe.
4. AlN is a material that can easily form a native oxide on top of it. It is not possible to form ohmic contacts, if this native oxide is not removed. For this purpose, $Ar/Cl_2(5/20\text{sccm})$ with 300W RF power and 150W ICP power etch recipe is used for 15 seconds to remove this native oxide layer.
5. Ti/Al/Ni/Au (20/60/40/50nm) metal stack is deposited. First, 20nm Titanium is deposited by e-beam evaporator. Then, 60nm Aluminum is deposited by thermal evaporator. Finally, Ni/Au (40/50nm) is deposited with e-beam evaporator.
6. Sample is put into acetone for lift-off
7. Contact annealing at 850 °C is performed for 30 seconds under N_2 by RTA.

Summary of this process can also be observed in Figure 3.14.

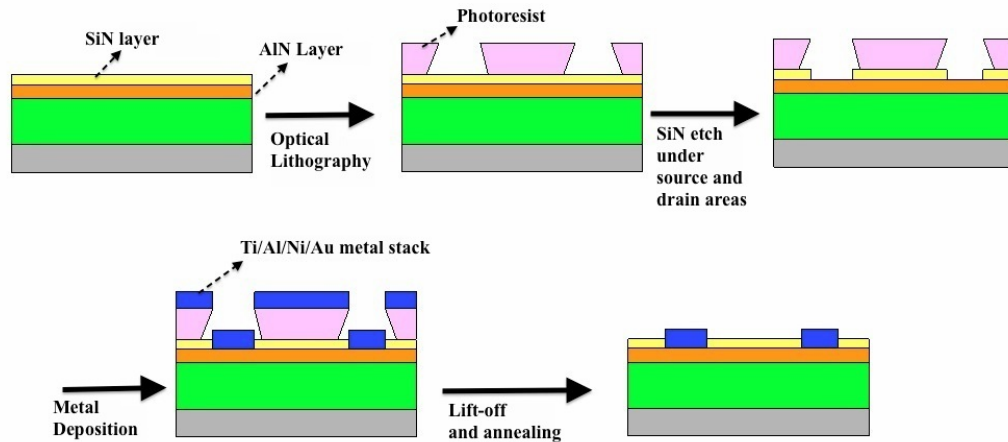


Figure 3.14: Steps of ohmic metallization steps

After deposition of source and drain contacts, mesa etching is performed for device isolation with following steps:

1. Positive lithography is done as defined in Section 3.4, for defining mesa etch area
2. $Ar/Cl_2(5/20\text{sccm})$ with 300W RF power and 150W ICP power etch recipe is used for 1 minute for device isolation. It has a rate of 290.1nm/min, therefore this treatment is enough for device isolation.
3. After ICP treatment, photoresist is damaged, therefore putting the sample in Acetone will not be enough to remove the photoresist. To remove the resist, sample is put in oxygen plasma with flow of 99sccm and 400W RF power for 15 minutes.

Summary of this process can also be seen in Figure 3.15.

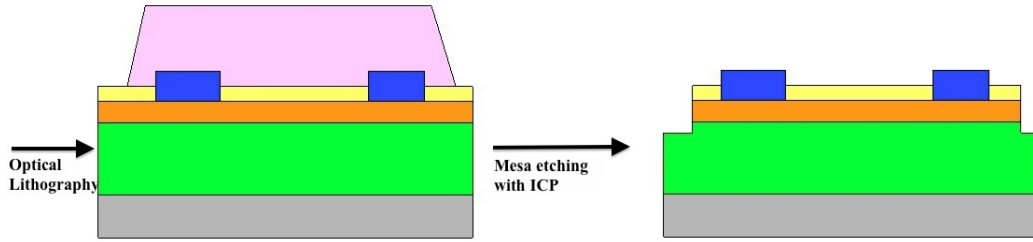


Figure 3.15: Mesa etching process

After mesa etching step, Schottky gate contact is deposited with following steps:

1. Positive lithography is done as defined in Section 3.4, for defining gate contact area. Generally, negative lithography is preferred in lift-off processes. However, defining gates with $L_G = 2\mu\text{m}$ is very hard by using AZ5214E as a negative photoresist. Therefore, positive lithography is preferred in this step.
2. Ni/Au(20/100nm) metal stack is deposited with e-beam evaporator.
3. Sample is put into Acetone for lift-off.

Summary of this process can also be seen in Figure 3.16.

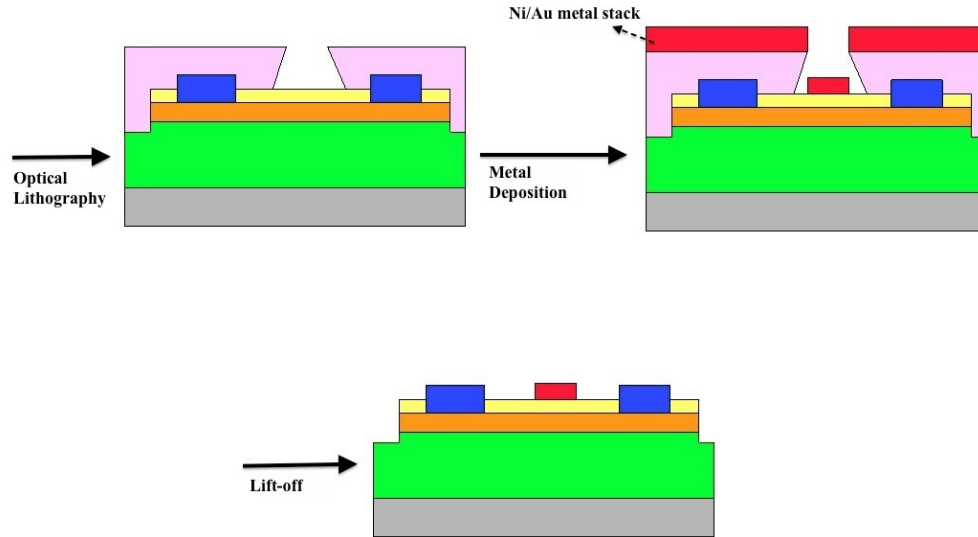


Figure 3.16: Deposition of gate metal

Also, it should be noted that, a dielectric layer is deposited with ALD in gate metallization step after defining contact areas with optical lithography and before deposition of Schottky metal contact for the samples with extra ALD deposited gate dielectric.

Chapter 4

Ohmic Contact Formation

4.1 Introduction

This chapter will explain the formation of ohmic contacts on AlN/GaN heterostructure. Formation of ohmic contacts on AlN is a challenging process, therefore, some experiments are made to obtain better ohmic contacts on AlN/GaN heterostructure. Also, methods used in this section to measure contact and film characteristics are explained in this chapter.

4.2 Transmission Line Method

Transmission Line Method(TLM) is a characterization method that is used to measure specific contact resistivity (ρ_c) (or contact resistance, R_c) and semiconductor sheet resistance. It is first proposed by Shockley [64], and then developed by Reeves and Harrison [65]. The model used in this measurement can be observed in Figure 4.1.

As in Figure 4.1, TLM structure consists of contact pads with width W , where the distance between these contact pads increases such as $L_1, L_2, L_3 \dots$ as in the

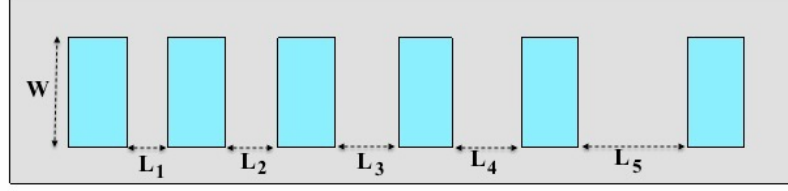


Figure 4.1: TLM structure

Figure.

This method includes the measurement of the resistance between each consecutive contacts by taking I-V curves, where the measured resistance between contacts are defined as R_T . As R_T is the total measured resistance, it should be sum of the resistance of two contacts and the resistance of the semiconductor film between the contacts. Therefore, R_T can be defined by the equation

$$R_T = 2R_C + \frac{R_{SH}L}{W}, \quad (4.1)$$

where L is the distance between contacts and R_{SH} is the semiconductor sheet resistance between contacts [65]. Also, it is possible to define contact resistance by the equation

$$R_C = \frac{R_{SK}L_T}{W}, \quad (4.2)$$

where R_{SK} is the sheet resistance under contact and L_T is the transfer length, the length that an electron can travel beneath the contact before it returns to the contact [66].

After obtaining R_T for each individual contact pad pair, the graph R_T vs distance between contact pads is drawn to obtain contact resistance R_C and semiconductor sheet resistance between contacts R_{SH} . An example of linear fit

of such a graph can be observed in Figure 4.2 [65]

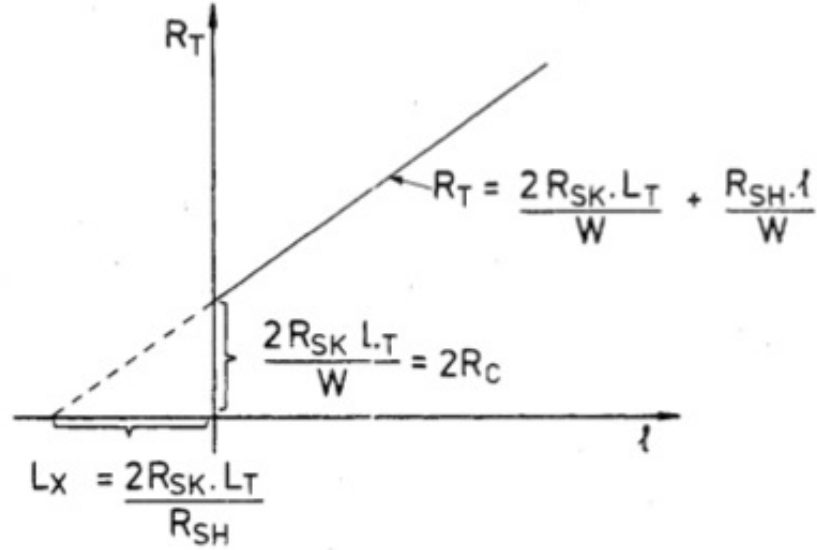


Figure 4.2: An example for R_T vs distance graph[65]

From this graph, y-intercept of the graph gives $2R_C$ value as it indicates the value at the distance between two contact pads is zero or in other words, $l = 0$. By dividing the y-intercept by two and multiplying it with the width of contact pad W , normalized contact resistance can be obtained with the unit of $\Omega.mm$. Also, slope of the graph gives R_{SH}/W value, which can be observed from Figure 4.2 or equation 4.1. Therefore, multiplication of the slope with contact pad width W will give the R_{SH} value with the unit of $\Omega/\square$.

4.3 Electrical Characterization of Ohmic Contacts

To characterize ohmic contacts on AlN/GaN heterostructure, TLM structures with contact length of $100\mu m$ and contact width of $200\mu m$ are fabricated. Distances between contact pads are defined as 2, 3, 5, 10, 20 and $50\mu m$ on the mask, but actual distances are also measured by SEM.

For fabrication of TLM structures, first, contact areas are defined with optical lithography with negative photoresist as defined in Section 3.4. Then, SiN at contact areas are etched with CF_4/O_2 ICP recipe, which is defined in Section 3.8. Finally Ti/Al/Ni/Au (20/60/40/50nm) metal stack is deposited as defined in section 3.5 and contacts are formed by a lift-off step by putting the samples in acetone. Also, the contacts are annealed at 800 °C. SEM image of resultant TLM structures can be observed in Figure 4.3.

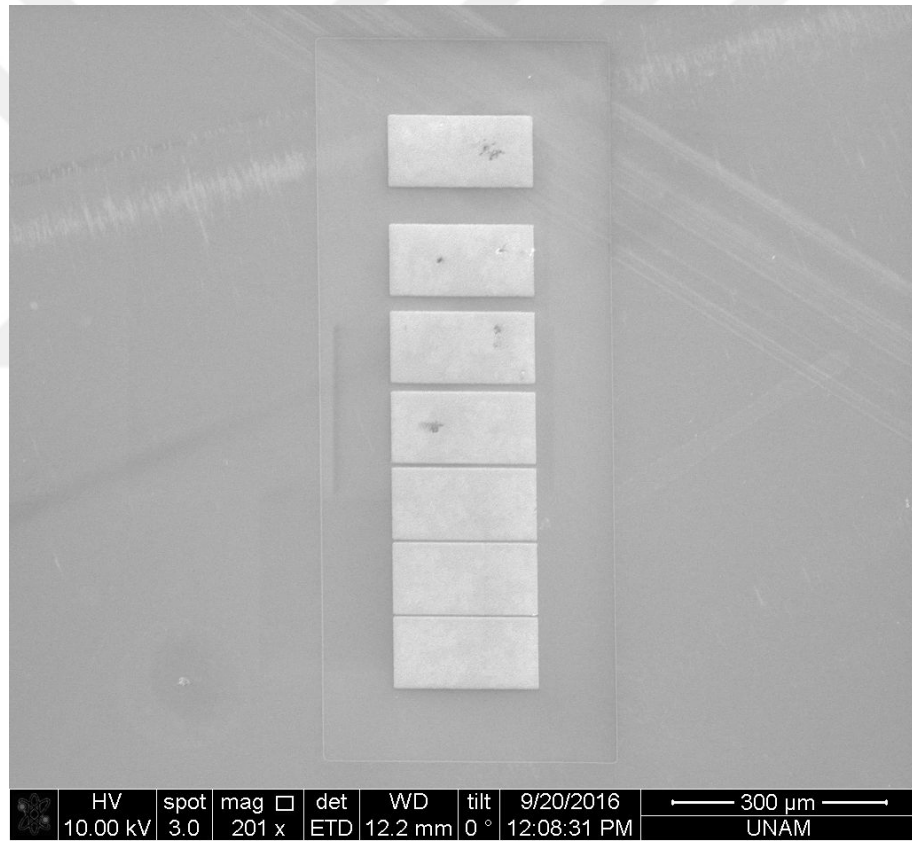


Figure 4.3: SEM image of TLM structures

Keithley 4200 Semiconductor Parameter Analyser is used to obtain the current vs voltage (I-V) characteristics of contacts and the result of this measurement can be observed in Figure 4.4.

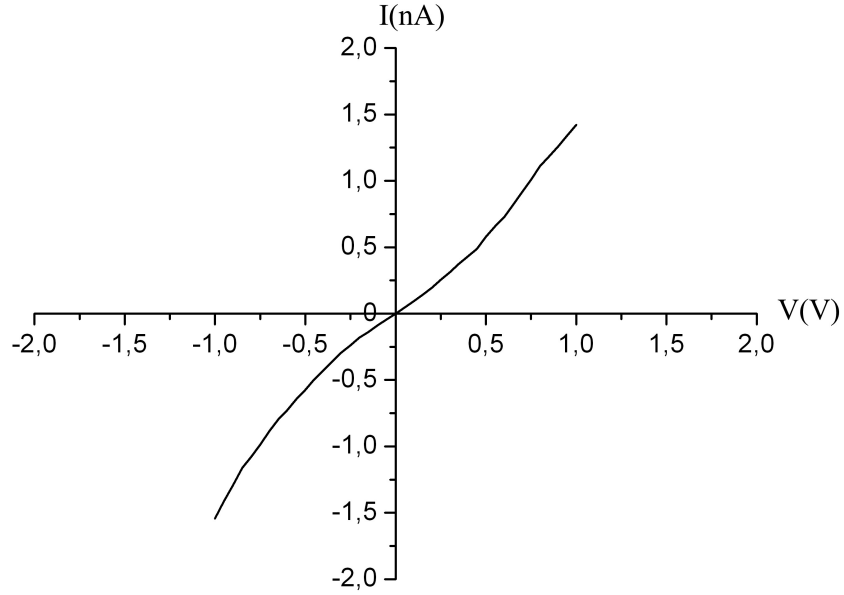
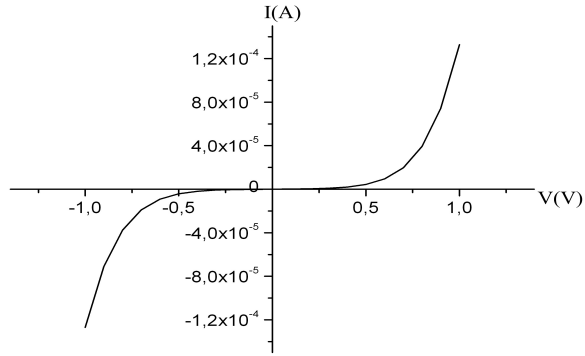


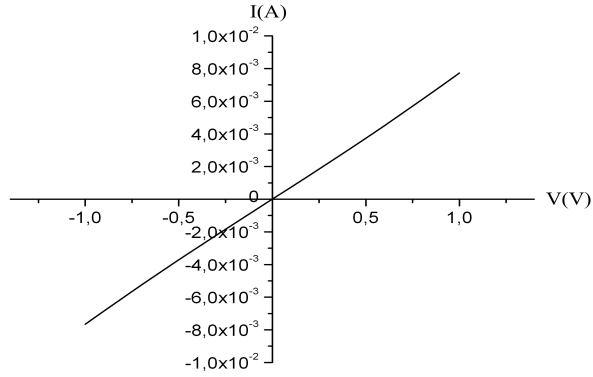
Figure 4.4: Current vs voltage graph for the sample without native oxide removal

The contacts obtained after this process had a very high contact resistance. The reason for this is the native oxide of AlN on the surface of sample, which is an insulator material. Therefore, this native oxide layer should be removed before deposition of metal stack. For this purpose, Ar/Cl_2 ICP etch recipe, which is defined in Section 3.8 is used for 15 seconds. After this shallow etching, ohmic contact behaviour is observed for the contacts. I-V results before and after annealing of contacts can be observed in Figure 4.5. Note that this time, annealing temperature was 850°C .

It can be seen from Figure 4.5 that, contact show a rectifying behaviour before annealing and show a linear behaviour after annealing, which indicates the ohmic behaviour after annealing.



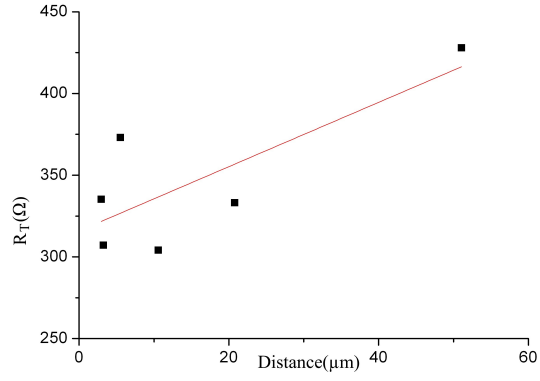
(a)



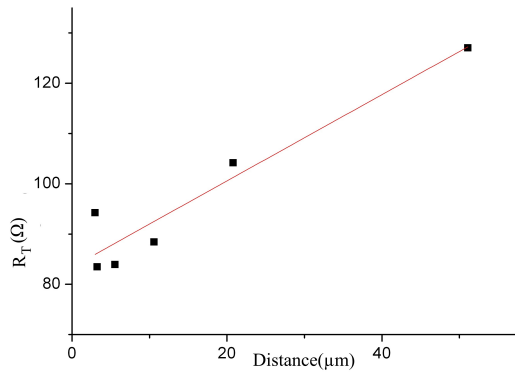
(b)

Figure 4.5: I-V results before(a) and after(b) annealing

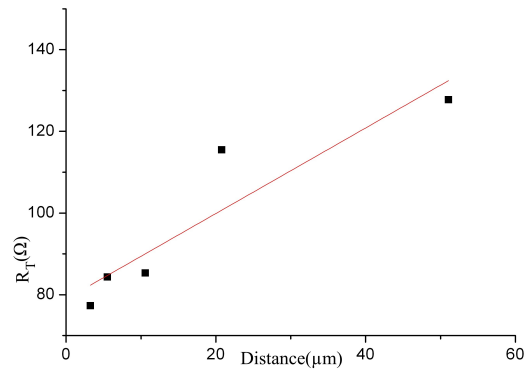
To see the effect of annealing temperature on contact resistance, ohmic contacts are formed with temperatures of 800, 850 and 900 °C. R_T vs distance graph for these three samples can be observed from Figure 4.6.



(a)



(b)



(c)

Figure 4.6: R_T vs distance graph for annealing temperatures of 800(a), 850(b) and 900 °C(c)

From R_T vs *distance* graph, the values of R_C and R_{SH} are obtained as explained in Section 4.2. These values can be seen in Table 4.1.

Temperature	R_C ($\Omega.mm$)	R_{SH} ($\Omega/\square$)
800 °C	31.587	393.56
850 °C	8.342	171.54
900 °C	7.894	209.43

Table 4.1: R_C and R_{SH} values at different annealing temperatures

These results show that contacts annealed at 800 °C show higher contact resistance, therefore, higher temperatures are required for better contacts. On the other hand, contacts annealed at 850 °C and 900 °C show lower resistances with similar R_C values(8.342 $\Omega.mm$ and 7.894 $\Omega.mm$). However, R_{SH} increases when annealing temperature increases from 850 °C to 900 °C, which may indicate a degradation in film structure. Therefore, annealing temperature is picked as 850 °C for further processes.

4.4 Van Der Pauw Structures

Van der Pauw method is first developed in 1958, which is a modified 4-point-probe method to measure resistivity, mobility and carrier concentration of a sample [67]. The illustration of the structure used in this project can be observed in Figure 4.7.

In this thesis, van der Pauw structures are used to find carrier concentration and mobility of 2DEG formed at the AlN/GaN interface. In this method, first, a number is given for each contact as 1,2,3,4 in counterclockwise direction. Then a current is applied to two of the contacts and voltage is measured from other two contacts. For example, if a current is applied to contacts 1 and 2, then voltage is measured from contacts 3 and 4. Applied currents are named as I_{xy} , where the current flows from contact x to contact y . (For example I_{12} is the current that flows from 1 to 2). Also, measured voltages are named as V_{xy} , where $V_{xy} = V_y - V_x$. To find carrier concentration and mobility from van

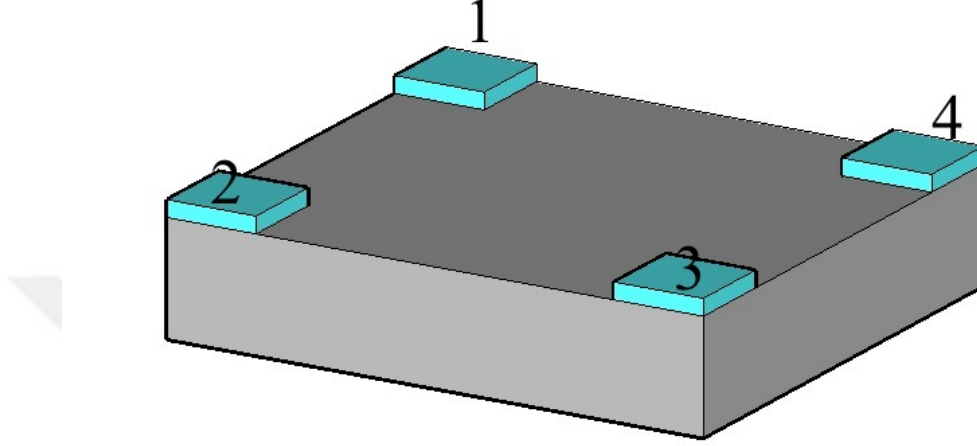


Figure 4.7: van der pauw structure used in this project

der pauw structures, first, resistivity measurement should be taken. For this purpose, following measurements should be taken:

- I_{12} is applied and V_{43} is measured.
- I_{21} is applied and V_{34} is measured.
- I_{32} is applied and V_{41} is measured.
- I_{23} is applied and V_{14} is measured.
- I_{43} is applied and V_{12} is measured.
- I_{34} is applied and V_{21} is measured.
- I_{14} is applied and V_{23} is measured.
- I_{41} is applied and V_{32} is measured.

Then the resistances are calculated for each I-V pair by dividing measured voltage to applied current. (For example $R_{12,43} = \frac{V_{43}}{I_{12}}$) After that, the following calculations are made:

$$R_A = \frac{R_{12,43} + R_{21,34} + R_{43,12} + R_{34,21}}{4}$$

$$R_B = \frac{R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32}}{4}$$

Finally, sheet resistance R_{SH} is taken from the equation,

$$e^{(\pi R_A/R_{SH})} + e^{(-\pi R_B/R_{SH})} = 1 \quad (4.3)$$

After taking resistivity measurements, Hall measurements should be taken to find mobility and carrier concentration, which means measurements should be taken under applied magnetic field. In this method, 2 sets of results should be obtained under magnetic fields with positive and negative z-direction. Then the following measurements are taken under both positive and negative applied magnetic field:

- I_{13} is applied and V_{24} is measured.
- I_{31} is applied and V_{42} is measured.
- I_{42} is applied and V_{13} is measured.
- I_{24} is applied and V_{31} is measured.

Then the following calculations are made:

$$V_C = V_{24,p} - V_{24,n}$$

$$V_D = V_{42,p} - V_{42,n}$$

$$V_E = V_{13,p} - V_{13,n}$$

$$V_F = V_{31,p} - V_{31,n}$$

where, voltages with subscript p indicates measurement under positive magnetic field and voltages with subscript n indicates measurement under negative magnetic field. Then the Hall voltage(V_H) is calculated by the equation

$$V_H = \frac{V_C + V_D + V_E + V_F}{8}. \quad (4.4)$$

The sign of the hall voltage shows the doping type of the material. The material is p-type if V_H is positive and it is n-type if V_H is negative. After finding V_H , it is possible to calculate carrier concentration n_s (in this case electron concentration in 2DEG layer) by the following equation

$$n_s = \frac{IB}{q|V_H|}, \quad (4.5)$$

where B is the strength of applied field, I is the magnitude of applied current and q is charge of an electron.

Finally mobility can be calculated by the equation

$$\mu = \frac{1}{qn_s R_{SH}}. \quad (4.6)$$

In this project, van der Pauw structures are fabricated on $4mm \times 4mm$ samples. Then, ohmic contact formation process defined in Section 3.10 is followed to deposit Ti/Al/Ni/Au (20/60/40/50nm) metal stack as contacts, where the contacts are placed at the corners as in Figure 4.7. To measure the mobility and sheet carrier concentration of the sample, ezHEMS Hall Effect Measurement System is used. This system can directly make the calculations defined in this section in its software, therefore, no extra calculations are required. Measurements are taken under three different current and results can be seen from Table 4.2.

Current(μA)	Sheet Concentration(cm^{-2})	Mobility($cm^2/V.s$)
1	1.60×10^{13}	1004.02
10	1.53×10^{13}	1046.52
100	1.57×10^{13}	1047.97

Table 4.2: eZHEMS measurement results for different applied current

Chapter 5

Electrical Characterization of AlN/GaN MIS-HEMTs

5.1 Introduction

This chapter will give the electrical characterization results of fabricated MIS-HEMTs. In first sample, which will be called s-MIS-HEMT in this thesis, SiN that already exist on top of purchased samples as in Figure 1.2 is used as gate dielectric. In second sample, which will be called as a-MIS-HEMT in this thesis, a 4nm thick Al_2O_3 is grown at 80 °C with ALD on top of SiN at gate area, therefore an Al_2O_3/SiN layer is used as gate dielectric. I_D vs V_{DS} and g_m vs V_{gs} characteristics of both s-MIS-HEMT and a-MIS-HEMT will be given and discussed and finally, gate leakage performance of both devices will be investigated. Keithley 4200 Semiconductor Parameter Analyser is used for all of these characterizations.

5.2 Characterization of s-MIS-HEMTs

Fabrication of s-MIS-HEMTs are performed as defined in Section 3.10. SEM image and optical microscope image of the fabricated transistors can be seen in Figure 5.1.

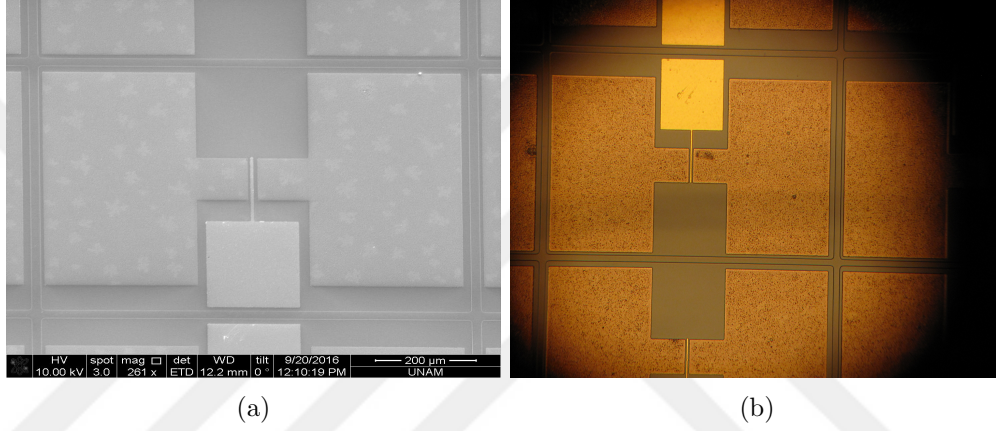


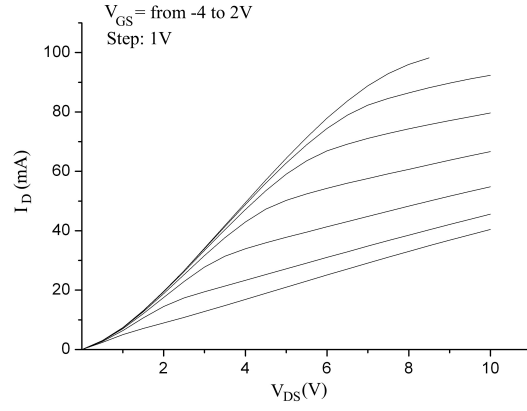
Figure 5.1: SEM(a) and optical microscope(b) image of fabricated HEMTs

Transistors with three different gate length are fabricated on the same sample in same process. Dimensions of fabricated devices can be seen in Table 5.1

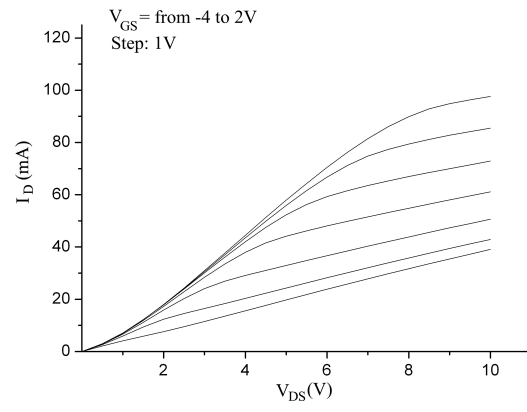
$L_G(\mu m)$	$L_{DS}(\mu m)$
2	6.5
3	10
5	18

Table 5.1: Transistor dimensions

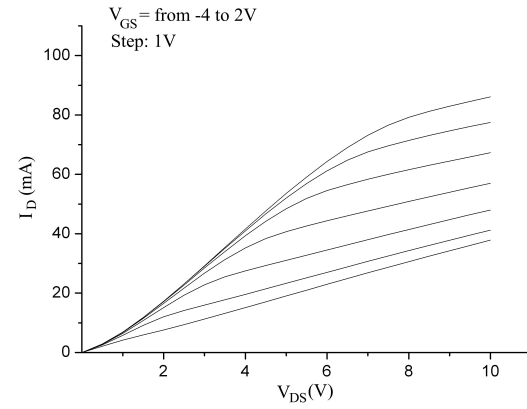
After the fabrication of s-MIS-HEMTs, first, I_D vs V_{DS} characteristics of these transistors are measured. Result of these measurements can be observed in Figure 5.2.



(a)



(b)



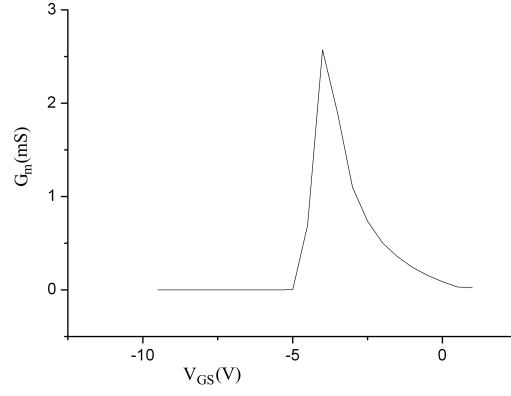
(c)

Figure 5.2: I_D vs V_{DS} characteristics of s-MIS-HEMTs with gate length of 2(a), 3(b) and 5(c) μm

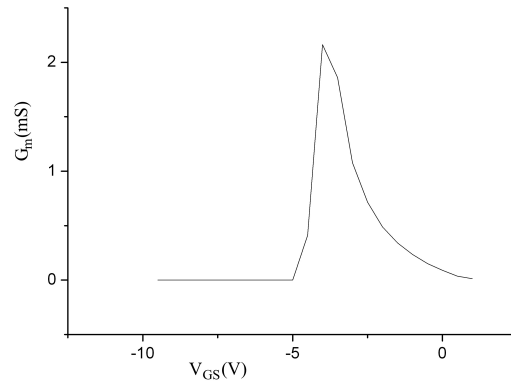
From the results, it is observed that higher current values are measured at same V_{DS} bias for transistors with smaller gate lengths, which is an expected situation [46]. Gate control can be remained for even at the bias of $V_{GS} = 2V$ for the transistors. Also, threshold voltage, V_{th} is found as -6.06 , -6.09 and $-6.38V$ for transistors with gate length of 2, 3 and $5\mu m$.

After this measurement, another measurement is taken with $V_{DS} = 1V$ to find G_m vs V_{GS} characteristics of the transistors, where G_m is the measured transconductance. Results of these measurements can be observed in Figure 5.3.

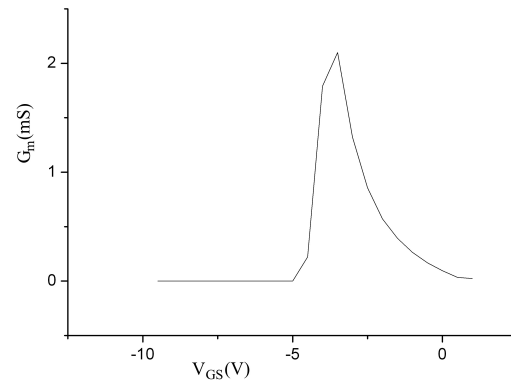
From the measurements, peak transconductance values of 2.57, 2.16 and $2.09mS$ are obtained for transistors with gate length of 2, 3 and $5\mu m$. An increase in maximum G_m is observed with a decrease in gate length.



(a)



(b)



(c)

Figure 5.3: G_m vs V_{GS} characteristics of s-MIS-HEMTs with gate length of 2(a), 3(b) and 5(c) μm

5.3 Characterization of a-MIS-HEMTs

Fabrication of a-MIS-HEMTs are carried out as defined in Section 3.10. A 4 nm thick Al_2O_3 dielectric layer is deposited at 80 °C with ALD under gate contact. By this way, a better carrier confinement at the AlN/GaN interface to improve DC characteristics is aimed. Also, lower gate leakage current due to the improved barrier to prevent tunneling of electrons from AlN to gate contact is expected. To test this, first, I_D vs V_{DS} characteristics of these transistors are measured and results of these measurements can be observed in Figure 5.4.

Again, an increase in I_D value is observed for same V_{DS} value with a decrease in gate length. Also, I_D values are higher for a-MIS-HEMTs, when compared with s-MIS-HEMTs at same drain and gate bias. This increase is due to the higher carrier concentration due to the addition of Al_2O_3 layer [68]. Like s-MIS-HEMTs, gate control can be remained for even at the bias of $V_{GS} = 2V$ for the transistors. This time, V_{th} is found as -10 , -9.55 and $-10.2V$ for transistors with gate length of 2, 3 and $5\mu m$, which are at more negative values when compared with s-MIS-HEMTs. This is an expected result, due to the increase in gate to channel separation by addition of extra dielectric with ALD [69].

After these measurements, G_m vs V_{GS} characteristics of the transistors are obtained under the bias of $V_{DS} = 1V$ and the results can be observed in Figure 5.5.

This time, G_m values of 1.71, 1.66 and $1.36mS$ are obtained for transistors with gate length of 2, 3 and $5\mu m$. An increase in maximum G_m is observed with a decrease in gate length as in the case with s-MIS-HEMTs. Also, obtained maximum G_m values are a bit lower than the results obtained for s-MIS-HEMTs, which is again an expected result [68].

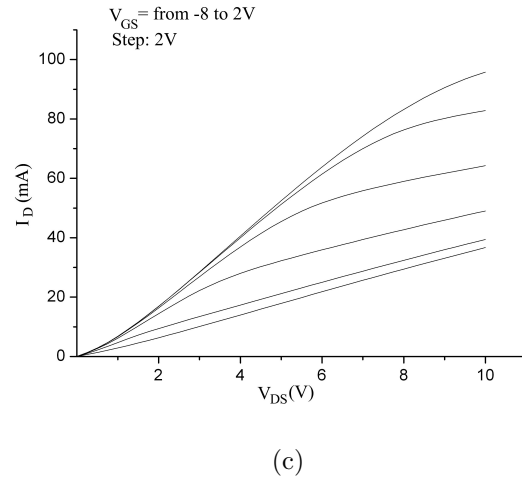
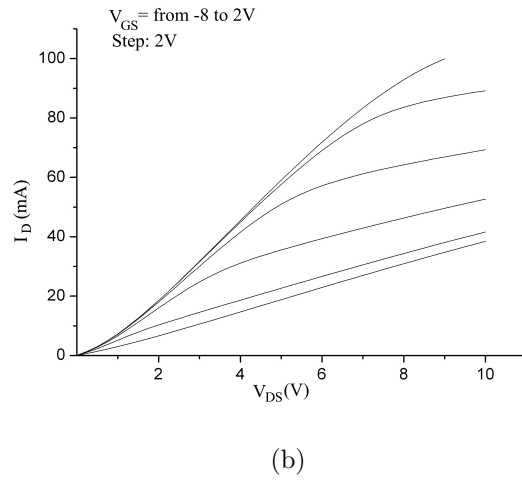
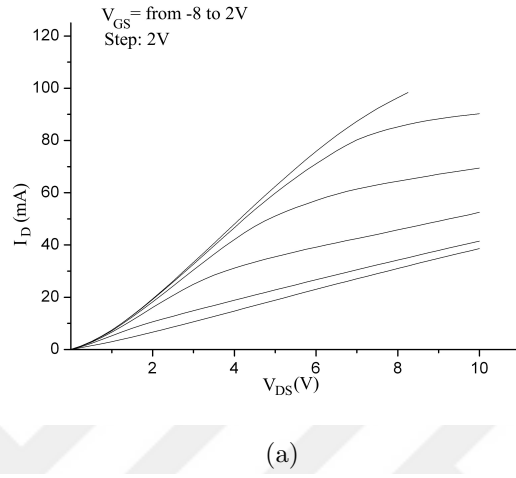
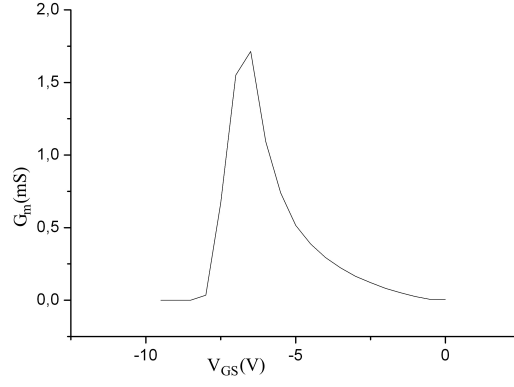
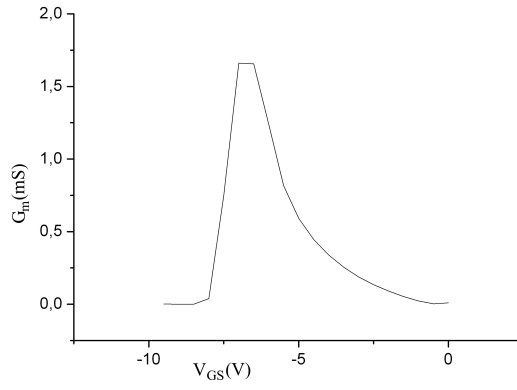


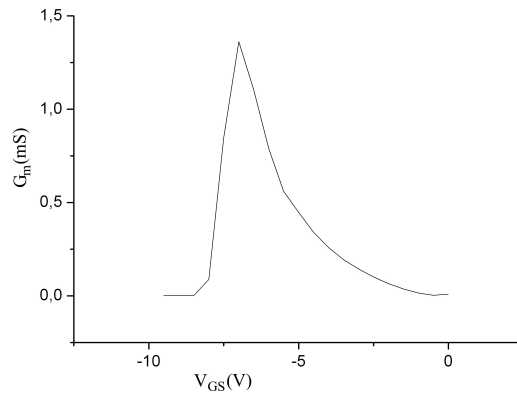
Figure 5.4: I_D vs V_{DS} characteristics of a-MIS-HEMTs with gate length of 2(a), 3(b) and 5(c) μm



(a)



(b)



(c)

Figure 5.5: G_m vs V_{GS} characteristics of a-MIS-HEMTs with gate length of 2(a), 3(b) and 5(c) μm

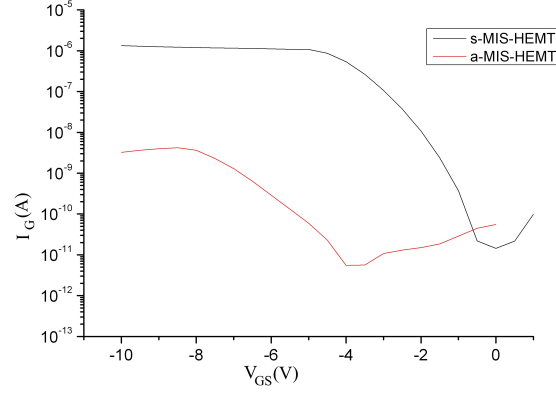
5.4 Gate Leakage Currents for s-MIS-HEMTs and a-MIS-HEMTs

In theory, gate current of a HEMT is expected to be equal to zero. However, in practise, some electrons can tunnel from the channel to the Schottky gate contact and create a nonzero gate current, which is called as leakage current. To lower the power consumption of the transistors, this leakage current should be as low as possible. One solution to decrease the leakage current is the addition of a thin dielectric layer under Schottky gate contact. Addition of this dielectric layer will prevent some of the electrons to tunnel from channel to contact.

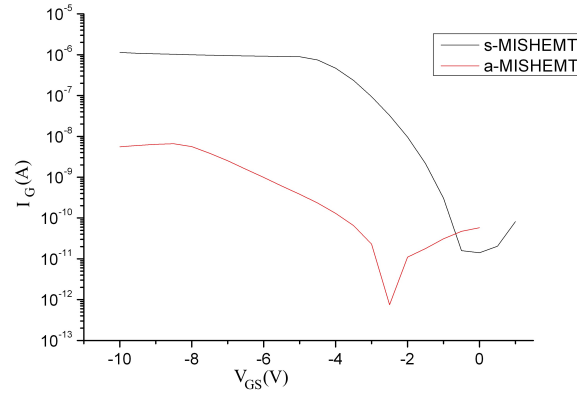
In this project, even s-MIS-HEMTs has a 6nm thick SiN dielectric layer under the gate. However, an enhancement in leakage performance of the transistors is expected by the addition of a thin Al_2O_3 layer with ALD. To verify this theory, gate currents of both s-MIS-HEMTs and a-MIS-HEMTs are measured under the DC bias of $V_{DS} = 1V$ for the transistors with $L_G = 2, 3$ and $5\mu m$. I_G vs V_{GS} characteristics of these transistors can be observed in Figure 5.6.

Under high negative V_{GS} bias, a-MIS-HEMTs have shown at least three orders of magnitude lower leakage current, therefore, it is possible to say that addition of even 4nm thick Al_2O_3 is enough to enhance the leakage performance. Under lower negative V_{GS} bias, both of the devices have leakage currents around the range of $10^{-10} - 10^{-11}A$.

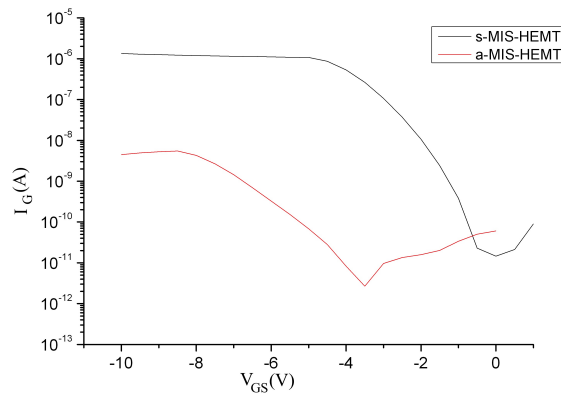
These results show that addition of a thin Al_2O_3 dielectric layer can successfully suppress the gate leakage current while remaining the gate control up to the gate bias of 2V.



(a)



(b)



(c)

Figure 5.6: I_G vs V_{GS} characteristics of s-MIS-HEMTs(black line) and a-MIS-HEMTs(red line) with gate length of 2(a),3(b) and 5(c) μm

Chapter 6

Conclusion

AlN/GaN HEMTs are promising transistors especially for high power and high frequency applications due to their excellent properties such as high breakdown voltage and high electron mobility provided by the 2DEG at their interface. Especially, by fabricating these transistors onto Silicon substrates, AlN/GaN HEMTs can be integrated easily in today's electronics technology. However, such transistors can suffer by high gate leakage currents. One solution to this problem is addition of a thin dielectric layer under gate area, where these transistors are called as MIS-HEMTs.

In this work, AlN/GaN heterostructure with a SiN top layer grown on Silicon substrate is used for fabrication of MIS-HEMTs. This work combines GaN-on-Silicon concept with AlN/GaN heterostructure concept, gate dielectric deposition with low temperature ALD concept and usage of Al_2O_3/SiN dielectric stack as gate dielectric concept, which makes this work as unique in this topic.

First step of this project was fabrication of the ohmic contact on AlN/GaN heterostructure. First contacts were suffering due to the existence of native oxide at the top of the samples and after the removal of this native oxide layer, ohmic contact behaviour could be observed. Then, effect of annealing temperature is

tested under annealing temperatures of 800, 850 and 900 °C. Especially, for annealing temperature of 850 °C, $R_C = 8.342\Omega.mm$ and $R_{SH} = 171.54\Omega/\square$ are obtained and annealing temperature is picked as 850 °C for further processes. In this step, finally, van der pauw structures are fabricated on $4mm \times 4mm$ samples to find the mobility and sheet carrier concentration of the samples. Sheet carrier concentration around $1.55 \times 10^{13} cm^{-2}$ and mobility value around $1047 cm^2/V.s$ is obtained from those measurements.

After successfully formation of ohmic contacts, MIS-HEMTs are fabricated on AlN/GaN heterosturcture by using the SiN layer that already exists on the samples as gate dielectric with three different gate lengths of 2, 3 and $5\mu m$ where these transistors are called as s-MIS-HEMTs in this thesis. A successful gate control is obtained up to a gate bias of $+2V$ and higher drain currents are obtained for transistors with smaller gates under same bias conditions. Also, a peak transconductance value of $2.57mS$ is obtained for the transistors with gate length of $2\mu m$ and a bit lower transconductances are obtained for transistors with larger gates ($2.16mS$ and $2.09mS$ for gate lengths of 3 and $5\mu m$). Increasing G_m with decreasing gate length will be result in an enhancement in RF performance of devices, which means devices with lower gate length can operate at higher frequencies as expected [46].

Another set of transistors are fabricated by addition of a 4nm thick Al_2O_3 layer on top of SiN layer at gate area to enhance the gate leakage performance of these transistors. These transistors are called as a-MIS-HEMTs in this thesis. Again, a successful gate control is obtained for the gate biases up to $+2V$. This time, higher drain currents are obtained when compared with s-MIS-HEMTs with same gate length, under same bias conditions. However, a bit lower peak transconductance value of $1.71mS$ is obtained for the transistors with gate length of $2\mu m$. This time, although there is a decrease in G_m value, due to the enhanced 2DEG quality, a negative effect on RF performance should not be expected [68]. Finally, gate leakage currents of s-MIS-HEMTs and a-MIS-HEMTs are compared and an enhanced suppression is observed for a-MIS-HEMTs. Especially for high negative gate biases, a decrease of at least three orders of magnitude is observed in gate current and it decrease from $10^{-6}A$ level to $10^{-9}A$ level. Moreover, for

low negative gate biases, gate currents around $10^{-10} - 10^{-11} A$ level are obtained.

To sum up, it is possible to say that, even adding a very thin(4nm) Al_2O_3 layer, the gate leakage and drain current performances of MIS-HEMTs could be enhanced. These shows that Al_2O_3/SiN stack as a gate dielectric can be a better barrier for electron tunneling between channel and gate contact and can provide higher 2DEG carrier concentration than transistors with just SiN as gate dielectric.

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