FPGA BASED PULSE WIDTH MODULATION DRIVE FOR UNDERWATER LOW FREQUENCY MAGNETIC FIELD GENERATION

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By

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ABSTRACT

FPGA BASED PULSE WIDTH MODULATION DRIVE FOR UNDERWATER LOW FREQUENCY MAGNETIC FIELD GENERATION

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M.S in Electrical and Electronics Engineering

Supervisor: Prof. Dr. Yusuf Ziya İder

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Main focus is to design an electronic circuit which drives a coil for producing underwater magnetic fields at aimed distances. This circuit should handle AC, DC drive individually and both at the same time. After some trials of quite lossy analogue circuitry, the switching converter & inverter structure is determined to be the framework. Although that brings extra complexity of controlling switches digitally with a processor circuitry; it is quite flexible for modes of operations. H-bridge with MOSFETs as switches, is the drive circuitry and with proper software selection, the hardware serves a DC-DC converter or a DC-AC inverter. In addition, because switches do operate at "saturation", it is much more efficient than the previous design.

Besides EMI handicap and some switching losses of the structure, controlling the switches is also somewhat cumbersome. The asynchronous double-edge natural sampling pulse width modulation is employed as the switching scheme of DC-AC inverter mode. With this technique, the output waveform has none of fundamental frequency harmonics which are of prime concern. However, digital application of such analog circuit compatible method will be problematic. There may occur "glitches" at PWM drive signals, because of the mismatch between sampling rates of fixed carrier and variable modulating signal frequencies. In addition, the finite switching duration also is another issue to be considered. For both inverter and

converter mode of operation, some precautions must be taken to prevent DC supply from being shoot-through.

For removing the previously mentioned "glitch", re-adjusting the sampling rate of the comparator to a suitable value seems practical. For preventing the shorting of the DC supply, an idle time along switching duration, “dead-time” is generated. For EMI and carrier harmonics in the output waveforms, no snubber or such switching-aid network is planned to be used because these high frequency components of the load current pass through the self-capacitance of the load coil. The magnetic field generating inductive part only has negligible ripple at the switching frequency. Even this situation is ignored; such high frequency alternating fields cannot penetrate through much distance underwater. They are attenuated sufficiently according to underwater characteristics of the magnetic fields propagations. Thus, magnetic field of the fundamental frequency at the target will not be distorted.

Keywords: Full-Bridge, Class-D, Underwater Magnetic Field, PWM, dead-time, natural sampling, uniform sampling, switching converter & inverter, class-D EMI

ÖZET

SUALTI MANYETİK ALAN YARATIMLARI İÇİN FPGA TABANLI DARBE GENİŞLİK MODÜLASYON SÜRÜŞÜ

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Ocak 2014

Araştırmanın temel odağı belirli bir mesafede manyetik alan üretebilmek için elektonik devre tasarımı yapmaktır. Bu devre AC ve DC işaretlerle sürülebildiği gibi aynı zamanda bu iki işaretin tipinin birleşimlerinde de çalışabilmelidir. Bir hayli verimsiz bir kaç analog devre denemesinden sonra, anahtarlanan dönüştürücü devre yapıları seçilmiştir. Bu yapıdaki anahtarların, bir mikroişlemci gibi dijital ortamlarda kontrol edilemesi ilave bir külfet getirir. Fakat bu, kontrol devrenin aynı zamanda farklı operasyonlar için esnek olmasını sağlar. Buna ek olarak "satürasyon" alanlarında kullanılan transistörler, devrenin ilk opsiyona gore çok daha verimli olmasını sağlar. Bu tez kapsamında, güç MOSFET'lerinin anahtar olarak kullanıldığı bir H-köprüsü kurulmuş ve uygun sürüş sinyalleriyle bu donanım hem DC-DC hem de DC-AC çevirici olarak kullanılmıştır.

Elektromanyetik enterferans ve önemsiz anahtarlama kayplarına ek olarak, devredeki anahtarların durum kontrolleri de bi derece karmaşıktır. Asenkronize çift-kenarlı doğal örneklemeli darbe genişlik modülasyon tekniği, DC-AC çeviriminde kullanılacak anahtarlama kontrolü için seçilmiştir. Bu tekniğin seçiminde temel sinyal harmoniklerinin çıkış dalga formunda gözükmemesi esas alınmıştır. Fakat analog sistem çıkışlı böyle bir tekniğin dijital ortamlarda işletilmesi bazı problemleri beraberinde getirebilir. Anahtarları süren kontrol sinyalleri yaratılırken istenmeyen küçük zamanlı darbeler ortaya çıkabilir. Bu durum modüle edilen ve taşıyıcı sinyal örnekleme frekanslarındaki uyumsuzluklardan ileri gelir. İlk sinyalin frekansının değişken ikincisin sabit olması böyle bir uyumsuzluğa neden olur. Bundan başka,

transistörlerin sonlu anahtarlanma süreleri dikkat edilmesi gereken başka bir konudur. Bu nedenle hem DC-DC hem DC-AC çevrim sırasında, DC güç kaynağının kısa devre olmasının engellenmesi için bazı tedbirler alınmalıdır.

Bahsi geçen problemlerden sinyal örnekleme frekans uyumsuzluğu ve sonucunda istenmeyen darbelerin sürüş işaretelerinde ortaya çıkması, taşıyıcı sinyal frekansının düşürülmesiyle önlenir. DC güç kaynağının kısa devre olması ise anahtarlama işaretlerine ölü zaman eklenerek önlenebilir. Buna karşın elektromanyetik interferans ve taşıyıcı sinyal harmonikleri için herhangi bir söndürücü devre yapısı kullanılmamıştır. Çünkü böylesine yüksek frekanslardaki yük akım bileşenleri, indüktif yükün iç kapasitansı üzerinden akar. Manyetik alan yaratımından sorumlu indüktif kısımda sadece önemsenmeyecek büyüklüklerde anahtarlama frekansı bileşeni gözlenir. Bu durumun göz önünde bulundurulmasa bile, bu frekanslardaki manyetik alanlar sualtında fazla bir mesafeye nüfuz edemezler. Sualtı manyetik yayılım karakterine göre yeterince sönümlenirler. Bu şekilde, çalışmada belirlenen hedef uzaklıkta, temel frekanstaki alan bozulmaz.

Anahtar sözcükler: tam-köprü, D-tip amfi, sualtı manyerik alan, darbe genlikli modülasyon, ölü-zaman, doğal örnekleme, tekdüze örnekleme, anahtarlanan çevirici, D-tip amfi elektromanyetik enterferans.

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Chapter 1

Introduction

1.1 Purpose of the Study

This thesis is the result of work for constructing an underwater magnetic and electromagnetic field generator circuitry. Basically, it consists of two main parts: a signal amplification stage (driver circuit) and a load which is a pre-designed inductor out of the scope of the study has been made here. Briefly, the casing concerns and reaching proper levels of target (in a 1m radius) magnetic field levels have determined the form of this coil. As the name of the work suggests, the driver circuit provides the required amounts of DC and AC currents. The type of the amplifier is selected to be a full-bridge Class-D amplifier which can be used as either a DC-DC converter or a DC-AC inverter. The pulse width modulation (PWM), which is the essential drive technique for this type of circuits, has been employed as the drive method and a Xilinx FPGA chip is used as the digital application platform.

1.2 Scope of the Study

This work has mainly dealt with issues which appear while deploying a pulse width modulation at a digital platform. The pulse width modulated signal generation has been discussed here with some modifications involved in for the proper operation of the circuitry. The hardware part, the driver circuit, has also been analyzed by simulations. In addition, the load signal characteristics have been investigated for their great influence on the spectrum of the generated target magnetic field.

1.3 Literature Survey

1.3.1 Full Bridge (H-Bridge)

A full bridge is a kind of a circuit structure used for the purpose of either an AC signal amplification (DC-AC inversion) or a DC voltage conversion [1]. As its name implies, a full bridge consists of four switches which are arranged in a bridge formation. The structure is like the letter "H" and this is why the circuitry is also called "H-bridge". As seen in "Figure 1" below, a load is connected between two arms of the bridge right in the middle of switches.

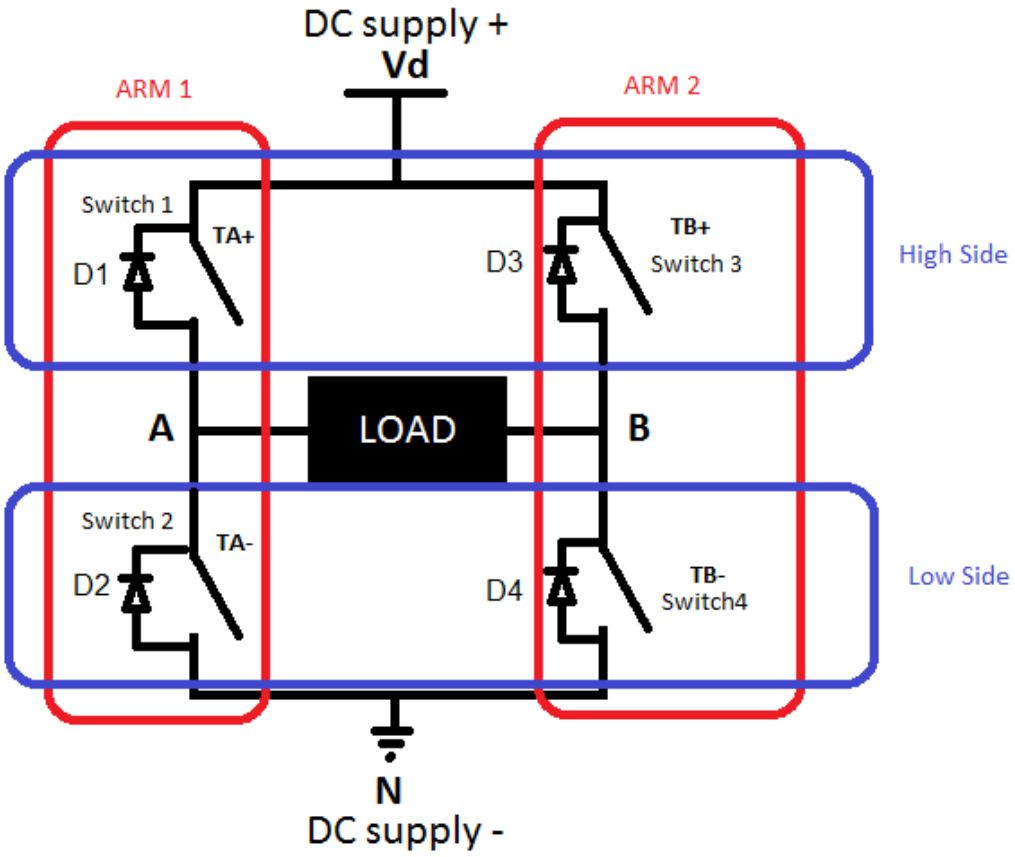

Figure 1 - Full Bridge (H-Bridge)

By controlling conducting and non-conducting durations of these switches, desired voltage and current levels are acquired at the output [1]. As mentioned before, a

special technique called “Pulse Width Modulation” (PWM) is used to produce drive voltage signals for the supervision of states of voltage controlled switches. In this work, the full bridge can be used either as a DC-DC converter or a DC-AC inverter by only modifying these PWM drive signals. This is accomplished by changing the type of the signal, called “modulating signal”, which is subjected to the modulation. If pulse widths of drive signals are determined by modulation of a DC signal, these pulse durations will be constant through the entire operation and the circuitry behaves as a DC-DC converter [1]. In case of the modulating signal to be an AC type, the amplitude information of this signal will be encoded into changing pulse widths of drive signals, then the circuit serves as a DC-AC inverter [1].

PWM signals are produced digitally at microprocessors which have simple digital logic voltage levels. The low state level is able to make a switch (transistor) not to conduct however; the high state is only able to make upper sides switches to conduct after proper voltage level adjustments. These are done by some electronic networks, called driver circuits. The reason behind this is either TTL or CMOS logic voltage levels are not sufficient to be higher than the source voltage plus the gate-to-source threshold of a transistor which resides at a high side of a bridge.

1.3.2 What is Pulse Width Modulation (PWM)?

The “Pulse Width Modulation” is a devoted drive technique for “Class-D” amplifiers and bridge type DC-DC converters. The essence of the method relies on modulating a signal by coding its amplitude variations in time (phase angles) into pulse widths of the produced PWM signal as a pulse train [1]. This resulting signal is called “modulated signal” [1]. Obviously, the signal of which amplitude levels are used is called “modulating signal” [1]. The modulation procedure also needs another signal called “carrier signal” in addition to a modulating signal. This is mostly triangular or saw-tooth shaped and compared with the modulating signal with respect to the amplitude [1]. The resulting modulated signal pulse widths are determined by the duration where the modulating signal is bigger than the carrier in amplitude [1]. This scenario is illustrated in “Figure 2” below.

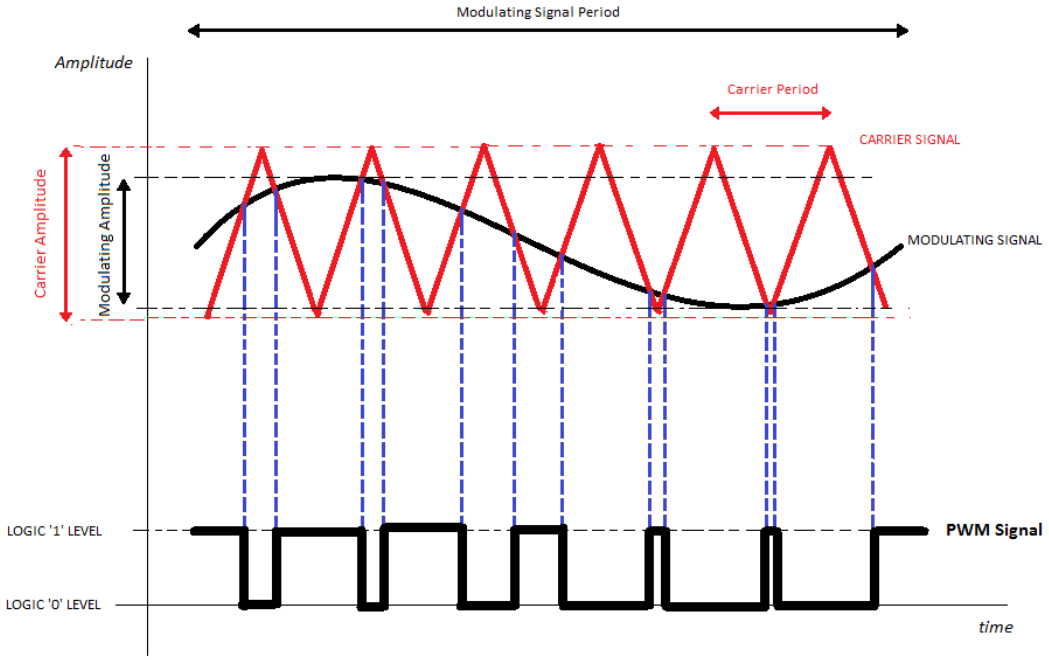

Figure 2 - Pulse Width Modulation Procedure

1.3.2.1 *DC-DC Converter*

In this type of use of a full-bridge, desired DC voltage levels at the output of the circuitry are produced from an independent level of a supply voltage [1]. In other words, a DC level is converted to another DC level. The modulating signal used here to produce the PWM signals is just a DC level. It is adjusted according to the carrier signal amplitude to get desired levels at the output. The fundamental component level of the voltage across the output load will then be the supply voltage multiplied with the ratio of the modulating DC signal level to the carrier peak [1].

There are two main switching schemes which are called PWM with a bipolar and PWM with a uni-polar voltage switching. For the bipolar case; "switch 1 (T_A+)" with "switch 4 (T_B-)" and "switch 3 (T_B+)" with "switch 2 (T_A-)" in "Figure 1" forms two switch pairs. Each switch of the couples, conducts or not simultaneously with their pairs [1]. In addition, the couples also work complementarily among themselves, not to short the power supply which refers a phenomenon called the "shoot-through" or the "cross-conduction". This means then, the both of the cross switches and the ones

at the same arm operate complementarily. However, for the unipolar switching, only the switches at same arms operate in that fashion. There is no relation in the working of the switches which belong to the different pairs [1].

1.3.2.1.1 PWM with Bipolar Voltage Switching

At the bipolar switching, either one of the pre-defined switch pairs conducts at switching periods (Following calculations are made by no dead time, which is going to be mentioned afterwards, is assumed to be involved.) [1].

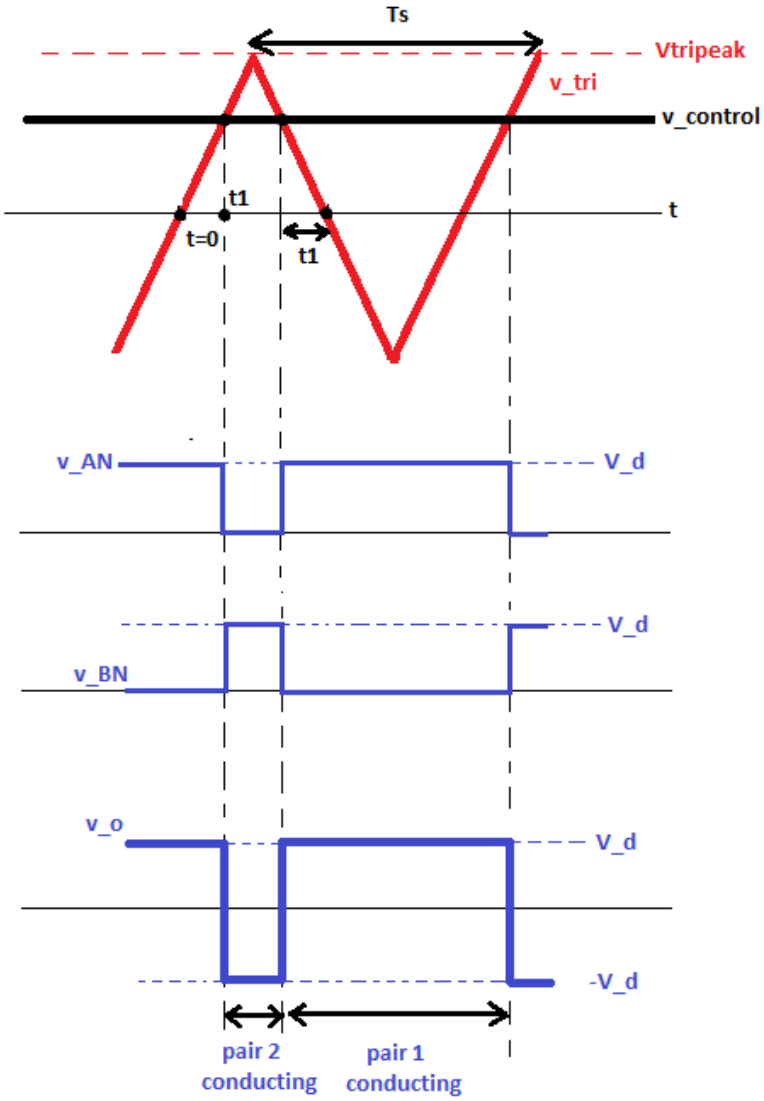

Figure 3 - DC-DC Conversion by bipolar switching

As can be seen in "Figure 3" above:

$$v_{tri} = V_{tri\_peak}\,\frac{t}{Ts/4} \qquad 0 < t < \frac{1}{4}\,Ts \qquad (1)$$

$$t = t_1, v_{tri} = v_{control} \qquad (2)$$

$$t_1 = \frac{v_{control}}{V_{tri\_peak}}\frac{Ts}{4} \qquad (3)\ [1].$$

It is found that the conducting duration "t_{on}" of the "switch pair 1" (T_A+, T_B-) is:

$$t_{on} = 2t + \frac{1}{2}T_s \qquad (4)$$

then the duty cycle of the same pair will be:

$$D_1 = \frac{t_{on}}{T_s} = \frac{1}{2}\left(1 + \frac{v_{control}}{V_{tri\_peak}}\right) \quad for \quad (T_A+, T_B-) \qquad (5)\ [1]$$

The duty cycle of the other pair, pair 2 (T_B+, T_A-), which works complementarily with first one is then:

$$D_2 = 1 - D_1 \quad for \quad (T_B+, T_A-) \qquad (6)$$

and, the average voltage across the output terminals will be:

$$V_o = V_{AN} - V_{BN} = D_1V_d - D_2V_d = (2D_1 - 1)V_d \qquad (7)\ [1]$$

Substituting "D_1":

$$V_o = \frac{V_d}{V_{tri\_peak}}\,v_{control} = kv_{control} \qquad (8)\ [1]$$

and "$k = \frac{V_d}{V_{tri\_peak}} = constant$" implies that the average output voltage changes linearly with the input control signal, as it is the case for a linear amplifier [1].

The output voltage "v_o" can only have two values: either "$+V_d$" or "$-V_d$". This is why the switching scheme is called the "bipolar voltage-switching PWM" [1].

1.3.2.1.2 PWM with Unipolar Voltage Switching

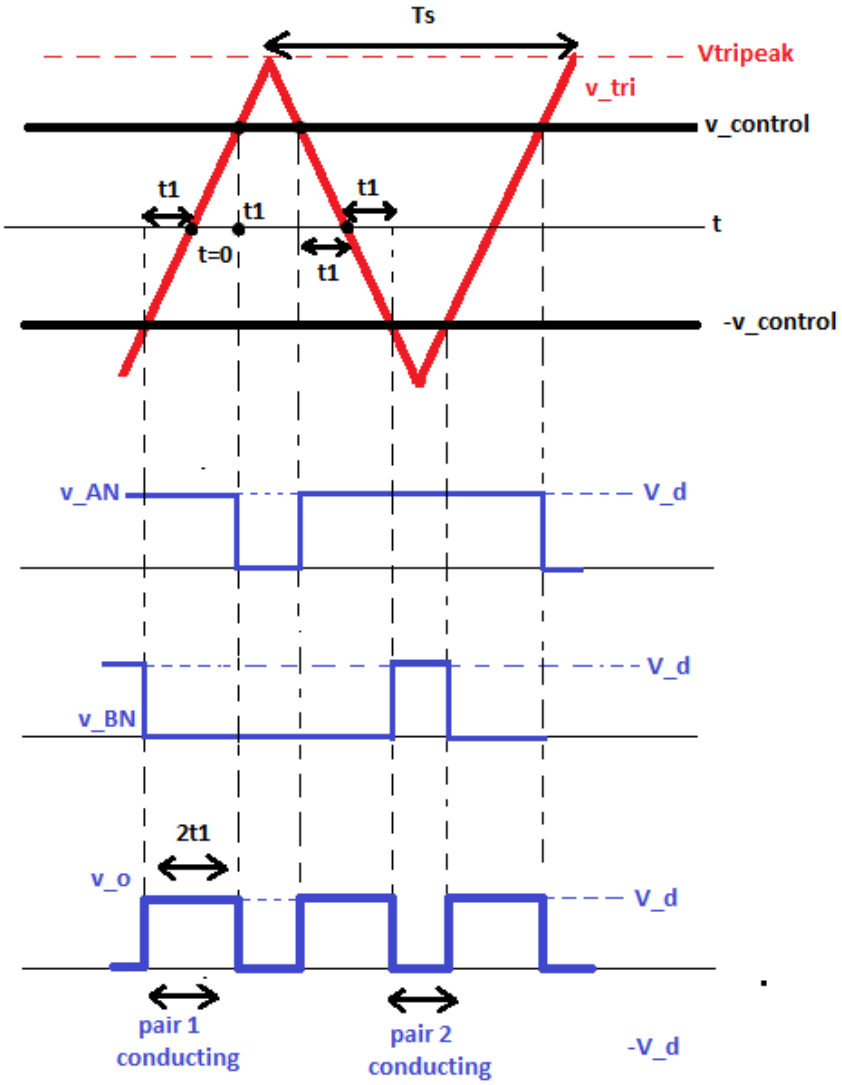

Figure 4 - DC-DC Conversion by Unipolar Switching

In "Figure 4" above, a triangular carrier signal is compared with both the control voltage (modulating signal) "$v_{control}$" and "$-v_{control}$" for producing PWM drive signals for the switches resides at first and second arm of the bridge, respectively [1]. States of these switches are determined then as the following comparison suggest:

$$T_A + \ on: \ if \ v_{control} > v_{tri} \qquad (9)$$

$$T_B + \ on: \ if \ -v_{control} > v_{tri} \qquad (10)\ [1]$$

By analyzing the "Figure 4", it is intuited that the duty cycle values are very similar to the ones bipolar PWM has:

$$D_1 = \frac{t_{on}}{T_s} = \frac{1}{2}\left(1 + \frac{v_{control}}{V_{tri\_peak}}\right) \qquad (T_A+, T_B-) \qquad (11)$$

$$D_2 = 1 - D_1 \qquad (T_B+, T_A-) \qquad (12)$$

$$V_o = (2D_1 - 1)V_d = \frac{V_d}{V_{tri\_peak}}\, v_{control} \qquad (13)\ [1]$$

Thus, the results shows that the average output voltage "V_o" of the unipolar switching PWM is same with the bipolar voltage-switching scheme's and again it varies linearly with the input control (modulating) signal, "$v_{control}$" [1].

For the same switching frequencies (carrier signal frequency), the use of the unipolar voltage switching method will result in a better frequency response at the output, a spectrum with lowered levels of unwanted harmonics [1]. In other words, ripple magnitudes at output waveforms will be reduced [1]. This is because of the "effective" switching frequency of the output voltage signal is twice the one belongs to bipolar case [1].

The output voltage of the two methods is assumed to be independent of the output load current "i_o", because a "dead-time", which will explained at the following sections, is not involved in PWM drive signals of switches [1]. Then the RMS value of the voltage ripple "V_r" across output terminals in terms of the average "V_o" can be calculated for [1]:

a) PWM with the bipolar switching:

   The RMS value of the output voltage signal "v_o" shown in "Figure 3" is calculated as follows:

$$V_{o,rms} = V_d \qquad (16)$$

$$V_o = (2D_1 - 1)V_d \qquad (17)$$

$$V_{r,rms} = \sqrt{V_{o,rms}^2 - V_o^2} = V_d\sqrt{1-(2D_1-1)^2} = 2V_d\sqrt{D_1 - D_1^2}$$

$$for\ 0 \le D_1 \le 1\ (14)\ [1]$$

b) PWM with the unipolar switching:

The RMS value of the output voltage "v_o" shown in "Figure 4" can be calculated as follows:

$$t_1 = \frac{v_{control}}{V_{tri\_peak}}\frac{Ts}{4} \qquad for\ v_{control} > 0 \qquad (15)$$

$$V_{o,rms} = \sqrt{\frac{4t_1V_d^2}{T_s}} = \sqrt{\frac{v_{control}}{V_{tri\_peak}}}\,V_d = \sqrt{(2D_1-1)}\,V_d \qquad (16)$$

$$V_{r,rms} = \sqrt{V_{o,rms}^2 - V_o^2} = \sqrt{6D_1 - 4D_1^2 - 2V_d},$$

$$for\ 0.5 \le D_1 \le 1\ (17)\ [1]$$

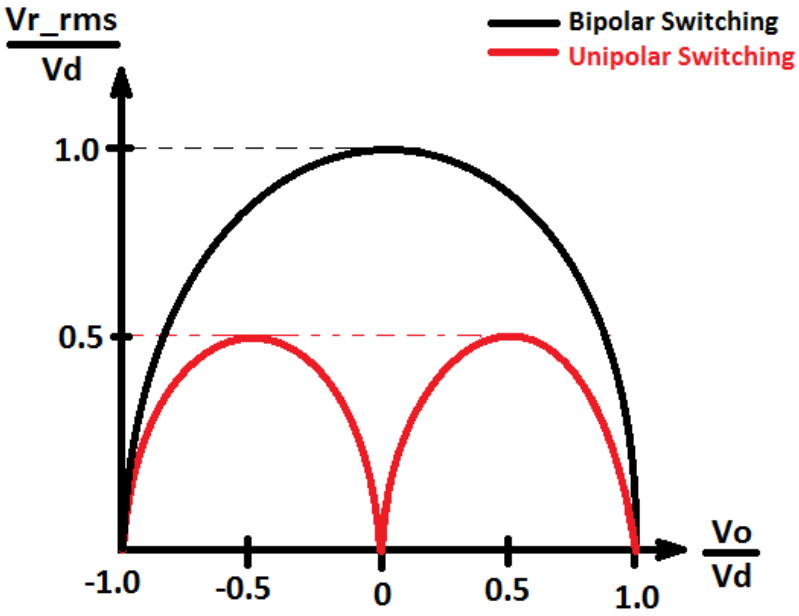

Figure 5 - Comparison between RMS Output Voltage Ripple of Unipolar and Bipolar Switching

1.3.2.2 *DC-AC Inverter (Class-D Amplifier)*

As its name suggests DC-AC inverters are used to produce AC signals from DC levels. This can be done by the use of proper AC modulating (control) signals to produce PWM signals. So, pulse widths vary for different switching periods with respect to the magnitude levels of the control signal sampled at the corresponding switching interval. Desired AC waveforms can be acquired by driving a full-bridge with this PWM signals. Before providing a more detailed explanation of full-bridge DC-AC inverters, a few points should be considered. The ratio of the amplitude of the modulating (control) signal to carrier's is called the "modulation index":

$$m_a = \frac{V_{control}}{V_{tri\_peak}} \qquad (18)$$

This index differs from '0' to '1' in general but also may exceed '1' in some special cases which are called the "over modulation" [1]. The other important ratio is made up from frequencies and it is the ratio of the modulating signal frequency to the carrier's and called the "frequency ratio" of the pulse width modulation:

$$m_a = \frac{f_{control}}{f_{tri}} \qquad (19)\ [1].$$

This is another important indicator of modulated signal characteristics accompanied with the modulation index. These characteristic, like the spectrum content, will be explained in further chapters.

The pulse-width modulation techniques which are used to generate drive signals for DC-AC inverters differ from analog to digital systems. Methods used in analog applications can be adapted to digital platforms. This means that the following remarks which have been given for analog systems are also valid for digital ones as well. However, solely digital methods have peculiar features and approaches.

1.3.2.2.1 Analog Technique

In the essence of analog techniques, which are called the "natural sampling" in general, analog carrier and modulating signals are compared with the help of a

comparator which output PWM signals. Although this seems easy in implementation, it is also very sensitive towards small amplitude variations of the input signal because switching instants are determined by detecting exact intersections of continuous signal amplitudes [2]. In theory, this results in a frequency spectrum of output PWM signals with lower levels of harmonics, but the method itself is very error prone under the practical situation of noisy signals. It is not surprising to encounter glitches and spikes in the output waveforms.

1.3.2.2.1.1 PWM with bipolar switching for Full-Bridge

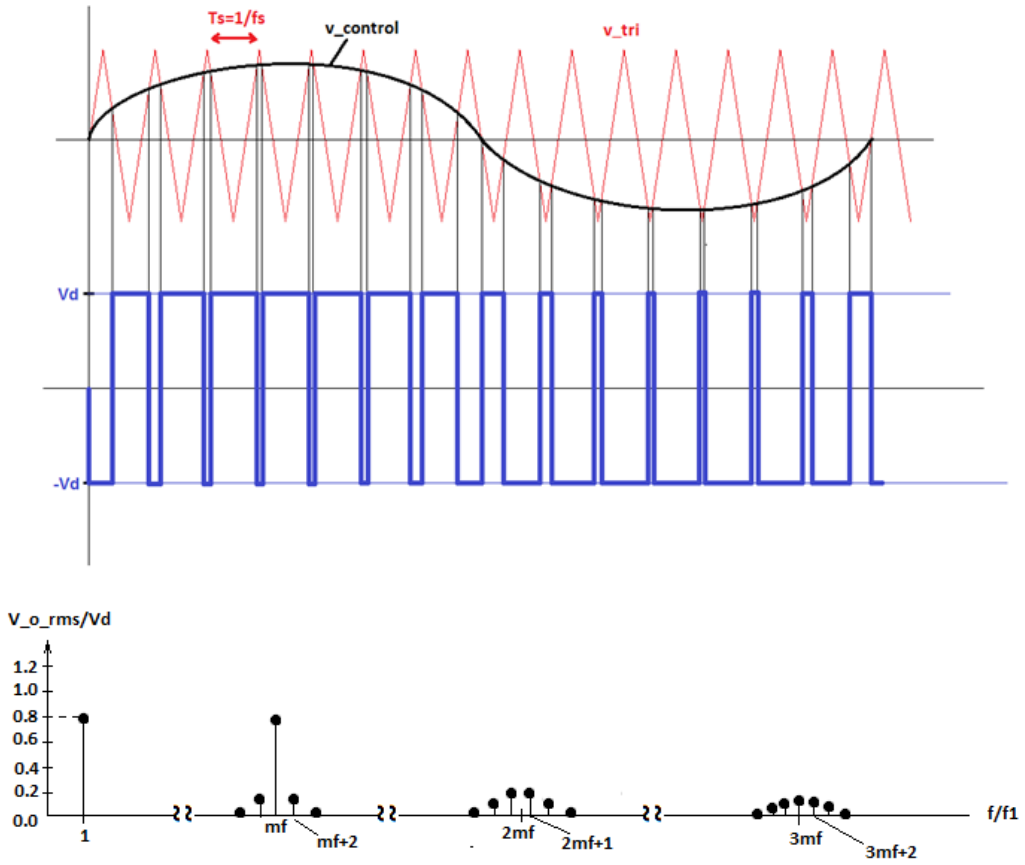

Figure 6 - Output Voltage and Its Spectrum of AC-DC inverter with Bipolar Sinusoidal PWM switching

"Figure 6" above shows the procedure of generating bipolar PWM signals for the DC-AC inversion purpose. The only difference from the DC-DC bipolar case is the control signal. Here, it is an AC signal which is a "sinusoid" in this. The third part of the same figure shows a section of the spectrum of the output voltage and it is obvious that the amplitude of the fundamental-frequency component "$(V_o)_{1\_peak}$" is equal to "m_a" times "V_d" [1]. This can be analyzed for the sinusoidal PWM by first assuming that "$v_{control}$" is constant during a switching period where "m_f" is provided to be very large [1]. Then the situation here is very similar to the one as in the DC-DC converter bipolar switching scheme, where the average output voltage (the output voltage averaged over switching period T_s) "V_o" depends on the ratio of the "$v_{control}$" to the "V_{tri}" for a given "V_d":

$$V_o = \frac{v_{control}}{V_{tri}} V_d \quad (v_{control} \leq V_{tri}) \equiv \ (m_a \leq 1) \qquad (20)\ [1].$$

It can also be assumed (though not necessarily) that the "$v_{control}$" signal changes very little during a switching period, which necessitates "m_f" to be large [1]. So, with the assumption made over the "$v_{control}$", the above equation indicates the variation of "the instantaneous average value" of the "v_o" from one switching instant to the following [1]. This "instantaneous average" is the fundamental component of the "v_o" [1]. If the "$v_{control}$" term at the above equation is substituted with the modulating signal peak value "$V_{control\_peak}$", the result will be the peak of the fundamental component of the "v_o", $(V_o)_1$:

$$(V_o)_1 = m_a V_d \qquad (21)\ [1].$$

This implies that in a sinusoidal PWM, the fundamental component of the output voltage changes linearly with the "m_a" (for $m_a \leq 1$) in other words with the input control signal level (modulating signal) as in linear amplifiers [1].The range of "$0 \leq m_a \leq 1$" is called the linear region [1].

At the output voltage spectrum, harmonics appear at the switching frequency, its multiples and also at their sidebands [1]. This generalization is valid for "m_a" values in between 0 and 1 [1]. Theoretically, the harmonic frequencies can be calculated as:

$$f_h = (jm_f \pm k)f_1 \qquad (22)$$

which can be turned into the harmonic order by dividing to the fundamental frequency [1]. Then, it corresponds to the "k^{th}" sideband of the harmonic which is centered at "j" times the frequency modulation ratio "m_f":

$$h = j(m_f) \pm k \qquad (23)$$

where "$h = 1$" means the fundamental component [1]. When the "j" is odd, the "k" may only takes even values; for even "j"s, the harmonics occurs only when the "k" is odd [1]. The reason for this will be explained later.

The equation, which is used to calculate the levels of the harmonic components at the output for sinusoidal PWM, is the following output voltage waveform equation (24):

$$v(t) = \frac{V_d m_a cos(nw_v t)}{2} + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \frac{2V_d J_n\left(\frac{m_a \pi m}{2}\right)}{\pi m} \sin\left(\frac{(m+n)\pi}{2}\right) \cos(nw_v t + mw_c t) \quad (24)$$

where the "w_v" is the angular frequency of the control signal and the "w_c" is the angular frequency of the carrier signal [3].

In "Table 1", the normalized harmonic levels "$\left(V_{o\_peak}\right)_h / V_d$" are given with respect to the amplitude modulation ratio "m_a" under the constraint of "$m_f \geq 9$" [1]. Harmonics up to "j=4" at the "equation (23)" with amplitude levels comparable to the fundamental component are given by using equation (24) [1].

ma	0.2	0.4	0.6	0.8	1.0
h					
1-Fundamental	0.2	0.4	0.6	0.8	1.0
mf	1.242	1.15	1.006	0.818	0.601
mf±2	0.016	0.061	0.131	0.22	0.318
mf±4					0.018
2mf±1	0.19	0.326	0.37	0.314	0.181
2mf±3		0.024	0.071	0.139	0.212
2mf±5				0.013	0.033
3mf	0.335	0.123	0.083	0.171	0.113
3mf±2	0.044	0.139	0.203	0.176	0.062
3mf±4		0.012	0.047	0.104	0.157
3mf±6				0.016	0.044
4mf±1	0.163	0.157	0.008	0.105	0.068
4mf±3	0.012	0.07	0.132	0.115	0.009
4mf±5			0.034	0.084	0.119
4mf±7				0.017	0.05

Table 1 - Normalized Harmonic Levels $\frac{(V_{o_{peak}})_h}{V_d}$

The "m_f" value should be chosen to be as an odd integer for the bipolar PWM to have an odd symmetry "$[f(-t) = -f(t)]$" as well as a half-wave symmetry "$\left[f(t) = -f\left(t + \frac{1}{2}T_1\right)\right]$" as it is the case at "Figure 6" plotted for the "m_f = 15" [1]. Therefore, no even harmonics occur at the spectrum of the output voltage signal "v_o" but only the odd ones do [1]. Thus, the "j" and the "k" values can be either odd or even oppositely for an odd "m_f" when only non-zero harmonic levels occur at odd harmonic orders.

For selecting the switching frequency, the relative ease in the filtering high frequency harmonics should be considered [1]. For this purpose, it is preferable to determine a high switching frequency as much as possible, with keeping in mind an important resulting drawback: switching losses which is the only significant dissipation source of the inverter which increase proportionally with the switching frequency "f_s" [1].

Therefore, in most applications, the switching frequency is chosen to be 20kHz, above the audible range [1].

The discussion of the switching frequency selection is carried on by analyzing situations under specific frequency ratio, "m_f", values. Arbitrarily; frequency ratios under the "21" are specified as small and above this level they are said to be large [1]. For the following evaluations, the amplitude modulation ratio "m_a" is assumed to be in the linear region, in between "0" and "1" [1].

- Small m_f ($m_f \leq 21$):

  1.Synchronous PWM: For the low values of the "m_f", the frequency of the carrier signal should be an integer multiple of the modulating signal's and the resulting PWM technique will be qualified as the synchronous PWM as shown in "Figure 6" [1]. The reason for the using synchronous PWM rather than the asynchronous (where the "m_f" is not an integer) is for avoiding from sub-harmonics which appears close to the fundamental component and should be avoided in most applications [1](book p. 208).

  2. Not to have the even orders of harmonics at the output waveforms as discussed previously, the "m_f" should be an odd integer for single-phase inverter applications with the bipolar switching PWM [1].

- Large m_f ($m_f > 21$):
  The sub-harmonic levels which are observed using the asynchronous PWM as the switching scheme are small at large values of the non-integer "m_f" [1]. Therefore, it is not inconvenient to use the asynchronous PWM with the large values of the "m_f"; as it is the case for constant carrier frequency applications where the modulating frequency varies [1].

- ***Over-modulation ($m_a \geq 1.0$):*** For linear region values of "$m_a \leq 1.0$", harmonics are shifted towards the switching frequency and its multiples with the drawback of the having fundamental component amplitude at the output

voltage not as great as desired [1]. As explained before, its amplitude varies linearly with the modulation index "m_a". Therefore, to increase the amplitude of the fundamental at the output further, the "m_a" can be increased beyond its linear range to be bigger than "1.0" [1]. The situation is described as the "over-modulation" [1]. However, this results in many more harmonics, even ones at the fundamental frequency multiples, to occur in the output voltage spectrum with respect to the case with "$m_a \leq 1.0$" [1].

Moreover, not only the fundamental component amplitude quits changing linearly with the modulation index as in the linear range but also it starts to be affected from the frequency ratio "m_f" additionally [1]. This is shown in "Figure 7" below:

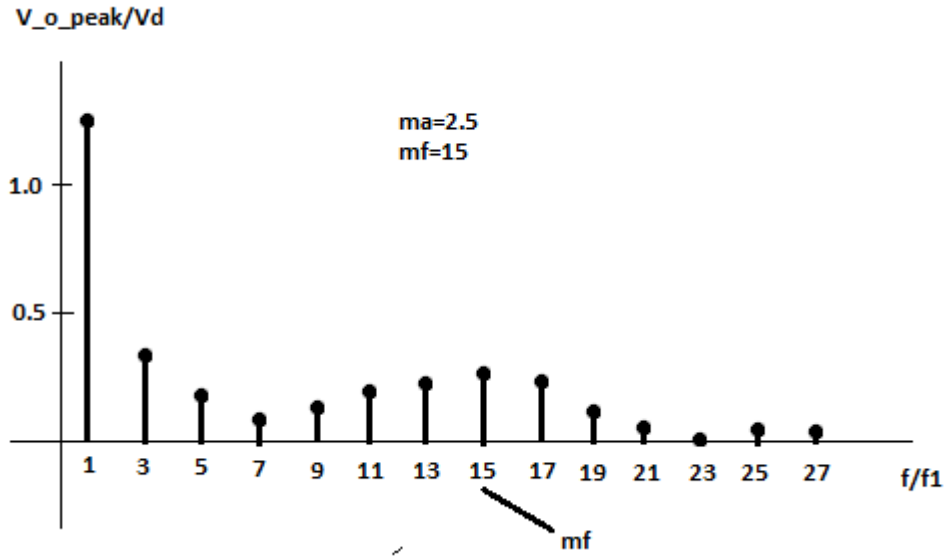

Figure 7 - Spectrum Performance of Over-modulation

As it can be seen in "Figure 8" below, increasing the "m_a" after a certain value outside the over-modulation range does not increase the fundamental amplitude any more. Since drive signals deteriorate from a PWM waveform and turns into a square wave with the frequency of the modulating signal [1].

As a result, the normalized fundamental component amplitude saturates to "$\frac{4}{\pi}$" for the "m_f=15" [1].

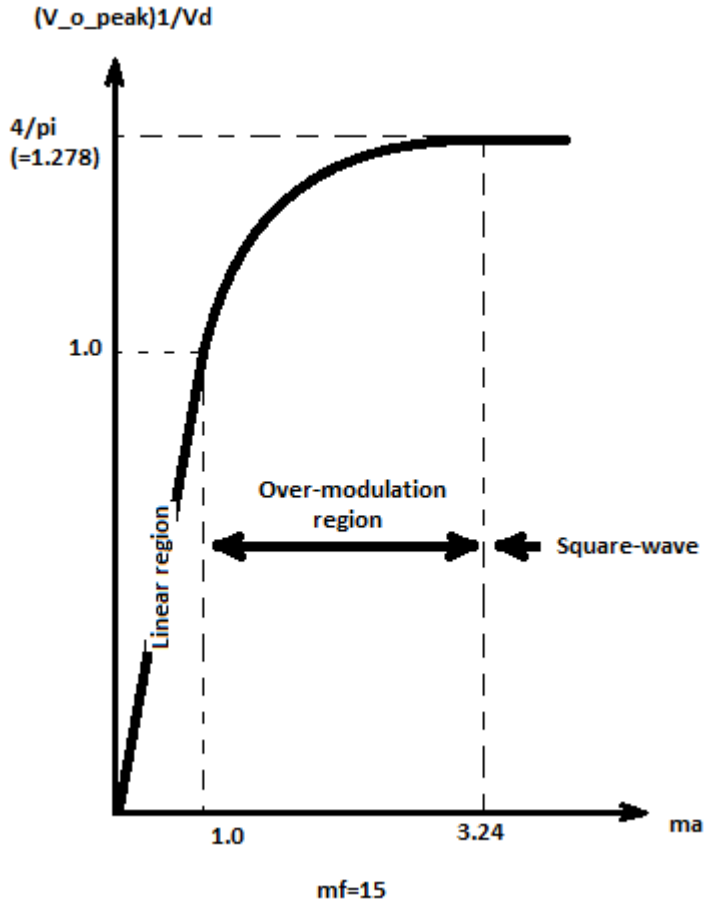

Figure 8 - Fundamental Component Variation With 'ma'

1.3.2.2.1.2 PWM with unipolar switching (double phase)

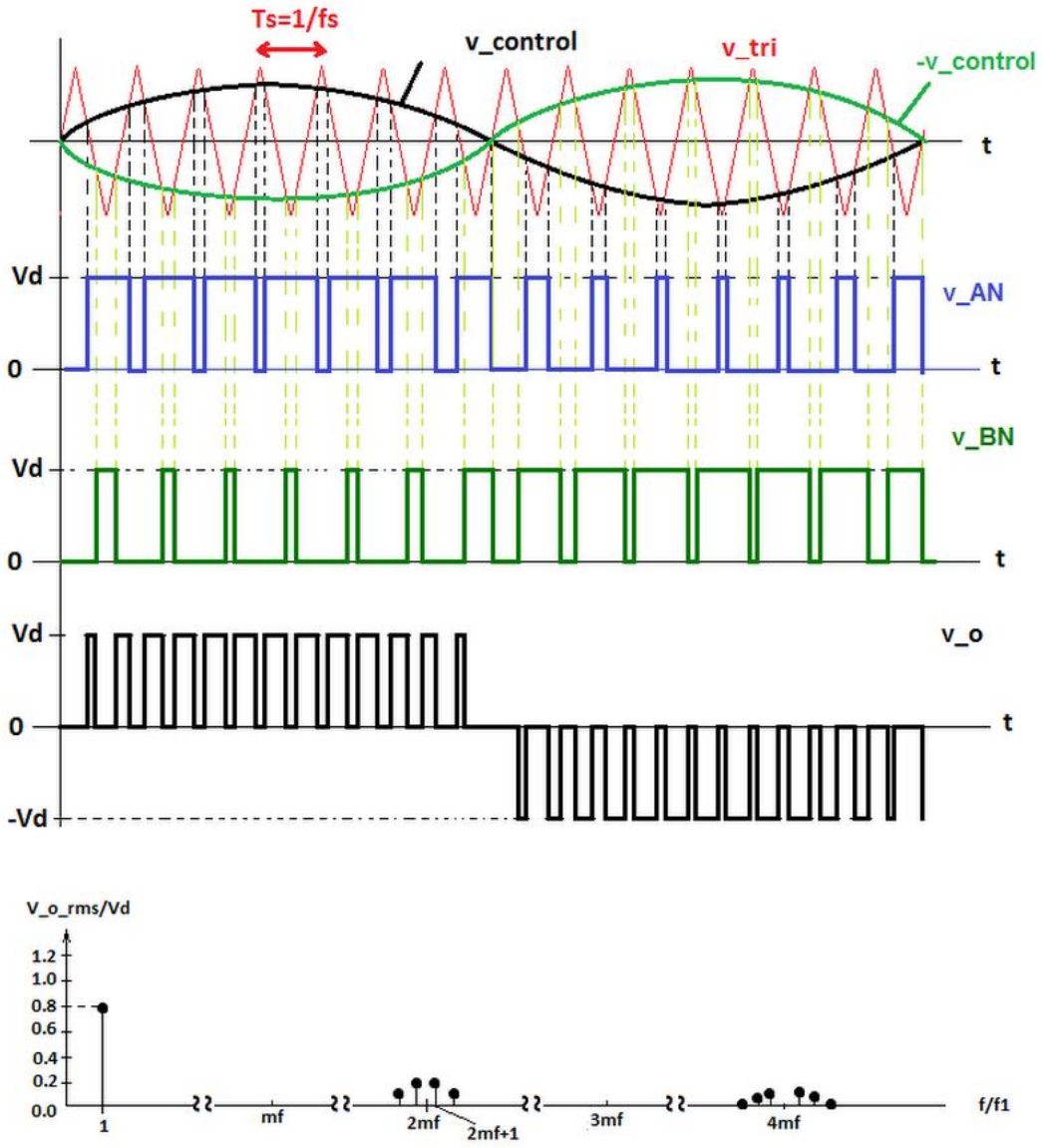

Figure 9 - DC-AC Uni-polar PWM Switching

As mentioned before, the unipolar PWM switching scheme suggests only the switches at the same arm of the full-bridge work complementarily. In this case, PWM signals are created from a modulating signal and its 180^{o} phase shifted version for controlling the legs A and B separately [1]. The switching instants which are shown in "Figure 9" are determined as follows:

$v_{control} > v_{tri}$: T_{A+} on and $V_{AN} = V_d$

$v_{control} < v_{tri}$: T_{A-} on and $V_{AN} = 0$

$(-v_{control}) > v_{tri}$: T_{B+} on and $V_{BN} = V_d$

$(-v_{control}) < v_{tri}$: T_{B-} on and $V_{BN} = 0$ [1]

For this switching scheme there are not any switch couples acts in the same way as in the bipolar case. Then, there occur four combinations of switch states rather than two. Except the simultaneous conduction and the non-conduction states for the switches at the same arm, every other state is valid as below:

T_{A+} T_{B-} on: $v_{AN} = V_d$, $v_{BN}=0$; $v_o=V_d$

T_{A-} T_{B+} on: $v_{AN} = 0$, $v_{BN}= V_d$; $v_o=-V_d$

T_{A+} T_{B+} on: $v_{AN} = V_d$, $v_{BN}= V_d$; $v_o=0$

T_{A-} T_{B-} on: $v_{AN} = 0$, $v_{BN}=0$; $v_o=0$

[1].

The output voltage can has three voltage levels as given above and the only transitions are either between the zero and the "$+V_d$" or between the zero and the "$–V_d$" voltage levels [1]. This is why this type of PWM technique is called the unipolar voltage switching [1]. The crucial superiority of this scheme over the bipolar switching is its "effectively" doubling the switching frequency in the output waveforms [1]. Thus, the switching harmonics in the corresponding signal spectrums only occur at the even multiples of the switching frequency and their sidebands. [1].

If the frequency modulation ratio "m_f" is selected as an even integer (odd for the PWM with bipolar switching), the harmonics at the exact switching frequency multiples are further disappeared in a single-phase inverter [1]. The fundamental components of the output terminal voltages, the "v_{AN}" and the "V_{BN}" are displaced by 180^o from each other's [1]. Therefore, the harmonic components of these signals

at the switching frequency are in-phase ((Φ_{AN}- Φ_{BN} =180^o) * mf =0^o, because the "m_f" is chosen even) [1]. As a result, the odd number order harmonics of the switching frequency will not appear in the output voltage, "v_o= v_{AN} - v_{BN}", spectrum [1].

For the unipolar voltage switching, the harmonic order "h" is:

$$h = j(2m_f) \pm k \qquad (25)$$

the order of the harmonics which occur at the multiples of the "2m_f" and its sidebands [1]. Additionally, because the "h" is odd, the "k" can only have odd values for the harmonic order to be odd [1].

If a comparison between the unipolar and the bipolar voltage switching should be made; then it can be said that, in both of the methods, the voltage levels of the fundamental-frequency component of the produced PWM signals are same for the use of equal "ma" values [1]. However, in the unipolar voltage switching with proper selection of the "mf", no harmonic components occur at odd multiples of "mf" and their sidebands and results in a remarkable reduction in the harmonic content [1].

1.3.2.2.2 Digital Techniques

For digital systems, as well as the natural sampling is an option with proper precautions taken, the most basic digital method of the PWM generation is the "uniform sampling". A similar trouble arises in the digital case of the "natural sampling" as in the analog one and it is caused by the unwanted amplitude variations at the modulating and carrier signals. This time the discrete structure of the signals makes it hard to compare them directly when they are sampled at different rates. As a result, glitches may occur at produced PWM signals. For avoiding this, one solution is to sample the modulating signal with the carrier signal frequency and make the comparison afterwards [4]. This corresponds to the sampling method of the "uniform sampling" [4]. However, this causes to miss the exact intersections of two signals. Therefore, erroneous pulse widths as well as increments in harmonics levels will occur as differently from the natural sampling [4]. The theoretical comparison of

these two methods can be seen in “Figure 10” below. If the PWM signals are inspected carefully, it is seen that their widths do differ.

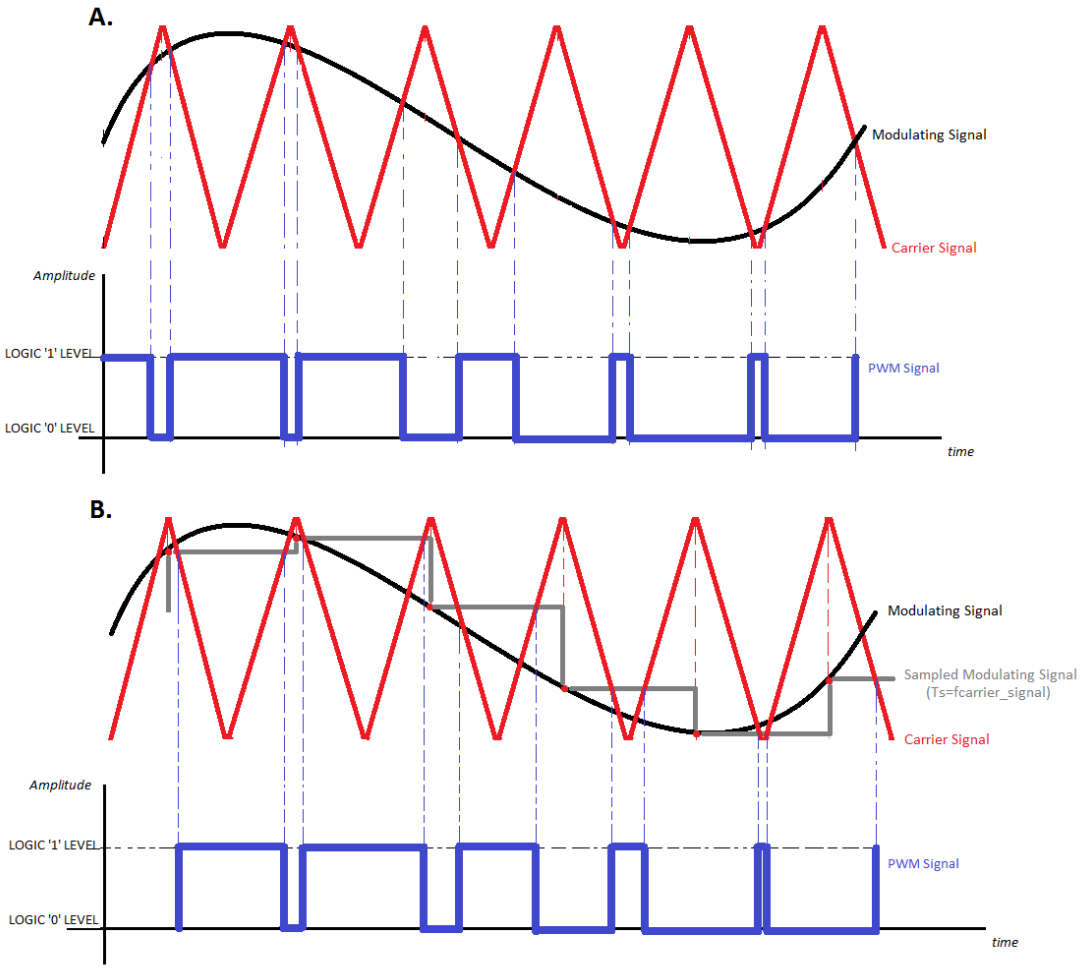

Figure 10 - A. Symmetrical Natural Sampling, B. Uniform Sampling

1.3.2.2.2.1 Asymmetrical and Symmetrical Uniform Sampling

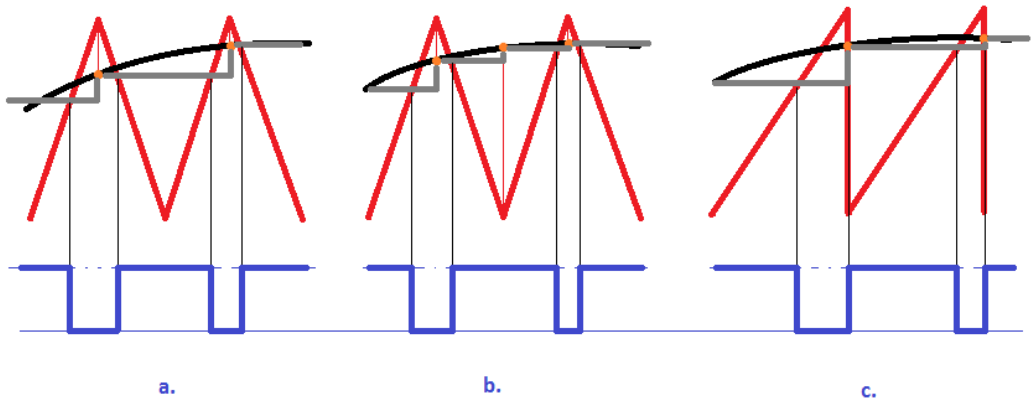

Figure 11 - Uniform Sampling Types

In "Figure 11" above, uniform sampling types are illustrated. These are separated into two as the "single sided" (c.) and the "double sided" (a., b.) with respect to the carrier signal shape. For the single sided uniform sampling, the modulating signal is compared with a saw-tooth type carrier signal [4]. This causes only the one of the two switching edges in each switching periods to be determined with the comparison process [4]. The other is just at the instant when the corresponding switching period ends [4]. The shape of the carrier waveform is triangular in the case of the double sided type which requires two comparison operations for deciding the switching instants [4]. This method has the two different implementations of using either one or two samples for determining the switching edges at a switching period [4]. The method is called the "asynchronous uniform sampling" in the case of the use of two samples. This implies the modulating signal should be sampled with the rate of twice the carrier (switching) frequency. The synchronous implementation involves the use of one sample and the modulating signal which is sampled at the switching rate.

The output voltage waveform of the asymmetrical uniform sampling of a sinusoid is as the following equation suggests:

$$f(t) = \sum_{n=1}^{\infty} \frac{2V_d J_n\left(\frac{m_a n\pi w_v}{2w_c}\right)}{\frac{n\pi w_v}{w_c}} \sin\left(\frac{n\pi}{2}\right) \cos\left(nw_v t - \frac{n\pi w_v}{2w_c}\right) + \ldots$$

$$\ldots \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2V_d J_n\left(\frac{m_a \pi}{2}\left(m+\frac{nw_v}{w_c}\right)\right)}{\pi\left(m+\frac{nw_v}{w_c}\right)} \sin\left(\frac{(m+n)\pi}{2}\right) \cos\left(nw_v t + mw_c t - \frac{n\pi w_v}{2w_c}\right) \quad (26)[3].$$

The PWM signal generation is easy and practical with digital platforms. Therefore, there are many different digital modulation techniques with different features [5]. One is the optimizing PWM signals of which switching angles are pre-determined with minimization algorithms for lowering harmonic levels in the output waveforms [5]. The "enhanced uniform PWM", which will be analyzed following, is the one of these examples among many digital PWM application methods.

1.3.2.2.2.2 Enhanced Uniform PWM – Interpolation (An Alternative Digital Sampling Process)

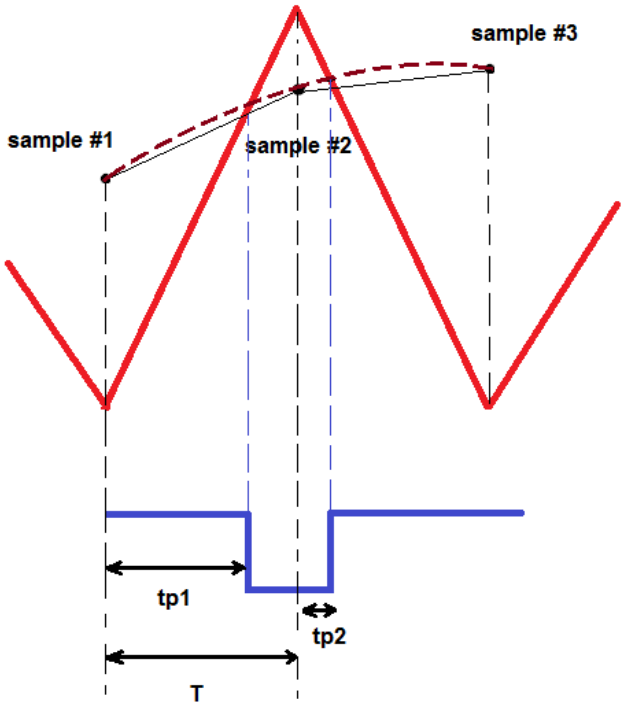

Figure 12 - Linear Interpolated Natural Sampling

For producing PWM signals digitally, one proposed solution which emulates the natural sampling is called the "Linear Interpolated Natural Sampling" [3]. This method interpolates the levels of the two consecutive samples of the modulating signal. So, the switching instants are determined more precisely as it is illustrated in "Figure 12" above [3].

The switching time instants which are shown in the figure above the "t_{p1}" and the "t_{p2}" can be calculated by using the amplitude values of the samples "S_1","S_2" and "S_3":

$$t_{p1} = \frac{S_1 + 1}{2 - (S_2 - S_1)}\, T \qquad (27)$$

$$t_{p2} = \frac{1 - S_2}{2 - (S_2 - S_3)}\, T \qquad (28)$$

where the "T" is the sampling interval which is equal to the half of the carrier signal period [3].

This type of modification improves the uniform PWM by lowering the harmonics levels in the output voltage spectrum [3]. However, their magnitudes do not decay rapidly with the increasing carrier frequency [3] .

For improving this method even more, a weight coefficient of the "ϵ" in the interval from "0" to "1" can be introduced to modify switching instants [3]. It changes the effect of the sample which determines the following switching instant in a switching period [3]. The pulse edge instants are now calculated as follows:

$$t_{p1} = \frac{S_1 + 1}{2 - (1 - \epsilon)(S_2 - S_1)}\, T \qquad (29)$$

$$t_{p2} = \frac{1 - S_2}{2 - (1 - \epsilon)(S_2 - S_3)}\, T \qquad (30)\ [3].$$

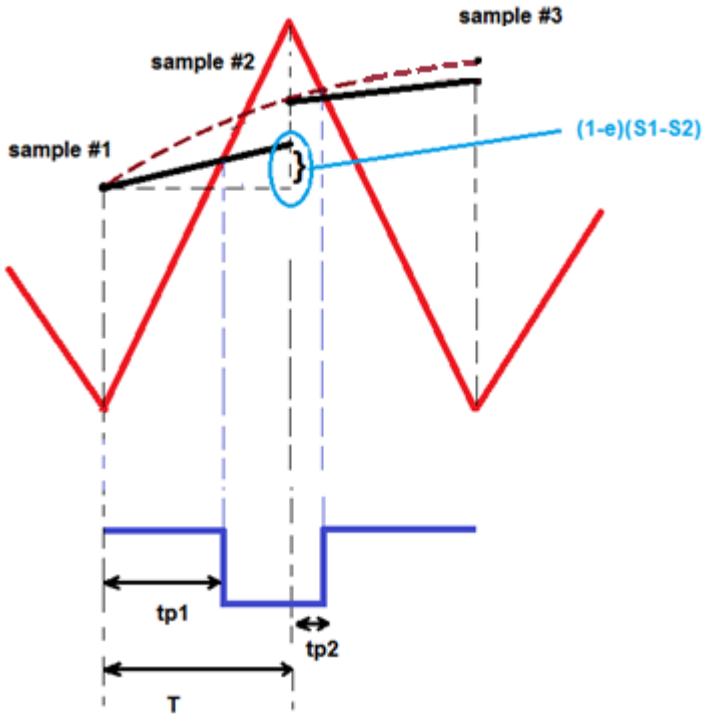

Figure 13 - Enhanced Uniform Sampling

The function of the weight "ϵ" is illustrated in "Figure 13" above. It is deduced that when the "$\epsilon = 0$", the method turns out to be the linear interpolated natural sampling [3]. Moreover, setting the "ϵ" equals to "1" will result with the uniform sampling [3].

The analysis of the spectrum of the enhanced sampling method shows the magnitude of the third harmonic distortion is a function of the coefficient "ϵ" [3]. The minimum distortion caused by this third harmonic is observed for the "ϵ" to be around "0.35" and this value does not depend on the signal or carrier frequencies [3]. With the use of this new method, it results in that, up to a 30dB decrease can be reached at the third harmonic level with respect to the conventional uniform sampling [3].

1.3.2.3 *Dead-Time for Single Phase Inverters*

In practice, since the switches used at the bridge have finite turn-off and turn-on times, the switching timings will be updated [1]. The instants of transistors' going into the conduction state will be delayed for a significant duration of time as can be seen in "Figure 14" [1]. This time durations which are called "dead-time", "t_{Δ}",

should be chosen conservatively to prevent the phenomena called “shoot through” [1]. This refers to the cross-conduction when DC supply is shorted through the arms of the bridge [1]. The amount of the dead-time is advised to be chosen a few microseconds for the fast responding MOSFETs [1].

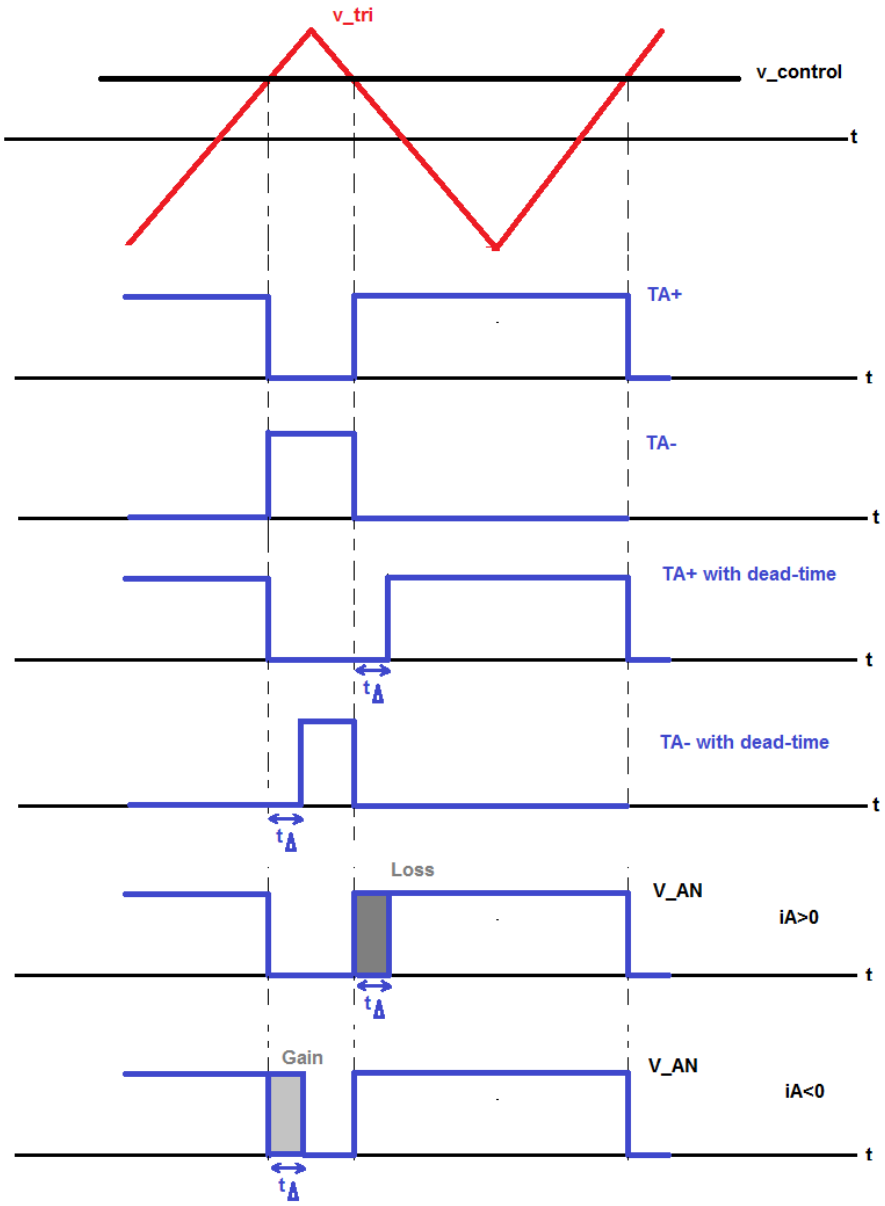

Figure 14 - Dead-time Effect on the Output Voltage Level with Load Current Direction

During the dead-time, the switches of the same arm are in non-conducting state, and the output terminal voltage levels "v_{AN}" or "v_{BN}" are determined according to the direction of the output load current "i_A" as shown in the figure above [1]. For the single phase inverters, the voltage level of the output terminal "A" becomes "V_d" when the "$i_A<0$" and "0" for the "$i_A<0$" because of the path which is provided by the conducting fly-back diodes for the load current. If the ideal voltage waveform of the output terminal "A", the "v_{AN}", in which no dead-time is imposed is subtracted from the actual waveform with the dead time, it results in an output voltage error function:

$$v_{\in} = (v_{AN})_{ideal} - (v_{AN})_{actual} \qquad (31)\ [1].$$

The variations (defined as a drop if positive) at the output voltage level because of "t_Δ" and the average voltage error over a switching period can be calculated as follows:

$$\Delta V_{AN} = \begin{cases} +\frac{t_\Delta}{Ts} V_d, & i_A > 0 \\ -\frac{t_\Delta}{Ts} V_d, & i_A < 0 \end{cases} \qquad (34)\ [1].$$

The "ΔV_{AN}" only depends on the direction of the output current but not on its magnitude as can be seen in the equation above [1]. Moreover, it is deduced from the same equation that the "ΔV_{AN}" is proportional to the dead-time duration "t_Δ" and the switching frequency "f_s" [1]. This is interpreted as the necessity of using fast responding devices which can operate with small dead-time durations in bridge inverter applications which require fast switching (high "f_s") [1].

The same analysis of the output voltage level variations can be made for the output terminal "B" as well, with considering "$i_A = i_B$":

$$\Delta V_{BN} = \begin{cases} -\frac{t_\Delta}{Ts} V_d, & i_A > 0 \\ +\frac{t_\Delta}{Ts} V_d, & i_A < 0 \end{cases} \qquad (35)\ [1].$$

Because "$v_o = v_{AN} - v_{BN}$" and "$i_o = i_A$", the instantaneous average value of the output error voltage over one switching period "T_s" is:

$$\Delta V_o = \begin{cases} +\frac{2t_\Delta}{Ts} V_d, & i_o > 0 \\ -\frac{2t_\Delta}{Ts} V_d, & i_o < 0 \end{cases} \qquad (36)\ [1].$$

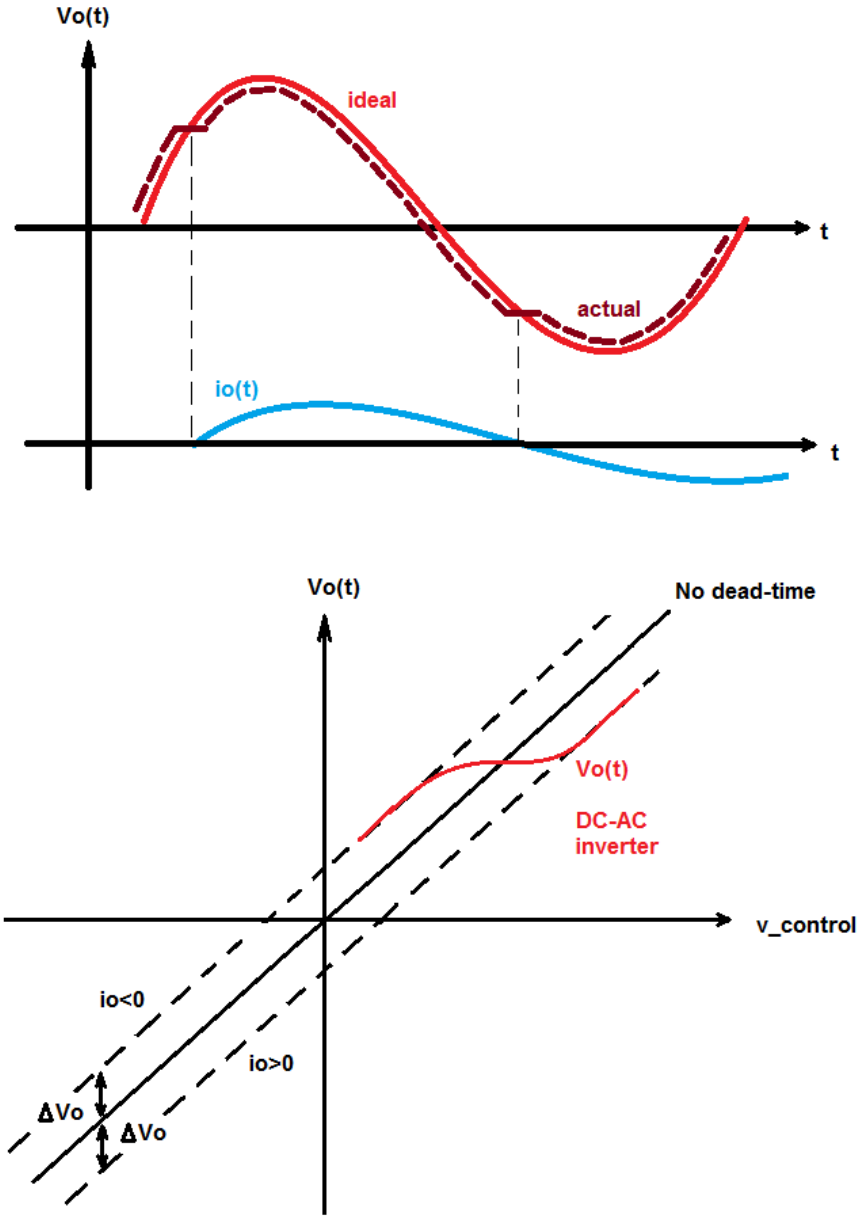

Figure 15 - Output Voltage Dead-Time Variation At Zero Crossings of The Output

For the application of a full-bridge with the single phase sinusoidal PWM, the instantaneous average output voltage "$V_o(t)$" is given in the "Figure 15" above. The dead-time causes an average voltage distortion in the output when the output current change its direction [1]. This can be modeled as seen in the same figure above and will results in low order fundamental frequency harmonics to appear: like third, fifth, seventh, and so forth [1].

1.3.2.3.1 The Analysis of Dead-Time Effect in PWM Inverter

It is discussed following that the effect of the dead-time on the output voltage spectrum of a full-bridge inverter in detail. A decrement at the fundamental component level as well as an increase in the low-order harmonics levels is observed [6]**.** It is also shown that these effects of the dead-time duration are highly related with the load power factor [6].

As mentioned before, the output voltage during the dead-time is determined by the output load current direction and it opposes the current flow in either direction [6]. In other words, there occurs such a voltage alteration which makes the current magnitude to be smaller than it should [6]**.**

The following assumptions are made for the analysis:

1-The switching frequency is sufficiently large in comparison with the fundamental frequency,

2-The output current is nearly sinusoidal [6]**.**

These assumptions make possible to calculate the cumulative effect of the dead –time durations, "Td", by averaging the voltage variations, which occur in these time intervals, over the fundamental period of the output current [6]**.**

At the each switching period, the variation at the output voltage "Δe" is calculated by

$$\Delta e = T_d V_d \qquad (37)$$

and its average, "ΔV", over a half cycle of the inverter output current is:

$$\Delta V = \frac{(M/2)\Delta e}{T/2} = \frac{MT_d}{T} V_d \quad (38)$$

where the "M" is the number of switching per one fundamental cycle and "T" is the fundamental component period [6].

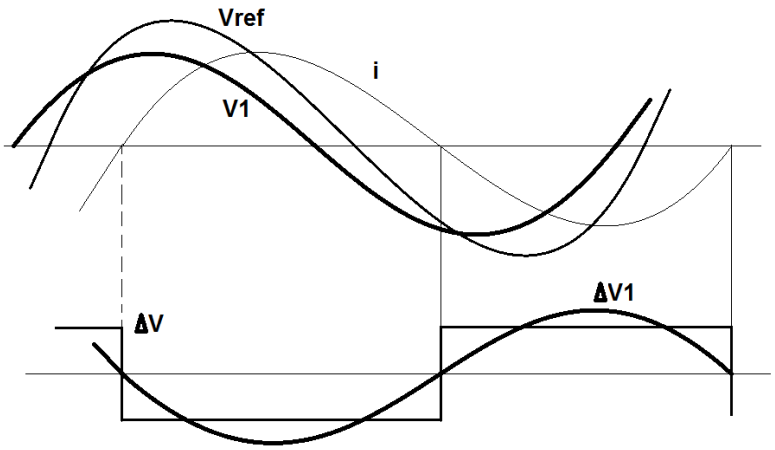

Figure 16 - Dead Time Effect On Fundamental Output Voltage

In "Figure 16" above, the "v_{ref}" is the output voltage fundamental component of the inverter in the case of no dead-time effect is ever involved. Additionally, it is assumed that the load is inductive and the current lags the "v_{ref}" with the "Φ' " [6]. The average voltage deviation over an entire fundamental cycle can be treated as the square wave "Δv" shown in the figure above [6]. It is shifted 180^o in phase with respect to the output current [6]. The "Δv_1" is the fundamental component of that representative voltage deviation square wave and its RMS value "ΔV_1" is calculated as:

$$\Delta V_1 = \frac{2\sqrt{2}}{\pi} \Delta V \qquad (39) \text{ [6].}$$

In the pre-determined assumption, it is said that the output current is nearly sinusoidal. So its harmonic components are neglected; and the phase difference "Φ" among the "v_1" and the "I" is defined as the load fundamental power factor [6].

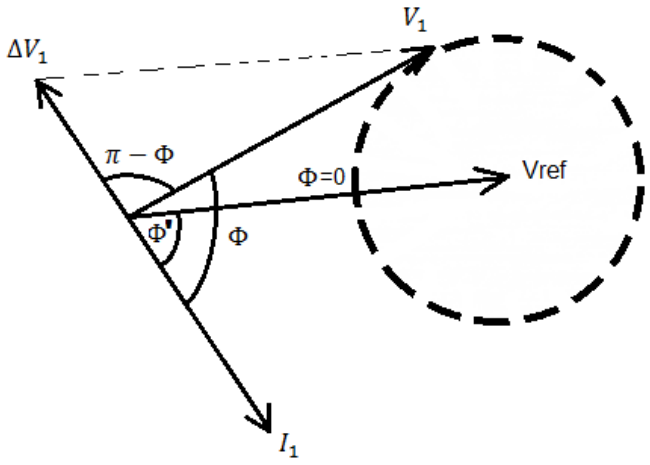

Figure 17 - Phasor Representation of Dead Time Effect

In "Figure 17" above, a phasor diagram is provided which shows that the "ΔV_1" and the output current has a 180^o phase difference between each other's [6]. The fundamental component of the output voltage with the dead-time imposed on, "V_1", leads the current with a phase angle of "Φ" [6]. Therefore, a phase difference of "$\pi - \Phi$" appears between the "ΔV_1" and the "V_1" [6]. Using the trigonometrical identity for the triangles which has sides of the "ΔV_1" and the "V_1", an equation for finding the unknown variable "V_1" can be derived:

$$V_{ref}^2 = \Delta V_1^2 + V_1^2 - 2\Delta V_1 V_1 \cos(\pi - \Phi) \qquad (40)$$

where the "V_{ref}", the "ΔV_1" and the "V_1" are the RMS values of the "v_{ref}", the "Δv_1" and the "v_1" [6]. Then the solution for the "V_1" is:

$$V_1 = -\Delta V_1 cos\Phi + \sqrt{V_{ref}^2 - (\Delta V_1 sin\Phi)^2} \qquad (41)\ [6].$$

A normalized form with respect to the "V_{ref}" is:

$$\frac{V_1}{V_{ref}} = -\eta cos\Phi + \sqrt{1-\eta^2 \sin^2 \Phi} \qquad (42)$$

where the "$\eta = \frac{\Delta V_1}{V_{ref}}$" is the normalized voltage deviation which is observed at the fundamental component of the output voltage waveform and is in the range of "0< η<1" [6].

The RMS value of the "V_{ref}" is:

$$V_{ref} = \frac{\delta V_d}{2\sqrt{2}} \qquad (43)$$

where "δ" is the modulation index [6]. Then the normalized voltage deviation can be written in terms of the "M", the "T_d" and the "δ" as:

$$\eta = \frac{8}{\pi}\frac{MT_d}{T}\frac{1}{\delta} \qquad (44)\ [6].$$

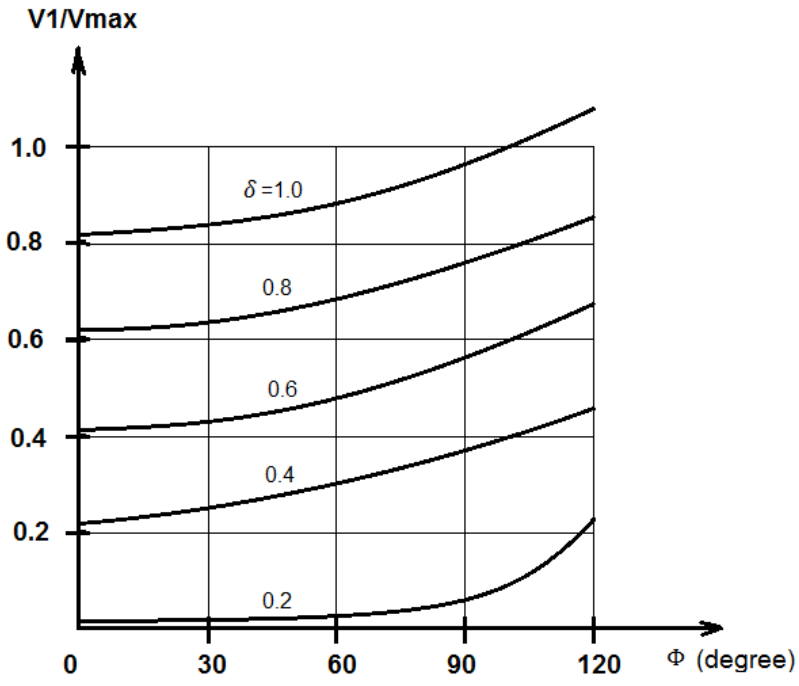

Figure 18 - Dead-time Effect with Respect to Load Power Factor Angle

As pointed before, the power factor does affect the output fundamental voltage level. It can be seen in "Figure 18" above that as the power factor increases, the voltage deviation becomes smaller and the decrement in fundamental current component will be less [6]. The "$V_{\max}(= V_d/2\sqrt{2})$" is the ideal value of the output voltage when modulation index is unity [6].

1.3.2.3.2 Harmonic distortion of Dead-Time Effect in PWM inverter output waveforms

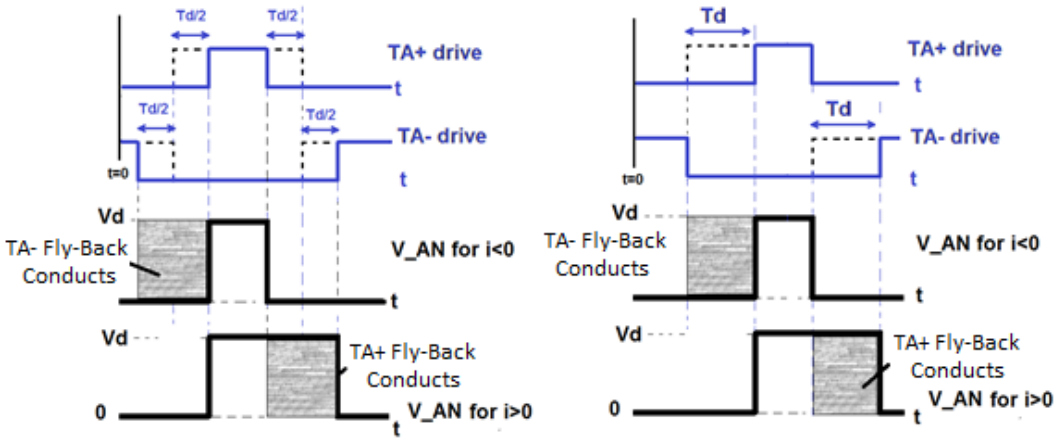

Figure 19 - Dead-time Insertion Method

The dead-time durations are inserted into the drive signals in such a way that; the "turn-off" instants are advanced and the "turn-on" instants are delayed for the half of the dead-time duration "$td/2$" from the ideal instants [7]. This result in the total dead-time period of the "td" as can be seen in the first part of the "Figure 19" above[7]. In the second part of the same figure the conventional way of the dead-time insertion is illustrated. The method depends on delaying only the turn-on switching edges for the exact amount of the dead-time [7]. Therefore the switching edges will be shifted right in each switching period with respect to the first method proposes [7]. The amount of this duration is the half of the dead-time "$td/2$" [7]. As a result the harmonic levels at the switching frequency multiples and at its sidebands will be differ because of the ruining the pulse symmetries in such a way [7]. However, the

low-order harmonics of the fundamental frequency which are considered important mainly will be substantially unchanged [7].

1.3.2.3.2.1 Method of analysis

The analysis of the spectrum is made for the output waveform which is produced with the asymmetrical double-edge uniform sampling pulse-width-modulation is the PWM [7]**.** This waveform consists of "p" pulses with the characteristics shown in the "Figure 20" below [7]. Then the amplitude of the "n_{th}" harmonic "A_{nk}" which is originated by the "k_{th}" pulse can be calculated as follows:

$$A_{nk} = \frac{jV_s}{2\pi n}\{\exp(-jn\delta_{2k}) - \exp(jn\delta_{1k}) + jsin\, n\,\Delta/2\, \exp(-jn\alpha_k)\} \qquad (45)$$

where the "V_s" is the supply voltage, the "Δ" is the switching period, the "α_k" is the position within the fundamental period of the midpoint of the "kth" pulse [7]. The "β_{1k}" and the "β_{2k}" are the normalized half-widths of the "k_{th}" pulse; the "δ_{1k}" and the "δ_{2k}" are the ideal half-widths of the same "k_{th}" pulse and can be calculated by:

$$\beta_{1k} = M\sin(\alpha_k - \delta_0) = \frac{\delta_{1k} - \delta_0}{\delta_0} \qquad (46)$$

$$\beta_{2k} = M\sin(\alpha_k + \delta_0) = \frac{\delta_{2k} - \delta_0}{\delta_0} \qquad (47)\ [7].$$

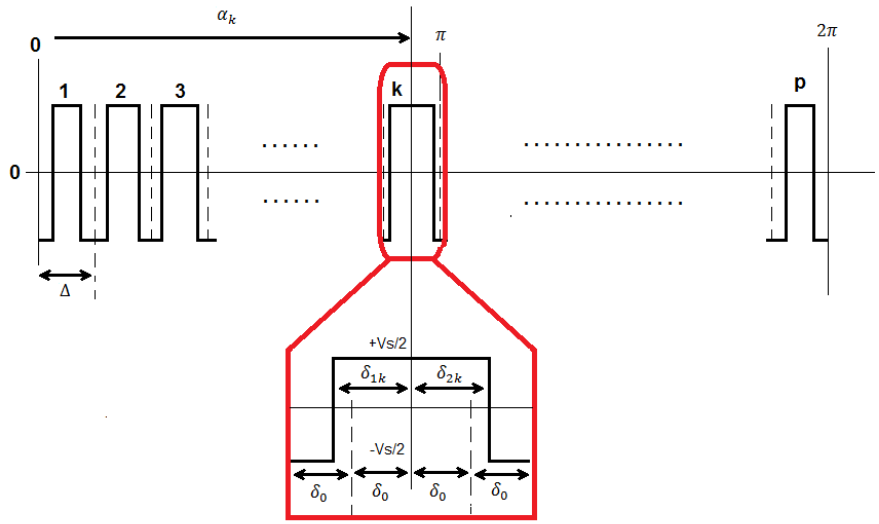

Figure 20 – The "kth" Pulse Characteristics

The "n_{th}" harmonic amplitude level "A_n" is calculated by considering the contributions of all "p" pulses in the fundamental period:

$$A_n = \sum_{k=1}^{P} A_{nk} \qquad (48)$$ [7].

The dead-time changes the values of the "δ_{1k}" and the "δ_{2k}" into the "δ'_{1k}" and the "δ'_{2k}" with the employment of the method of the dead-time insertion as proposed in the first part of the "Figure 19" as:

- For the positive load current direction:
  - $\delta'_{1k} = \delta_{1k} - t_d/2 \qquad (49)$
  - $\delta'_{2k} = \delta_{2k} - t_d/2 \qquad (50)$
- For the negative load current direction:
  - $\delta'_{1k} = \delta_{1k} + t_d/2 \qquad (51)$
  - $\delta'_{2k} = \delta_{2k} + t_d/2 \qquad (52)$ [7]

For both of the current directions, these half cycles can be found by calculating "Φ′" as stated in the section "1.2.3.2-The Analysis of Dead-Time Effect in PWM Inverter " [7].

"Figure 21" and "Figure 22" below show that the levels of the low-order harmonics at the output voltage waveforms increase linearly with dead time duration [7]. For example, the calculated 5th harmonic level increases from 1.1% to 5.5% while the dead time duration increases from 5 to 25 us for the corresponding switching period [7].

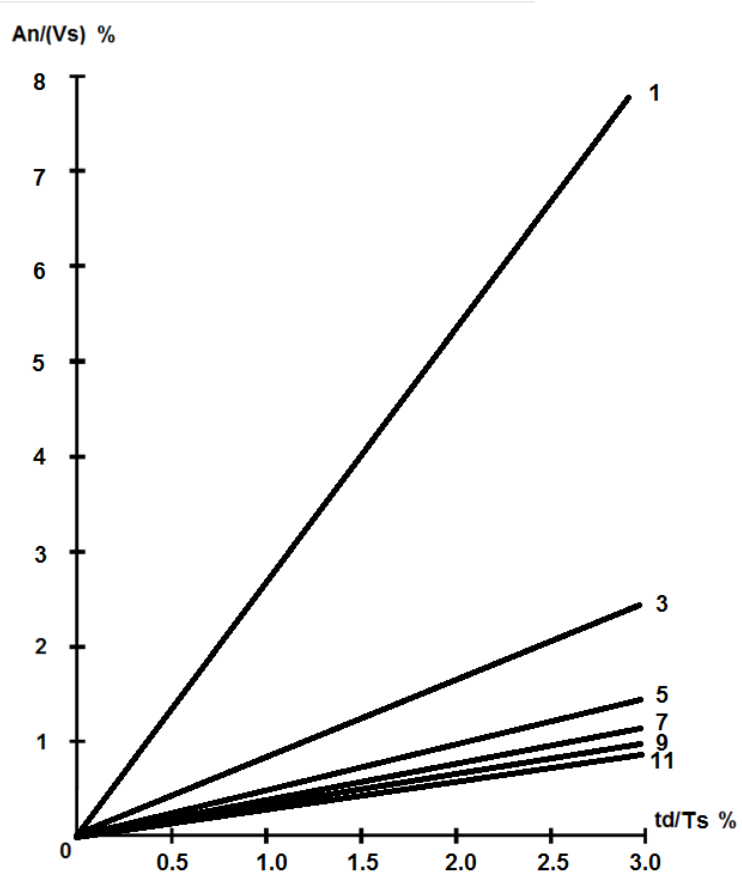

Figure 21 - Low-order Odd Harmonics vs. The Ratio of The Dead-time Duration to The Switching Period

In "Figure 21" above, the relative amplitude change (with respect to the supply voltage level) in the fundamental component can be seen with respect to the amounts of dead-time durations. Therefore, it is interpreted from the same graph that the net amplitude level of the fundamental component at the output voltage waveform decreases linearly while the increasing dead time durations [7].

"Figure 21" also shows that the low-order odd harmonic amplitudes vary linearly with the ratio of the dead-time duration to the switching period "td/Ts" [7]. Therefore, this implies that harmonic levels will not change for the cases of the "td" and the "Ts" values change as long as their ratio stays the same [7]. Then the odd low-order harmonic content of the cases of 10us dead time with a switching frequency of 2 kHz and a dead time of 1us with a switching frequency of 20 kHz will be same [7].

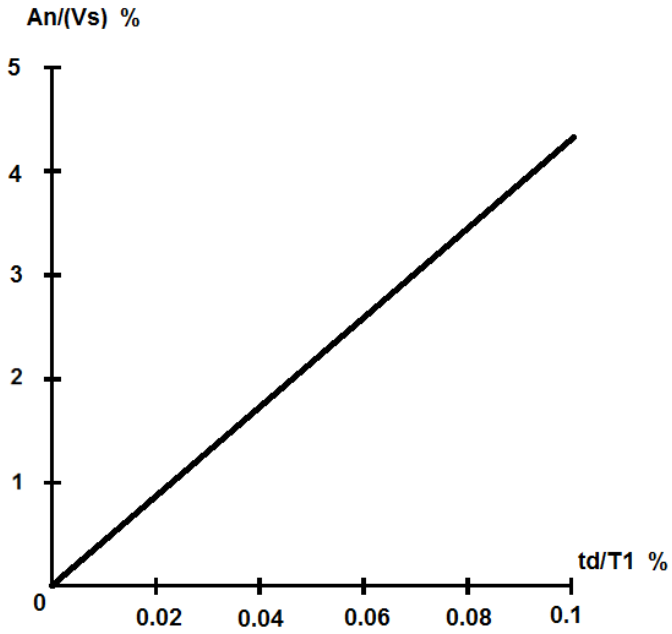

Figure 22 - Low-order Even Harmonics vs. The Ratio of the Dead-time Duration to Fundamental Period for Even Frequency Ratios

The amplitude levels of the even order fundamental frequency harmonics in the output voltage varies with the ratio of the dead-time duration to the fundamental period “td/T1” [7]. It can also be deduced that these levels of the even harmonics do not depend on the switching frequency directly [7].

Chapter 2

Design of the System

2.1 System Layout

The overall system layout is like the one in “Figure 23” below. As for the hardware, an H-bridge has been designed for the driver circuitry. However, before the design was finalized, some alternative designs were tried for this power stage. A detailed analysis is provided in “Appendix A” and the reasons are given in very same section why the alternative design was not successful.

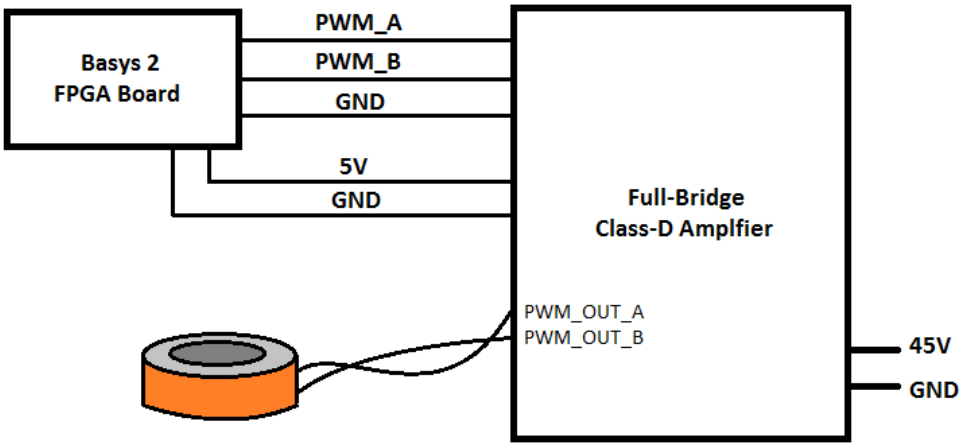

Figure 23 - System Layout

As previously mentioned, a BASYS2 FPGA demo board is used for producing PWM signals. The signals “PWM_A” and “PWM_B” are the complementary PWM signals. The “PWM_A” is the reference for determining the “duty cycle” value. These signals are in 3.3V voltage level and are increased to the 5V level with the help of a simple

inverter IC supplied with 5V. This is necessary for the MOS gate driver ICs' to be able to input signals. Driver ICs are also required to increase PWM signals to full-bridge network supply voltages. For high side transistors to be able to conduct, their gate voltages should be higher than their source voltages which should be either ground reference or circuit supply level. The "PWM_OUT_A" and the "PWM_OUT_B" are the final output voltages of the full-bridge class-D amplifier outputs'. They should be either ground reference or 45V amplifier supply voltage.

2.2 Driver Circuitry – Full Bridge (H-Bridge)

Class-D type amplifiers are very flexible for different operations; by varying drive signals, hardware becomes either a DC-DC converter or a DC-AC inverter [5]. Because these drive signals are mostly produced by microprocessors or controllers; therefore, the operation of the circuitry is a matter of changing of a few lines of the software without altering the hardware [5].

The design of the processor circuitries and codes are extra tasks which the alternative design requires none of it. However, it can be interpreted as a pay for overcoming the troubles which the alternative circuit structure has. This alternative circuit structure is widely used and its responses are known from the many studies that have been done on this. Additionally, the structure itself is simple and not as big as the first option's Class-A stage. Power transistors are driven as switches by either turning on or off at their SAT regions, as a result only significant power will be dissipated at the switching instants [8]**.** Therefore, this provides high power efficiency greater than 90% for a large output swing in case of a high modulation index [9]. The reason behind this is the small "SAT" region drain-to-source resistance with respect to the power transistor's "R_{DS}" of the first option which is used in the active region. This saves designers from using bulky coolers and concern about thermal stability. Although it seems efficient, an extra electrical energy loss occurs from transistors switching as mentioned. However, this will not negatively impact high efficiency; losses are much less than the previous case.

The digital class-D type amplifiers have also astonishingly linear responses and are very immune against noise**.** Moreover, the circuitry has a wide operation band, as from DC in DC-DC conversion applications and up-to one half of the sampling frequency when it is used as a DC-AC inverter [8]. While providing these advantages, the amplifier can be constructed to be compact which is a crucial feature for mobile systems as here [4]**.**

Among other digital D-type amplifier structures like the half-bridge, the full-bridge is selected in this work despite space concerns because of the additional number of its components. Because the maximum output voltage swing that can be provided by a full-bridge inverter is twice that of the half-bridge under the same supply voltage levels, the full-bridge is selected [1]. This means that more output current levels and as well as higher electromagnetic fields can be reached. Also with the use of the full-bridge there is no need for dual polarity power supplying as in the half-bridge in order to have DC free output waveforms.

In addition, for the microprocessor side, a Xilinx FPGA is used to produce PWM signals digitally. The choice is favorable because FPGA promises concurrent operation, less hardware (demo boards), comparatively low cost for a complex circuitry and quick prototyping [10].

2.2.1 Circuit Simulations

Simulated analogue circuitry is as seen in “Figure 24 - Simulation Circuit” below.

The “U1” and the “U2” are MOS gate drivers. The typical application circuitry provided in the datasheet of this product is set up with other passive components. Power MOSFETs are named as the “Q1, Q2, Q3 and Q4” and the load inductor is modeled with “L1”. Digital PWM signal inputs of the gate drivers are pulse trains with 20 kHz frequency and constant duty cycle of 95% (5% complementary signal). They are also produced with a fundamental frequency of 600 Hz by using analog comparator and 20 kHz carrier with a 600Hz sinusoidal signal.

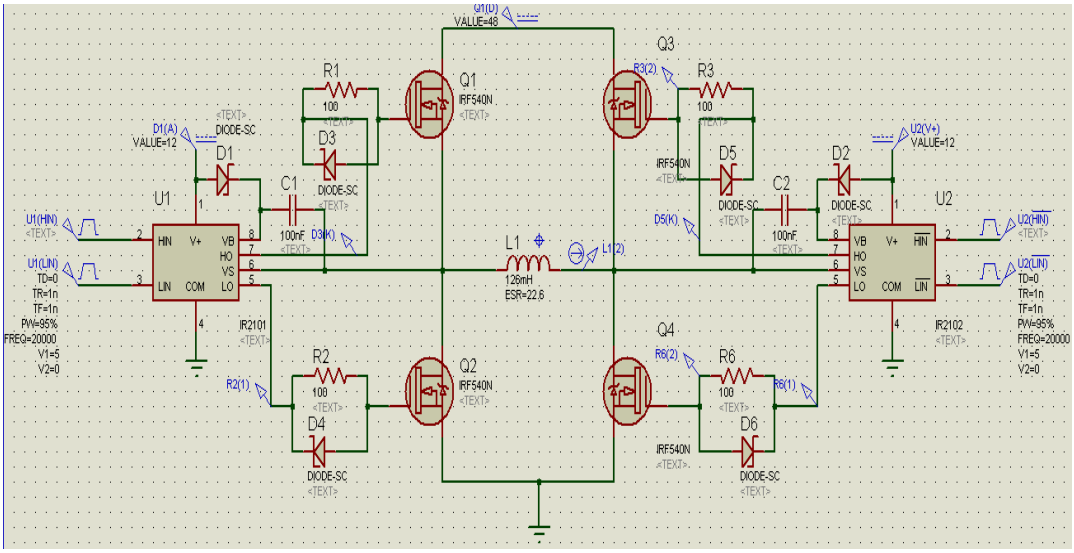

Figure 24 - Simulation Circuit

The full bridge is constructed from two arms of transistor couples. “Q1 and “Q2” couples reside at the 1st arm and the “Q3 and Q4” couple at the 2nd. Also term high side transistors or switches are used for pointing the “Q1 and Q3” couple while low side mean “Q2 and Q4”. As will be explained in the section employed PWM techniques, for both AC and DC cases (PWM with variable or constant duty cycle) only one transistor conducts at each arm and side. This type of drive is called “Bipolar PWM”.

The load inductor at the output of the bridge circuit filters the PWM voltage signal and provides electrical current with a fundamental frequency of same PWM signal. Its low pass filtering characteristic can be modeled by considering a 126mH inductance and a 22.6 Ω serial resistance as seen in “Figure 25” below. In practice, the inter-winding capacitance disturbs this response. At much higher frequencies than the range of the graph below, low pass filtering characteristic of the inductor degrades. Thus, current ripples are observed in the output, originated from the switching frequency harmonics in PWM drive signals.

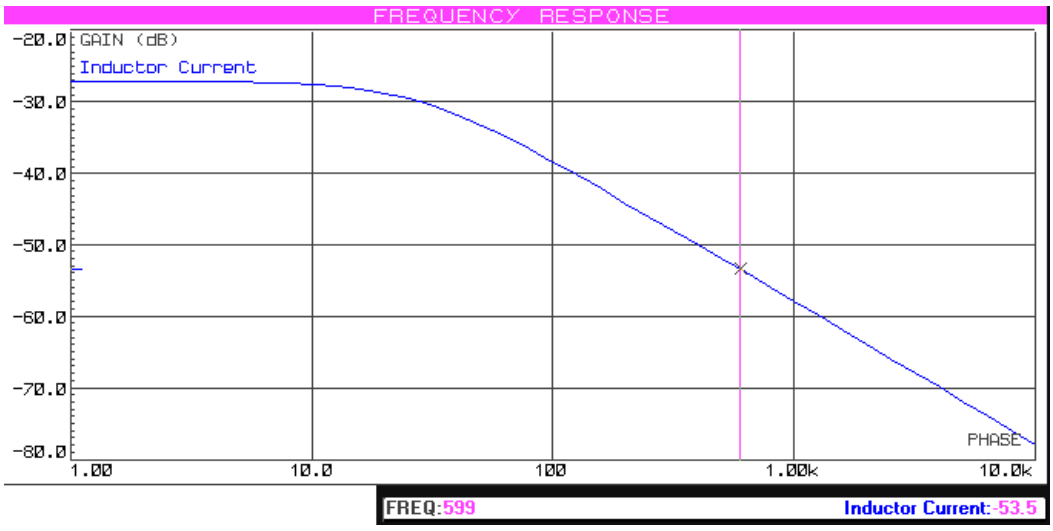

Figure 25 - Load Inductor Frequency Response

As stated before, transistors in the circuitry operate like switches changing between on and off. In other words transistors are used outside their active regions of I-V characteristics. This situation provides efficiency and keeps transistors from dissipating much energy which requires thermal precautions.

As mentioned before, MOS gate drivers are required to make high side transistors able to open. This is because the conducting high side transistor has a source voltage of "Vcc-$V_{DS(SAT)}$". Then for these transistors to be able open, their gate voltage must be higher than the source voltage plus the gate-to-source threshold voltage. Thus to be able pull FPGA PWM output voltage signal levels to such high levels like Vcc, gate drivers are used.

As mentioned before, when PWM drive signals with constant duty cycles (DC [modulation] case) are used, the average voltage across the circuit output is: "$(2 * Duty\_Cycle - 1)V_{cc}$". If this value is divided by the serial resistance of the inductor, it will be found that the fundamental DC current flows through the inductor. For the supply voltage "Vcc" of 48V, if 95% duty cycle PWM voltage signal is applied across the load inductor with a 22.6 Ω internal resistance, the load current will be approximately:

$$48 * \frac{(2 * 0.95 - 1)}{22.6} \cong 1.911\ A$$

like the simulation result in “Figure 26” below.

In this case, the power driven from the DC supply is approximately:

$$Vdc * Idc = 48 * 1.911 \cong 91.7\ W$$

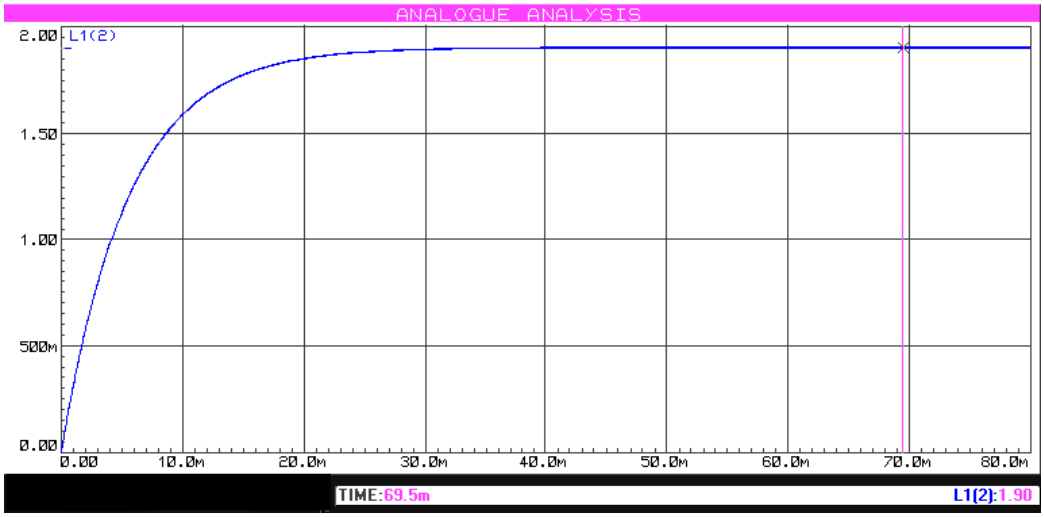

Figure 26 - Load Inductor Current

The PWM drive signals with variable duty cycle are produced in the AC mode. In this simulation, a sinusoid with 600Hz frequency is modulated in 95% modulation index with a 20 kHz carrier and fed into the gate drivers. From “Figure 25”, it can be seen that the load inductor model has a cut-off frequency of 28.3 kHz and attenuation at 600 Hz frequency is "-53.5dB". Therefore the output current flowing through the inductor is similar to the simulation result in “Figure 27” below.

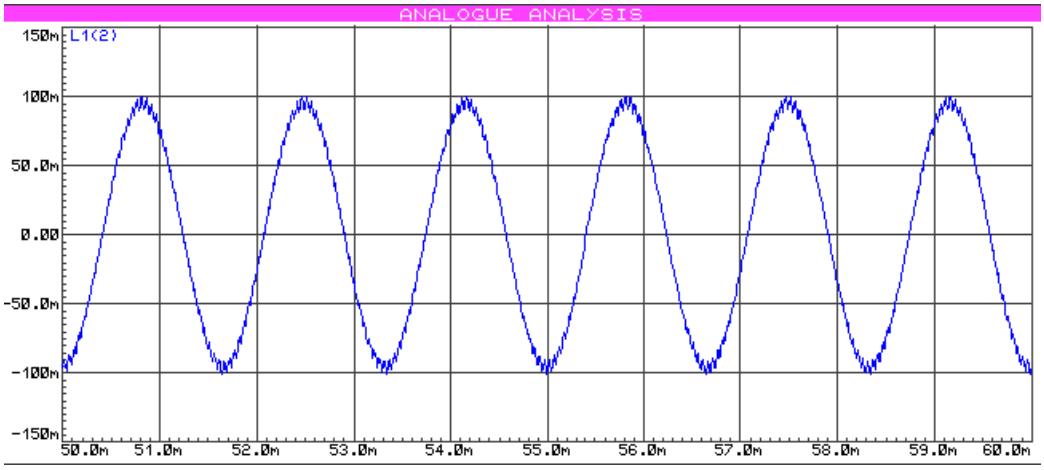

Figure 27 - Load Inductor Current AC Mode

In the graph above, the current ripple can be observed significantly. As mentioned before this is because of the switching frequency harmonics which cannot be attenuated fully.

2.3 Choice of PWM Method

The circuit structure choice is explained in the previous section and now the employed method of the PWM generation will be discussed following.

The frequency spectrum of the PWM drive signals can be analyzed by using the equations (24) and (26) which was given previously for the sinusoidal PWM waveforms generated with the "double-edged natural" and the "asymmetrical uniform sampling" methods respectively [3]. After an evaluation of these expressions, it results in that the harmonic levels and their distribution over the frequency spectrum differ between the two PWM techniques and yet these harmonics can be specified as the two different kinds of distortion components:

1) The forward harmonic components which appear at the odd multiples of the modulating signal frequency are confined within the first term of the equation (26) [3]. These belong to the uniform sampling and do not exist in the natural sampling [3].

2) The combinational components which appears at the sideband frequencies of the carrier frequency multiples, e.g. "$w_c - 4w_v$" [3]. This type of the distortion is higher in the natural sampling [3].

The other PWM sampling methods, like the pre-mentioned "enhanced uniform PWM", are considered to offer only a trade-off between either having the fundamental or higher switching frequency harmonics [4]. These are the cases that the uniform and the natural sampling offer respectively [4]. There is a significant distance in the frequency spectrum between the switching/combinational tones and the fundamental. So, these switching harmonics can effectively be attenuated with respect to the fundamental suppression by the output inductor. The levels of the fundamental harmonics are the prime concern here, not to interfere with and disguise the fundamental component of the generated target magnetic field. Therefore, the amplitudes of the magnetic fields which are produced by these distortion elements should not be comparable with respect to the fundamental amplitude. As mentioned previously, the natural sampling gives the ultimate PWM signal spectrum performance in this respect. Thus, it is feasible to prefer the natural over the uniform sampling which has already designed for digital platforms.

It is also important to pick the frequency ratio appropriately in the sense of the spectrum concerns [5]. So, to fully utilize the harmonic minimization performance of a PWM method, it is preferable to make the inverter to work with the maximum allowable switching frequency [5]. This shifts the harmonic components towards the higher frequencies [10]. Therefore, the switching and combinational harmonics at and around the switching frequency multiples are filtered easily from the output waveforms [11]. However, in this circumstance, the fundamental harmonics which are not related to the switching frequency do not get affected [11]. Thus, the uniform sampling can be revealed to be an exception because even at high carrier frequencies, the "Forward Harmonic" (fundamental harmonic) levels decay slowly which are the majorly concerned distortion source [3]. On the other hand, the natural sampling, of which spectrum does not involve any fundamental harmonics already, further makes

the only distortion source of its, the switching harmonic levels, to be negligible for the carrier frequencies beyond 132 kHz [3].

Although the low levels of the distortion can be attained with the high switching frequency values as explained in this section so far, this frequency should not be selected more than a few hundred kilohertz practically [3]. This is required in order to have reasonable efficiency levels since higher the switching frequency the more switching stress and power losses occur [3, 10].

After the choice of the natural sampling as the PWM sampling scheme, some other PWM properties should also be decided like the edge type. The PWM method is defined as either the "double-edged" or the "single-edged", with the selection of the carrier waveform shape as the triangular or the saw-tooth respectively. The double-edge modulation is superior over the single-edge in harmonic levels [12, 13]. In addition, it only takes a little much more effort to employ the double-edge modulation than the single-edge modulation [12, 13]. Thus the shape of the carrier is preferred to be triangular which makes the PWM technique to be featured as "double-edge natural sampling PWM".

The synchronism of the natural PWM technique will be determined following. In this work, this property of the method has to be asynchronous eventually. Because the modulating signal frequency differs with 5 Hz steps in the 500-700Hz frequency band while the carrier signal frequency stays constant at 20 kHz. As the drawback, sub-harmonics can occur since the carrier frequency is not an integer multiple of the modulating frequency [11]. This results in the modulated PWM signals to be non-periodic [11]. The low values of the ratio of the carrier frequency to modulating's as "6" and below, urge the harmonics at the sidebands of the switching frequency multiples to approach the fundamental frequency [12]. So, those combinational harmonics are turned into sub-harmonics at significant amplitudes with respect to the fundamental level [12]. Any PWM switching scheme that ensures the high ratio of the carrier frequency to the modulating's, the sub-harmonic distortion in the output waveform will be negligible even for several hundred hertz fundamental frequencies

[11]. Then the selection of high carrier frequencies like at the order of 20 kHz makes it possible to use a fixed carrier frequency for varying modulating signal frequencies [11]. Thus, the asynchronous scheme will be adopted with ensuring such high frequency ratios. In this work they are in between “28” and “40”.

On the other hand, for the frequency ratios which are lower than ten, the synchronous PWM should be employed to provide the adequate separation of the fundamental component from the carrier sideband components in the spectrum [12]. Alternatively; the pre-mentioned optimized method, which suggests using pre-calculated switching instants with harmonic minimization algorithms, are substantially attractive at such low frequency ratios [5]. In the situations like this, they can have a significant influence on the harmonic content [5].

To sum up, although a digital platform is used to create PWM signals in this work, an FPGA, the “natural sampling” is used as the method of PWM which may seem to be more appropriate for analog systems at first glance. In practice, this is mainly because of the poor spectral performance of “uniform sampling” at frequencies around the multiple of the modulating signal’s with respect to the harmonic levels [3]. The reason for this is the manipulation which is done to the modulating signal by sampling it at the carrier frequency. Because the processed signal is the modulating one, additional harmonics around modulating signal frequency multiples are observed in the produced PWM signal spectrum. Furthermore, even both of the natural and the uniform sampling techniques provide a similar carrier harmonic levels, the very first concern is to eliminate modulating signal harmonics as much as possible. It is much more important than the high frequency components at around the carrier frequency multiples. The main reason lying behind this is the fact that it gets harder for magnetic fields to penetrate underwater for increasing frequencies. Thus, it is important not to have unwanted components, with comparable frequencies to the fundamental’s, which will perturb the target field significantly. This will be analyzed in more detail afterwards.

2.4 Digital Signal Generation at FPGA with VHDL

The harmonic content of a PWM waveform which is created in digital platforms also depends on the sampling frequency and the number of the bits used to generate the "modulating" and the "carrier" signals, as being differently than the analog applications [12]. The bit resolution of look-up tables for these signals should be determined by considering the type of the modulation technique employed [5]. Additionally, the aimed accuracy of the pulse widths of the produced PWM drive signals is another important issue to be considered [5]. The accuracy of the pulse widths reduces harmonic levels from the spectrum [5]. For most applications, 8-bits word-length is sufficient to build look-up tables for the purpose [5]. Then for the precise quantization of sample magnitudes, the word length of both the triangular carrier signal and the modulating signal is selected to be "11" in signed integer. However, the magnitude levels of the signal samples do not cover the full range of the eleven bit quantization. They only varies in a range of [-625,625], yet this is almost as five times better than a full scale 8-bit quantization with respect to the number of quantization levels.

The sampling frequency of the signals will be discussed following as mentioned previously as an important parameter for the harmonic content of the modulated pulse train signals. While comparing the carrier and the modulating signal amplitudes, signal level intersections are detected faultily because they are shifted in time and this situation affects the accuracy of the switching instants [2]. As explained previously in the introduction, the dead-time involvement causes a similar result by delaying the switching instants for a proper duration of time over the faulty detection of the signal level intersections. Moreover, as it will be analyzed in the following section, decreasing the sampling rate of the signal comparison for preventing unwanted glitches in the modulated signals is also another reason. The effects of these will be explained afterwards but the main focus of the paragraph is to analyze the effects of the sampling frequencies of the signals over the intersection instant. In this case the problem is that the samples of two signals may not exist at the actual intersection as in continuous waveforms. Thus, this results in the misplacements of

the switching edges (intersections) to another time instant when previously sampled levels of these intersect. As a result of this situation and the previously talked reasons, the amplitude of the fundamental component differs from its actual level and some additional harmonics appear near it [2]. However, the effects of the sampling periods on the results depend on the frequency of the modulating signal and the triangle [2]. Since the carrier has a much lower period than the modulating signal, the ratio of the carrier sampling period to the carrier signal frequency "Ts/Tt" is essential in determining these effects [2]. It is provided that the effects are small when this ratio is small enough [2].

2.4.1 Glitch Avoidance

The most basic handicap of the natural sampling is its pre-mentioned sensitivity towards small changes in signals used for modulation operation. This is a problem which should be overcame both in the digital as well as the analog applications of the method. In analog systems, such level variations which are observed in signals are mostly originated by the electrical noise. However, the main reason why they occur in digital systems is the discretization of the signals by sampling them for the use in these platforms. The stepped form of the sampled signals causes erroneous results while comparing the modulating and the carrier signals. This is because the signal levels are not exact values of the signals between two samples. In addition, the reason is identical for the occurrence of glitches. When the sampling rates of two signals are not matched, the level jumps of the modulation input signal at the instants (phase) of the new sample appearances are the reason for glitches. As a result, the levels of both the modulating and the carrier signal harmonics are increased in the spectrum of the produced PWM signals [3].

In "Figure 28" below, the scenario of the glitch occurrence in PWM signals is illustrated. As can be seen, the carrier sampling rate is much higher than of the modulating signal. Therefore, the discrete levels of the carrier signal may intersect the discrete levels of the modulating signal twice even there is not any actual intersection between the actual continuous forms of the two signals. This

phenomenon causes faulty comparison results and so the glitches to appear in the modulated signal waveforms.

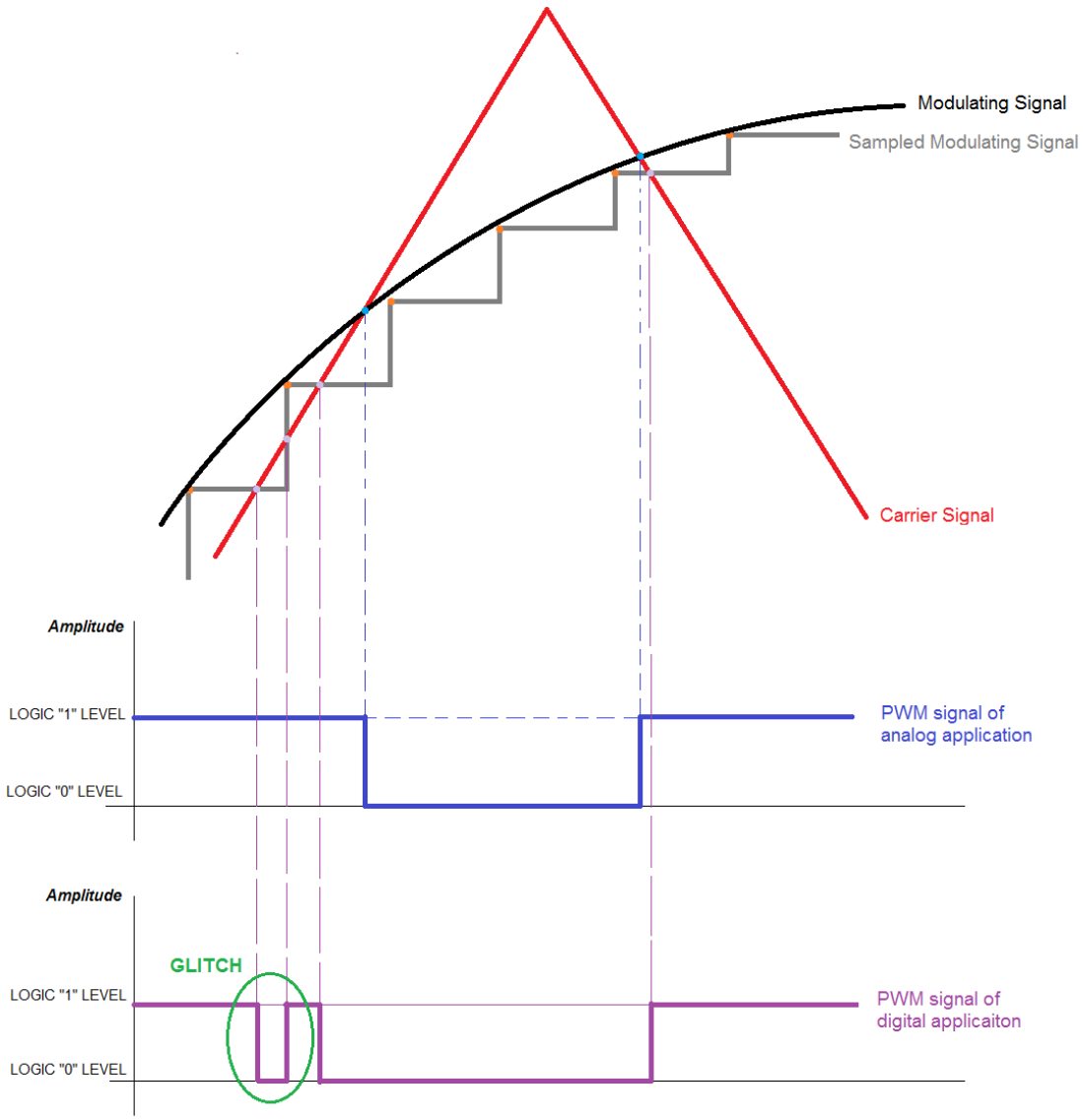

Figure 28 - Modulation under Signals Sampling Rate Mismatch

Because the carrier sampling frequency is much higher than the modulating signal's, it is selected as the comparison rate, for the sake of detecting the intersections of the signal levels more precisely. Then, the proposed solution for the "glitch" problem suggests decreasing this rate of the signals amplitude. Therefore, such a manipulation implies decreasing the sampling frequency of carrier signal as well. The new carrier

sampling period and the comparison rate are then adjusted to be at least as long as the duration of the widest possible glitch pulse.

The related calculations for the new periods are made with respect to behavior of the modulating signal around zero crossings where its rate of change is highest. This is because, for the same sampling period; the level difference between two consecutive samples is maximum there. It is also the region where the pre-defined double crossing of the compared signals in other words a glitch is most likely to occur. Also it will be the widest one in time duration. Therefore, as mentioned if this one special worst case is handled then there will never be such a problem in the comparison at any phase of the signals. Because the glitches which occurs in regions other than that particular one are smaller in widths with respect to the one in the worst case. In this context; for finding the new comparison rate which is equal to carrier sampling frequency at the same time, calculations are made in following steps:

1. Pick the two consecutive samples of modulating signal around its zero crossings. If possible, these samples had better have the “zero” level in between.
2. Calculate the carrier signal slope.
3. Locate the signals as showed in “Figure 29” as the carrier signal intersects the second modulating signal sample. Then automatically, a perpendicular triangle will be constituted among the carrier and the digital modulating signal.
4. With the help of the carrier signal slope and the level difference between modulating signal samples, the “critical time duration” can be calculated.

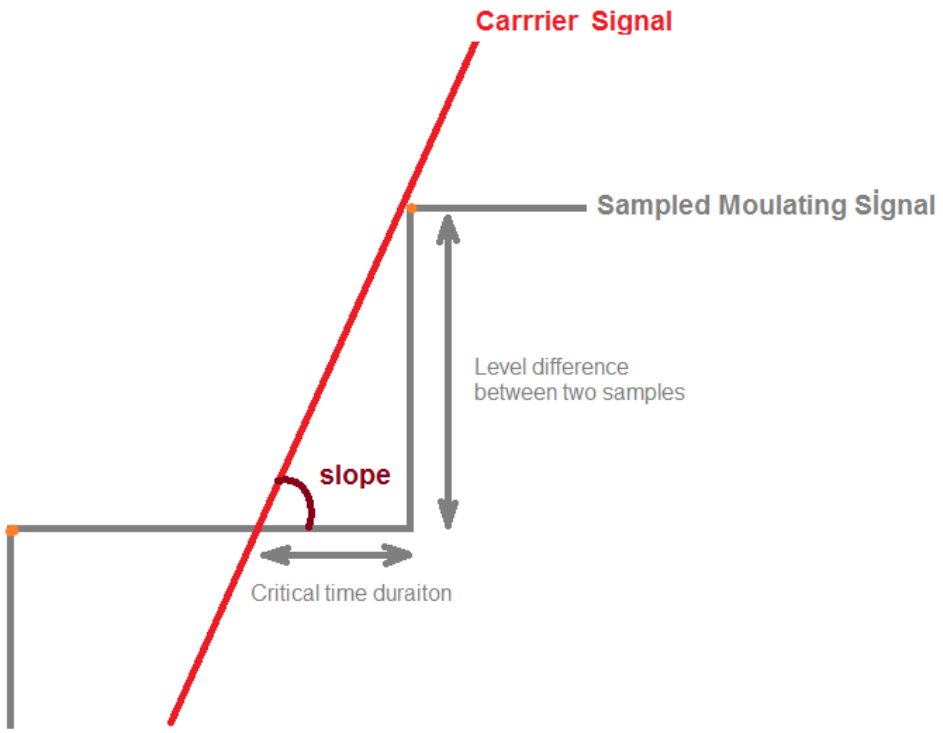

Figure 29 - Glitch avoiding calculations

The resulting calculated critical time is a little less than 80 ns. Then, the new comparison and carrier sampling periods are changed from “20ns” to “80ns”. As mentioned previously, the intersections of the signal levels will be manipulated once again and this results in the shifting of switching instants in time. Unfortunately, the spectrum of the modulated signal spectrum will be affected and even the undesired fundamental harmonics will occur which are advised to be avoided in the first place [2]. However; the situation here is nothing but the change of the carrier sampling frequency. The effect of the sampling periods depends on the frequency of the modulating signal and the carrier [2]. Since the carrier still has a much lower period than the modulating signal which is not changed in the progress, the ratio of the carrier sampling period to the carrier signal frequency “Ts/Tt” is essential in determining these effects [2]. The effects are small when this ratio is small and it is calculated to be (Tt=1/20kHz)/(Ts=80ns)=0.16% after the frequency modification. Yet, this ratio is still small enough to make the additional fundamental harmonics

negligible as can be seen in “Figure 30” and “Figure 31” below [2]. They provide the frequency spectrum of the modulated signal and no fundamental harmonics with significant amplitudes are observed.

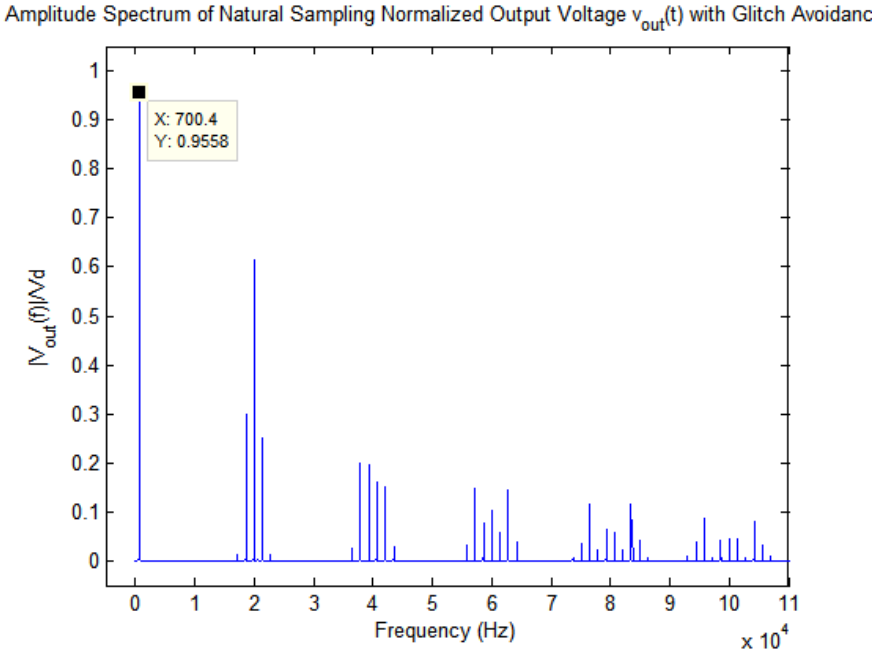

Figure 30 – Natural Sampling Modulated Signal Normalized Spectrum

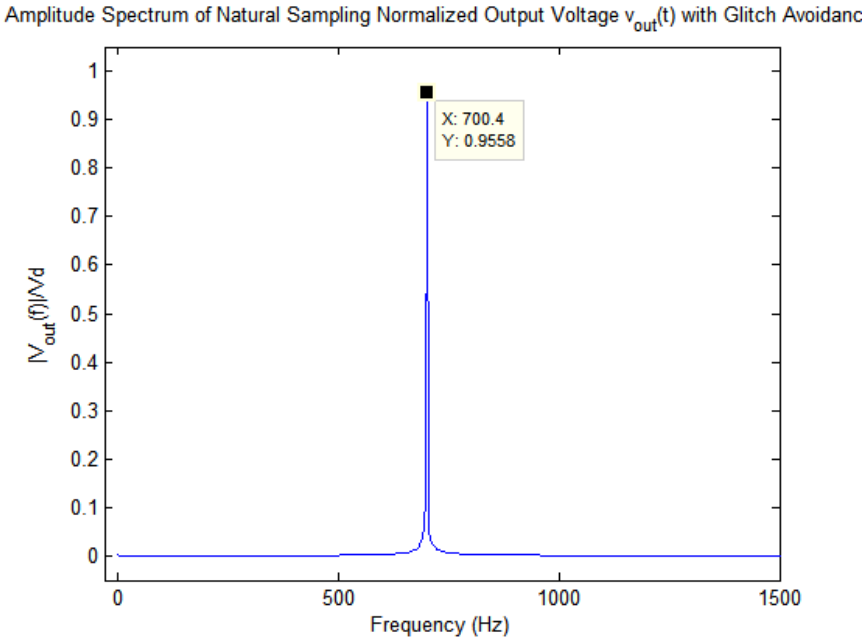

Figure 31 - Natural Sampling Modulated Signal Normalized Fundamental Component

The asynchronous type PWM is employed in this work as stated before. The drawback of the method is said to be the sub-harmonics which may occur in the spectrum of the produced non-periodic PWM signals [11]. However with any of the PWM switching scheme that ensures a high frequency ratio, the sub-harmonic distortion at the output waveform will be negligible even for several hundred hertz fundamental frequencies [11]. Then, it can also be concluded from the spectrum figures above that, the value of this ratio which is selected in this work is sufficient in order to make such sub-harmonics negligible.

The spectrum performance of the "natural sampled PWM", which is modified by increasing the carrier frequency as previously, can be analyzed in comparison with the "uniform sampled PWM"s. This is important to see whether the method of "digital application of natural sampling" maintains its superiority in the frequency spectrum over the uniform sampling or not. "Figure 32" and "Figure 33" below show the frequency components of the PWM signals which are produce with the use of the uniform sampling. As can be seen, the high frequency ratio makes it possible even for the uniform sampling that fundamental harmonics' having negligible levels. However, the amplitude of the fundamental component is observed to be lower than it is in the modified natural sampling case. Even though the natural sampling is modified by the glitch avoidance manipulations, the harmonic levels of the carrier frequency multiples and their combinational are lower in the natural sampling method.

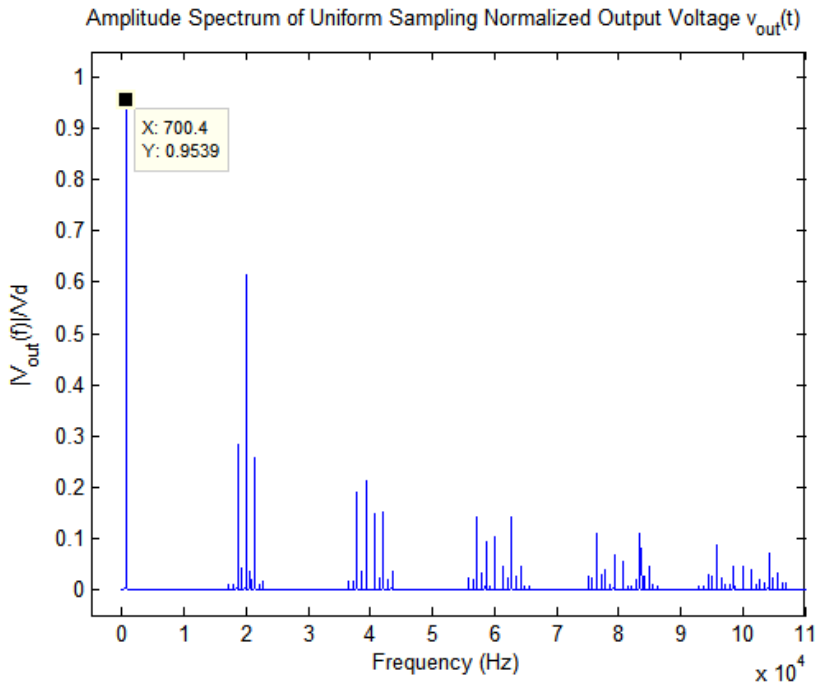

Figure 32 – Uniform Sampling Modulated Signal Normalized Spectrum

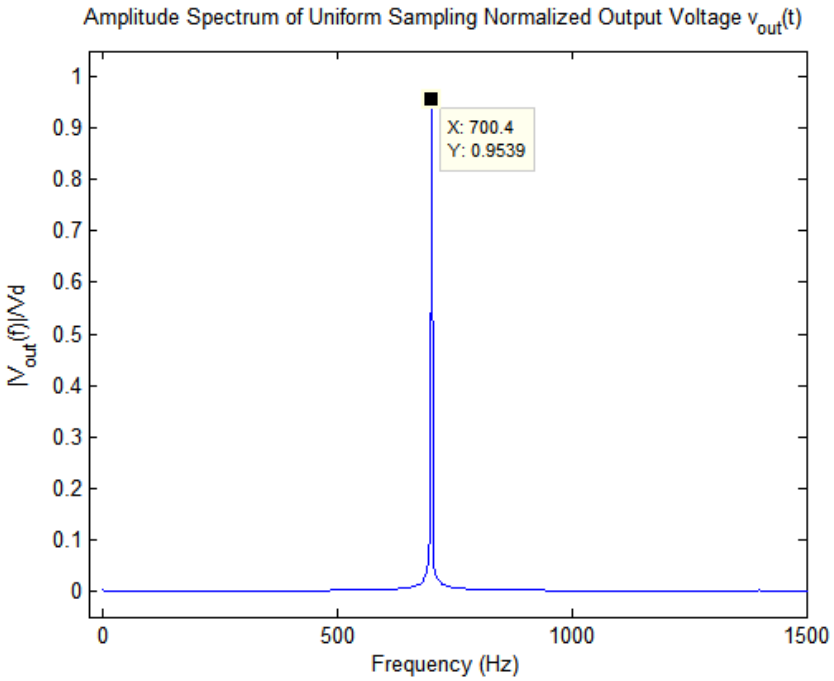

Figure 33 - Uniform Sampling Modulated Signal Normalized Fundamental Component

2.4.2 Dead-Time Requirement

Besides the natural sampling which is the sampling method of the PWM, the drive technique used in this work is the “single phase bipolar”. So the switches at the same arms of the H-bridge circuitry are driven in a complementary fashion. Because only a PWM signal and its complement are used, just the two voltage levels observed at the output differentially, which are the plus or minus supply voltage. Then the technique is called bipolar.

Although it is said complement, those two PWM signals which are applied to the gates of the switches in same the arms of the H-bridge are not exact complement of each other’s. This is because of the transistors’ finite turn-on and turn-off times. They cannot be switched from conductive to non-conductive state as fast as in the way of their gate drive signals change. If the exact complementary signals are used, then there will be an instant of simultaneous conduction of the both of the transistors at the same arm of the bridge. In this circumstance, the power supply will be short circuited which refers a phenomena called the “shoot-through”. Therefore, some precautions should be taken by further modifying PWM drive signals. Then, the low-to-high transitions which turn the states of the transistors into the conductive are delayed during whole the turning off process of the other transistor on the same arm. Actually, this process is not delaying but is decreasing the high state durations of the signals as well as the on states durations of the transistors. In practice, the high-to-low transitions which put the transistors in non-conductive state are not altered as in the following “Figure 34”:

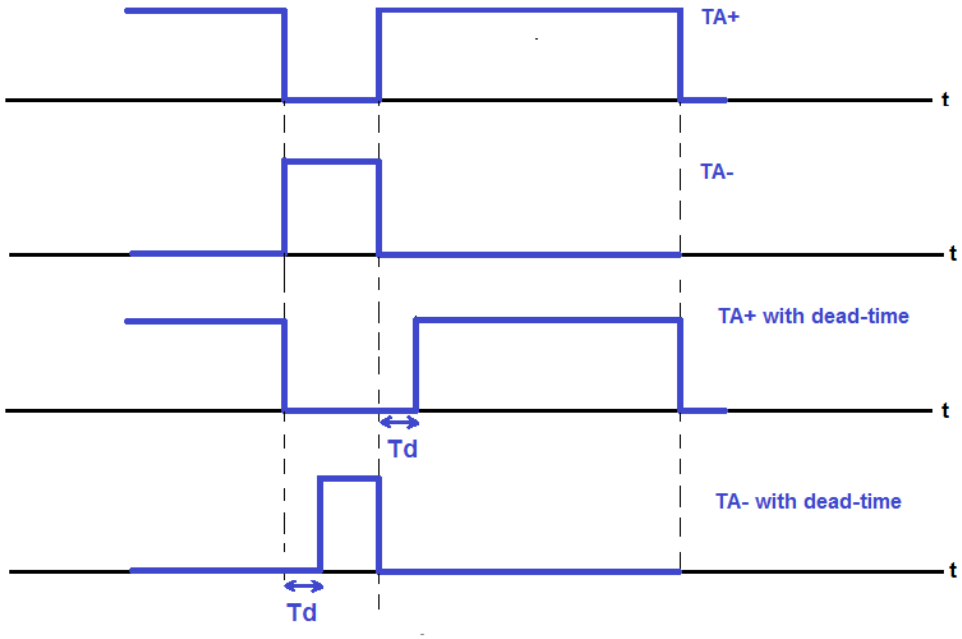

Figure 34 - Dead-time Application on PWM Drive Signals

For both of AC and DC cases, the amount of the dead-time which is inserted into the PWM signal is determined with respect to the hardware timing characteristics. The measurement in “Figure 35” below has been done by using a half-bridge version of the driver circuit with a resistive load at the output. In the scope snapshot, the blue waveform is the output PWM signal of the FPGA board in other words the PWM input signal of the MOSFET gate drivers. The red one is the voltage across the resistive load which represents the waveform of the current which flows through the transistor. The both of the latency from the gate driver input (FPGA output) to the corresponding transistor response and the turn-off delay of the same transistor turn-off delay can be seen in the figure. After the turn-off transition is inputted to the gate driver, it takes around 220 ns for the transistor to response. Moreover, the turn-off duration of the transistor is around 100 ns. Therefore, a dead-band of 500 ns duration is inserted. It is ensured that this time interval is bigger than the sum of the both of the latency from the gate driver input to the transistor and the turn-off duration of the transistor.

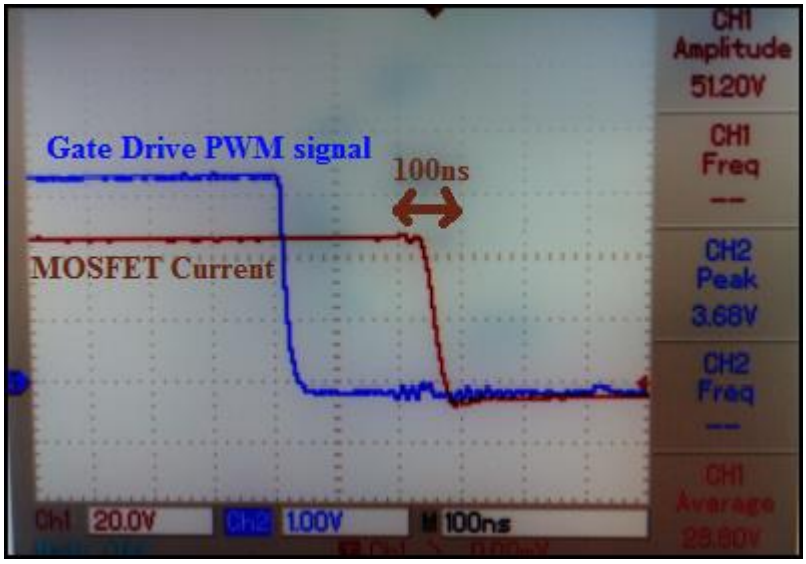

Figure 35 - Circuit Timing Measurements

Furthermore, the exact behavior of the PWM voltage signal which output load inductor sees across the output terminals is a bit different. As mentioned previously, all switches at the bridge are in non-conductive state during the dead-time. Then the inductive load current should find itself a path to flow through. At the instant when the transistors in conductive state starts to turning off, the corresponding fly-back diodes also start to turning on. The diodes which are in the same direction with the load current throughout the way between the supply terminals control the voltage levels of the output nodes. So, either the "D1 & D4" or the "D2 & D3" couples provide the required path for the load current with respect to its direction. Then the current loop is completed through those diodes and DC supply. If the load current direction is as in the "Figure 36Figure 37" below, the diodes "D2" and "D3" will conduct. Then the voltage level of "node A" will be supply reference level minus the diode threshold voltage. Furthermore the "node B" voltage will be the supply level plus the diode threshold voltage. In that manner, the voltage difference at the output will be as in the "Figure 37".

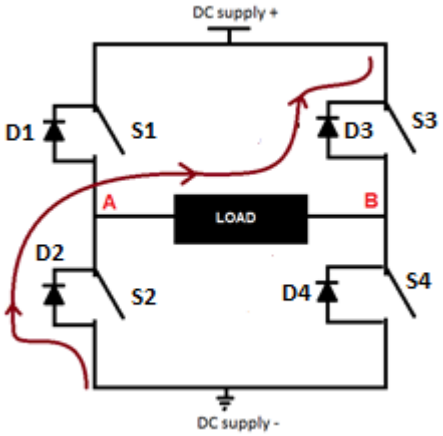

Figure 36 - The Load Current Path during the Dead Time

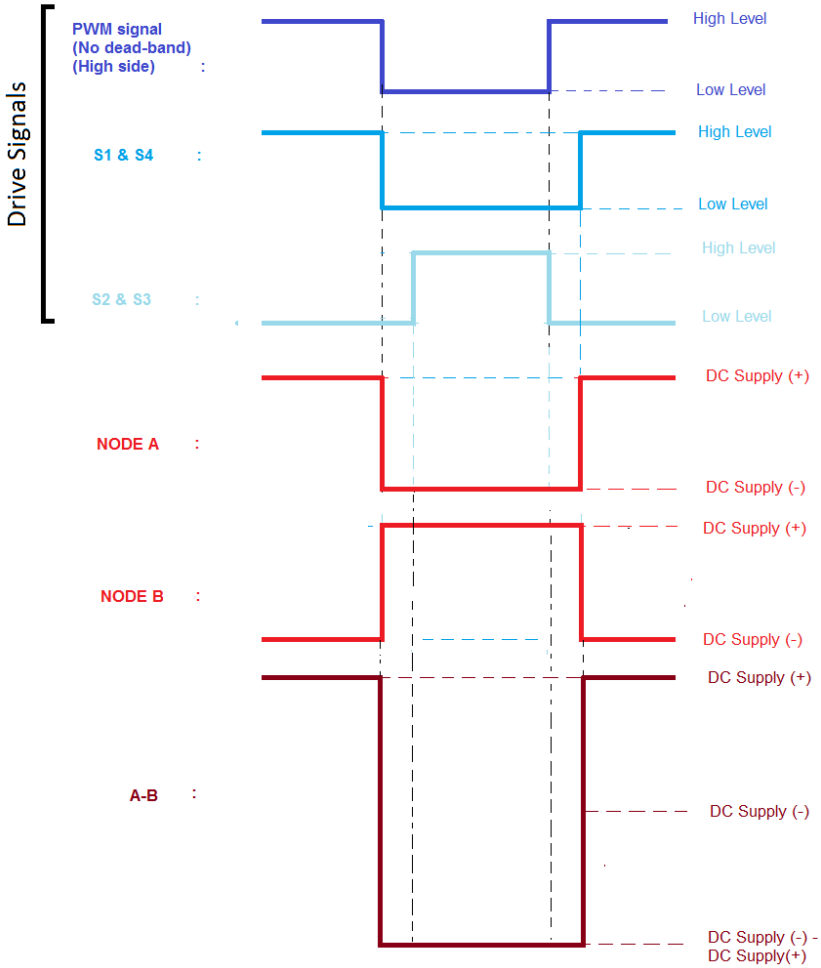

Figure 37 – Variation of the Full-Bridge Output Voltage in Dead-time Intervals With the Output Current Direction

In the case of opposite load current direction the other diode couple (D1&D4) conduct the load current during the dead-time duration. Therefore, the voltage levels at the output terminals of the circuit will swap accordingly. A voltage error waveform is derived by simply subtracting the output voltage waveform of the case with the dead-time from the one with no dead-time involvement. As mentioned about the altered switching instants previously, some additional frequency components appears in the spectrum of the PWM waveforms and the levels of the existing ones are increased with respect to the PWM waveforms with the lack of dead-time [2]. This difference in the frequency domain can be observed by inspecting the spectrum of this output voltage error waveform in "Figure 38" below:

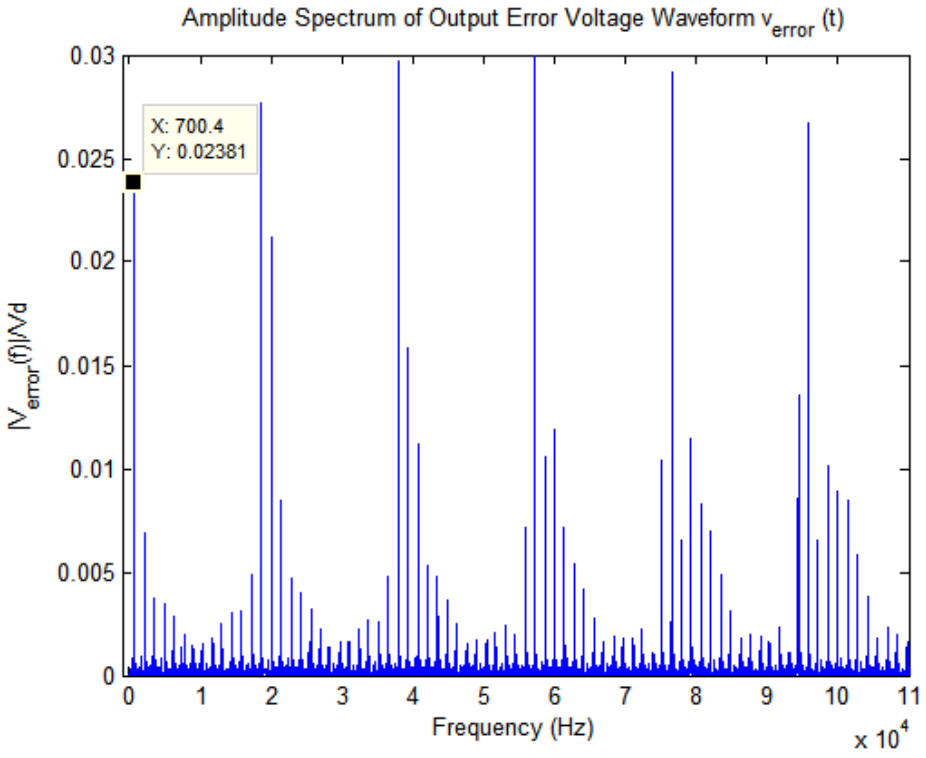

Figure 38 - Voltage Error Waveform Spectrum

As can be seen in graph above, the voltage error waveform contains lots of harmonics even ones at the comparable frequencies with the fundamental one. These are combinational the components at the switching frequency multiples and the forward harmonics of the fundamental component. For constituting the actual output PWM

waveform, all these frequency components will be attached to the ideal output voltage waveform with no dead-time [7].

However, it is proposed in the article [7] that these frequency components will be added to the ideal output voltage signal (with no dead-time) in phasor domain. This means their phases matter for resulting amplitude levels of the output components at their frequencies. As it is indicated again in the same work, the fundamental error voltage components are subtracted vectorially from the ideal ones by considering the influence of the power factor angle [7]. Hence the actual level of the fundamental component will be:

$$V_1 = -\Delta V_1 cos\Phi + \sqrt{V_{ref}^2 - (\Delta V_1 sin\Phi)^2} \qquad [6].$$

The calculated spectrum of the resulting output voltage waveform can be analyzed to see the effect of the dead-time duration on its frequency content in "Figure 39" below.

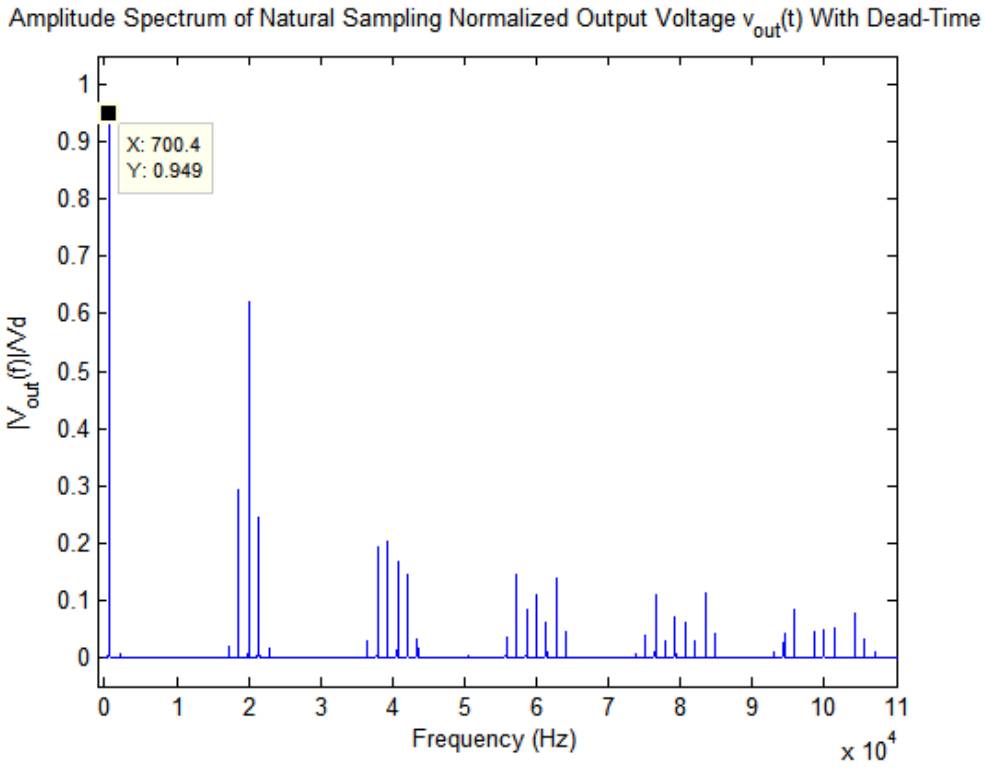

Figure 39 - Output Voltage Spectrum (Dead-time involved)

As can be seen in the figure above, the level of the fundamental frequency component is reduced and the dead-time involvement does not make much impact on the rest of the output voltage spectrum. This is because the low-order odd harmonic amplitudes varies linearly with the ratio of the dead-time duration to the switching period "$\frac{td}{Ts}$" as stated before in [7]. This ratio is "$\frac{500ns}{(20kHz)^{-1}} = 1\%$" here and in "Figure 21", it corresponds to a fundamental error voltage peak at around "2.5%" with respect to the supply voltage level "$48V$".

However, the actual fundamental level is calculated by taking also the output power angle factor of "73.44^{o}" into account. So it results in new amplitude of fundamental output voltage level:

$$V_1 = -\Delta V_1 cos\Phi + \sqrt{V_{ref}^2 - (\Delta V_1 sin\Phi)^2} = -\frac{2\sqrt{2}}{\pi}\left(\frac{20kHz * 500ns}{700Hz}48V\right)\cos(73.44) + \cdots$$

$$\cdots\sqrt{(48V * 0.9558)^2 - \left(\Delta V_1 * sin(73.44)\right)^2} = 45.7535V$$

where "$\left(\Delta V = \frac{MT_d}{T}V_d\right)$","$(\Delta V_1 = \frac{2\sqrt{2}}{\pi}\Delta V)$".

Furthermore, "$(48 * 0.9558 - 45.7535)/48 = 0.26\%$" is the calculated decrement (normalized with the supply voltage level) in the fundamental component level with respect to the ideal output voltage waveform's. By comparing the fundamental component levels in "Figure 31" and "Figure 39" above, the reduction is found as "0.68%". The normalized levels of the higher order forward harmonics, the 3rd and so, are below 1% and negligible as can be seen in "Figure 21".

Another important issue is to adjust the dead-band duration properly. It should be long enough to cover transistors' turn off durations to prevent the simultaneous conduction of the transistors which are on the same arms of the bridge. However, it should also be small as much as possible to make the output PWM spectrum to be distorted less.

Chapter 3

VHDL MODULES

The generation of the PWM signals is made digitally on the BASYS2 board of the DIGILENT with the "Xilinx xc3s100e" as FPGA chip. The designed VHDL code has following modules which will be explained throughout the chapter.

3.1 PWM-Top Module

This is the top module for assembling sub-modules and it has the I/O interface as in “Figure 40”. Three inputs, the “dutyfreq(7:0)”, the “clk”, the “slct” and five outputs, the “digit(3:0)”, the “segout(6:0)”, the “led”, the “notout1” and finally the “output1”. The “clk” is the clock signal provided from an on-board 50 MHz oscillator. The “slct” is a serial input for the mode alterations. The 8-bit “dutyfreq” input controls the PWM duty cycle value. Outputs, the “digit(3:0)” and the “segout(6:0)” are for the 7-segment display to display either the modulating frequency in the AC mode or the duty cycle value in the DC mode. The “led” notifies the appropriate instants for mode changes. The actual PWM signals are provided by the outputs, the “output1” and the “notout1”.

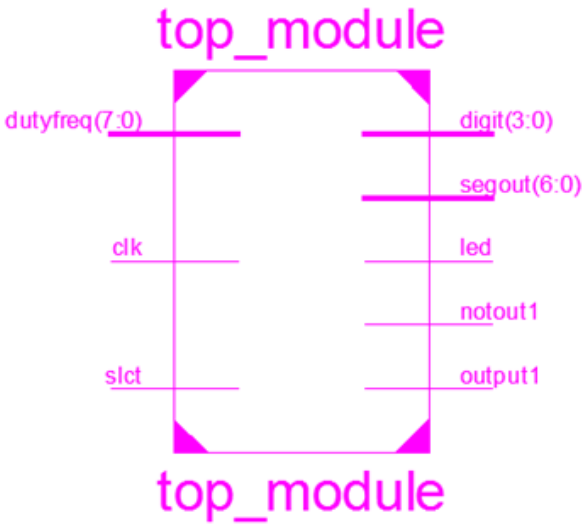

Figure 40 - Top Module I/Os

The number of the sub-modules are eight many as can be seen in RTL schematic in "Figure 41". These are the "square", the "triange", the "mod_signal", the "comparator", the "modslct", the "freq_change", the "deadtime" and the "sseg".

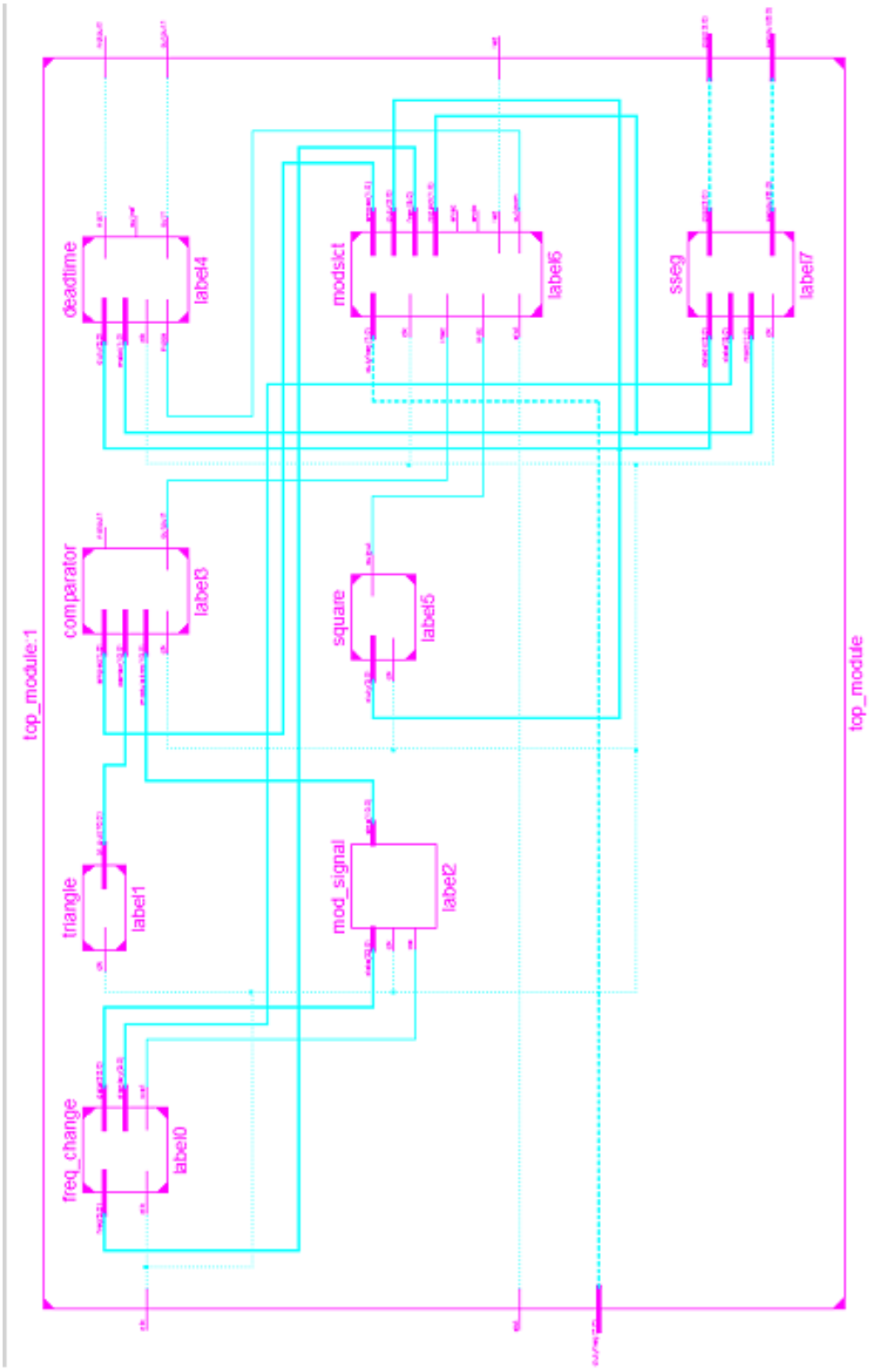

Figure 41 - RTL Schematic

3.2 Sub-Modules

3.2.1 Square

This is the module where the DC mode PWM signals are produced with the 20 kHz switching frequency and the duty cycle with respect to the 4-bit input “duty”. This input is the first (LSB) four bits of the top module input “dutyfreq” when the mode of the operation is the DC. Duty cycle values for corresponding combinations of bit values are as in “Table 2” below:

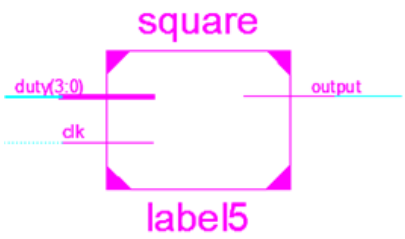

Figure 42 – Square Module

duty(4:0)	Duty Cycle
1111	%98(max)
1110	%75
[0000 : 1001]	%10*[0 : 9]
o/w	%50

Table 2 - Duty Cycle Values For "Duty(4:0)"

3.2.2 Triangle

This module generates the required 20 kHz triangular carrier waveform for the AC mode. It swings between ±625 peaks with a sample frequency equal to FPGA clock frequency of 50MHz.

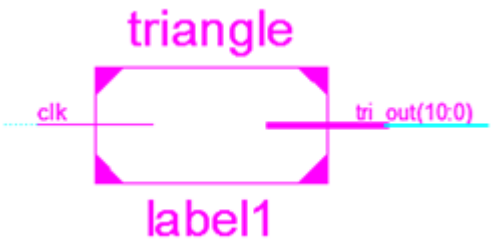

Figure 43 – Triangle Module

3.2.3 Mod_Signal

The “CORDIC” ip-core is used to create this module as a sinusoidal signal generator. Corresponding “DDS Compiler” design GUI is used for configuration the module. The width of the look-up table for sinusoid values is determined by the “phase width”

input, “N”. Therefore, the frequency resolution of the output signal becomes “$f_{CLK}/2^{N}$” where the “f_{CLK}” is the clock frequency. The input “phase angle increment values” “ΔΘ”, specifies the number of increments in the index of the look-up table per clock period. Thus, the output signal frequency will be configured as “$\Delta\Theta*(f_{CLK}/2^{N})$”. The clock frequency is 50MHz and the “N” is selected as 33, then the frequency resolution becomes $50MHz/2^{33}$=0.00582076609134674072265625 Hz. Moreover, for the value of the “ΔΘ” of "00.....0.....00101001111100011 00" (33-bits), the output frequency will be:

$\Delta\Theta*(f_{CLK}/2^{N})$=85900*0.00582076609134674072265625=500.003807246685028 Hz.

The assertion of the “we” input makes the “data” content to be written into the phase angle increment register to change this frequency value.

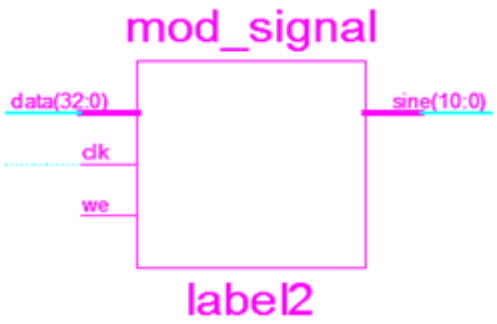

Figure 44 - Mod_signal Module

3.2.4 Comparator

This module is for the generating AC mode PWM signals. The triangle signal produced in the “triangle” module and the sinusoidal signal which is provided from the “mod_signal” will be compared with respect to the magnitude. The modulation index control is also made by the “ampac” input coming from the “modslct” module. For the binary value $(00)_2$ of this input, the modulation index becomes %25; for $(01)_2$ it is %50; for $(10)_2$ %75 and in case of $(11)_2$ the modulation index is at its maximum as %98. In addition, the glitch avoidance modifications are made here.

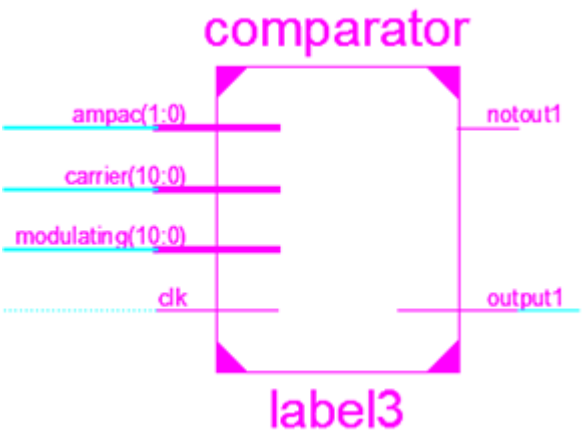

Figure 45 – Comparator Module

3.2.5 Modslct

The mode control of the PWM is done here by using the top module inputs, the “slct” and the “dutyfreq”. The “slct” is a serial input and it keeps the track of the high level occurrences on the corresponding pin. The value of a 2-bit counter is increased by one for each high level input which is apart from the previous high input by a low level input which has a duration of at least a 1 second. When the counter has the binary value $(00)_2$, PWM outputs provides the voltage of the ground reference. For $(01)_2$, the DC mode PWM signal which is provided from the “square” module to the “indc” input of this module will be outputted as the “outpwm”. When it is $(10)_2$, the AC mode PWM which is coming from “comparator” module and inputted to the “inac” will be outputted to the “outpwm”. The $(11)_2$ case is for “BIT” mode which stands for the “Built-In Test”. In this mode the output PWM signal alters between the DC and the AC mode for 10 seconds periods. Moreover, the “slct” input controls the use of the “dutyfreq” input for modes. For the DC mode, the first (LSB) four bits are passed through the “duty” output and reach the “square” module as the duty cycle information. In the AC mode, the first (LSB) six bits are given to the “freq” output and provided to the “mod_signal” module to be used for frequency calculations of the modulating signal. The most significant two bits are connected to the “ampac” output and delivered to the “comparator” module as the modulation index data as explained in the corresponding module.

The "mdslct" output has the 2-bit counter content which is controlled by “slct” input. The mode information is preserved here and transferred to the “deadtime”, the “sseg” modules. The “led” is the output signal to inform the user that the only one mode change is possible in a one second time duration. It is named “led” because it may be assigned to a led to notify the user for the one second period after the “slct” input is asserted.

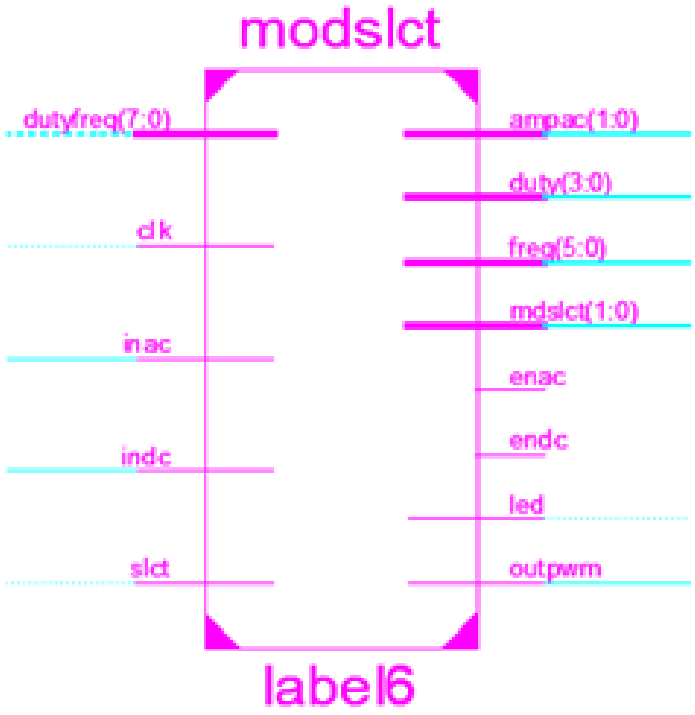

Figure 46 – Modslct Module

3.2.6 Freq_change

The "freq_change" module controls the frequency of the modulating signal to be used in the AC mode. The “freq” input with six bits which comes from the “modslct” module is turned into the phase angle increment value and fed into the “mod_signal” module with the “data” output. When the “freq” equals to $(000000)_2$, the “data” has the corresponding value to make the “mod_signal” module to produce a sinusoid with 500 Hz. Each of the $(1)_2$ increment in “freq” means a rise of 5Hz in the frequency till 700 Hz. Also, after each change of the “freq” input, the “data” output is

updated and the “we1” will be pulled to the digital high level to be able to write into the corresponding phase angle increment register of the “mod_signal” module. Additionally, the actual frequency information is turned into 10 bits and passed into the “display” module for the 7-segment displaying.

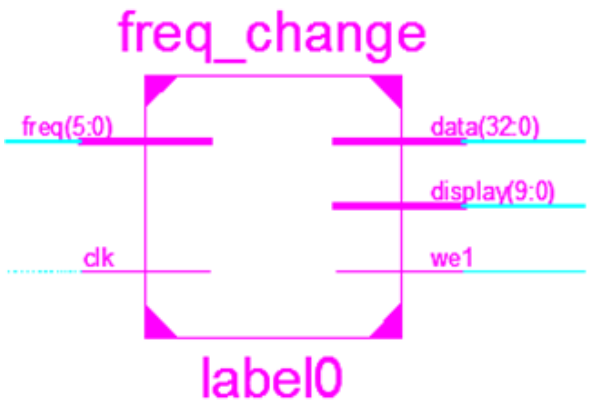

Figure 47 - Freq_change Module

3.2.7 Deadtime

In this module both the AC and the DC mode PWM signals are brought to their final form by the insertion of the dead-bands. As stated previously, the hardware characteristics suggest a dead-band duration of 500ns to be imposed on the PWM signals. The insertion is made as the beginning of the dead-band to be at the instant of turning-on edges of the PWM signals. Then, the level of the signal stays low for the dead-band duration. Besides, in the case of the “mslct” is $(00)_2$ or, it is $(01)_2$ (DC mode) and the “duty” input equals to $(0000)_2$, the PWM outputs “not1” and “out1” are pulled to the ground reference level.

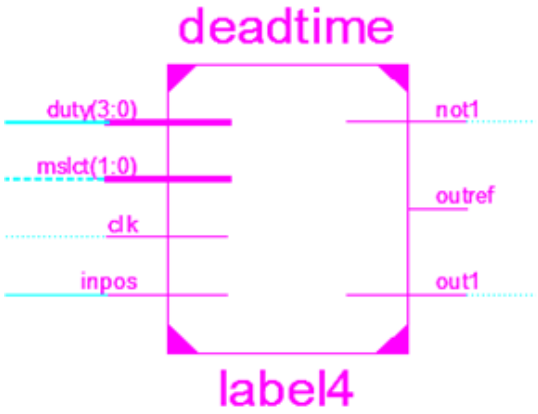

Figure 48 – Dead-time Module

3.2.8 Sseg

This module controls the 7-segment display. With respect to the content of the “mslct” input, in other words according to the selected mode, the corresponding notifications are displayed in four digit 7-segment display. In the DC mode, the duty cycle value at “datadc” input; in the AC mode, the modulating signal frequency at “dataf” input are displayed. This is done by the means of the output control signals “digit” and “segout” which drives the 7-segment display. Moreover, during the mode transitions, the selected mode is displayed for one second duration in the display. The “0000” value is displayed for the idle mode in which the PWM outputs are at the ground reference voltage level. The “dC” is shown for the DC mode, the “AC” for the AC mode and the "CIt" for the BIT mode.

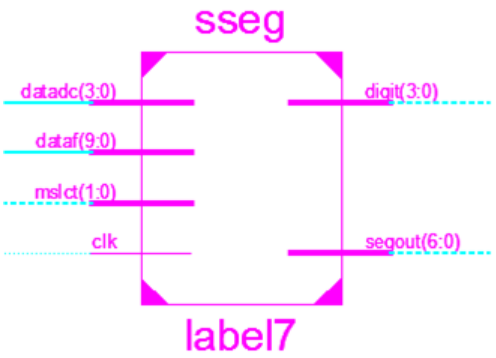

Figure 49 – Sseg Module

3.3 Module Simulations

3.3.1 DC Mode

The simulations have been made with the ISIM simulator of the Xilinx ISE v12.1. The DC mode PWM outputs are simulated firstly with the "dutyfreq" equals to "11010100". The first four (LSB) bits of this sequence corresponds to the duty cycle value of 40%. As can be seen in "Figure 50" below, this duty cycle value corresponds to a 20 us period for the switching frequency of 20 kHz. It is shown that the 500ns dead-band durations exist for each complementary PWM signals. Thus this decreases the actual duty cycle durations to 19.5us.

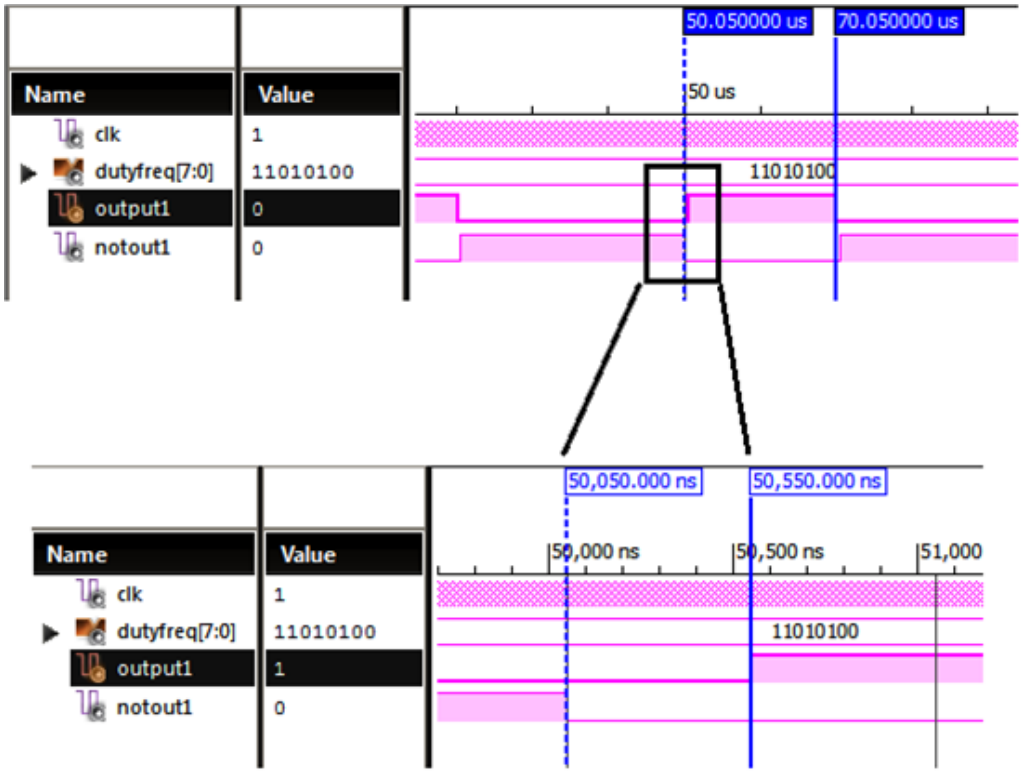

Figure 50 - DC Mode ISim Simulation

3.3.2 AC Mode

In the simulation results in “Figure 51” and “Figure 52” below, the triangular carrier signal is represented with the red waveform, the modulating signal with the black and the blue is for the PWM signal. In first simulation of which results are provided in “Figure 51”, the “dutyfreq” parameter is selected as “11010100”. The most significant two bits determine the modulation index and because they are “11”, the modulation index becomes 98%. The rest of the bits are reserved for the modulating signal frequency information. The value of “010100” is equal to 20 in decimal, therefore the modulating signal frequency is calculated as 500Hz+20*(5Hz)=600Hz.

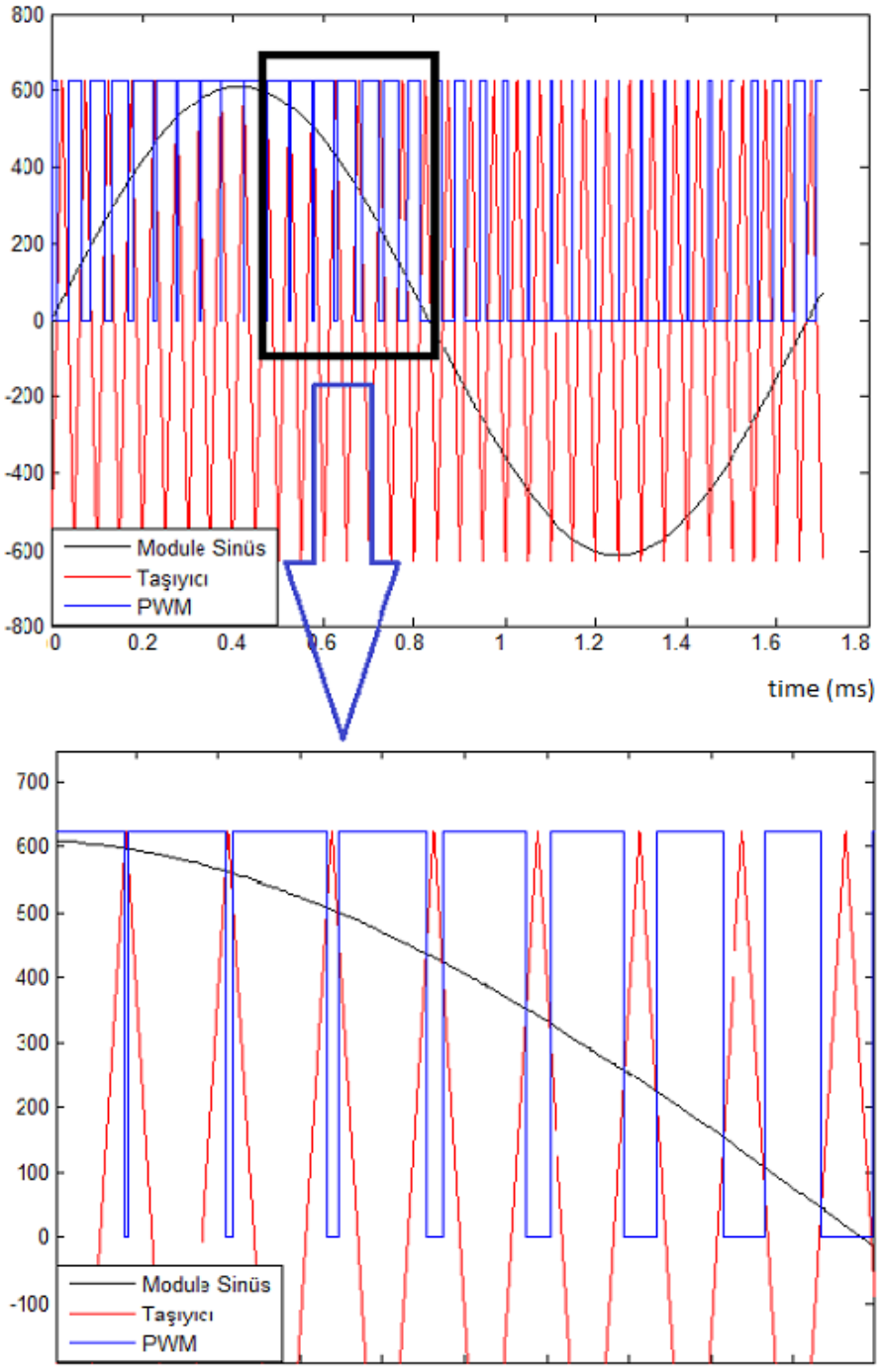

Figure 51 - AC Mode Simulation with Modulation Index=98% & Modulating Frequency=600Hz

For the simulation in "Figure 52Figure 52 - AC Mode Simulations with Modulation Index=50% & Modulating Frequency=700Hz", the "dutyfreq" is provided as

"01101000". This results in the modulation index of 50% and the modulating signal frequency of 700Hz.

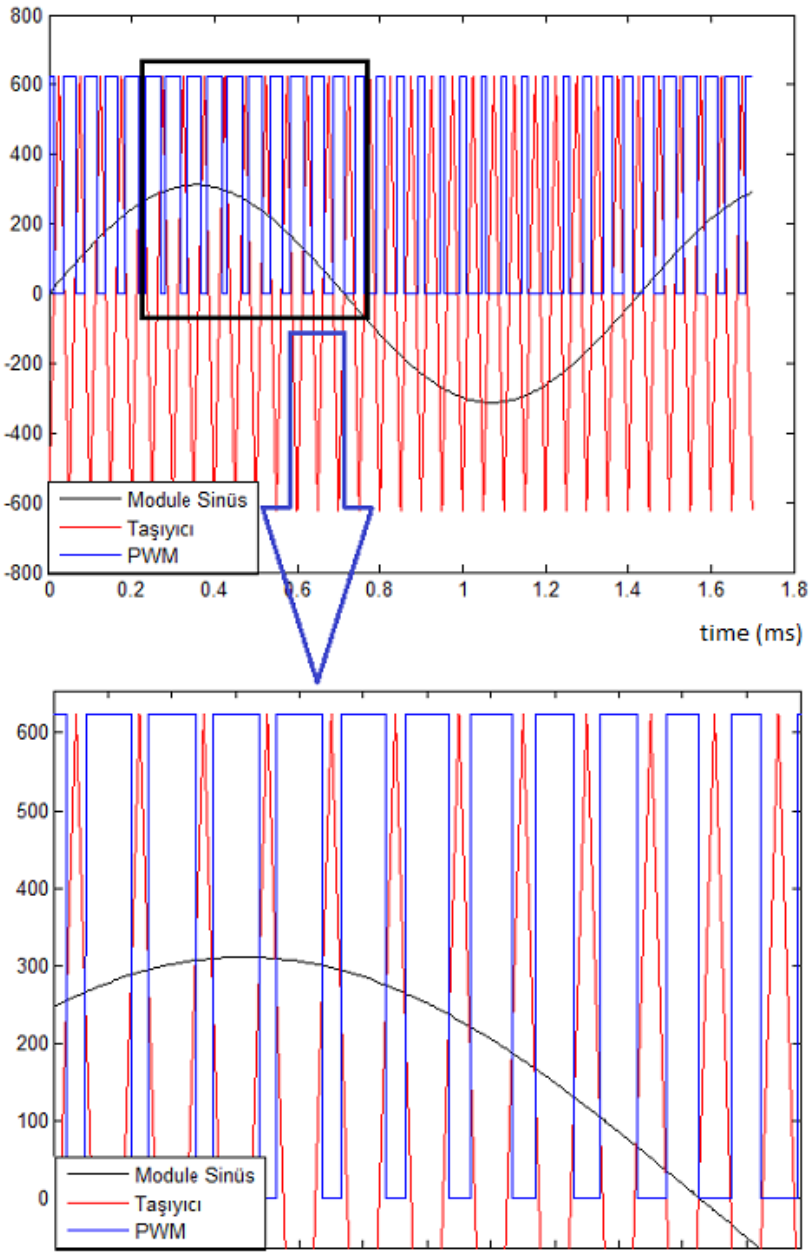

Figure 52 - AC Mode Simulations with Modulation Index=50% & Modulating Frequency=700Hz

3.4 Measurements

The measurements which will be provided in this section have been made at the PWM outputs of the FPGA board. These pins of the board has been open circuited as well.

3.4.1 DC Mode

These measurements have been done in the DC mode with a 30% duty cycle.

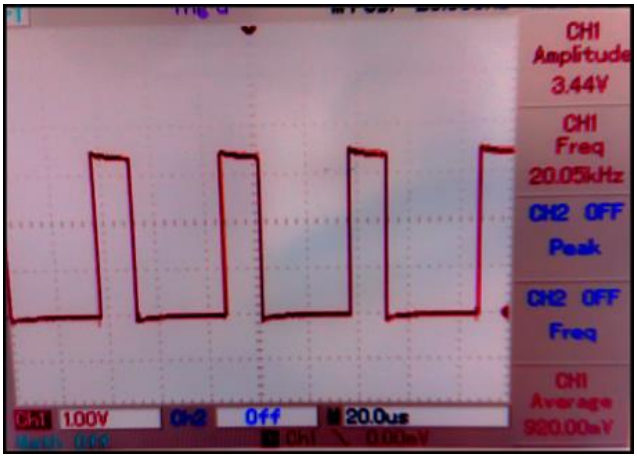

Figure 53 - DC Mode with 30% Duty Cycle

The dead-band with the duration of 500ns can be seen in following scope snapshots in “Figure 54” and “Figure 55”.

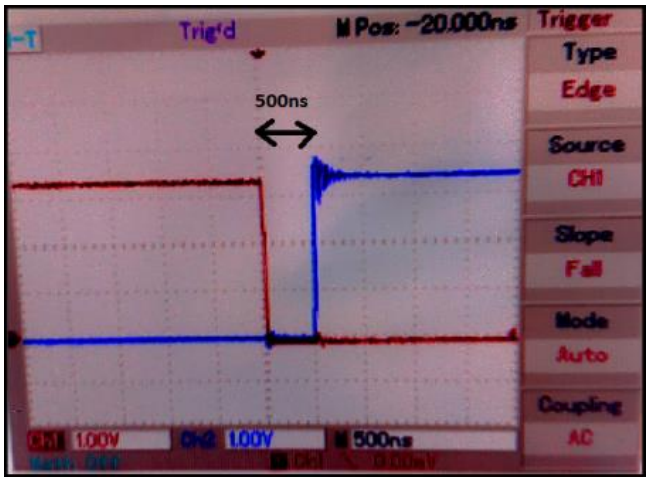

Figure 54 - Dead-Band

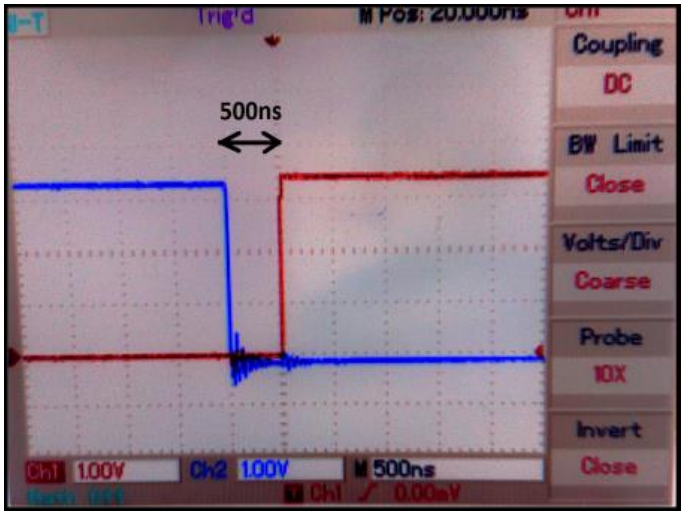

Figure 55 - Dead-band of Complementary Signal

3.4.2 AC Mode

The AC mode measurements have been made with a 700Hz modulating signal for the two different modulation indexes of 98% and 25%. Although the complementary signals are not shown here to visualize the dead-band, the same amount of the dead-band exists here as it was illustrated with the DC mode complementary PWM signal couples.

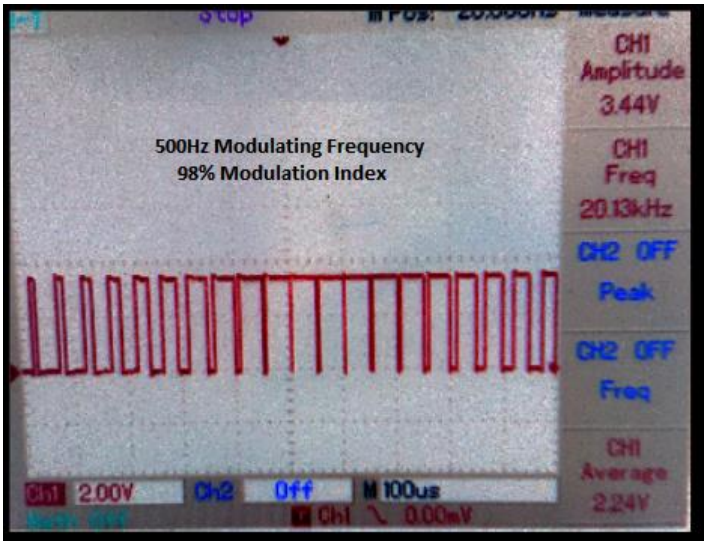

Figure 56 - AC Mode Measurement with 98% Modulation Index

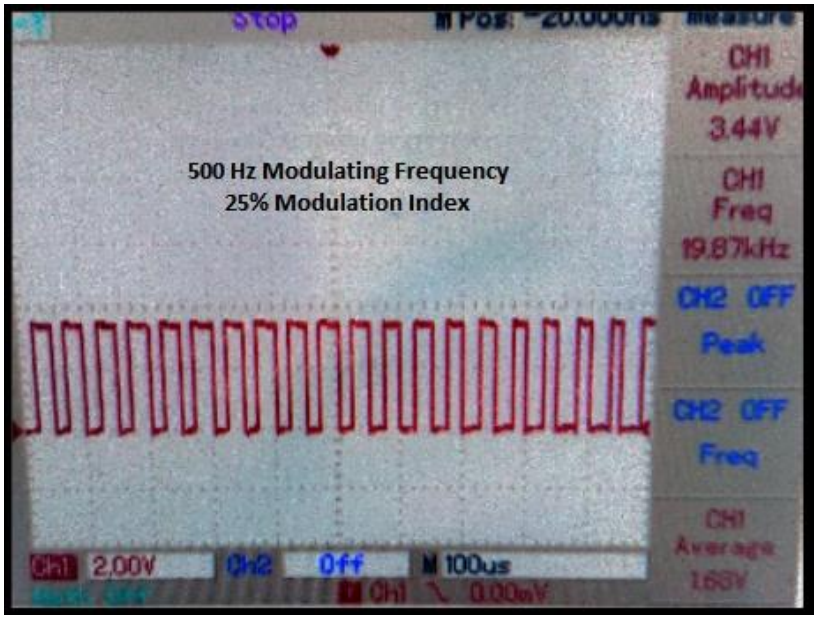

Figure 57 - AC Mode Measurement with 25% Modulation Index

3.4.3 BIT (Built-In Test) Mode

In the device interior test mode, either the DC mode PWM signal with the 98% duty cycle or the AC mode PWM signal with the 700Hz fundamental frequency and 98% modulation index will be provided to the outputs for the cycles of 10 seconds periods.

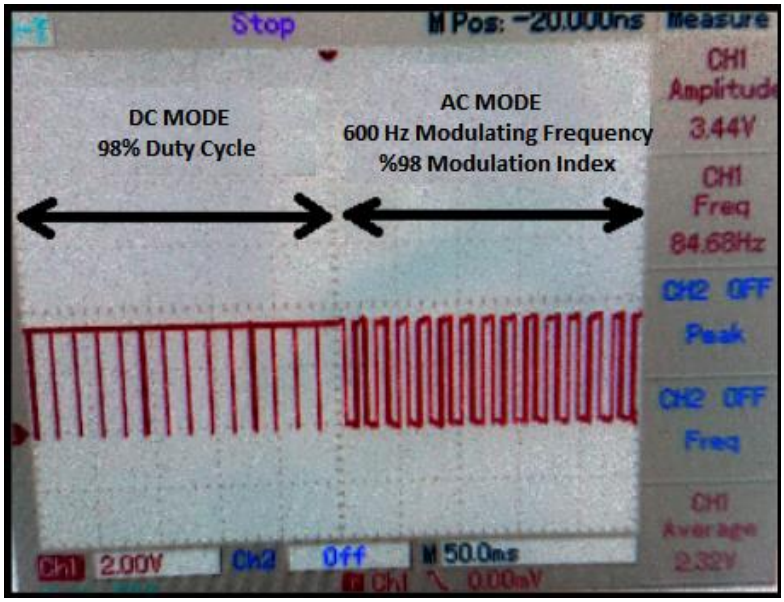

Figure 58 - BIT Mode

Chapter 4

Results and Discussion

In this section, the previously analyzed and digitally simulated PWM signals have been fed to the load coil. The resulting practical voltage and current waveforms will be evaluated.

4.1 Load Inductor Current and PWM Voltage Waveform Measurements

The current measurements of the load coil have been made for the two modes of the PWM with particular subsequent adjustments. The voltage has been measured with the portable oscilloscope "Agilent U1600A" which has a ground reference that is isolated from the mains ground. So, the one of the probe channels is connected across the output nodes of the driver circuitry to observe the potential difference across the load inductor differentially. The other channel is reserved for the measurements of the load current through the coil. This is done by measuring the voltage across a 1 Ω 11 Watt resistor connected in series with the coil.

4.1.1 DC Mode Measurements

The DC mode measurements have been made with a DC power supply voltage level of 45.6V. The measured load current values can be normalized as if a 48V supply is used, by simply multiplying the results with 48 and then dividing by 45.6 which are the corresponding supply levels. The measured load currents for the corresponding duty-cycles are given as the dual couples which provide exactly same magnitude of the current but in the opposite directions as can be seen in following scope snapshots.

(Note: The blue waveform corresponds to the output voltage and the red one does the load current):

DC Mode Measurement #1
***Duty Cycle…..:* 10%**
***Load Current..:* -1.26A**

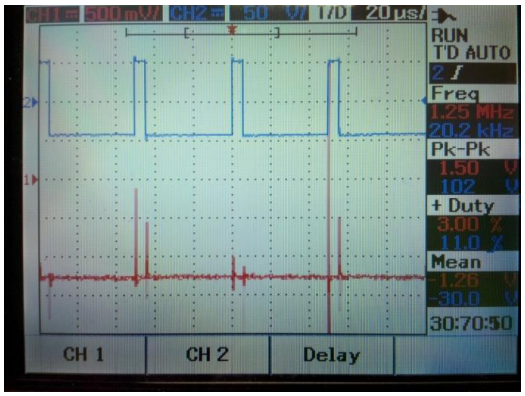

Figure 59 - DC Mode Measuremen#1

DC Mode Measurement #1
***Duty Cycle…..:* 90%**
***Load Current..:* 1.26A**

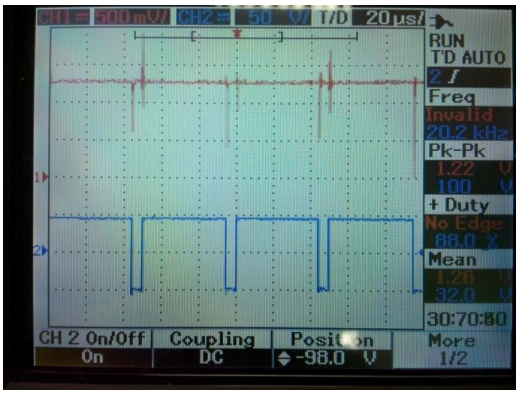

Figure 60 - DC Mode Measurement#2

DC Mode Measurement #3
***Duty Cycle…..:* 20%**
***Load Current..:* -945mA**

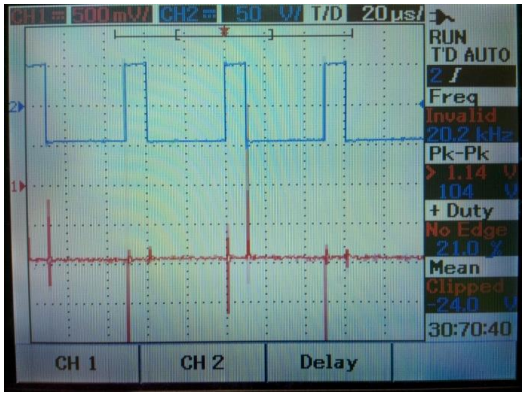

Figure 61 - DC Mode Measuremen#3

DC Mode Measurement #4
***Duty Cycle…..:* 80%**
***Load Current..:* 952mA**

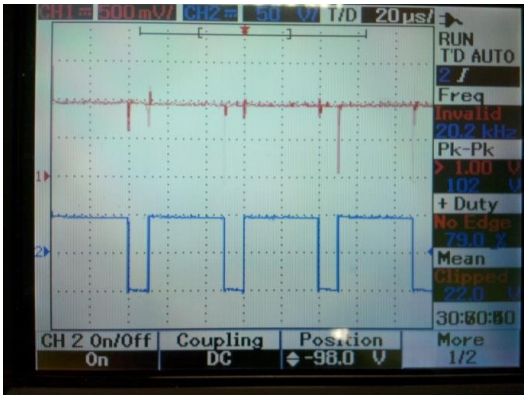

Figure 62 - DC Mode Measuremen#4

DC Mode Measurement #5
Duty Cycle…..: **30%**
Load Current..: **-600mA**

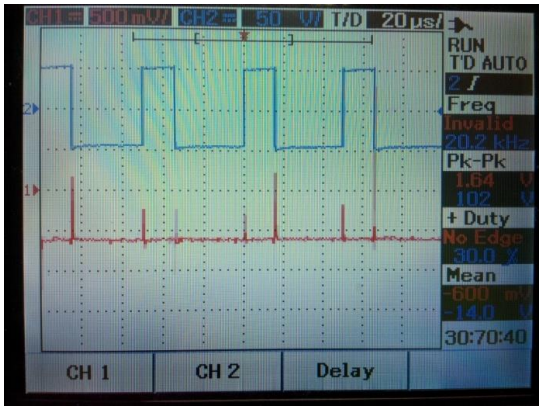

Figure 63 - DC Mode Measuremen#5

DC Mode Measurement #6
Duty Cycle…..: **70%**
Load Current..: **600mA**

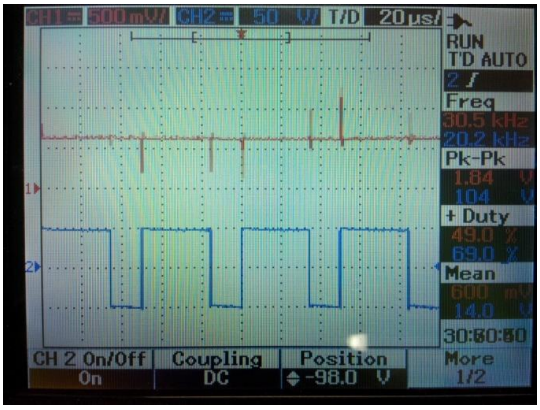

Figure 64 - DC Mode Measuremen#6

DC Mode Measurement #7
Duty Cycle…..: **40%**
Load Current..: **-280mA**

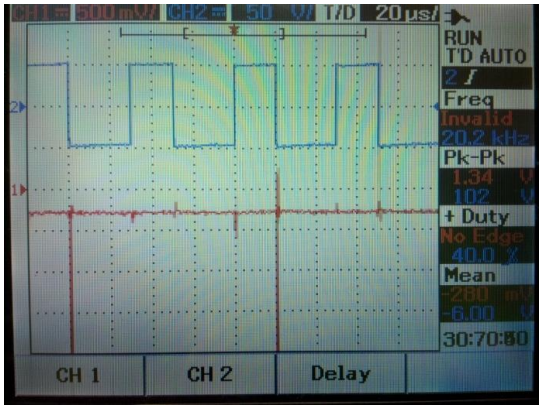

Figure 65 - DC Mode Measuremen#7

DC Mode Measurement #8
Duty Cycle…..: **60%**
Load Current..: **280mA**

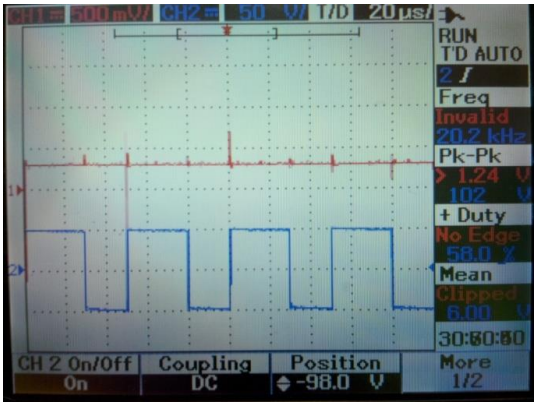

Figure 66 - DC Mode Measuremen#8

DC Mode Measurement #9
Duty Cycle…..: **98%**
Load Current..: **-1.5A**

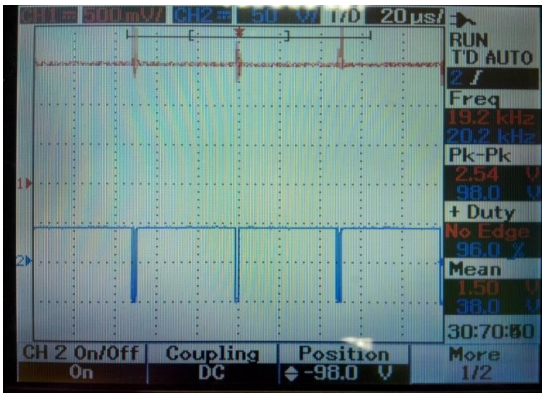

Figure 67 - DC Mode Measuremen#9

The current waveforms in the figure above, looks alright unless the spikes occur at the switching instants. This phenomenon will be analyzed in more detail in the following sections.

4.1.2 AC Mode Measurements

The measurement setup is the same as it is in the DC mode measurements. The frequencies of the modulating signals are adjusted as 500Hz, 600Hz and 700Hz while the modulation indexes take the values of 25%, 50% 75% and 98%. Additionally, because the fundamental period of the load current is much bigger than the PWM switching frequency, the voltage across the output is given in a different scope snapshot.

4.1.2.1 *500 Hz Modulating Frequency*

AC Mode Measurement #1

Modulation Index…….: **25%**

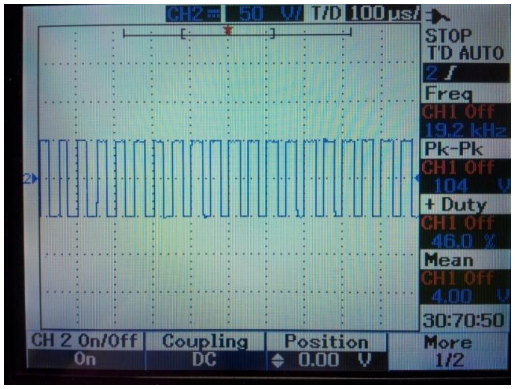

Figure 68 - AC Mode Measuremen#1 / Load Voltage

Load Current (Pk-Pk)...: **70mA**

Figure 69 - AC Mode Measuremen#1 / Load Current

AC Mode Measurement #2

Modulation Index…....: **50%**

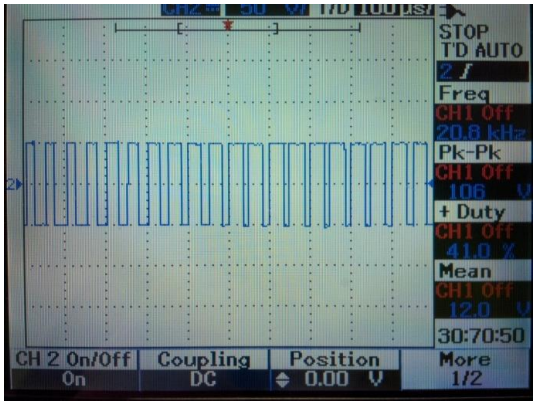

Figure 70 - AC Mode Measuremen#2 / Load Voltage

Load Current (Pk-Pk)...: **120mA**

Figure 71 - AC Mode Measuremen#2 / Load Current

AC Mode Measurement #3

Modulation Index…....: **75%**

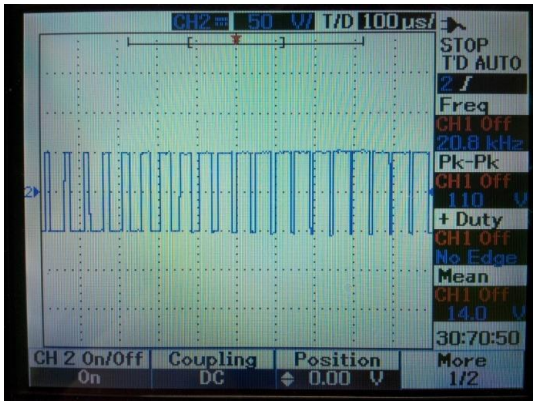

Figure 72 - AC Mode Measuremen#3 / Load Voltage

Load Current (Pk-Pk)...: **200mA**

Figure 73 - AC Mode Measuremen#3 / Load Current

AC Mode Measurement #4

Modulation Index…....: **98%**

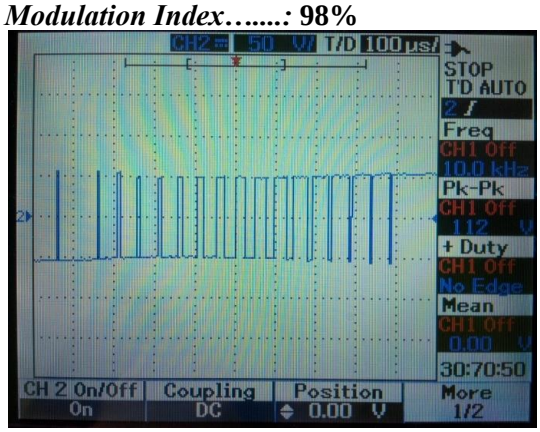

Figure 74 - AC Mode Measuremen#4 / Load Voltage

Load Current (Pk-Pk)...: **250mA**

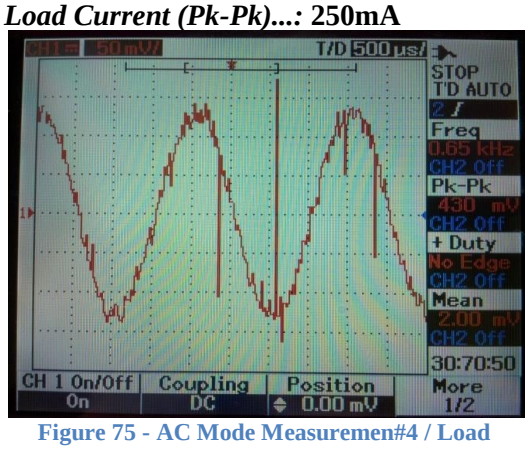

Figure 75 - AC Mode Measuremen#4 / Load Current

4.1.2.2 *600 Hz Modulating Frequency*

AC Mode Measurement #5

Modulation Index…….: **25%**

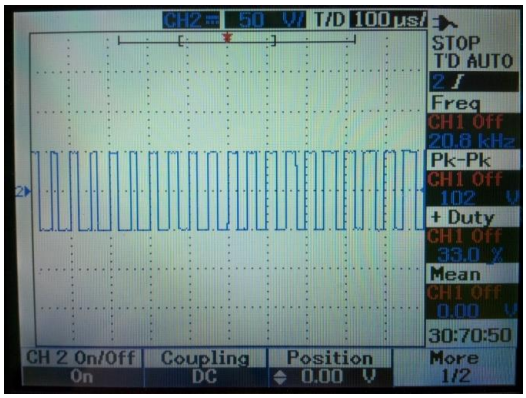

Figure 76 - AC Mode Measuremen#5 / Load Voltage

Load Current (Pk-Pk)...: **50mA**

Figure 77 - AC Mode Measuremen#5 / Load Current

AC Mode Measurement #6

Modulation Index…….: **50%**

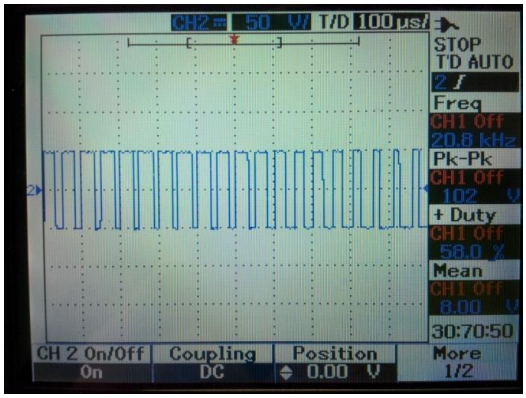

Figure 78 - AC Mode Measuremen#6 / Load Voltage

Load Current (Pk-Pk)...: **110mA**

Figure 79 - AC Mode Measuremen#6 / Load Current

AC Mode Measurement #7

Modulation Index…….: **75%**

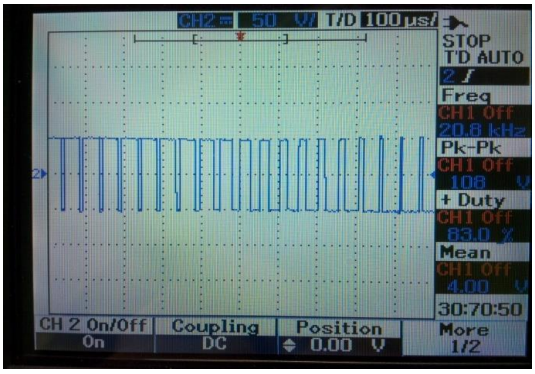

Figure 80 - AC Mode Measuremen#7 / Load Voltage

Load Current (Pk-Pk)...: **160mA**

Figure 81 - AC Mode Measuremen#7 / Load Current

AC Mode Measurement #8

Modulation Index…….: **98%**

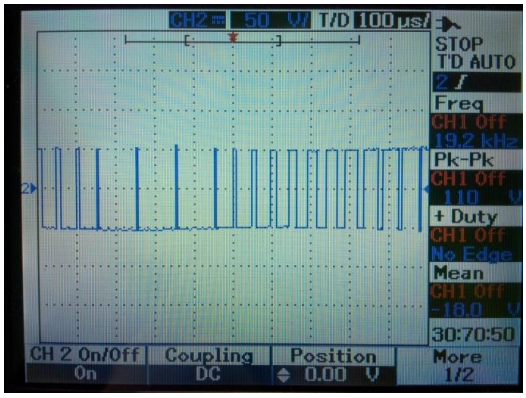

Figure 82 - AC Mode Measuremen#8 / Load Voltage

Load Current (Pk-Pk)...: **210mA**

Figure 83 - AC Mode Measuremen#8 / Load Current

4.1.2.3 *700 Hz Modulating Frequency*

AC Mode Measurement #9

Modulation Index…….: **25%**

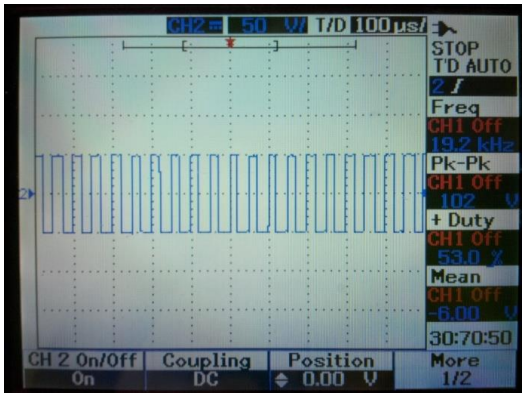

Figure 84 - AC Mode Measuremen#9 / Load Voltage

Load Current (Pk-Pk)...: **50mA**

Figure 85 - AC Mode Measuremen#9 / Load Current

AC Mode Measurement #10

Modulation Index…….: **50%**

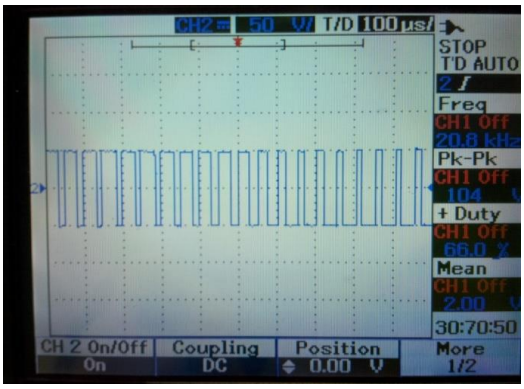

Figure 86 - AC Mode Measuremen#10 / Load Voltage

Load Current (Pk-Pk)...: **88mA**

Figure 87 - AC Mode Measuremen#10 / Load Current

AC Mode Measurement #11

Modulation Index…….: **75%**

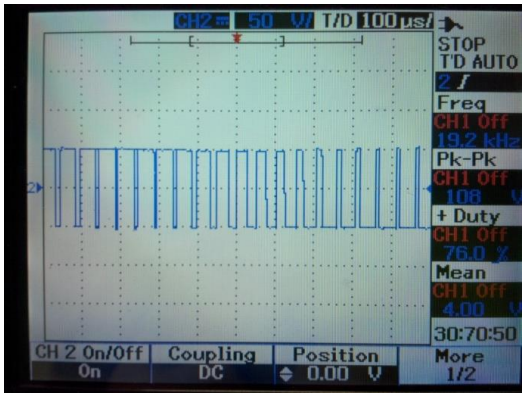

Figure 88 - AC Mode Measuremen#11 / Load Voltage

Load Current (Pk-Pk)...: **140mA**

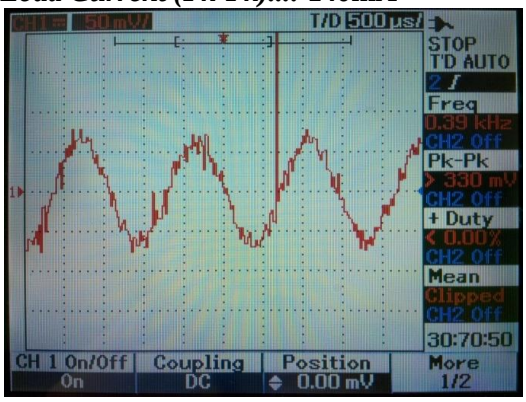

Figure 89 - AC Mode Measuremen#11 / Load Current

AC Mode Measurement #12

Modulation Index…….: **98%**

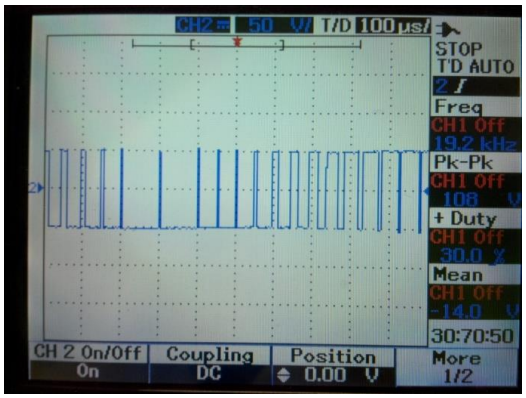

Figure 90 - AC Mode Measuremen#12 / Load Voltage

Load Current (Pk-Pk)...: **180mA**

Figure 91 - AC Mode Measuremen#12 / Load Current

As in DC mode measurements, there are some spiky disturbances in the load current waveforms which will be analyzed in the next section. Some other deductions can be made as follows: the level of the fundamental component of the load current for 600 Hz 98% modulation index case is around 100mA which is similar to the results of the corresponding circuit simulation in "Figure 27". As the fundamental (modulating) frequency of the PWM signals increase from 500Hz to 700Hz, the level of the fundamental component of the current decreases. This is expected because of the low pass characteristic of the load inductor in this band. For the same modulating frequency, the current waveforms of the measurements with higher modulation index look smoother. This is not because of lowered levels of the ripple amplitudes but

because of the increased level of the fundamental component. It is like improving the signal-to-noise ratio by increasing the signal level while the noise level stays the same.

4.2 Load Current Analysis with the Coil Impedance

In this section the spikes which are seen at the output current waveforms will be analyzed by considering the influence of the load coil impedance.

The switching events are the primary causes of the "electromagnetic interference" with the excitation of the parasitic elements of the circuit layout by these switching events [14]. This is because of the fast rise times of the pulse edges of the PWM signals which involve high "dv/dt" and "di/dt" [15, 16]. Thus, with these characteristics of the drive signals, a high number of harmonic components are observed in the output waveforms [14].

The excited parasitic elements, are the parasitic inductance and the capacitance in device modules, passive components, the leads of electrical components and their interconnections [15]. The EMI noise splits up into two as the differential (DM) or the common mode (CM) with respect to the path it follows through the circuitry [16]. The common mode (CM) noise can either appears as radiated or conducted in the ground reference line, as an electrical interference with respect to a reference ground [16]. The conducted CM noise current frequency drives the radiated EMI which grows out of the large loop antenna which is formed by the unshielded phase leads and the ground line [16]. On the other hand, the conducted CM noise is excited by the capacitance constituted between the both of the phase conductors to the ground reference [16]. This coupling provides a low impedance path for the frequency components which make such fast rising pulse edges possible for the modulated signal [16]. As a result, the cable charging currents flows by the means of the such capacitive coupling of the load inductor phase conductors [16]. Unless they are shielded, any two conductors will have a capacitive interaction [16]. The capacitor theory states that it is more probable for them to allow a current flow through the

capacitance among themselves, even it is small when the excitation frequency is high accordingly [16].

On the other hand, the current path of the differential EMI noise substantially consists of the parasitic inductance of devices, the bulk capacitor, and interconnects [15]. This current follows through a path along the load inductor windings, the winding capacitance of the same inductor, and ending at the dc power supply bus [15]. In "Figure 92 to Figure 99Figure 92 - Resistance of the Coil vs. Frequency (100Hz-100Khz)", the impedance measurements of the load coil are provided.

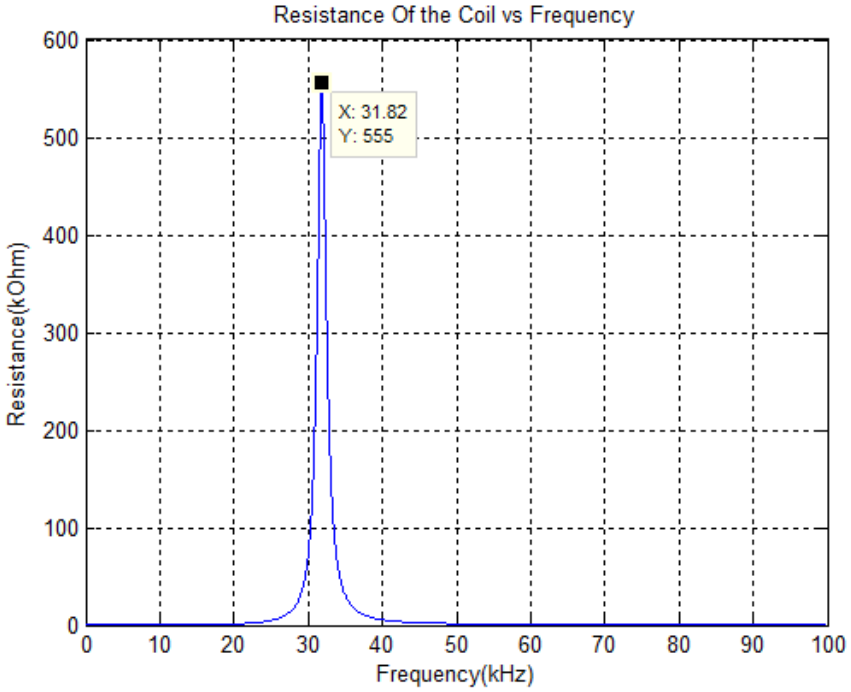

Figure 92 - Resistance of the Coil vs. Frequency (100Hz-100Khz)

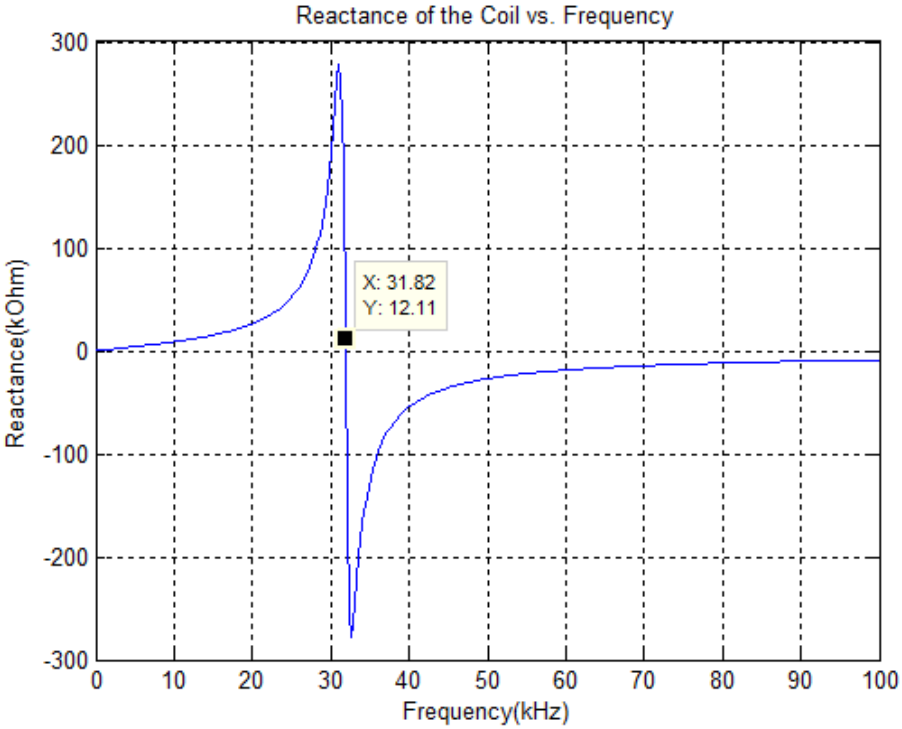

Figure 93 - Reactance of the Coil vs. Frequency (100Hz-100Khz)

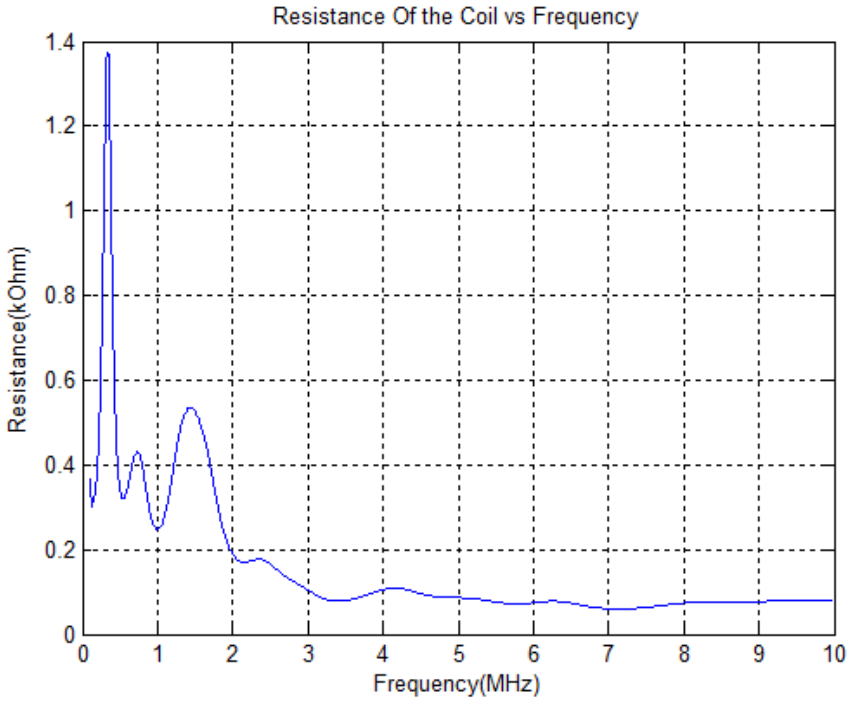

Figure 94 - Resistance of the Coil vs. Frequency (100kHz-10Mhz)

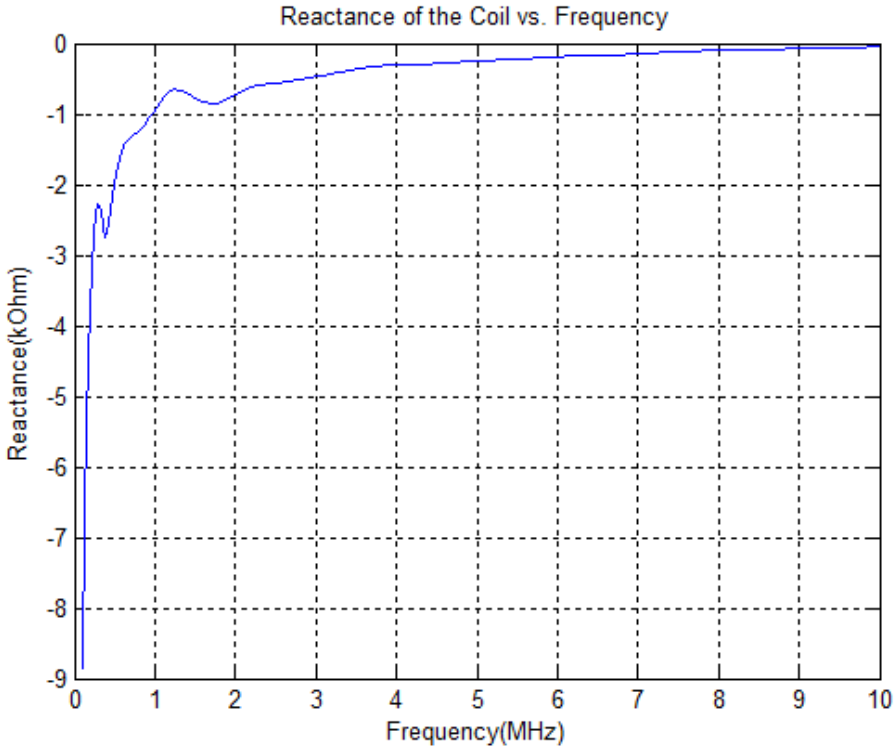

Figure 95 - Reactance of the Coil vs. Frequency (100kHz-10Mhz)

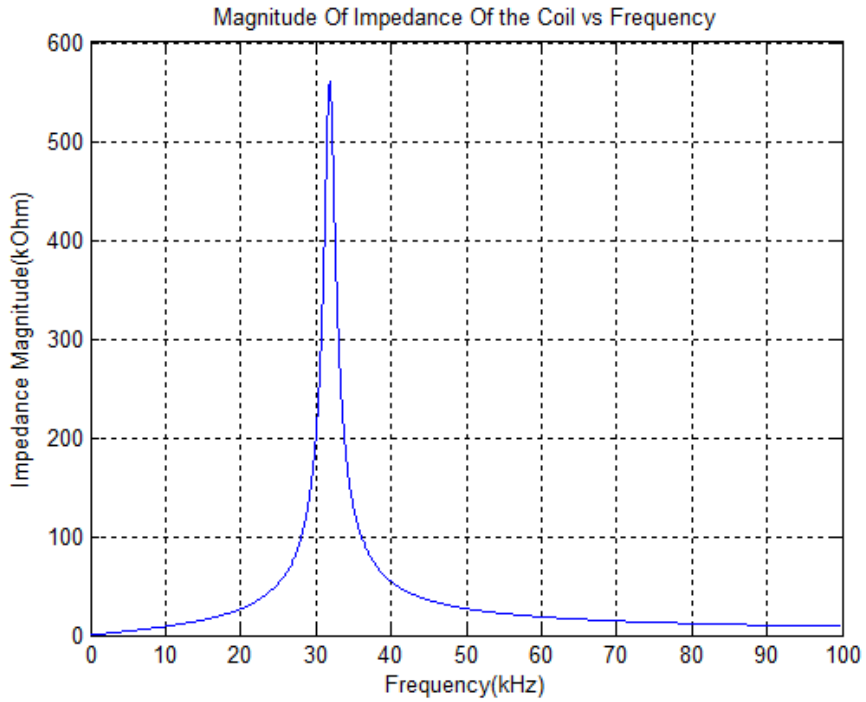

Figure 96 - Impedance Magnitude of the Coil vs. Frequency (100Hz-100khz)

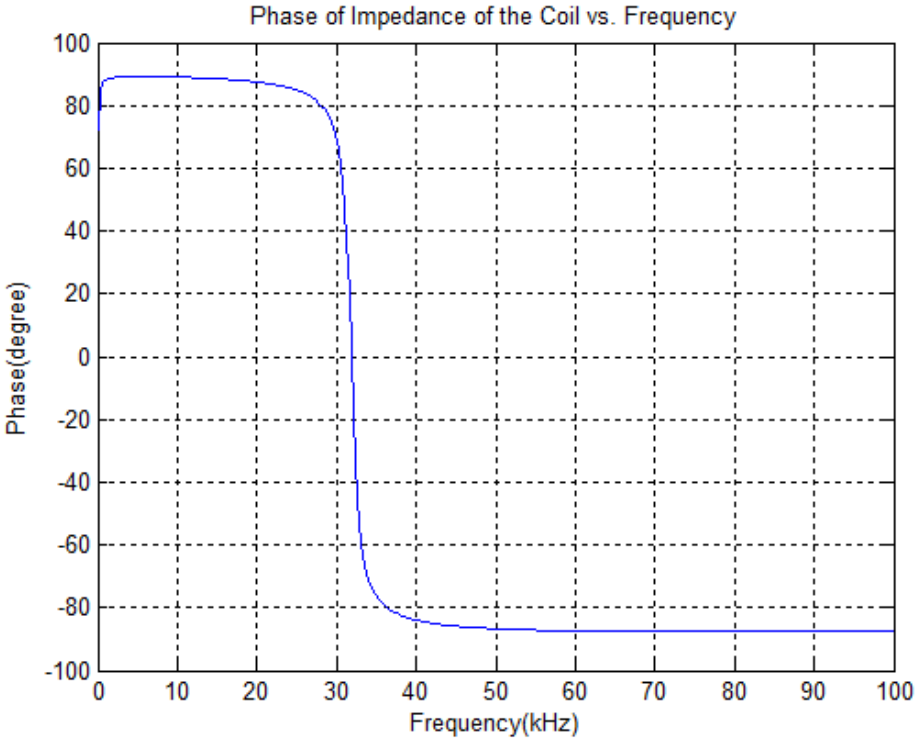

Figure 97 - Phase of Impedance of the Coil vs. Frequency (100Hz-100khz)

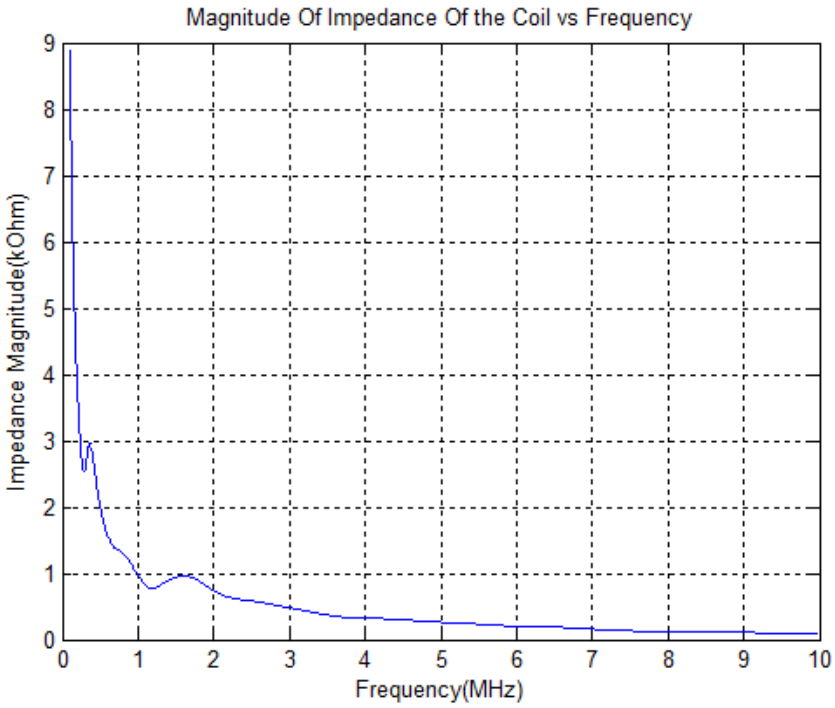

Figure 98 - Impedance Of The Coil vs Frequency (100kHz-10Mhz)

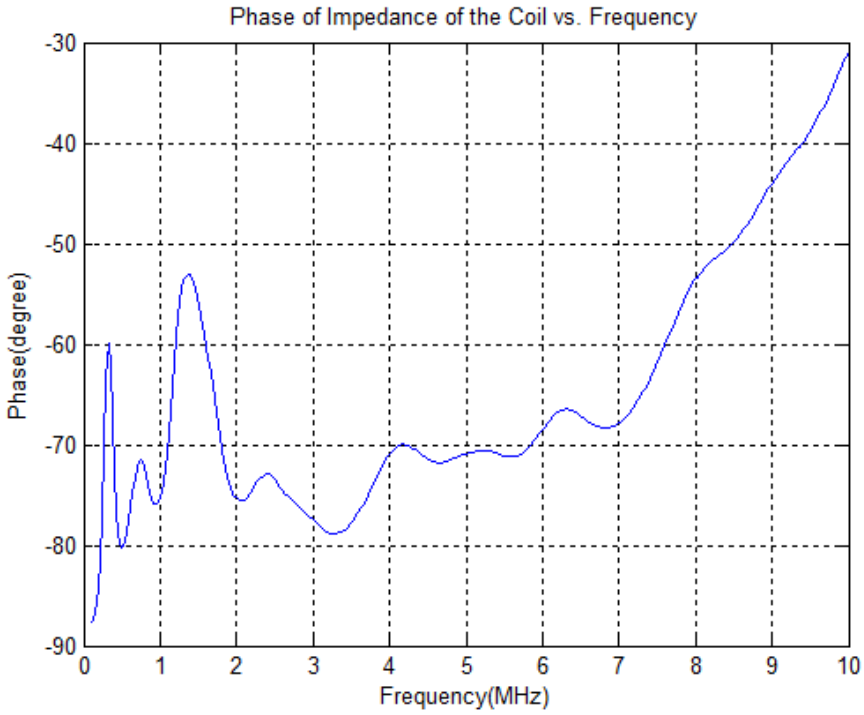

Figure 99 - Phase of Impedance of the Coil vs. Frequency (100kHz-10Mhz)

As can be seen in the figures above, the load coil has a resonance at around 32 kHz and for the excitation with the signals which have higher frequencies than this; the inductor behaves like a capacitor. This is why the ripples and the spikes are observed in the load current measurements which have the content of the signal components at the higher frequencies out of this resonance band. The spectral content of the current is calculated by using the calculated spectrum of the PWM drive signals and the measured coil impedance as in “Figure 100” and “Figure 101” below.

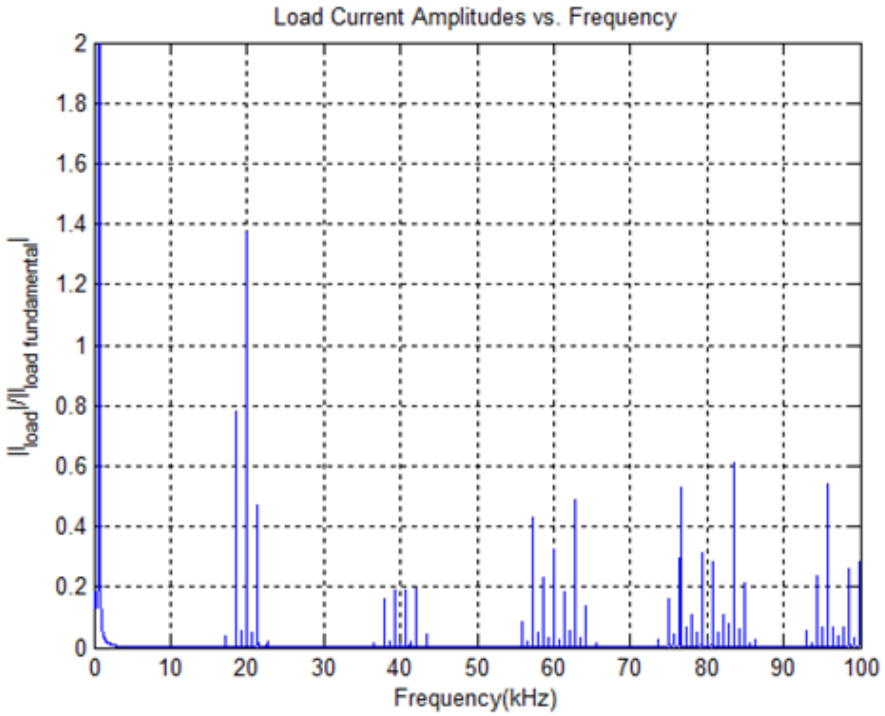

Figure 100 - Load Current Amplitude vs. Frequency (100Hz-100kHz)

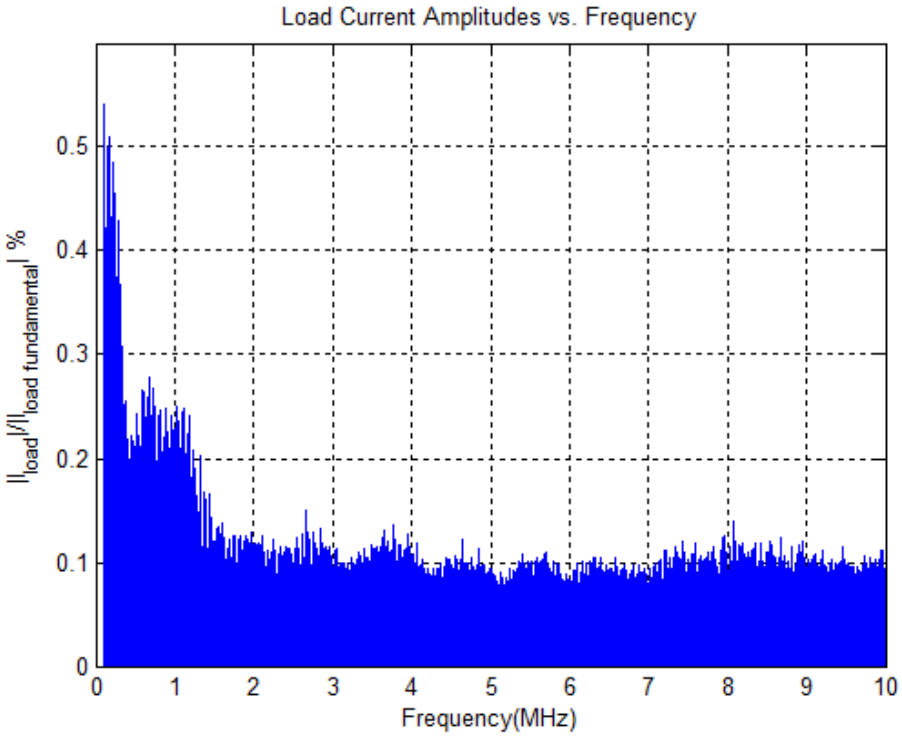

Figure 101 - Load Current Amplitude vs. Frequency (100kHz-10MHz)

In addition, the behavior of the inductor resistance around the resonance as in “Figure 92” and “Figure 94” can be explained by skin and proximity effects [17]. They cause the parasitic winding resistance to increase with respect to the frequency [17].

The real inductors have the equivalent circuit model with an inductance in serial with a resistance, and a self-capacitance which is in parallel with the whole serial RL network [17]. This self-capacitance represents the lumped element model of the distributed parasitic capacitance of the inductor windings [17].

4.2.1 Spice Simulations of the Equivalent Circuit Model of the Inductor

The following simulations have been made for inspecting the current flowing through the coil by employing the inductor model which can be seen in “Figure 102” below. The model has the measured inductance of 126mH, the measured serial 25Ohm DC resistance (not AC) and the self-capacitance of 220pF which is calculated from the formulas for finding the RLC resonance frequency. In the simulations, the h-bridge is replaced by the pulse sources serves for the same purpose. These two voltage sources provide DC mode PWM signals with 70% and 30% duty cycles respectively. They also simulate the turn-off durations of the transistors which can be taken as 60ns as in “Figure 35”. This duration is used to configure the rise and the fall time of the pulses.

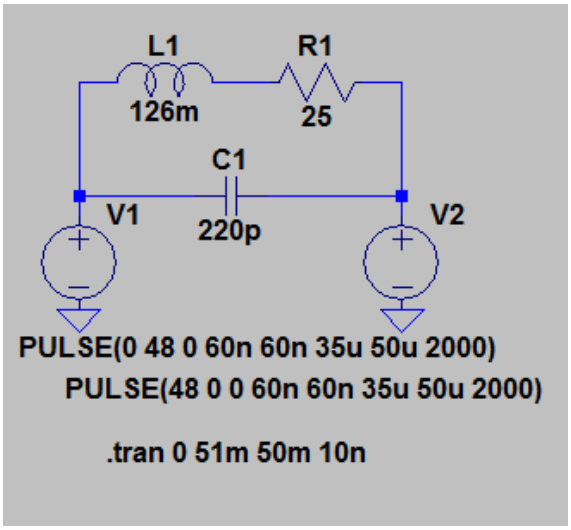

Figure 102 - Inductor Equivalent Circuit Model Simulations

In “Figure 103” below, the simulation result are provided for the transient analysis of the steady state current which are flowing through the inductor model. The pink waveform shows the current through inductance and the cyan is for the current of the parallel self-capacitance. As seen in the figure below, the spiky components of the load coil current are generated by the excitation of the parallel self-capacitance of the coil with voltage pulses. The rise and fall times of the voltage level transitions are 60ns for the pulses in this case. Because the current through the self-capacitance is the derivative of the voltage across this capacitance, the waveform of its current will contain spiky components. However, the inductive part of the coil has none of such current components. Therefore the effects of these distortions are not observed in generated magnetic fields.

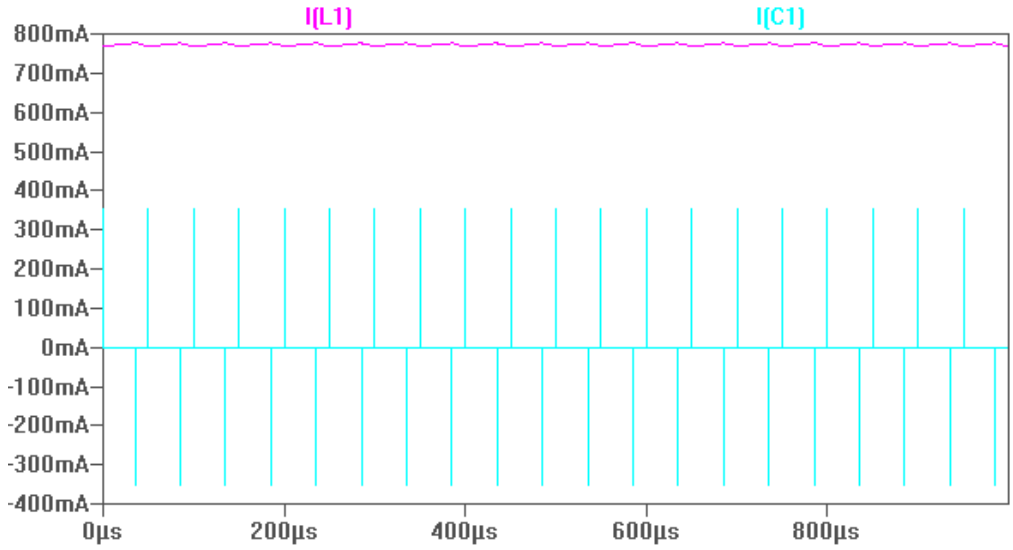

Figure 103 - Inductive and Capacitive Currents Of the Real Inductor

Further analysis of the equivalent circuit model can be done by making an AC analysis simulation with the circuit in “Figure 104” below.

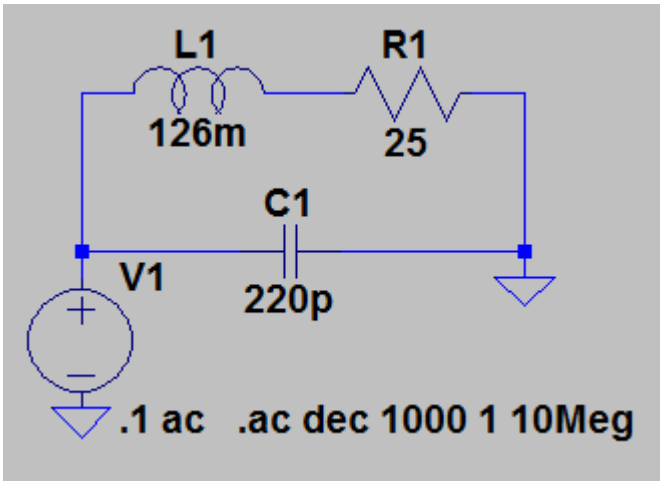

Figure 104 - AC Analysis Of The Real Inductor Model

The results which are given in "Figure 105" below are a bit different than the coil impedance measurements suggest. Firstly, the attenuation levels are different. This is because the real part of the impedance varies for frequency in practice as well as the imaginary part. The AC resistance peaks at the resonance frequency which can be seen in the corresponding impedance graphs. These variations are caused by the proximity and the skin effect [17]. The winding technique is highly influential also. Secondly, in practice, the phase shifts between the voltage and the current of the same frequency components differ with the frequency, not in a proper fashion as in the figure below. After the resonance frequency, the phase difference is seen to be almost flat here. In practice, the (capacitive) current components at those frequencies have different phases with respect to the each other's and the superposition of these signals results in the varying levels of the current spikes for different switching periods.

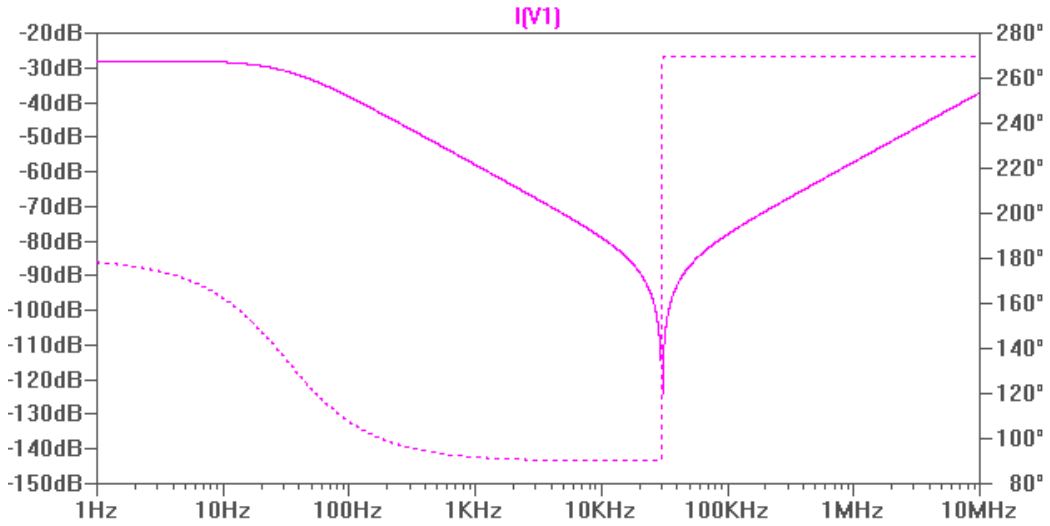

Figure 105 - Frequency Response of the Model

The spikes which are caused by differential and common mode EMI noise may result insulation detriment and may lead even the failure of the inductor [15]. Some precautions can be taken to prevent this situation, like minimizing the loop areas and the parasitic inductances in the circuit layout [14]. The inter-turn capacitance of the output load inductor could be decreased by using wires with rather thick insulations for the windings [14]. To reduce the CM noise further, specially designed cables can be used which have shields around to disrupt the capacitive coupling between phase lines [16]. These cables also include ground conductors which have smaller impedances at the EMI frequencies than the actual ground grid [16]. The difference is in the several orders of magnitude to be able make the dc power bus free from the noise [16]. For handling the radiated EMI noise, the appropriate amount of spacing between circuit equipments can be provided [16]. This also decreases the coupling capacitances between the lines and results in reduction in conducted EMI noise [16]. The use of shielded components and cables can also be applied to prevent electromagnetic interaction between lines which forms an antenna [16].

However; every additional efforts for reducing the EMI noise which emanates from an inverter, have to outweigh the required cost [14]. If it is still safe for the circuit to

operate or the levels of EMI noise stays in the limits imposed on, some of the precautions may not to be applied [14].

As mentioned earlier, during the turn-off of power MOSFETS, current snubbers are not required [18]. However, voltage clampers can be benefited for limiting the magnitude levels of the voltage spikes caused by stray inductances during the switching transitions [18]. The voltage clamps also manage the "dv/dt" across the device in their turning-offs [18]. These all only serve the purpose of not violating the corresponding constraints [18]. This is because the power MOSFETS do not suffer the second breakdown and they can safely withstand high "dv/dt" levels as thousands of volts per microsecond [18].

From the explanation above, it is deduced that the power MOSFET switches can operate safely under proper levels of EMI noise which is generated by the circuit itself. It is also tested that such noise doesn't harm the load inductor by causing premature insulation fails. The system which is designed in the scope of this work, has run safely for "1 hour". The coil temperature has reached a value around 130^{o}C. If it is considered that, the system will only be operated for 8 minute underwater; it will be free from thermal considerations. Nevertheless; the limits on EMI noise levels, even when circuits operate safely, would become stricter for the increasing number of converters or inverters which are connected to the same supply networks [14]. However, for the system here, only an inverter resides with a dedicated battery.

On the other hand, the effect of the EMI noise over the underwater target field will be investigated following even they are not predicted to appear in this produced magnetic fields. Even the prediction is not valid; it is proven with the COMSOL® simulations of which results are provided in "Table 3" below that the acceptable levels of magnetic flux density fundamental component and distortion values can be produced at "5 meter" away from the load coil on its radial axis. At such distances, frequency components which are involved in the spiky load currents cannot generate comparable levels of magnetic fields with respect to the fundamental component of

the current. This is because the seawater is a lossy medium with the conductivity "σ" around "4 S/m". It gets harder for the higher frequency components of the electromagnetic energy to penetrate as the following absorption coefficient suggest:

$$\alpha = 17.3x10^{-3}(\sigma f)^{1/2} \ \frac{dB}{m} \qquad (53).$$

The coil which is used in the simulations, of which results can be seen in the table below, has "1400" windings. Each of these windings is assumed to have an AC current with 1A peak.

Frequency	**Magnetic flux density norm (nT)** at 1m distance on the radial axis	**Magnetic flux density norm (nT)** at 5m distance on the radial axis
500 Hz	1536.25	6.6083
700 Hz	1536.16	6.604
20 kHz	1460.23	3.364
40 kHz	1369.06	1.458
60 kHz	1284.56	0.730
100 kHz	1137.24	0.226
200 kHz	864.65	0.0227
500 kHz	444.22	1.9942e-4
1 MHz	187.62	8.367e-7
2 MHz	49.74	3.189e-10
50 MHz	2.208e-7	1.127e-52

Table 3 - Magnetic Flux Density Norm at 1m and 5m Distances on the Radial Axis

The situation is a bit tedious for the carrier frequency component as seen in the table above. Magnetic flux density produced by this frequency component of the current is almost one half of the fundamental did. However, the simulations are made by assuming AC inductive currents flow through the windings for each frequency components. However, 20 kHz switching frequency component of PWM waveform is the one with the second highest magnitude level which is about half of the fundamental's. Moreover, the components at the switching frequency and its multiple are attenuated according to the load coil impedance. It can be interpreted from the impedance magnitude measurements that the attenuation at the carrier frequency is:

$$| Z(20kHz)| / | Z(600)Hz| = (26650.3\ \Omega) / (482.27\ \Omega) = 55.26$$

times bigger than it is at the fundamental frequency. Thus, the levels of the magnetic fields which are generated by the excitation of the coil with the currents at carrier harmonics will be negligible as well. Moreover, such high frequency current components are already predicted not to flow through the inductive part significantly but through the self-capacitance of the coil. Thus no magnetic fields components are observed at the target fields.

By also considering the safe circuit operation under the EMI noise, the use of switching-aid networks is dismissed most certainly after the magnetic field simulations. Because the passive switching-aid networks (snubbers) have the effect of reducing the rise times of the pulse edges by suppressing only the high frequency components to some extent but without influencing much the low-order harmonics of the fundamental component and the low order switching harmonics, which are interest primarily [7]. Moreover, when these passive filters are used the overall power dissipation of the circuit is not reduce; since the power dissipated with such unwanted high frequency signals are only transferred to the switching-aid networks [19]. Thus, they cannot increase the fundamental voltage component at the output rather filters (by suppressing opposite directed fundamental harmonics) the harmonics which are not cared much in the underwater applications of the electromagnetic field generation like in this work. Moreover, the device is a single use remote system which is constrained to be built with the minimum number of components to keep number of points of failure minimum. Because the system will then be cased as a mobile device, it is also important to save space. Thus, no snubber or other kind of switching aid networks are used to handle the switching transition effects.

4.3 Magnetic Field Measurements

The measurements which are given here have been done by my fellow Fatih Emre Şimşek. A magnetometer, "Spectramag-6" of Bartington Inc., has been used which is designed for the measurements of the spatial components of the magnetic flux densities in the frequency band of 0-3kHz at three dimension in space.

The measurements have been executed indoor and 1 meter away from the load coil which is the magnetic field source of the system. The magnetic sensor has been positioned at different angles with respect to the radial axis of the coil in horizontal plane. For example the angle value of "90^{o}" corresponds to the radial axis of the coil. The "0^{o}" represents the plane which is perpendicular to this radial axis which divides the coil into two equal parts.

4.3.1 DC Fields

For the DC magnetic field measurements, the duty cycle parameter of the PWM signals has been adjusted as 80%. A DC power source which supplies 49.8V has been constituted by using four 13V batteries. So the DC load current of 1.160 Amps has got flowing through the coil.

Because earth also has a DC magnetic (magneto-static) field, then its effect must be removed from magnetic field measurements. For this purpose, the first 20 seconds duration of total measurement time, which is 1 minute, is employed for measuring corresponding spatial component level of the earth magnetic field. At this time the coil is not driven by the circuitry. Then, the coil is excited with the DC mode PWM voltage signal for the following 20 seconds. The last 20 seconds of the minute is again reserved for earth magnetic field measurements.

After each 1 minute long measurements which have been taken for the different angle positions of the sensor, the resulting field data has been filtered to suppress the disturbances of the 50Hz main and its harmonics. The spatial components of the magnetic flux densities are processed by a low pass filter with 23Hz cutoff which is provided by the user GUI of the magnetometer. The examples of resulting waveforms are provided in "Figure 106", "Figure 107" and "Figure 108" below.

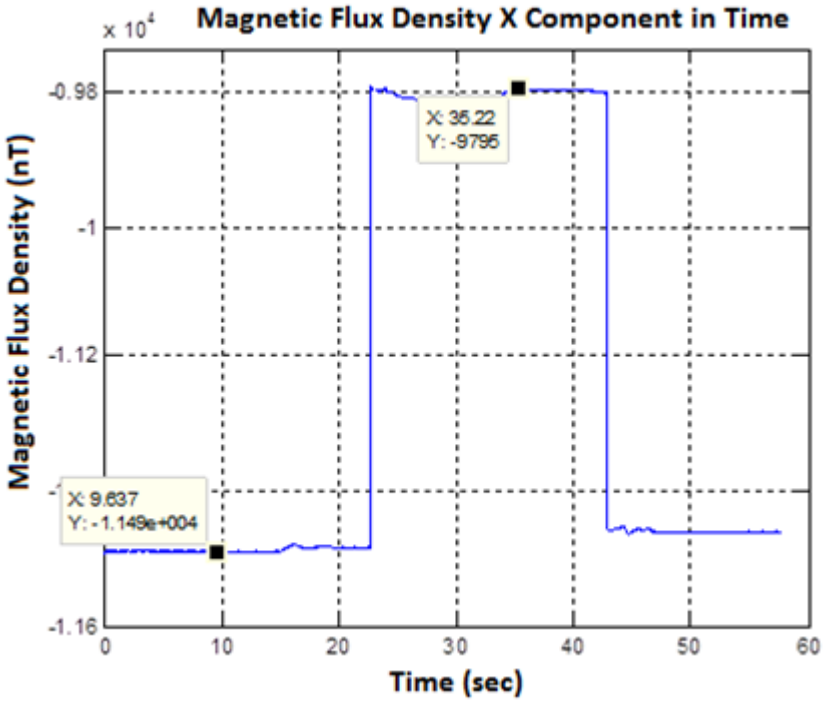

Figure 106 - DC Magnetic Flux Density X Component at 80 Degree

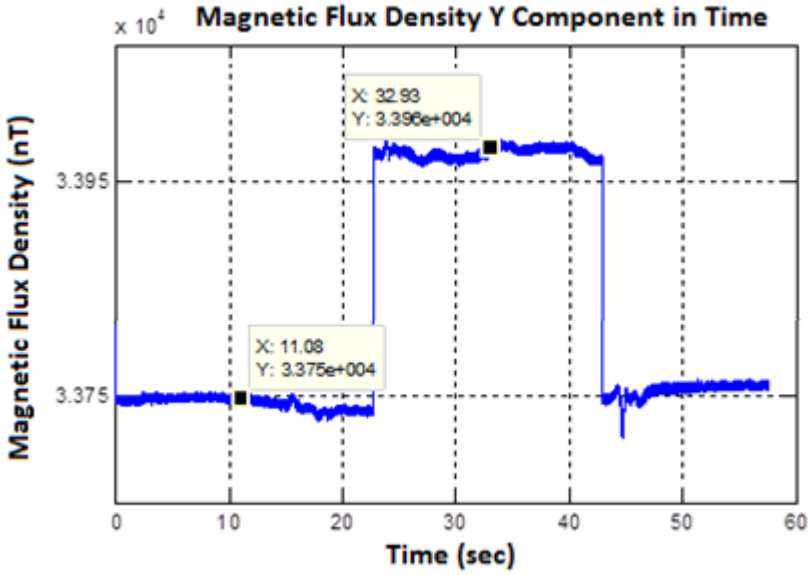

Figure 107 - DC Magnetic Flux Density Y Component at 80 Degree

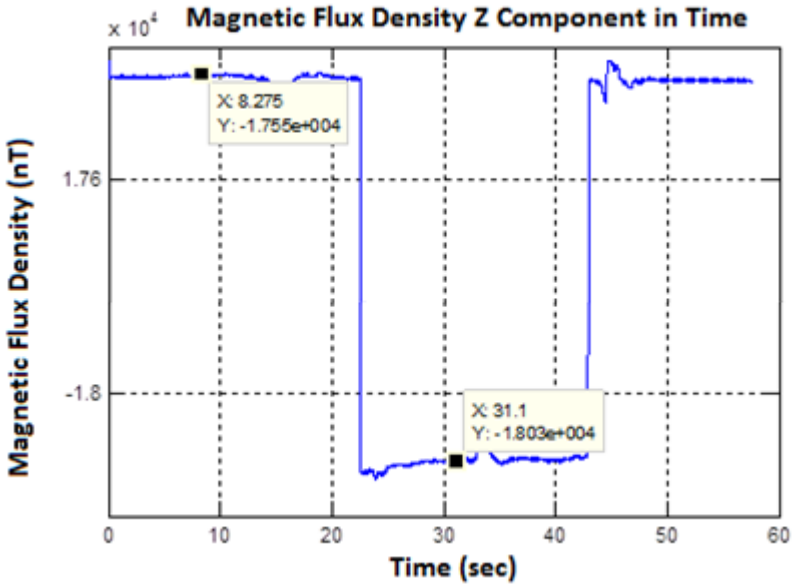

Figure 108 - DC Magnetic Flux Density Z Component at 80 Degree

The level of spatial components of static magnetic flux density are found as follows: the level of the corresponding spatial component of the earth static magnetic field which is measured in the first 20 second period of the experiment is subtracted from the static magnetic field level observed in the following period of 20 seconds. For example, by using values which are marked in the figures above, the magnetic field flux density magnitude at 80^o can be found as:

$$B_x = -9795 — 11490 = 1695\ nT$$

$$B_y = 33960 - 33750 = 210\ nT$$

$$B_z - 18030 - (-17550) = -480\ nT$$

$$|B| = \sqrt{(B_x^2 + B_y^2 + B_z^2\ )} = 1774\ nT$$

Some other measurement results for different angle positions are given in “Table 4” below, for the same drive conditions as stated previously:

	0°	10°	20°	30°	40°	50°	60°	70°	80°	90°
B_x(nT)	-910	-830	-630	-290	+160	+560	+1000	+1390	+1695	+1776
B_y(nT)	-50	-10	+50	+50	+80	+80	+100	+200	+210	+160
B_z(nT)	+90	-440	-810	-1110	-1270	-1300	-1160	-900	-480	+6
B_{NORM}(nT)	916	940	1027	1148	1282	1417	1535	1668	1774	1783

Table 4 – DC Magnetic Field Flux Density Values for Angles

The effects of current spikes, which are observed in the DC mode current measurements of the coil, cannot be observed in the previous magnetic field waveforms. This is because these spiky current components flow through the self-capacitance of the inductor not through the inductance, as mentioned before. Even if they flow through the inductive part, the data coming from the sensor is filtered by a low pass with a cut-off of 23Hz as mentioned and this result in the attenuation of the high frequency content like the spikes. Moreover, the sensor operation is limited for the measurements of the magnetic fields in the frequency band of 0-3kHz.

4.3.2 AC Fields

The PWM signals which have been used for the AC magnetic field measurements, have 98% modulation index and a fundamental frequency of 600Hz. As a result, a 600Hz AC load current of 225 mA peak-to-peak has been got flowing through the coil.

In addition, the magnetic sensor has been adjusted to the AC coupling mode for excluding earth static magnetic field from AC measurements. To suppress mains disturbances at 50Hz and its harmonic, the high pass filter with 170Hz cutoff has been designed in the MATLAB® FDA tool. The waveforms of the magnetic flux density components in 80° position are provided in “Figure 109Figure 109 - AC Magnetic Flux Density X Component at 80 Degree”, “Figure 110” and “Figure 111” below.

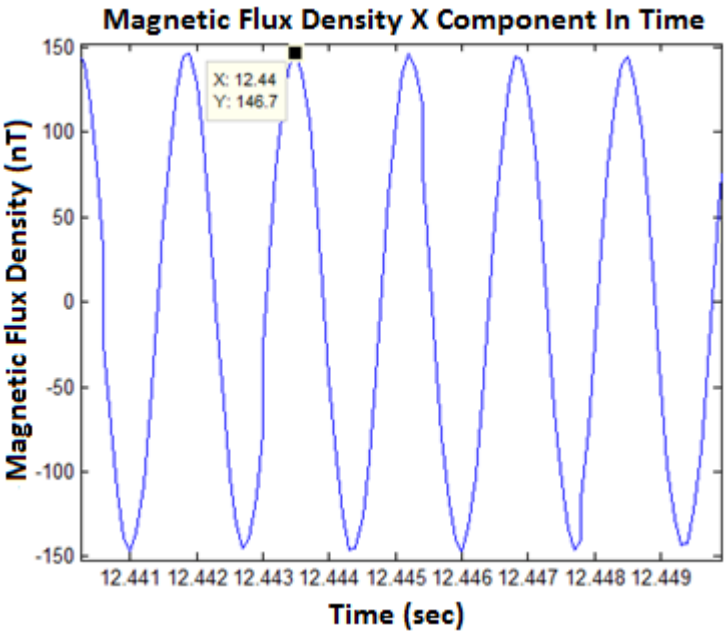

Figure 109 - AC Magnetic Flux Density X Component at 80 Degree

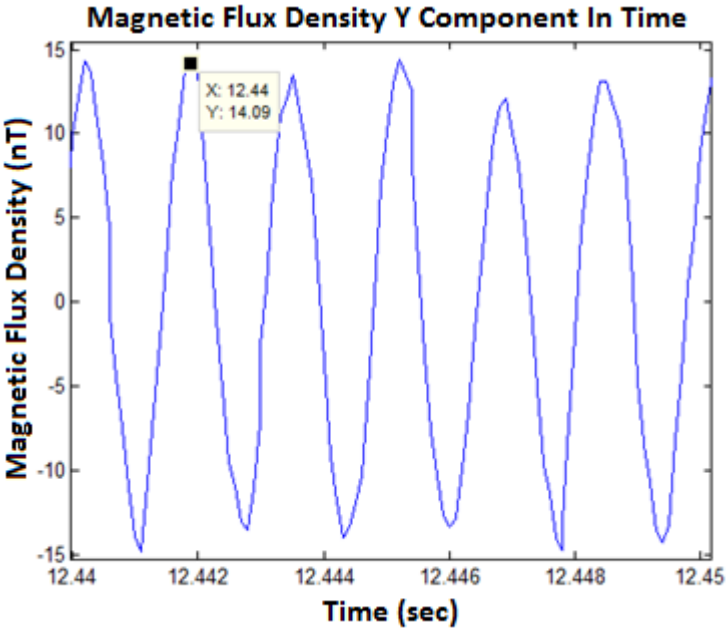

Figure 110 - AC Magnetic Flux Density Y Component at 80 Degree

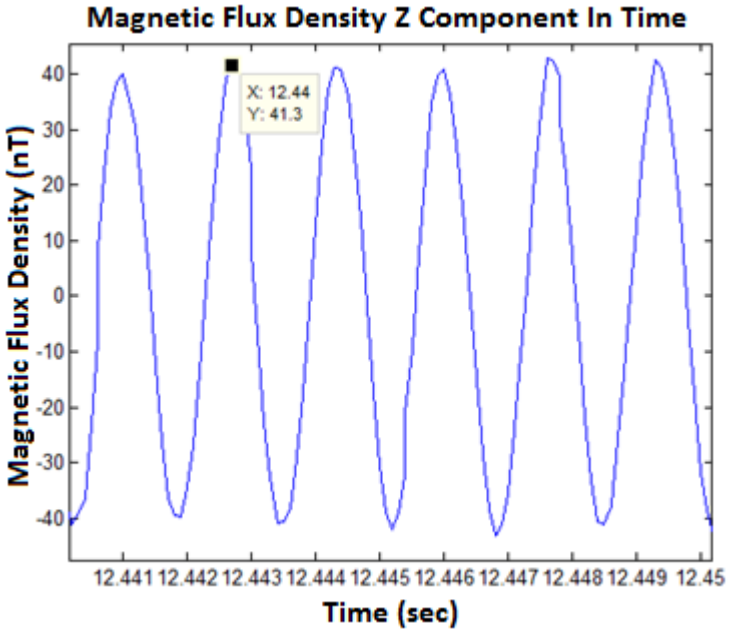

Figure 111 - AC Magnetic Flux Density Z Component at 80 Degree

Some other measurement results for different angle values are given in "Table 5" below, for the same drive conditions as stated previously:

	0°	**10°**	**20°**	**30°**	**40°**	**50°**	**60°**	**70°**	**80°**	**90**
B_{NORM} (nT)	83.5	87	95	108	119	130	140.8	148	151.7	156

Table 5 - AC Magnetic Field Flux Density Values for Angles

The effects of current spikes, which are observed in the AC mode current measurements of the coil, cannot be observed in the previous magnetic field waveforms. This is because of the exact same reason as in the DC case. The spiky current components flow through the self-capacitance of the inductor not through the inductance, as mentioned before. Even such high frequency magnetic field components exist, the magnetic sensor with the operating frequency band of 0-3kHz will suppress these.

Chapter 5

Conclusion

In this work, the full-bridge circuit structure has been selected as the drive circuitry for the load is an inductor for generating underwater magnetic fields. This is because, class-D type amplifiers have lots of advantages like being flexible for different operations [5]. By only varying its pulse width modulated drive signals, hardware becomes either a DC-DC converter or a DC-AC inverter which make it possible to produce both static and alternating magnetic fields [5]. They also achieve:

- A high power efficiency greater than 90% for a large output swing in the case of the high modulation index which saves designers from using bulky coolers and thermal consideration [9].
- Astonishing linear responses and being very noise immune [4].
- They are compact which is a crucial feature for mobile systems as here [4].
- A wide operation band, from DC (DC-DC conversion) up-to one half of the sampling frequency (DC-AC inversion) [8].

Furthermore the full-bridge is preferred over the half-bridge which is another type of digital class-D amplifier structures; because the maximum output voltage swing is twice at full-bridge inverter than the half-bridge under the same supply voltage levels [1]. This means higher output currents as well as higher target magnetic fields can be reached with the use of full bridges. Also there is no need for dual polarity power supplies as in the half-bridge to have DC free output waveforms.

Afterwards the PWM drive technique has been decided. The spectral content of the modulated drive signal is mainly concerned. Some fundamental harmonic components may interfere with and distort the target magnetic field. Because the high orders of switching harmonics flows through the self-capacitance of the coil already. Even they does not, the underwater electromagnetic propagation is much harder for these high frequency components. Therefore the natural sampling is selected for its having none of fundamental harmonics differently than the uniform sampling, which has odd multiples of the modulating signal frequency [3]. Moreover, other PWM sampling methods are considered to be only a compromise between the natural sampling's having none of fundamental but higher combinational switching harmonics against uniform sampling's having lower switching but fundamental harmonics [4].

Other features of the modulation should also be decided. The shape of the carrier waveform is selected triangular (double-edged) over the saw-tooth (single-edged) type; since the double-edge modulation, the use of the triangular carrier, is superior over using saw-tooth shape with respect to harmonic levels [12, 13].

The synchronism of the natural PWM technique is also another important property of the modulation method to be determined. In this work it is automatically asynchronous because the modulating signal frequency varies with 25Hz steps in the 500-700 Hz band for different runs while the carrier signal frequency is fixed to 20 kHz. Although the drawback is the sub-harmonics, their levels will be negligible with any of PWM switching scheme, that ensures a high frequency ratio [11]. Then the use of high carrier frequencies like as 20kHz so, make it possible to use a fixed carrier frequency for varying modulating signal frequency, even for the values of several hundred hertz [11]. Thus, the asynchronous scheme is adopted with high frequency ratios in between "28" to "40".

For even further utilizing the harmonic minimization performance of a PWM method, the frequency ratio is preferably picked to make the inverter work with the maximum allowable switching frequency [5]. The natural sampling, which does not

involve fundamental harmonics already, makes its only distortion sources of carrier frequency and combinatorial harmonic levels to be negligible for carrier frequencies greater than 132 kHz [3].

On the other hand, switching frequency should not be more than a few hundred kHz practically if it is wanted to obtain reasonable efficiency levels [3]. Because higher the switching frequency the more switching stress and power losses occur [10].

The harmonic content of a PWM waveform created in digital platforms, as being differently from analog applications, also depends on the sampling frequencies of the "modulating" and the "carrier" signals [12]. The exact intersection of signal levels cannot be detected since they are sampled and not continuous anymore [2]. As a result, the amplitude of the fundamental component differs from its actual level and some additional harmonics appear at frequencies close to this [2]. These results depend on the ratio of the sampling periods of the carrier and modulating signal to their actual signal frequencies respectively [2]. Since the carrier has a much lower period than the modulating signal, the ratio of sampling period of carrier signal to its own period "Ts/Tt" is essential in minimizing these effects [2]. It is confronted that the effects are small when this ratio is small like $80ns/(20kHz)^1 = 0.16\%$ as in here [2].

The misdetection of the signal intersections are also encountered as following. While implementing the natural sampling digitally, glitches occur in the modulated signal waveforms because of the sampling frequency difference of the carrier and the modulating signal. Therefore, the sampling frequency of the carrier signal has been reduced. This has also decreased the comparison rate of the signal levels. The ratio of "Ts/Tt" which was actually $20ns/(20kHz)^1 = 0.04\%$ before turned into $80ns/(20kHz)^1 = 0.16\%$ since the carrier signal period is increased from 20ns to 80ns. However, still the ratio of carrier sampling period to the actual carrier signal frequency is low sufficiently so that additional sub-harmonics or fundamental harmonics are negligible.

One similar case is as in the dead-time insertion into the PWM drive signals. Lots of harmonics at the multiples of the modulating frequency appear as the drawback. The fundamental voltage level at the output is also decreased depending on the power factor angle as well as the dead-time duration. The rest of the output spectrum does not change significantly. This is because the low-order odd harmonic amplitudes increase linearly with the ratio of the dead-time duration to the switching period [7]. These amplitudes are low enough for the value of this ratio as $\frac{500ns}{(20kHz)^{-1}} = 1\%$ which is the case here.

Even higher frequency components come into play with "electromagnetic interference noise" (EMI) which is caused by the switching events exciting the parasitic elements of the circuit layout [14]. This is because the modulated pulse train signals have fast rise times in other words high "dv/dt" values [15, 16]. The output waveforms suffer from such high "dv/dt" and "di/dt" therefore having a high number of harmonic components [14]. However as explained before, the self-capacitance part of the coil has the spiky currents with high frequency content. So they are independent from the inductive part which produces the magnetic field. Only some negligible level of the ripple at the switching frequency is observed in the inductive current.

High "dv/dt" and "di/dt" at the output waveforms caused by differential and common mode EMI may even lead the inductor fail [15]. Some precautions can be taken like minimizing the parasitic inductances in the circuit layout [14]. The coil can be wound with a wire which has a thicker insulation and this reduces the inter-turn capacitance and the levels of DM noise as well [14]. To decrease the CM noise, special cables with shields are advised to be used for preventing capacitive coupling between phase conductors of the inductor [16]. Those cables may also have ground conductors with smaller impedance in several orders of magnitude for the EMI frequencies than of the actual ground line to clear the noise from the dc power bus [16]. Appropriate amount of spacing between circuit equipments, not only improve conducted EMI attenuation by lowering the coupling capacitances between phase lines but also decrease the level

of the radiated EMI [16]. This is made possible by reducing the area of the loop antenna formed between the phase leads and the ground line [16]. The use of shielded components and cables also prevent electromagnetic interactions like antenna responses [16].

However, every precaution which is applied for reducing the EMI noise has to outweigh its cost [14]. If it does not interfere with the safe operation of the circuit or emanated EMI levels do not exceed the limits imposed on, some of the improvements for reducing EMI noise may not to be applied [14]. As mentioned earlier, no current snubber is required during the turn-off of the power MOSFETS [18]. However, the voltage clampers still can be used for decreasing the levels of the voltage spikes during switching for the sake of satisfying the constraints [18]. These voltage clampers also regulate the "dv/dt" across the switch which is turning-off [18]. But this is redundant when power MOSFETS are used, which do not suffer from second breakdown [18]. Furthermore, they can withstand "dv/dt" levels as high as thousands of volts per microsecond during the operation [18].

It is deduced from above sayings that the power MOSFET switches will operate safely under EMI and it is also proven by testing that EMI noise doesn't harm load inductor with causing premature insulation fails. The device has been run for "1 hour" safely and the inductor has reached a temperature around 130^{o}C. It should also be considered that the device will only operate for 8min and underwater, there will not be important thermal considerations.

Magnetic field levels have to be also analyzed in context of EMI noise. As mentioned before, such noisy current components flow through the self-capacitance of the load coil and the inductive part has nothing to do with that. Therefore the effects of these distortions are not observed in the generated magnetic fields. Even if this situation is ignored, it has been shown by the simulations that at the target distance of 5m, corresponding high frequency components of the current cannot create comparable

levels of magnetic fields with respect to the fundamental component. This is because water is a lossy medium with conductivity of “4 S/m” and it gets harder for electromagnetic waves to penetrate for increasing frequencies. It should also be remembered that such high frequency components appear in the PWM voltage spectrum at smaller levels than the fundamental. Their current forms are also attenuated by the load inductor with respect to its impedance.

To conclude, the system operates safely under EMI noise, and the target magnetic fields do not include such high frequency components. The passive switching-aid networks (snubbers) which have the benefit of reducing the rise times of the switching pulse edges aim to suppress only the high frequency (EMI noise, carrier harmonics) components to some extent. Therefore the use of switching-aid networks is dismissed. Moreover, for such a single use remote system, it is crucial to construct the circuitry with the minimum number of components for reducing the number of points of failure. Because this circuit will be encapsulated afterwards so it is important to save space.

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Appendix A

First Design Trial for the Driver Circuit

The alternative circuitry structure is like in “Figure 112” below. It includes a “Class-A” power amplifier for AC amplification in AC operation and a power transistor for supplying necessary DC current to the load in DC operation. The class-A amplifier has been bought from an audio amplifier store and it was bulky. Additionally, even there are no power limitations; the power transistor which supplies DC current gets hot too much. Beside the efficiency considerations, because gate biasing is done in active region; it becomes cumbersome with changing drain-source resistance till thermal equilibrium. Therefore, the calculated current levels which are related to appropriate bias voltages cannot be observed exactly.

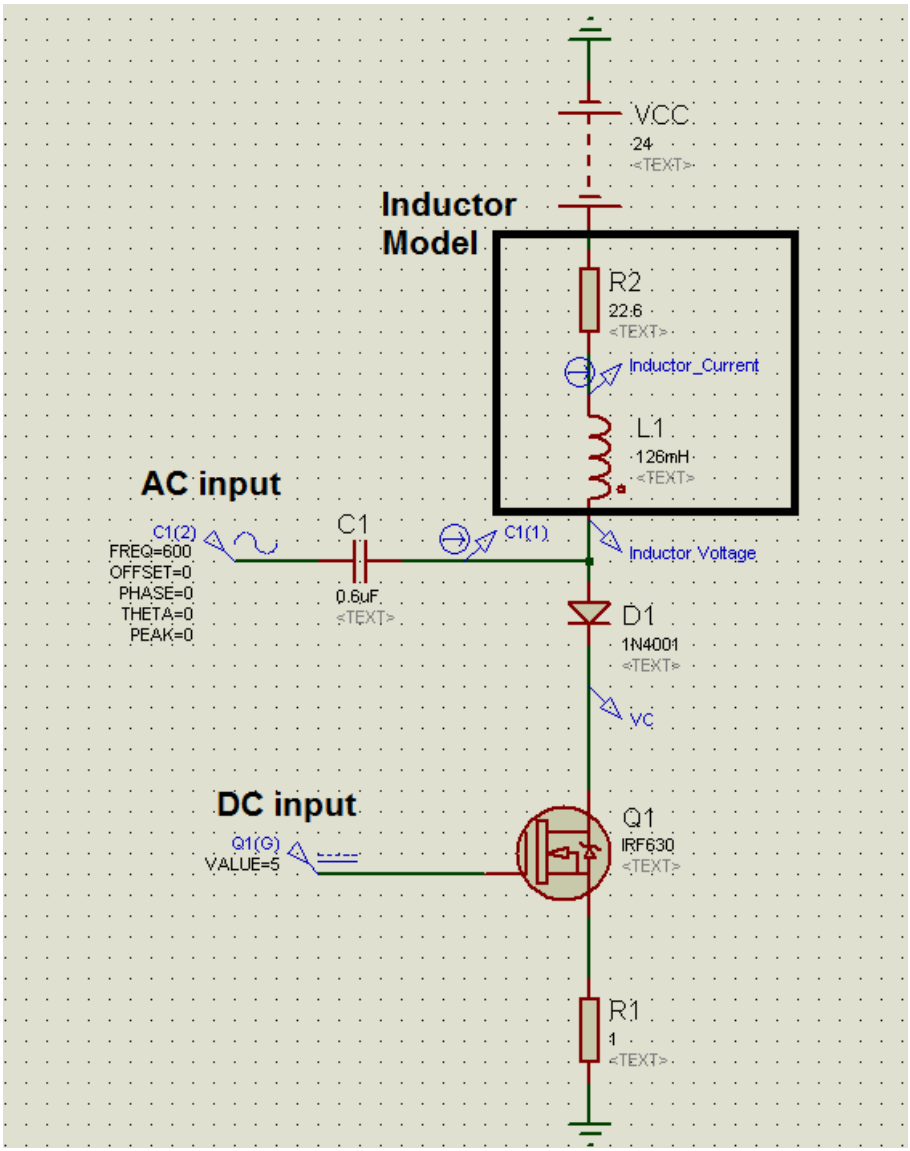

Figure 112 - First Circuit Structure Choice

In addition, while coupling the AC output signal of the amplifier with the help of a coupling capacitor to the DC current through the power transistor, the circuitry responded in somewhat ambiguous way. The amplitude of the coupled AC voltage is also affected while the bias of the power MOS is changed. This is like changing the quiescent point of the class-A, although the transistor is employed for DC operations. Then the AC+DC operation is decided not to be suitable. Because of all these reasons, the final structure is determined as "Full-Bridge (H-bridge)" with PWM drive.

Appendix B

List of Materials & Circuit Schematics

#	Product	Producer	Part Number	Explanation (Material etc.)	Quantity	PCB Placement
1	Inductor Carcass	Tolga Plastik	-	Delrin	1 piece	-
2	Coil	Uğur Trafo	-	Wound 1427 many turn around carcass with AWG-23 type Cu wire	1 adet	-
3	GRP Prepreg	Advanced Composites Group	VTM243FRB /GF2302-33% RW290gr/m^2 E-glass fabric prepreg	Coil is covered by Epsilom Kompozit Ostim.	Around 0.12 m^2 (0.02 m^2 x6 layers)	-
4	IR2113	International Rectifier	-	MOSFET gate driver IC with 14 pins PDIP package	2 piece	U1, U2
5	HD74HC04P	RENESAS	-	14 bacaklı, DLIP paketli hex inverter	1 piece	U3
6	L7805CV	SGS-THOMPSON microelectronics	-	5V DC regulator with TO-220 package	1 piece	U4
7	IRF540NS	International Rectifier	-	Power MOSFETs with TO-262 package	4 piece	Q1, Q2, Q3, Q4

8	100nF Capacitor	-		100V	6 piece	C1, C2, C3, C4, C5, C6
9	330nF Capacitor	-		100V	1 piece	C7
10	3.3uF Capacitor	-		250V	1 piece	C8
11	100Ω Resistor	-	-	Carbon resistor with resistance tolerance of ±5%	4 piece	R1, R2
12	1N4148 Diode	Fairchild Semiconductor		300mA, 100V	6 piece	D1, D2, D3, D4 D5, D6
13	BYV28-150 Diode	Phillips Semiconductors	-	3.5 A, 150 V	1 piece	D7
14	D-sub 9 pins Socket Type Connector	-	-	FPGA Board PWM Interface Connector	1 piece	S1
15	OSTTE020161 Clamp Electrical Connector	-	-	DC Power Supply and Output Interface Connectors (200V, 18A)	4 piece	S2, S2, S3

Table 6 - List of Materials

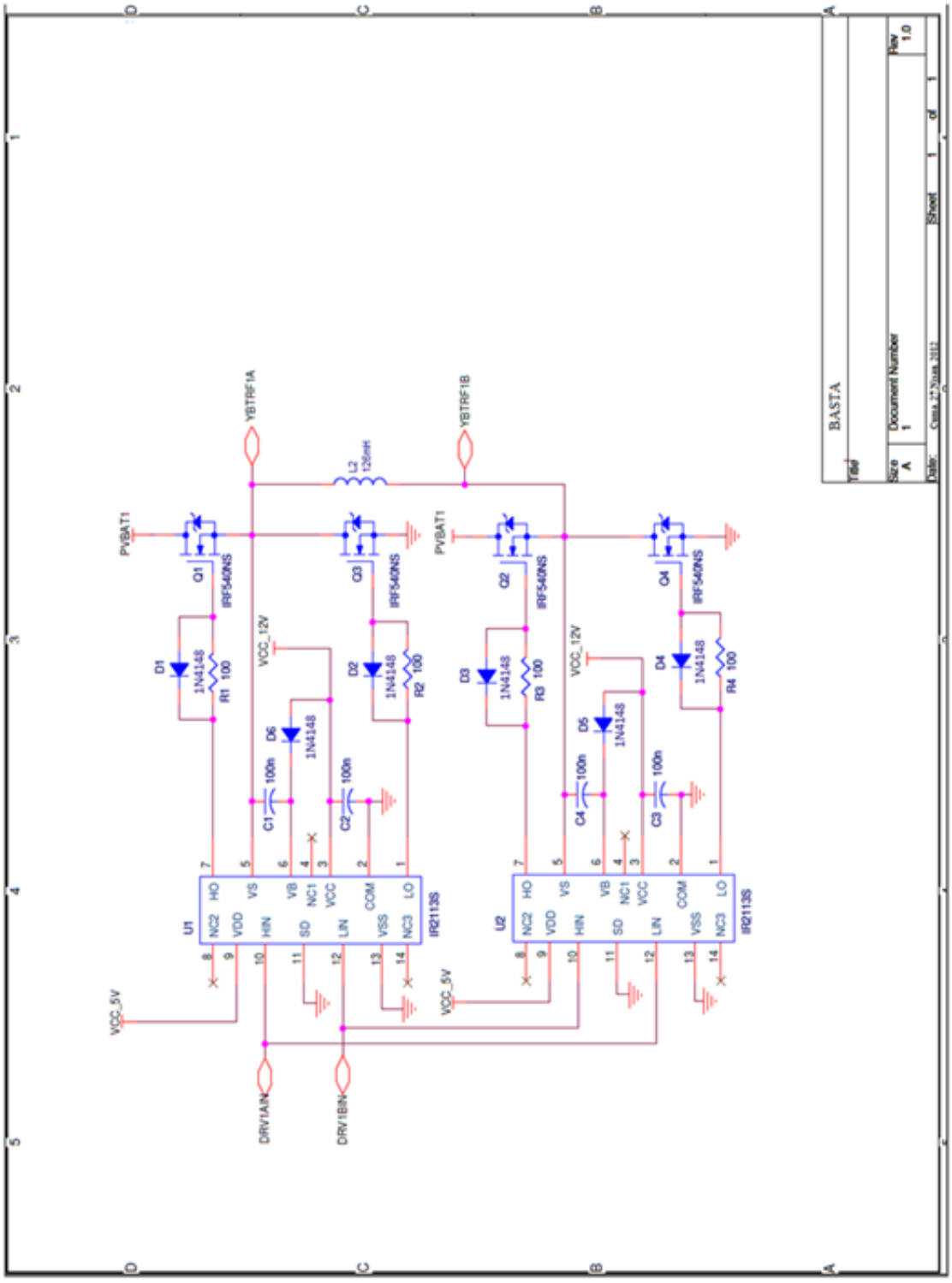

Figure 113 - Circuit Schematic-1/H-Bridge and Gate Driver ICs Connections

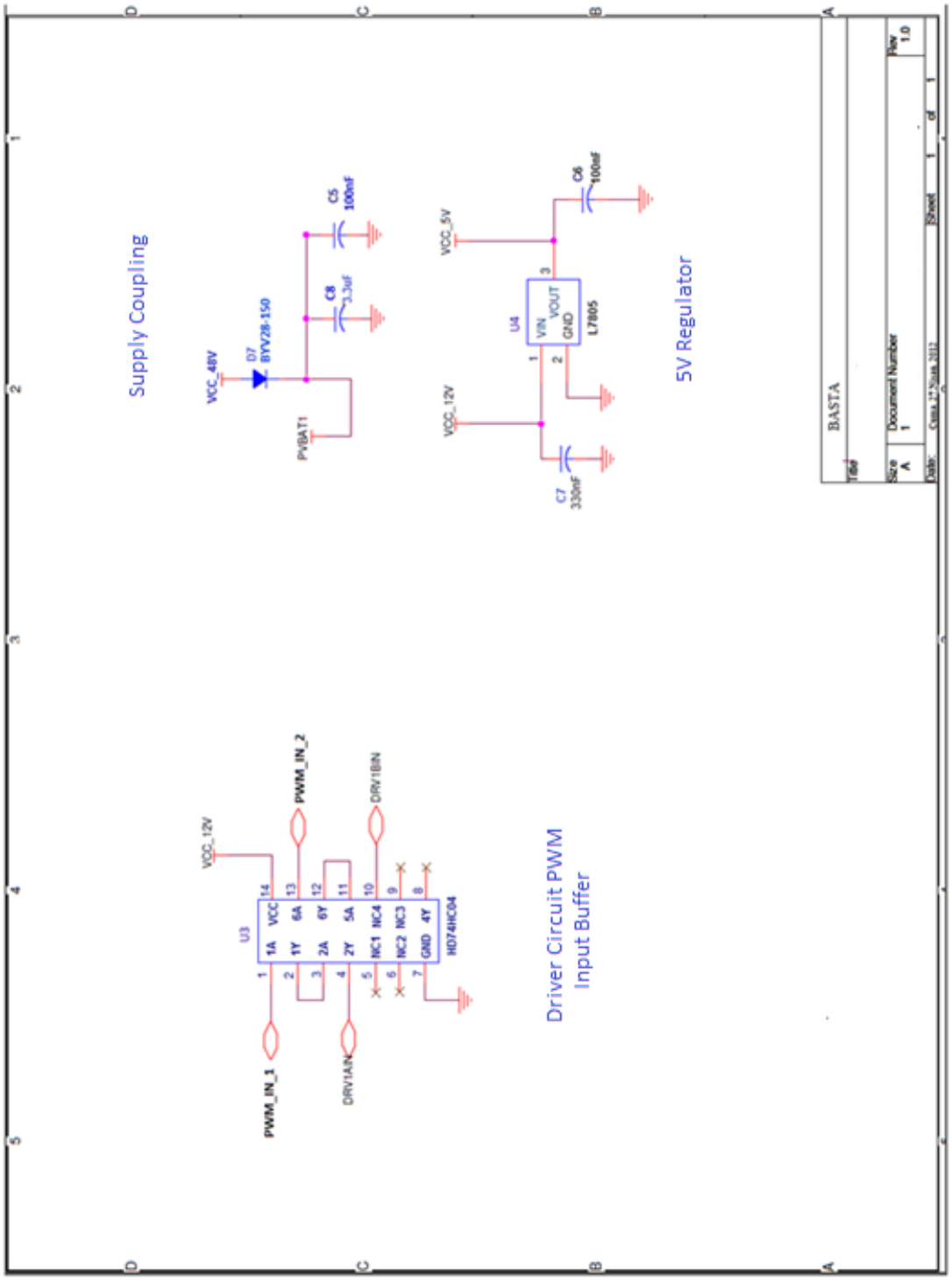

Figure 114 - Circuit Schematics-2/DC Power Supply Interface, 5V Regulator Circuit and PWM Buffer Stage

Appendix C

PCB Layout

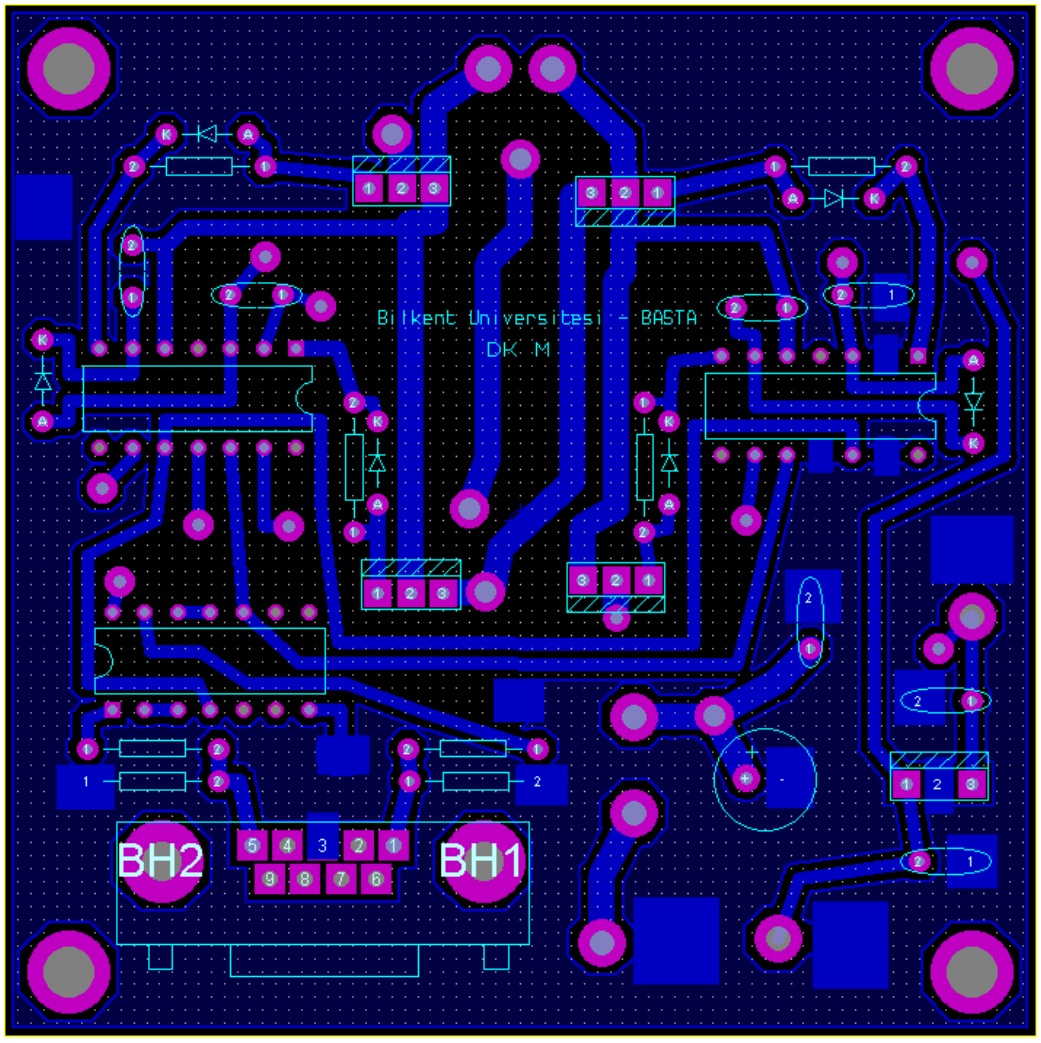

Figure 115 - PCB Component Side Layout

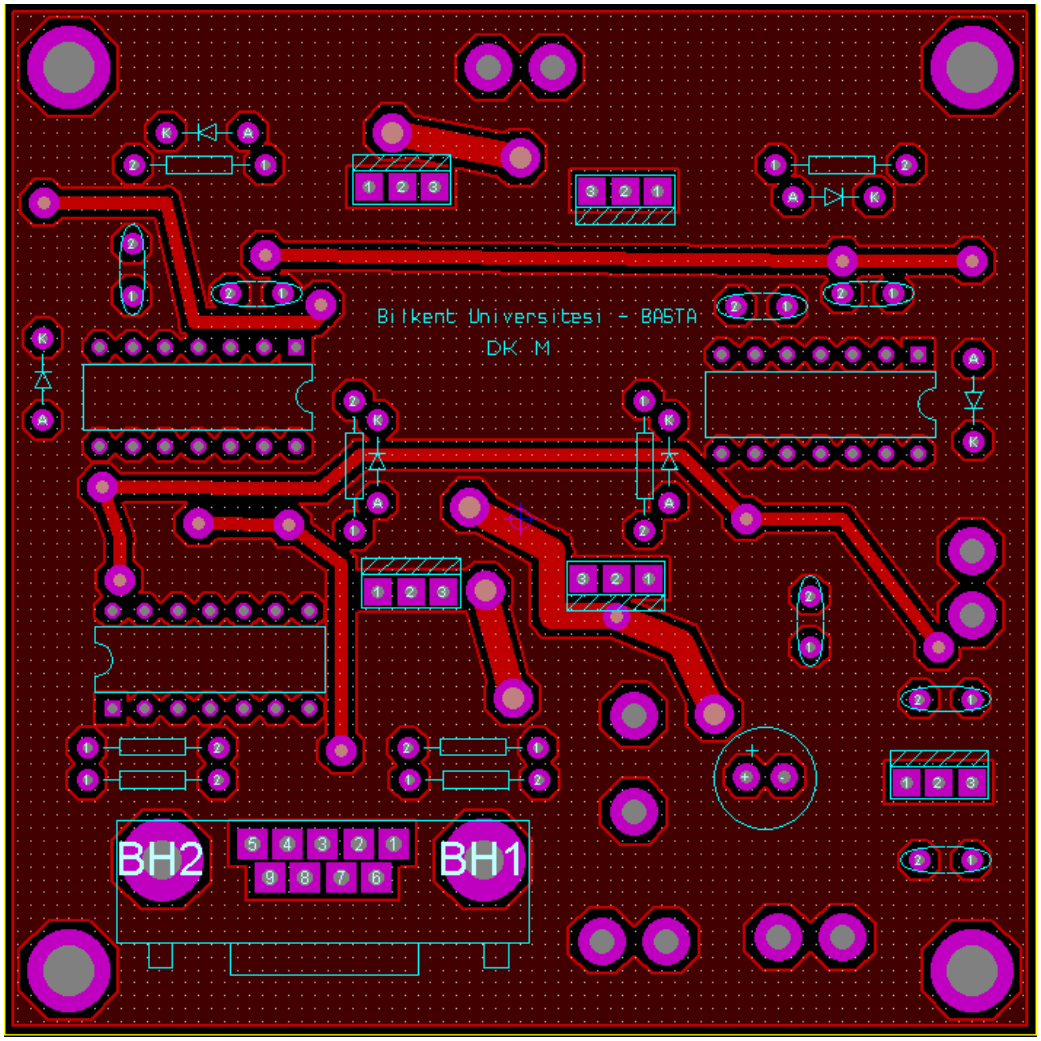

Figure 116 - PCB Solder Side Layout

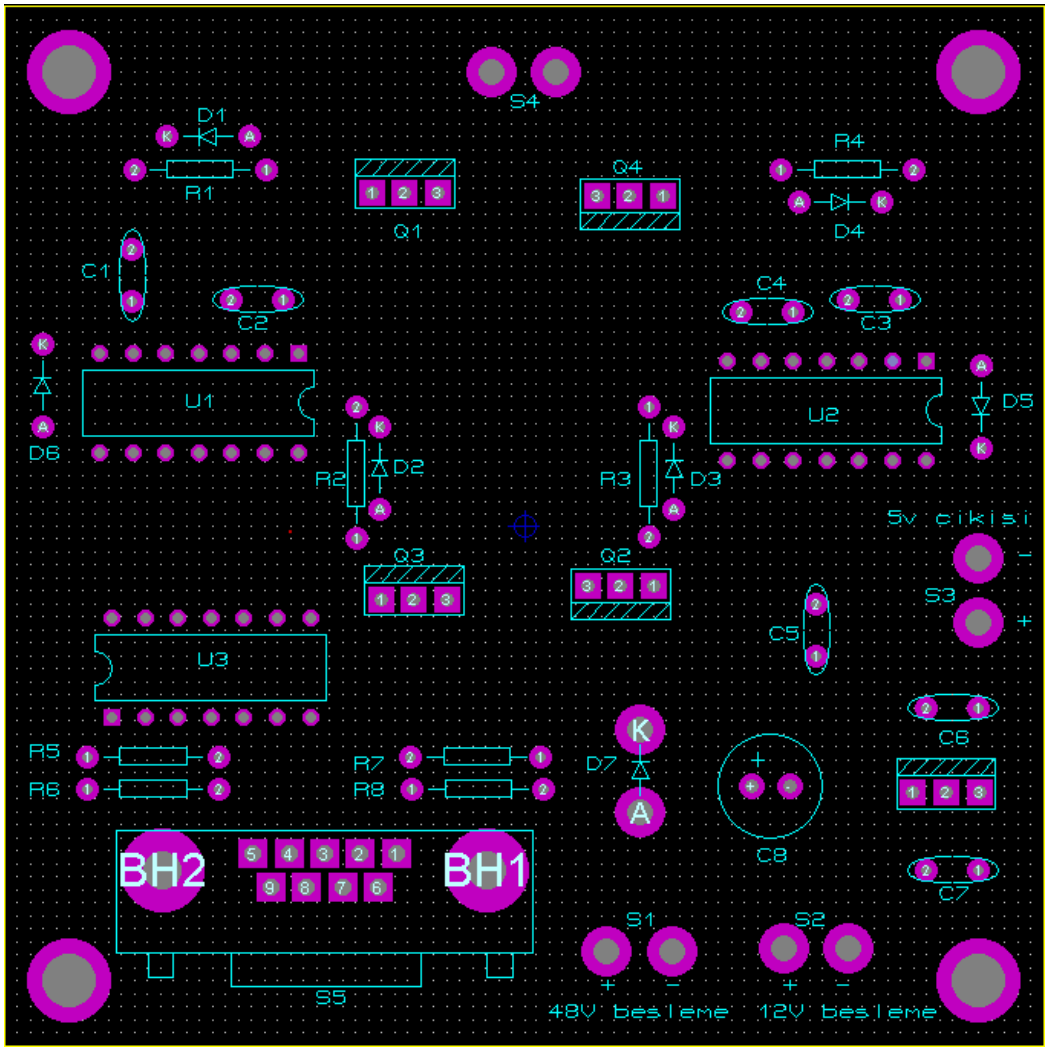

Figure 117 - PCB Component References

There are some important issues which should be considered while soldering and using the PCB board as follows:

- Connector S1 is for 48V DC power supply interface,
- Connector S2 for 12V DC supply interface,
- Connector S3 for supplying 5V DC to the FPGA board.
- The connector “S5” is used as input PWM signal interface from the FPGA board to the driver circuitry. The duty cycle reference PWM signal “PWM_IN_1” is assigned to the 5th pin, the complementary “PWM_IN_2” to

the 1st pin and the ground reference “GND” to the 3rd pin of the connector.

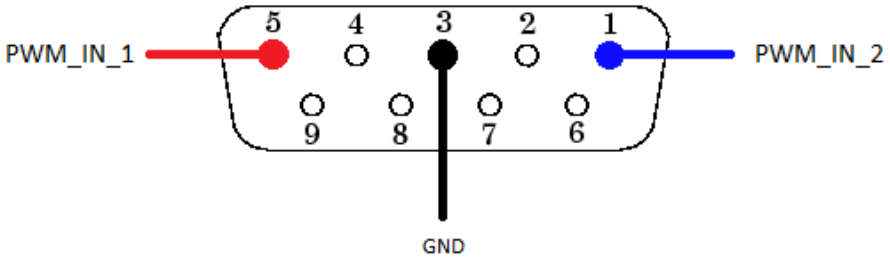

Figure 118 - FPGA Board/Driver Circuitry PWM Interface

- The connector “S4” is reserved for the output interface between driver circuit output and the load coil.
- The resistors “R5”, “R6”, “R7” and “R8” are not placed. The via couples of “R5” and “R7” places are shorted among themselves.

Appendix D

Photos of the System

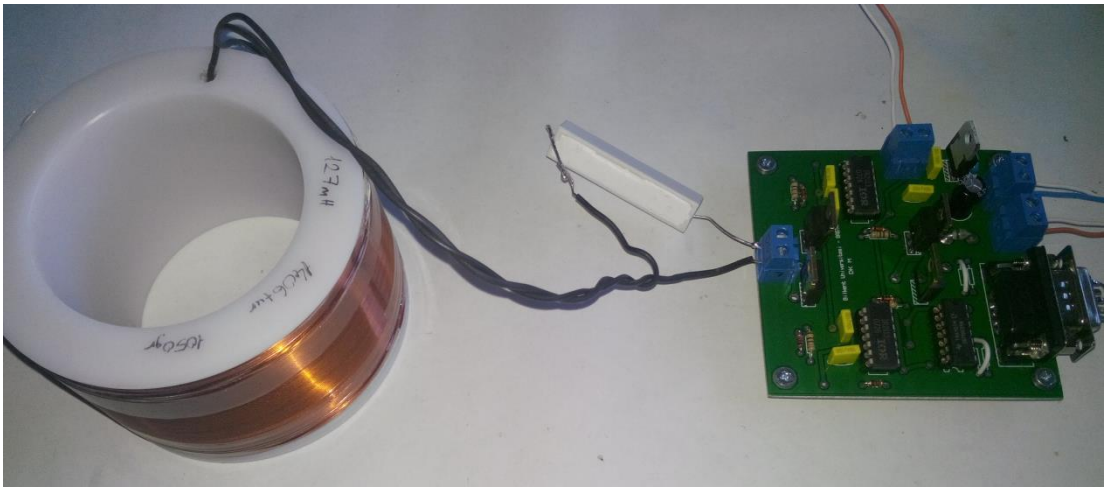

Figure 119 - Load Inductor & Driver Circuit

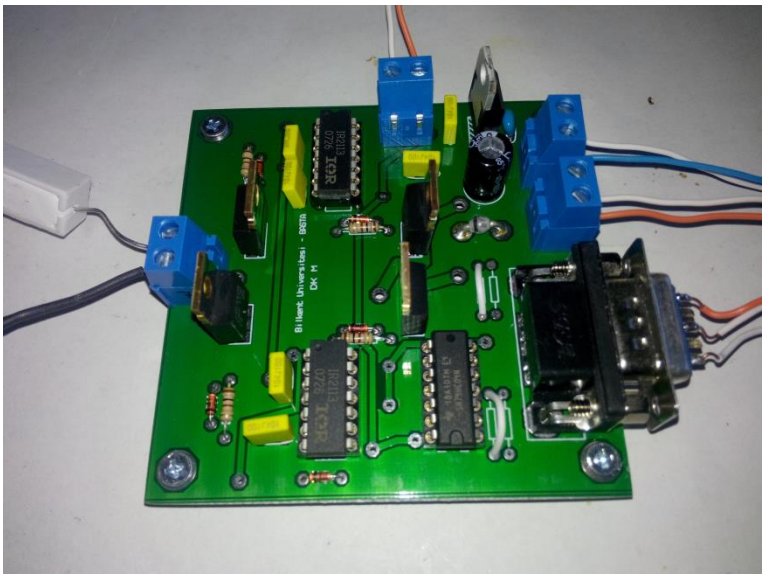

Figure 120 - Driver Circuit Board

Appendix E

VHDL Codes

The VHDL codes for corresponding modules are provided here.

Square

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity square is
    Port ( clk : in  STD_LOGIC;
           duty:in STD_LOGIC_VECTOR(3 downto 0);
           output : out  STD_LOGIC);
end square;

architecture Behavioral of square is
signal outro:std_logic;
signal a:integer;
begin

process(clk)
variable k:integer  range 0 to 2500:=0;
begin
if rising_edge(clk) then
           if k=0 then
           outro<='1';--- after 1 us;
                    k:=k+1;
           elsif k<a then
                    k:=k+1;
           elsif k=a then
                    outro<='0';
                    k:=k+1;
           elsif k>a and k<2500 then
                    k:=k+1;
                    if k=2500 then
                      k:=0;
                    end if;
           end if;

end if;
```

```
end process;

process(clk)
begin
if rising_edge(clk) then
        if duty=15 then
                        a<=2450;
        elsif duty<10 and duty>=0 then
                        a<=250*conv_integer(duty);
        elsif duty=14 then
                        a<=1875;
        elsif duty=13 then
                        a<=1325;
        else
                        a<=1250;
        end if;
end if;
end process;

output<=outro;

end Behavioral;
```

Triangle

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_SIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity triangle is
   Port ( clk : in  STD_LOGIC;
          tri_out : out  STD_LOGIC_VECTOR (10 downto 0));
end triangle;

architecture Behavioral of triangle is
signal k:STD_LOGIC_VECTOR (10 downto 0):="10110001111";
begin

process(clk)
variable down:std_logic;
constant Th_carrier: integer :=25000; --- half period of carrier (ns)
constant carrier_bit: integer :=10;
        begin
        if rising_edge(clk) then
                if k="01001110001" then
                        down:='1';
                elsif k="10110001111" then
                        down:='0';--up='1'
                end if;

                if k<"01001110001" and down='0' then
                        k<=k+1;
                elsif k>"10110001111" and down='1' then
                        k<=k-1;
```

```
                end if;
        end if;
end process;

tri_out<=k;
end Behavioral;
```

Mod_signal

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
-- synthesis translate_off
Library XilinxCoreLib;
-- synthesis translate_on
ENTITY mod_signal IS
        port (
        clk: IN std_logic;
        we: IN std_logic;
        data: IN std_logic_VECTOR(32 downto 0);
        sine: OUT std_logic_VECTOR(10 downto 0));
END mod_signal;

ARCHITECTURE mod_signal_a OF mod_signal IS
-- synthesis translate_off
component wrapped_mod_signal
        port (
        clk: IN std_logic;
        we: IN std_logic;
        data: IN std_logic_VECTOR(32 downto 0);
        sine: OUT std_logic_VECTOR(10 downto 0));
end component;
-- Configuration specification
        for all : wrapped_mod_signal use entity XilinxCoreLib.dds_compiler_v4_0(behavioral)
                generic map(
                        c_use_dsp48 => 0,
                        c_phase_offset_value => "0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0",
                        c_amplitude => 1,
                        c_channels => 1,
                        c_phase_increment_value => "10100111110001100,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0",
                        c_has_rdy => 0,
                        c_has_sincos => 1,
                        c_has_sclr => 0,
                        c_phase_offset => 0,
                        c_phase_angle_width => 11,
                        c_phase_increment => 1,
                        c_has_rfd => 0,
                        c_negative_sine => 0,
                        c_has_phasegen => 1,
                        c_has_channel_index => 0,
                        c_latency => -1,
                        c_por_mode => 0,
                        c_has_ce => 0,
                        c_outputs_required => 0,
                        c_accumulator_width => 33,
```

```
                        c_mem_type => 1,
                        c_optimise_goal => 0,
                        c_negative_cosine => 0,
                        c_has_phase_out => 0,
                        c_noise_shaping => 0,
                        c_xdevicefamily => "spartan3e",
                        c_output_width => 11);
-- synthesis translate_on
BEGIN
-- synthesis translate_off
U0 : wrapped_mod_signal
                port map (
                        clk => clk,
                        we => we,
                        data => data,
                        sine => sine);
-- synthesis translate_on

END mod_signal_a;
```

Comparator

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_SIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity comparator is
   Port ( clk:in STD_LOGIC;
          carrier : in  STD_LOGIC_VECTOR (10 downto 0);
          modulating : in  STD_LOGIC_VECTOR (10 downto 0);
          ampac: in  STD_LOGIC_VECTOR (1 downto 0);
          output1 : out  STD_LOGIC;
          notout1: out  STD_LOGIC);
end comparator;

architecture Behavioral of comparator is
signal modulating1: std_logic_vector (10 downto 0);
signal modulating2: std_logic_vector (21 downto 0);

signal outr1, notr1, outro2, notro2:std_logic;
signal dup_nflag1, dup_oflag1:std_logic_vector(1 downto 0);

signal clk2:std_logic:='1';
signal nflag1, oflag1:std_logic_vector(1 downto 0):="00";
signal oooflag1, nnnflag1:std_logic:='0';

begin
modulating1<=modulating2(19 downto 9);

process(clk)
begin
        if rising_edge(clk) then
                if ampac="01" then
```

```
                    modulating2<=modulating*"00100111000";--%50
                elsif ampac="10" then
                    modulating2<=modulating*"00111010100";--%75
                elsif ampac="11" then
                    modulating2<=modulating*"01001100011";--%98 max
                else --"00" and o/w
                    modulating2<=modulating*"00010011100";
                end if;
        end if;
end process;

w:process(clk2)
begin
        if rising_edge(clk2) then
                if carrier < modulating1 then
                    outr1<='1';
                    notr1<='0';
                elsif carrier >= modulating1 then
                    outr1<='0';
                    notr1<='1';
                end if;
        end if;
end process w;

clclk:process(clk)
        variable t:integer range 0 to 1:=0;
        begin
                if rising_edge(clk) then
                    if t<1 then
                        t:=t+1;
                    elsif t=1 then
                        t:=0;
                        clk2<=not clk2;
                    end if;
                end if;
        end process clclk;

output1<=outr1;
notout1<=notr1;

end Behavioral;
```

Modslct

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity modslct is
   Port ( clk : in  STD_LOGIC;
          slct : in STD_LOGIC;
          dutyfreq: in STD_LOGIC _VECTOR(7 downto 0);
          inac : in  STD_LOGIC;
          indc : in  STD_LOGIC;
           mdslct: out STD_LOGIC _VECTOR (1 downto 0);
           duty: out STD_LOGIC _VECTOR (3 downto 0);
           freq: out STD_LOGIC _VECTOR (5 downto 0);
```

```
        ampac: out STD_LOGIC _VECTOR (1 downto 0);
        outpwm : out  STD_LOGIC;
        led: out  STD_LOGIC;
        endc: out  STD_LOGIC;
        enac: out  STD_LOGIC);
end modslct;

architecture Behavioral of modslct is
signal premslct: std_logic_vector(1 downto 0);
signal outmod:std_logic:='0';
signal cit:std_logic:='0';
signal acdc:std_logic_vector(1 downto 0):="01";
signal mslct:std_logic_vector(1 downto 0);

begin
mdslct<=mslct;
process(clk)
variable m:integer range 0 to 50000000:=0;
variable preslct:std_logic:='0';
variable count:integer range 0 to 3:=0;
begin
        if rising_edge(clk) then
                if slct='1' and preslct/='1' then
                        preslct:='1';
                end if;
                if preslct='1' then
                        if m=0 then
                                count:=count+1;
                                m:=m+1;
                                led<='1';
                        elsif   m>0 and m<50000000 then
                                m:=m+1;
                        elsif m=50000000 then
                                m:=0;
                                preslct:='0';
                                led<='0';
                        end if;
                end if;
                if count=0 then
                                mslct<="00";
                        elsif count=1 then
                                mslct<="01";
                        elsif count=2 then
                                mslct<="10";
                        elsif count=3 then
                                mslct<="11";
                end if;
        end if;

end process;

process(clk)
begin
        if rising_edge(clk) then
```

```
                if mslct="10" or (mslct="11" and acdc="10") then
                        outmod<=inac;
                        if mslct="10" and premslct/="10" then
                                cit<='0';
                                premslct<="10";
                        elsif mslct="11" and premslct/="11" then
                                cit<='1';
                                premslct<="11";
                        end if;
                        endc<='0';
                        enac<='1';
                elsif mslct="01" or (mslct="11" and acdc="01") then
                        outmod<=indc;
                        if mslct="01" and premslct/="01" then
                                cit<='0';
                                premslct<="01";
                        elsif mslct="11" and premslct/="11" then
                                cit<='1';
                                premslct<="11";
                        end if;

                        endc<='1';
                        enac<='0';--dc enable, ac disable
                else
                                outmod<='0';
                end if;

        end if;
end process;

process(clk)
variable k:integer range 0 to 500000000:=0;
begin
        if rising_edge(clk) then
                if cit='1' then
                        if k<500000000 then
                                k:=k+1;
                                if k=500000000 then
                                acdc<=not acdc;
                                k:=0;
                                end if;
                        end if;
                else
                        k:=0;
                end if;
        end if;
end process;

process(clk)
begin
        if rising_edge(clk) then
                if mslct="10" then
                        freq<=dutyfreq(5 downto 0);
                        ampac<=dutyfreq(7 downto 6);
```

```
                    duty<="0000";
                elsif mslct="01" then
                    duty<=dutyfreq(3 DOWNTO 0);
                    freq<="000000";
                    ampac<="00";
                elsif mslct="11" then
                    duty<="1111";
                    freq<="010100";
                    ampac<="00";
                else
                    duty<="0000";
                    freq<="000000";
                    ampac<="00";
                end if;
        end if;
end process;

outpwm<=outmod;
end Behavioral;
```

Freq_change

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
USE ieee.std_logic_arith.all;

entity freq_change is
   Port ( clk : in  STD_LOGIC;
          freq: in  STD_LOGIC_VECTOR(5 downto 0);
          we1 : out  STD_LOGIC;
          data : out  STD_LOGIC_VECTOR (32 downto 0);
          display: out STD_LOGIC_VECTOR (9 downto 0));
end freq_change;

architecture Behavioral of freq_change is
signal prefreq:std_logic_vector(5 downto 0):="111111";
signal frequency500:std_logic_vector(32 downto 0):="00000000000000001010011111000110O";
signal frequency:std_logic_vector(32 downto 0);

signal Pinc:std_logic_vector(9 downto 0):="1101011011";--5Hz steps

signal fout:std_logic_vector(30 downto 0);

signal flag1,flag2:std_logic:='0';

begin

data<=frequency;
display<=fout(30 downto 21);

process(clk)
begin
        if rising_edge(clk) then
                if freq/=prefreq and freq<="101000" then
```

```
                frequency<=freq*Pinc+frequency500;
                prefreq<=freq;

                flag1<='1';
            end if;

            if flag2='1' then
                flag1<='0';
            end if;
        end if;
end process;


process(clk)
begin
        if rising_edge(clk) then
            if flag1='1' and flag2/='1' then
                fout<=frequency(16 downto 0)*"10111110101111";--50MHz

                we1<='1';

                flag2<='1';
            else--if flag1='0' then --elsif freq=prefreq then
                we1<='0';

                flag2<='0';
            end if;
        end if;
end process;
end Behavioral;
```

Deadtime

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_arith.ALL;
use IEEE.STD_LOGIC_SIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity deadtime is
   Port ( clk : in STD_LOGIC;
          mslct :in STD_LOGIC_VECTOR(1 downto 0);
         duty:in STD_LOGIC_VECTOR(3 downto 0);
          inpos : in STD_LOGIC;
          out1 : out  STD_LOGIC;
          not1 : out  STD_LOGIC;
         outref : out std_logic
          );
end deadtime;
architecture Behavioral of deadtime is
signal outro1, notro1:std_logic:='0';
signal nflag1, oflag1:std_logic_vector(1 downto 0):="00";
signal oooflag1, nnnflag1:std_logic:='0';

begin
```

```
process(clk)
variable k,m:integer range 1 to 25:=1;
begin
	if rising_edge(clk) then

		if (mslct="00" or (mslct="01" and duty="0000"))=false then
			if inpos='1' then
				notro1<='0';
				nflag1<="00";
				if oflag1="00" then
					oflag1<="01";
				end if;

			elsif inpos='0' then
				outro1<='0';
				oflag1<="00";
				if nflag1="00" then
					nflag1<="01";
				end if;

			end if;


			if oflag1="01" then
				if k<25 then
					k:=k+1;
				elsif k=25 then
					outro1<='1';
					oflag1<="11";
					k:=1;
				end if;
			end if;

			if nflag1="01" then
				if m<25 then
					m:=m+1;
				elsif m=25 then
					notro1<='1';
					nflag1<="11";
					m:=1;
				end if;
			end if;
		else
			notro1<='0';
			outro1<='0';
		end if;

	end if;
end process;

out1<=outro1;
not1<=notro1;
outref<=outro1 and notro1;
```

```
end Behavioral;
```

Sseg

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.std_logic_arith.all;

entity sseg is
port(       mslct:in std_logic_vector(1 downto 0);
           datadc:in STD_LOGIC_VECTOR(3 downto 0);
            dataf:in STD_LOGIC_VECTOR(9 downto 0);
            digit:out std_logic_vector(3 downto 0);
            segout:out std_logic_vector(6 downto 0);
            clk:in std_logic);
end sseg;

architecture Behavioral of sseg is
signal segment: std_logic_vector(27 downto 0);
signal binbcd: std_logic_vector(11 downto 0):="000000000000";

--_____________________________BIN2BCD_____________________________
function bin2bcd ( bin : std_logic_vector(9 downto 0) ) return std_logic_vector is
variable i : integer:=0;
variable bcd : std_logic_vector(11 downto 0) := (others => '0');
variable bint : std_logic_vector(9 downto 0) := bin;

begin
for i in 0 to 9 loop  -- repeating 9 times.
bcd(11 downto 1) := bcd(10 downto 0);  --shifting the bits.
bcd(0) := bint(9);
bint(9 downto 1) := bint(8 downto 0);
bint(0) :='0';


if(i < 9 and bcd(3 downto 0) > "0100") then --add 3 if BCD digit is greater than 4.
bcd(3 downto 0) := bcd(3 downto 0) + "0011";
end if;

if(i < 9 and bcd(7 downto 4) > "0100") then --add 3 if BCD digit is greater than 4.
bcd(7 downto 4) := bcd(7 downto 4) + "0011";
end if;

if(i < 9 and bcd(11 downto 8) > "0100") then  --add 3 if BCD digit is greater than 4.
bcd(11 downto 8) := bcd(11 downto 8) + "0011";
end if;


end loop;
return bcd;
end bin2bcd;
--_____________________________________________________________________

signal newclk:std_logic:='0';
```

```
signal signin:std_logic;

signal dutyc:std_logic_vector(9 downto 0);

begin

process(clk)
variable ac,dc:integer range 0 to 100000000:=0;
begin
        if      rising_edge(clk) then
                if mslct="10" then

                        if ac=0 then
                                dc:=0;
                                binbcd<="101011001110";
                                ac:=ac+1;
                        elsif   ac>0 and ac<100000000 then
                                ac:=ac+1;
                        elsif ac=100000000 then
                                binbcd<=bin2bcd(dataf);
                        end if;

                elsif mslct="01" then

                        if datadc=15 then
                                        dutyc<="0001100010"; ---98%
                        elsif datadc<10 and datadc>=0 then
                                        dutyc<=datadc*"1010"+"0000000000"; --(10-90)%
                        elsif datadc=14 then
                                        dutyc<="0001001011";  --75%
                        elsif datadc=13 then
                                        dutyc<="0000110101";  --53%
                        else
                                        dutyc<="0000110010"; --%50
                        end if;


                        if dc=0 then
                                ac:=0;
                                binbcd<="110111001110";
                                dc:=dc+1;
                        elsif   dc<100000000 then
                                dc:=dc+1;
                        elsif dc=100000000 then
                                binbcd<=bin2bcd(dutyc);
                        end if;

                elsif mslct="11" then
                        ac:=0;
                        dc:=0;
                        binbcd<="110000011111";

                else
                        ac:=0;
```

```
                        dc:=0;
                        binbcd<="000000000000";
                end if;
        end if;
end process;

clkdiv:process(clk)
variable k:integer range 0 to 100000000;
begin
        if rising_edge(clk) then
                if k<100000000 then
                        k:=k+1;
                elsif k=100000000 then
                        k:=0;
                        newclk<=not newclk;
                end if;
        end if;
end process clkdiv;


seg:process(binbcd)
begin

        segment(27 downto 21) <= "1111111";

        for i in 0 to 2
        loop
                if binbcd(4*i+3 downto 4*i)="0000" then
                        segment(7*i+6 downto 7*i) <= "0000001";
                elsif binbcd(4*i+3 downto 4*i)="0001" then
                        segment(7*i+6 downto 7*i) <= "1001111";
                elsif binbcd(4*i+3 downto 4*i)="0010" then
                        segment(7*i+6 downto 7*i) <= "0010010";
                elsif binbcd(4*i+3 downto 4*i)="0011" then
                        segment(7*i+6 downto 7*i) <= "0000110";
                elsif binbcd(4*i+3 downto 4*i)="0100" then
                        segment(7*i+6 downto 7*i) <= "1001100";
                elsif binbcd(4*i+3 downto 4*i)="0101" then
                        segment(7*i+6 downto 7*i) <= "0100100";
                elsif binbcd(4*i+3 downto 4*i)="0110" then
                        segment(7*i+6 downto 7*i) <= "0100000";
                elsif binbcd(4*i+3 downto 4*i)="0111" then
                        segment(7*i+6 downto 7*i) <= "0001111";
                elsif binbcd(4*i+3 downto 4*i)="1000" then
                        segment(7*i+6 downto 7*i) <= "0000000";
                elsif binbcd(4*i+3 downto 4*i)="1001" then
                        segment(7*i+6 downto 7*i) <= "0000100";
                elsif binbcd(4*i+3 downto 4*i)="1010" then
                        segment(7*i+6 downto 7*i) <= "0001000";
                elsif binbcd(4*i+3 downto 4*i)="1011" then
                        segment(7*i+6 downto 7*i) <= "1100000";
                elsif binbcd(4*i+3 downto 4*i)="1100" then
                        segment(7*i+6 downto 7*i) <= "0110001";
                elsif binbcd(4*i+3 downto 4*i)="1101" then
```

```
                segment(7*i+6 downto 7*i) <= "1000010";
            elsif binbcd(4*i+3 downto 4*i)="1110" then
                segment(7*i+6 downto 7*i) <= "1111111";
            elsif binbcd(4*i+3 downto 4*i)="1111" then--letter t
                segment(7*i+6 downto 7*i) <= "1110000";

            else
                segment(7*i+6 downto 7*i) <= "1111111";
            end if;
        end loop;

end process seg;

disp:process(clk)
variable m:integer range 0 to 50000;
begin
        if rising_edge(clk) then
            if m<12500 then
                digit<="0111";
                segout<=segment(27 downto 21);
            elsif m>12500 and m<25000 then
                digit<="1011";
                segout<=segment(20 downto 14);
            elsif m>25000 and m<37500 then
                digit<="1101";
                segout<=segment(13 downto 7);
            elsif m>37500 and m<50000 then
                digit<="1110";
                segout<=segment(6 downto 0);
            end if;

            if m<50000 then
                m:=m+1;
            else
                m:=0;
            end if;

        end if;
end process disp;

end Behavioral;
```

Pin Assignment

```
NET "clk" LOC = "B8";

NET "output1" LOC = "C6";
NET "notout1" LOC = "C5";


NET "dutyfreq(7)" LOC = "N3";
NET "dutyfreq(6)" LOC = "E2";

NET "dutyfreq(5)" LOC = "F3";
NET "dutyfreq(4)" LOC = "G3";
```

```
NET "dutyfreq(3)" LOC = "B4";
NET "dutyfreq(2)" LOC = "K3";
NET "dutyfreq(1)" LOC = "L3";
NET "dutyfreq(0)" LOC = "P11";

NET "slct" LOC = "G12";
NET "led" LOC = "M5";

NET "digit(3)" LOC = "K14";
NET "digit(2)" LOC = "M13";
NET "digit(1)" LOC = "J12";
NET "digit(0)" LOC = "F12";


NET "segout(6)" LOC = "L14";
NET "segout(5)" LOC = "H12";
NET "segout(4)" LOC = "N14";
NET "segout(3)" LOC = "N11";
NET "segout(2)" LOC = "P12";
NET "segout(1)" LOC = "L13";
NET "segout(0)" LOC = "M12";
```

Appendix F

Line-Current Distortion (RMS definition & ripple calculation)

A signal with no dc component, can be written as the sum of its Fourier (harmonic) components:

$$i_s(t) = i_{s1}(t) + \sum_{h\neq 1} i_{sh}(t)$$

RMS: $I_S = \left[\frac{1}{T_1}\int_0^{T_1} i_s^2(t)dt\right]^{1/2}$

The cross product terms cancelled:

$$I_S = (I_{s1}^2 + \sum_{h\neq 1} I_{sh}^2)^{1/2} \text{ [1].}$$

- $i_{dis}(t) = i_s(t) - i_{s1}(t) = \sum_{h\neq 1} i_{sh}(t)$

⇨ In terms of rms values:

$$I_{dis} = [I_s^2 - I_{s1}^2]^{1/2} = (\sum_{h\neq 1} I_{sh}^2)^{1/2} \text{ [1].}$$