UNIVERSITY OF ÇUKUROVA
INSTITUE OF NATURAL AND APPLIED SCIENCE

MSc THESIS

Ahu AKÇAM

SYMBOLIC ANALYSIS OF ANALOG INTEGRATED CIRCUITS IN MATLAB

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ADANA, 2006

ÇUKUROVA ÜNİVERSİTESİ
FEN BİLİMLERİ ENSTİTÜSÜ

SYMBOLIC ANALYSIS OF ANALOG INTEGRATED CIRCUITS IN MATLAB

Ahu AKÇAM

YÜKSEK LİSANS TEZİ
ELEKTRİK-ELEKTRONİK MÜHENDİSLİĞİ ANA BİLİM DALI

Bu tez 25.12.2006 Tarihinde Aşağıdaki Jüri Üyeleri Tarafından Oybirliği ile Kabul Edilmiştir.

İmza ……...	İmza ……	İmza ……...
Yrd.Doç.Dr.Murat AKSOY	Doç.Dr. Turgut İKİZ	Yrd.Doç.Dr.Mehmet KARAKILÇIK
DANIŞMAN	ÜYE	ÜYE

Bu tez Enstitümüz Elektrik-Elektronik Mühendisliği Anabilim Dalında hazırlanmıştır

Kod No:

Prof. Dr. Aziz ERTUNÇ
Enstitü Müdürü

ÖZ

YÜKSEK LİSANS TEZİ

ANALOG TÜMLEŞİK DEVRELERİN MATLABDA SEMBOLİK ANALİZİ

Ahu AKÇAM

ÇUKUROVA ÜNİVERSİTESİ
FEN BİLİMLERİ ENSTİTÜSÜ
ELEKTRİK-ELEKTRONİK MÜHENDİSLİĞİ ANA BİLİM DALI

Danışman :Yrd.Doç.Dr. Murat AKSOY
Yıl :2006, Sayfa : 75
Jüri :Doç.Dr. Turgut İKİZ
Yrd.Doç.Dr. Murat AKSOY
Yrd.Doç.Dr. Mehmet KARAKILÇIK

Bu tez çalışmasında, Analog Tümleşik Devrelerin Sembolik Analizi devre analizi yönünden incelenmiştir ve lineer çözümleme için sistematik metotlar gösterilmiştir.

Analog devrelerin MATLAB / GUI modeli kuruldu. Bu oluşturulan devre modellerinin transfer fonksiyonları elde edildi.

Anahtar Kelimeler : Sembolik Analiz, Matlab, Tümleşik Devre.

ABSTRACT

MSc THESIS

SYMBOLIC ANALYSIS OF ANALOG INTEGRATED CIRCUITS IN MATLAB

Ahu AKÇAM

DEPARTMENT OF ELECTRICAL AND
ELECTRONICS ENGINEERING
INSTITUTE OF NATURAL AND APPLIED SCIENCES
UNIVERSITY OF ÇUKUROVA

Supervisor :Asst.Prof.Dr. Murat AKSOY
Year :2006, Pages : 75
Jury :Assoc. Prof.Dr. Turgut İKİZ
Asst.Prof.Dr. Murat AKSOY
Asst.Prof.Dr. Mehmet KARAKILÇIK

In this thesis, Symbolic Analysis of Analog Integrated Circuits has been examined circuit analysis and presented systematic methods for solving linearly.

The MATLAB / GUI models of analog circuits have been constituted and transfer function of these circuit models have been obtained.

Keywords : Symbolic Analysis, Matlab , Integrated Circuit

ACKNOWLEDGEMENTS

Although this thesis bears my name, there are many people who were essential in its realization.

I would like to thank them here.

I would like to express my gratitude to my supervisor Assist.Prof.Dr. Murat AKSOY for his support, guidance and encouragement.

I would like to thank Ramazan TOKMAK for his great support and encouragement, and Mehmet KANAL for his guidance.

I would also like to thank my brother Bülent AKÇAM, my mother AYŞE AKÇAM and whole family, especially, for their patience, moral support and understanding. But for you all, this thesis would never have been finished

CONTENTS **PAGE**

LIST OF FIGURES **PAGE**

LIST OF TABLES **PAGE**

1. INTRODUCTION

1.1. Symbolic Analysis Background

Several methods have been proposed to solve the problem of symbolic circuit simulation. A transfer function H(s) was produced with the frequency variable *s* being the only symbolic variable in early works. The more general case is when some or all of the circuit elements are represented by symbolic variables. The methods developed fall under one of the following categories (Hassoun Marwan M., Lin P.; April 1995):

1. The tree enumeration method: The method is based on by using the sum of all tree admittance products to find the determinant of the node admittance matrix several programs have been obtained based on this method.
2. The signal flow graph method: The methods developed here are based on the idea proposed by Mason in the 1950's. Formulation of the signal flow graph and then the evaluation of the gain formula associated with it (Mason's formula) is the basis for symbolic analysis using this method. This method is used in the publicly available programs NASAP and SNAP. An improved signal flow graph method which avoids term cancellations.
3. The interpolation method: This method is best suited when the frequency variable *s* is the only symbolic variable in the network. It requires the finding of the coefficients of the network's determinant polynomial by evaluating it at different values of *s*. However, using real values for *s* leads to ill-conditioned equations in addition to generating inaccurate solutions. Therefore, it is best to use complex values for *s*. Some implementations of this method use Fast Fourier Transforms to find the coefficients of the determinant.
4. The parameter extraction method: This method was introduced in 1973. Other variations on the method were proposed later. The advantage of the method is that it is directly related to the basic determinant properties of widely used equation formulation methods like the modified nodal method and the tableau

method. The first generation of computer programs available for symbolic circuit simulation based on these methods includes CORNAP, NASAP, and SNAP. Research in the late 1980's and early 1990's has produced newer symbolic analysis programs. These programs include ISAAC, ASAP, EASY, BRAINS and SSPICE.

These methods have network size limitations. The main problem is the exponential growth of the number of terms involved in the expression for the transfer function in a circuit as the network gets larger. The solution to analyzing large-scale circuits lies in a total departure from the traditional procedure of trying to state the transfer function as a single expression and using a sequence of expressions procedure instead. The idea is to produce a succession of small expressions with a backward hierarchical dependency on each other. The growth of the number of expressions in this case will be shown to be linear for practical circuits. (Hassoun Marwan M., Lin P.; April 1995)

1.2. Analog Integrated Circuits

*Analog c*ircuits are circuits dealing with signals free to vary from zero to full power supply voltage. This stands in contrast to *digital* circuits, which almost exclusively employ "all or nothing" signals: voltages restricted to values of zero and full supply voltage, with no valid state in between those extreme limits. Analog circuits are often referred to as *linear* circuits to emphasize the valid continuity of signal range forbidden in digital circuits, but this label is unfortunately misleading. Just because a voltage or current signal is allowed to vary smoothly between the extremes of zero and full power supply limits does not necessarily mean that all mathematical relationships between these signals are linear in the "straight-line" or "proportional" sense of the word. In this chapter, many so-called "linear" circuits are quite *non*linear in their behavior, either by necessity of physics or by design. (www.allaboutcircuits.com)

The circuits in this thesis make use of *IC* or *integrated circuit*, components. Such components are actually networks of interconnected components manufactured

on a single wafer of semiconducting material. Integrated circuits providing a multitude of pre-engineered functions are available at very low cost, benefiting students, hobbyists and professional circuit designers alike. Most integrated circuits provide the same functionality as "discrete" semiconductor circuits at higher levels of reliability and at a fraction of the cost. Usually, discrete-component circuit construction is favored only when power dissipation levels are too high for integrated circuits to handle.

Perhaps the most versatile and important analog integrated circuit for the student to master is the *operational amplifier*, or *op-amp*. Essentially nothing more than a differential amplifier with very high voltage gain; op-amps are the workhorse of the analog design world. By cleverly applying feedback from the output of an op-amp to one or more of its inputs, a wide variety of behaviors may be obtained from this single device. Many different models of op-amp are available at low cost, but circuits described in this thesis will incorporate only commonly available op amp models. (www.allaboutcircuits.com)

1.3. Overview of the Thesis

The title of this thesis is “Symbolic Analysis of Analog Integrated Circuits in Matlab”. The symbolical simulation of electrical circuits is important for Electrical Engineering education. The main aims of this thesis are to obtain the knowledge of circuit analysis and to see the experience of actual behavior of typical circuits. This purpose needs using of powerful software mathematical tools.

The MATLAB is numeric computation software for package engineering and scientific calculations. The main reasons for wide spread using of MATLAB are following: easy to learn and use; powerful, flexible and extensible; accurate, robust and fast; widely used in engineering and science; backed by a professional software company.

This thesis presents an approach according to Symbolic Analysis of Analog Integrated Circuits using specially designed examples that can be done on the base of MATLAB running on personal computers.

The thesis is built up as follows. In Chapter 2, Network analysis and synthesis will be defined and differs between these will be described. Kirchhoff Laws will be considered circuit equations can be assembled from a description of the circuit. Several methods exist for this; although the resulting systems of equations are mathematically equivalent, some methods produce systems which are more amenable to numerical computation. Some of these methods will be discussed.

In Chapter 3, Analog Integrated Circuits Analysis using Matlab; first of all it will be described analog integrated circuits. BJT, FET, OP AMP and OTA are modeled. It can be derived AC and DC models of this analog circuit to define in symbolic analysis program. There will be explained Matlab Program and graphical user interface (GUI) that is a graphical display that contains devices and examples using commands.

In Chapter 4, modeling and simulation of analog circuits will be discussed. Circuit modeling is presented using the levels of abstraction and hierarchy concepts. Furthermore, simulation techniques will be addressed that they are used for simulating analog circuits. Finally, a general overview of circuit simulation will be discussed.

In last chapter, the results and conclusions will be presented and discussed directions and recommendations for further research.

2. NETWORK ANALYSIS AND SYNTHESIS

Two important topics within the domain of electric network theory are network analysis and network synthesis. Three such words which are used extensively in describing the behavior of electric networks are the network, the excitation and the response. An example of the identification of the network, excitation and the response is given in Fig.2.1.

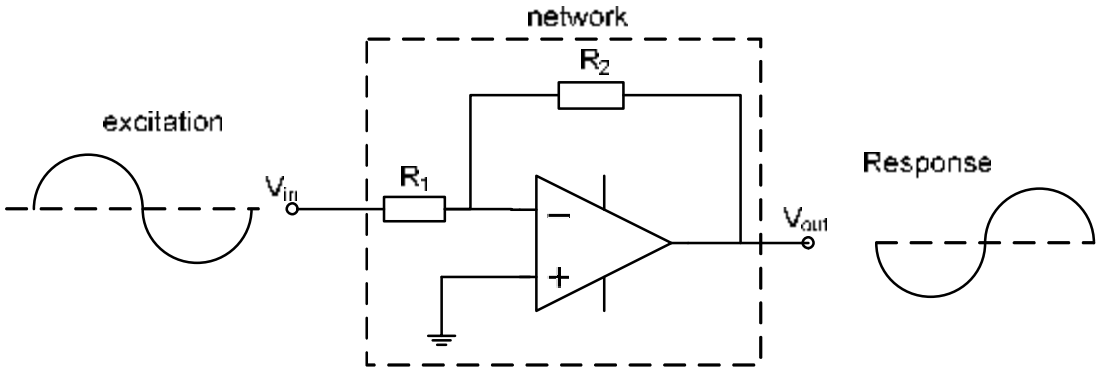


Figure 2.1. An example of the identification of the network, excitation, and response.

These words are used to describe electric networks have counterparts in practically all areas of scientific study. A wide variety of physical and biological phenomena may be described in terms of an action called a stimulus and a resultant reaction called a response if any two of the three quantities -the network, the excitation, and the response- are given, the third may be found for linear networks. (Balabanian N., 1958) If the network and the excitation are given and the response is to be determined, the problem is defined as analysis that is represented as in Fig.2.2.

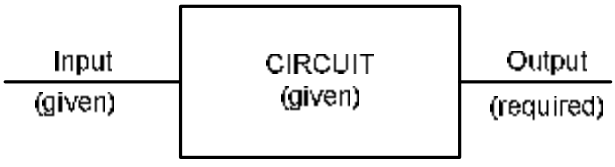


Figure 2.2. A typical “analysis problem” diagram.

When the excitation and the response are given and it is required to determine a network, the problem is defined as synthesis. It is shown in Fig.2.3. The third possibility, given the network and the response and required to find the excitation, has no generally accepted name and is not common.

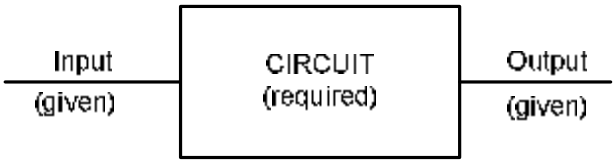


Figure 2.3. A typical “synthesis problem” diagram.

There is another important difference between analysis and synthesis. In analysis there is a unique solution although it may be difficult to find. In synthesis, however, solutions are not unique and there may exist no solution at all. If there is any solution to a given problem, there are an indefinite number of other solutions from which a choice may be made (a general characteristic of engineering design).

It might be found by the approximation methods just described correspond to networks with passive elements. A comparison of the approximation function with a list of requirements or necessary and sufficient conditions is known as testing.

In analysis there are standard tools for a systematic approach (e.g. circuit theory, Fourier/ Laplace transforms, convolution). In synthesis there are far too many design approaches to enumerate here, and plenty of scope for anyone to invent new ones. It is a less clearly defined problem and then, there are many ways to approach a solution. There is need of judgment as well as calculation.

2.1. Electrical Circuit Analysis

2.1.1. Electrical Sources

A practical energy source may take one of many forms, depending, for example, on electro-chemical, electromagnetic, thermo-electric, photo-electric, etc.,

principles, but for the purpose of circuit analysis only two idealized forms are recognized, to one of which all practical sources approximate. These are

- The voltage source
- The current source

The *voltage source* delivers to the circuit whatever currents is necessary to maintains its terminal. Fig.2.4a and Fig.2.4b shows the symbols for independent voltage sources.

It is important to appreciate that the voltage may be a function of, for example, time, temperature, pressure, etc.; it is constant only with respect to variations of load.

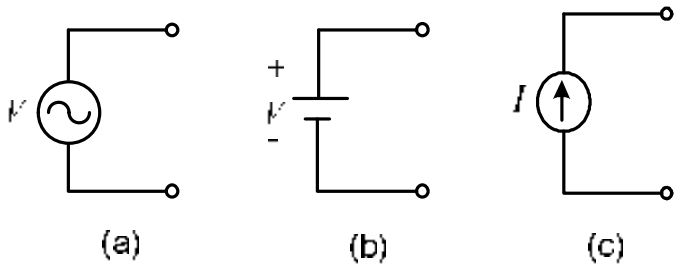


Figure 2.4. Symbols for independent voltage source: (a) used for constant or time-varying voltage, (b) used for constant voltage (dc), (c) a current source.

The *current source* maintains a constant current in the load irrespective of the terminal voltage-which, in this case, is determined by the magnitude of the load. As with the voltage source, the generated current may depend on many other factors, but its one essential attribute is the independence of load. The symbol for an independent current source is shown in Fig.2.4c where the arrow indicates the direction of current *i*.

It should be noted that, conventionally, current flows through the source from the negative to the positive terminal

2.1.2. Dependent Sources

Dependent sources, also known as controlled sources, are mathematical source whose are not arbitrarily specified but dependent upon, or its output controlled by the voltages and currents that exist at some other part of the circuit. The output is proportionality that called gain. Both voltage and current types of sources may be dependent, and either may be controlled by a voltage or a current. Thus, as shown in Fig.2.5, there are four types of dependent sources. These are v*oltage-controlled voltage-source* (VCVS), *voltage-controlled current source* (VCCS), *current-controlled voltage- source* (CCVS), current-*controlled current source* (CCCS). Form the Fig.2.5 the gain constants have dimensions of resistance (CCVS), conductance (VCCS), or are dimensionless (VCVS and CCCS). (Huelsman L. P., 1998)

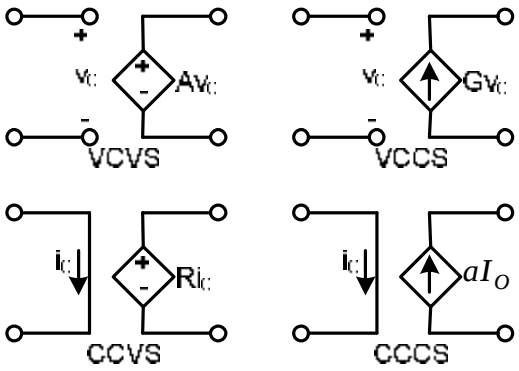


Figure 2.5. Types of ideal dependent sources.

2.1.3. The Load

By a method similar to that adopter for energy sources, the load -or passive element of a circuit– may be idealized and defined by its terminal *voltage / current* relationship. All practical passive devices possess energy dissipative properties, often accompanied by energy – storage properties so that three distinct idealized types are possible. (Yorke R., 1986)

(a) The resistance parameter

Materials in general have a characteristic behavior the flow of electric charge. The physical property or ability to resist current is known as *resistance* and is represented by the symbol *R*. The resistor is the simplest passive element.

Ohm's Law states that the voltage *v* across a resistor is directly proportional to the current to *i* flowing through the resistor.

$$v = iR \tag{2.1}$$

where R in Eq. (2.1) is measured in the unit of ohms, designated Ω. Since the value of R can change from zero to infinity. An element with $R = 0$ is called a short circuit, as shown in Fig.2.6a. Similarity, an element with $R = \infty$ is shown open circuit.

The corresponding diagrammatic representation is shown in Fig.2.6 (a) which also shows the positive directions of potential difference and current. It should be noted that, unlike an active element, a passive element develops a potential difference in opposition to the current flow so that there is a fall of potential through the element in the direction of the current flow.

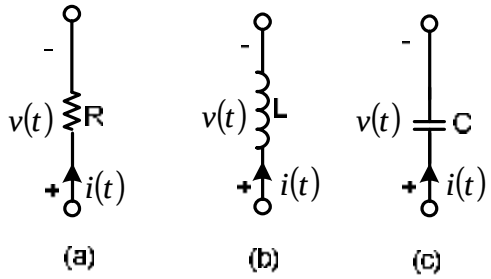


Figure 2.6. Symbols for (a) resistance, (b) inductance, (c) capacitance.

For this reason the terminal potential difference is called a potential drop-or voltage drop. The element which possesses resistance is termed a resistor.

The reciprocal of resistance is conductance designated by the symbol *G*. The conductance is a measure of how well an element will conduct electric circuit.

Thus,

$$G = \frac{1}{R} = \frac{i}{v} \tag{2.2}$$

The units of conductance the mho, siemens or reciprocal ohms with symbol, the inverted omega (Ω).

Hence an alternative form of Ohm's Law is:

$$i(t) = v(t)\, G \tag{2.3}$$

(b) The inductance parameter

An inductor is a passive element designed to store energy in this magnetic field. An inductor consists of coil of conducting wire.

If the current is allowed to pass through an inductor, it is found that the voltage across the inductor is directly proportional to the time rate of change of the current.

$$v(t) = L\, \frac{di(t)}{dt} \tag{2.4}$$

where *L* is the constant of proportionality called the inductance of the inductor. The unit of inductance is the Henry (H). The current-voltage relationship is obtained from Eq. (2.4) as,

$$i(t) = \frac{1}{L} \int_{t_0}^{t} v(t)\, dt + i(t_0) \tag{2.5}$$

where $i(t_0)$ is the initial current at t_0.

(c) The capacitance parameter

A capacitor is a passive element designed to store energy in its electric field. When a voltage source *v* is connected to the capacitor, it is stored the electric charge. The amount of charge stored, represented by *q*, is directly proportional to the applied voltage *v* so that

$$q = C\,v \tag{2.6}$$

where *C*, the constant of proportionality, is known *capacitance of capacitor*. The unit of capacitance is Farad (F). Its symbol is shown in Fig.2.6c. To obtain the current-voltage relationship of the capacitor, taking derivative of both sides of Eq.2.6.

$$i = \frac{dq}{dt} \tag{2.7}$$

differentiating both sides of Eq.2.6

$$i(t) = C\,\frac{dv(t)}{dt} \tag{2.8}$$

integrating both sides of Eq.2.8

$$v(t) = \frac{1}{C}\int_{t_0}^{t} i(t)\,dt + v(t_0) \tag{2.9}$$

where $v(t_0)$ is initial voltage across the capacitor at t_0.

2.2. Network Equilibrium Equations

The preceding section provided an introduction to the subject of network synthesis. The remainder of this chapter devoted to a review of topics to be used

later. It has begun by considering the Kirchhoff laws for the formulation of network equations. (Yorker, 1986)

In formulating equilibrium equations for networks, the Kirchhoff voltage law gives a summation of terms of the following three kinds:

$$V_R = R\, i(t), \quad V_L = L\frac{di(t)}{dt}, \quad V_C = \frac{1}{C}\int i(t)dt \tag{2.10}$$

Similarly, the Kirchhoff current law gives a summation of terms of the forms:

$$G\, v(t), \quad C\frac{dv(t)}{dt}, \quad \frac{1}{L}\int v(t)dt \tag{2.11}$$

The Laplace transforms of these terms are found using the following identities:

$$\mathrm{L}\,\mathrm{i}(\mathrm{t}) = \int_0^\infty i(t)e^{-st}dt \equiv I(s) \tag{2.12}$$

$$\mathrm{L}\,\frac{\mathrm{di}(\mathrm{t})}{\mathrm{dt}} = s\,I(s) - i(0+) \tag{2.13}$$

$$\int \mathrm{i}(\mathrm{t})dt = \frac{I(s)}{s} - \frac{1}{s}\int \mathrm{i}(\mathrm{t})dt\Big|_{t=0^+} \tag{2.14}$$

In network synthesis, it is conventional to neglect initial condition terms. Specifications are often given in terms of the sinusoidal steady state for which network functions are independent of initial conditions, leading to this convention. Neglecting initial conditions, terms in Eq.2.10 have the following transforms:

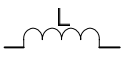
$$V_R(s) = R\, I(s), \quad V_L(s) = sLI(s), \quad V_C(s) = \frac{1}{Cs}I(s) \tag{2.15}$$

Here the multipliers of the transform current are *impedance functions*. Similarly, for Eq. 2.11, the transform terms are

$$I_R(s) = G\,V(s), \quad I_C(s) = CsV(s), \quad I_L(s) = \frac{1}{Ls}V(s) \tag{2.16}$$

and the multipliers of V(s) are *admittance functions*. These equations for *R, L,* and *C* are summarized in Table 2.1.

Table 2.1. Network Equilibrium Equations

	R	*L*	*C*
Symbol			
Relationship of $v(t)$ and $i(t)$, instantaneous voltage and current	$v = R\,i$	$v = L\frac{di}{dt}$	$v = \frac{1}{C}\int idt$
Transform equations, initial conditions set equal to zero	$V = R\,I$	$V = LsI$	$V = \frac{1}{Cs}\,I$
Impedance , Z(s)	R	Ls	$\frac{1}{Cs}$
Admittance, Y(s)	$\frac{1}{R}$	$\frac{1}{Ls}$	Cs

2.3. Kirchhoff's Voltage and Current Laws

There are two fundamental laws which govern the voltages and currents in a circuit. They are *Kirchhoff Voltage Law* and the *Kirchhoff Current Law.* Regardless of the composition of the circuit, the voltages and the currents of the circuit are constrained to satisfy these laws at all times.

The Kirchhoff Voltage Law (KVL) states that *the algebraic sum of all voltages around a closed path (or loop) in a circuit is zero.* The closed path (loop)

may be taken over a set of two-terminal element or over a set of nodes between which multiterminal elements are connected.

For every loop in the circuit a KVL equation can be written.

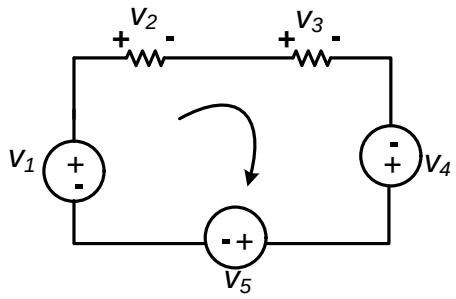


Figure 2.7. A single-loop circuit illustrating KVL.

In Fig.2.7 when KVL yields

$$(-v_1)+v_2+v_3+(-v_4)+v_5=0 \tag{2.17}$$

Rearranging terms gives

$$v_2+v_3+v_5=v_4+v_1 \tag{2.18}$$

The Kirchhoff Current Law (KCL) states that *algebraic the sum of the currents entering a node (or a closed boundary) is zero.* In a two-terminal element, the current entering into it is the same as the current leaving it.

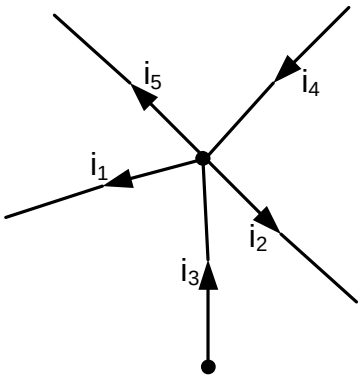


Figure 2.8. Currents at a node illustrating KCL.

Consider a node in Fig.2.8. Applying KCL gives

$$(-i_1)+(-i_2)+i_3+i_4+(-i_5)=0 \tag{2.19}$$

since currents i_1, i_2, i_5 are leaving the node, while i_3 and i_4 are entering it. By rearranging the terms,

$$i_3+i_4=i_1+i_2+i_5 \tag{2.20}$$

The sum of the currents entering a node is equal to the sum of the currents leaving the node.

These two laws, which are extraordinarily simple, govern the behavior of all circuits. From the point of view the mathematical theory of circuits, they constitute the basic axioms from which theorems concerning circuits are deduced. From the physical point of view, the equations based on the two laws are equilibrium equations of the physical system, which is the circuit. At all times, the voltages and currents in a circuit must be such that the KVL equations are satisfied for every closed loop and the KCL equations are satisfied at every node and for every element.

The actual values of the voltages and currents in a circuit will depend on the types of elements that are present.

2.3.1. Mesh Analysis

Having establishes that the KVL equations written for the meshes constitute a maximal set of independent voltages equations, now another scheme of formulating equations for planar circuits will be introduced. The scheme is very much like that the loop equations except that it is easier to apply by inspection. However, the scheme for loop equations is applicable to planar and nonplanar graphs, whereas the scheme for the meshes is applicable to planar graphs only.

Consider a general network consisting of *m* loops. Let $I_1, I_2, \mathbf{L}, I_m$ be the transforms of the *m* loop currents and $V_1, V_2, \mathbf{L}, V_m$ be the sums of the transforms of the driving voltage in each of the loops. The application of Kirchhoff's voltages law to this network results in *m* simultaneous equations

$$\begin{aligned} &\mathrm{Z}_{11} I_1 + \mathrm{Z}_{12} I_2 + \mathbf{L} + \mathrm{Z}_{1m} I_m = V_1 \\ &\mathrm{Z}_{21} I_1 + \mathrm{Z}_{22} I_2 + \mathbf{L} + \mathrm{Z}_{2m} I_m = V_2 \\ &\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K} \\ &\mathrm{Z}_{m1} I_1 + \mathrm{Z}_{m2} I_2 + \mathbf{L} + \mathrm{Z}_{mm} I_m = V_m \end{aligned} \tag{2.21}$$

Where Z_{jj} is the self-impedance of loop *j* and Z_{jk} is the impedance common to loops *j* and *k*, *j* and *k* being any numbers from 1 to *m*. The sing of Z_{jk} is positive when I_j and I_k have the reference direction but otherwise negative. These equations may be solved for the currents by the use of determinants. The determinant can be defined

$$\Delta = \begin{bmatrix} \mathrm{Z}_{11} & \mathrm{Z}_{12} & \mathrm{Z}_{13}\,\mathbf{L} & \mathrm{Z}_{1m} \\ \mathrm{Z}_{21} & \mathrm{Z}_{22} & \mathrm{Z}_{23}\,\mathbf{L} & \mathrm{Z}_{2m} \\ \mathbf{K}\,\mathbf{K} & \mathbf{K}\,\mathbf{K} & \mathbf{K}\,\mathbf{K}\,\mathbf{K} & \mathbf{K}\,\mathbf{K} \\ \mathrm{Z}_{m1} & \mathrm{Z}_{m2} & \mathrm{Z}_{l3}\,\mathbf{L} & \mathrm{Z}_{mm} \end{bmatrix} \tag{2.22}$$

to be the loop-basis system determinant.

Example 1 :

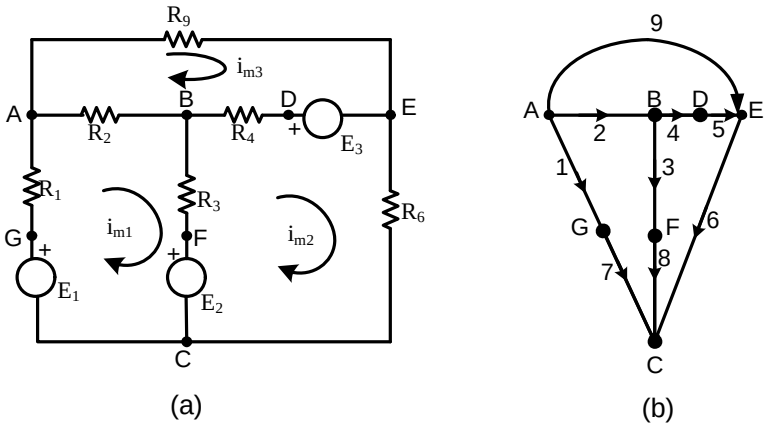


Figure 2.9. Illustration of mesh analysis (a) a mesh current is assigned to each mesh, (b) the graph of the circuit.

Consider Fig.2.9 Let the meshes be numbered and oriented as follows:

Mesh 1 : ABFCGA clockwise
Mesh 2 : BDECFB clockwise
Mesh 3 : AEDBA clockwise

Now there is a set of fictitious current variables known as the mesh currents. In each of meshes there is a circulating current flowing in the elements that constitute mesh. The mesh currents are denoted as i_{m1}, i_{m2} *and* i_{m3} in this example and are assigned the same orientations as those of the meshes. The mesh currents are not physical currents and, in the general, cannot be measured directly. Because of the last remark of the last section, mesh currents, in general, are not loop currents.

Suppose KVL equations for the meshes are written. In mesh 1,

$$v_1 + v_2 + v_3 + v_8 - v_7 = 0 \tag{2.23}$$

Now, express all the resistor voltages in terms of mesh currents. For example,

$$v_1 = R_1 i_{m1} \tag{2.24}$$

$$v_2 = R_2 (i_{m1} - i_{m3}) \tag{2.25}$$

Note that R_2 is shared by both mesh 1 and mesh 3. The current in R_2 is the algebraic sum of mesh currents i_{m1} and i_{m3} following this procedure, for the three meshes can be written, the following three KVL equations:

$$\begin{aligned} &R_1 i_{m1} + R_2 (i_{m1} - i_{m3}) + R_3 (i_{m1} - i_{m2}) - E_1 + E_2 = 0 \\ &R_4 (i_{m2} - i_{m3}) + R_6 i_{m2} - R_3 (i_{m1} - i_{m2}) + E_3 - E_2 = 0 \\ &R_9 i_{m3} - R_4 (i_{m2} - i_{m3}) - R_2 (i_{m1} - i_{m3}) - E_3 = 0 \end{aligned} \tag{2.26}$$

Rearranging the terms,

$$\begin{aligned} &(R_1 + R_2 + R_3) i_{m1} - R_3 i_{m2} - R_2 i_{m3} = E_1 - E_2 \\ &-R_3 i_{m1} + (R_3 + R_4 + R_6) i_{m2} - R_4 i_{m3} = E_2 - E_3 \\ &-R_2 i_{m1} - R_4 i_{m2} + (R_2 + R_4 + R_9) i_{m3} = E_3 \end{aligned} \tag{2.27}$$

which is a set of simultaneous algebraic equations in the unknowns i_{m1}, i_{m2} *and* i_{m3}. The set of equations is of the form in Eq. (2.21).

Eq. (2.27) are known as the *mesh equations*. They are merely the KVL equations expressed in terms of the fictitious variables, the mesh currents.

2.3.2. Node Analysis

Another scheme of writing circuit equations by inspection that is applicable to both planar and nonplanar graphs is that of *node analysis*, provided that the circuit contains only current sources as the excitations. In the case of mesh equations, KVL

equations can be written for the meshes in terms of set new current variables. In the case of node analysis, KCL equations can be written at each and every node except one in terms of a set of new voltage variables.

For a network of *n* nodes and a datum (or reference) node with current sources whose sums at of each of the nodes have transforms $I_1, I_2, \mathbf{L}, I_n$, a set of equilibrium equations may be written on the node basis. Let the transforms of the voltages of the various nodes with respect to the datum node be $V_1, V_2, \mathbf{L}, V_n$. Then the application of Kirchhoff's current law to the network result in the following simultaneous equations

$$\begin{aligned} &Y_{11}V_1 + Y_{12}V_2 + \mathbf{L} + Y_{1n}V_n = I_1 \\ &Y_{21}V_1 + Y_{22}V_2 + \mathbf{L} + Y_{2n}V_n = I_2 \\ &\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K}\,\mathbf{K} \\ &Y_{n1}V_1 + Y_{n2}V_2 + \mathbf{L} + Y_{nn}V_n = I_n \end{aligned} \tag{2.28}$$

where the admittance terms of the form Y_{jj} represent the admittance of all elements connected to node *j* with all other nodes grounded (to the datum), and the Y_{jk} terms represent the negative of admittance common to nodes *j* and *k, j* and *k* being any numbers from 1 to *n.* The node-basis equations may be solved for the voltages by means of determinants by defining the node-basis system determinant:

$$\Delta' = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & \mathbf{K} & Y_{1n} \\ Y_{21} & Y_{22} & Y_{23} & \mathbf{K} & Y_{2n} \\ \mathbf{K} & \mathbf{K} & \mathbf{K} & \mathbf{K} & \mathbf{K} \\ Y_{n1} & Y_{n2} & Y_{n3} & \mathbf{K} & Y_{nn} \end{bmatrix} \tag{2.29}$$

Example 2:

Consider the circuit of Fig.2.10 number the nodes as shown. Define four voltage variables, one from each of the four nodes 1, 2, 3 and 4 to node 5, which shall be called the reference node. The voltage graph is a tree with node 5 as the

"root" as shown Fig.2.10. denote the four voltages as v_{1r} , v_{2r} , v_{3r} *and* v_{4r} . All the branch voltages can be expressed in terms of the four voltages as follows:

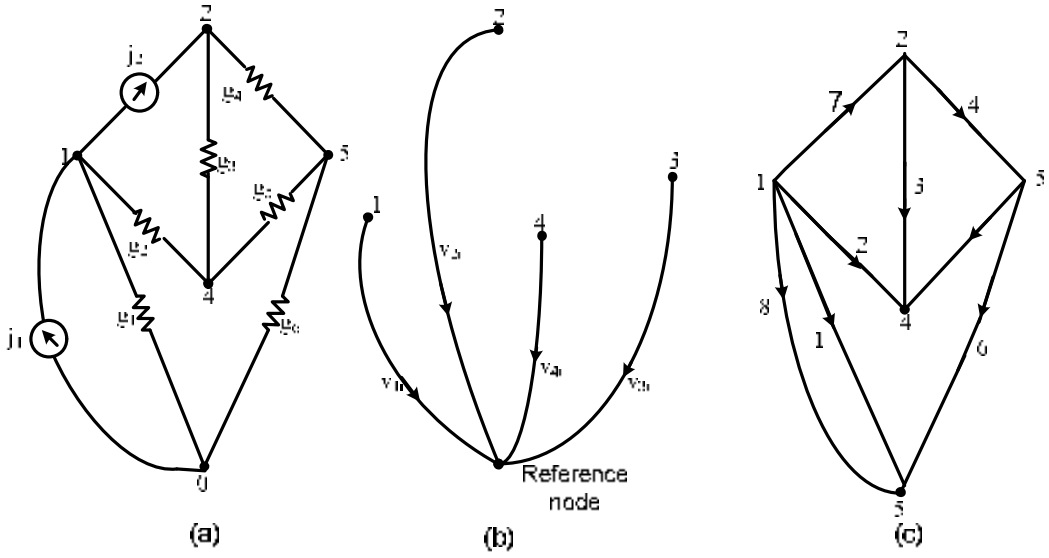


Figure 2.10. Node analysis (a) The circuit, (b) its voltage graph with node 5 chosen as the reference node, (c) the graph of the circuit

The branch currents can also be expressed in terms of the node-to-reference voltages. For example,

$$i_1 = g_1 v_1 = g_1 v_{1r} \tag{2.30}$$

$$i_2 = g_2 v_2 = g_2 (v_{1r} - v_{4r}) \tag{2.31}$$

Next writing the KCL equations for each of the four nodes 1, 2, 3 and 4 for example, at node1,

$$i_1 + i_2 + i_8 + i_7 = 0 \tag{2.32}$$

Expressing the currents in terms of the node-to-reference voltages and the sources,

$$
\begin{aligned}
& g_1 v_{1r} + g_2 \left(v_{1r} - v_{4r}\right) + j_2 + j_1 = 0 \\
& or \\
& \left(g_1 + g_2\right) v_{1r} + 0 v_{2r} + 0 v_{3r} - g_2 v_{4r} = j_1 - j_2
\end{aligned}
\tag{2.33}
$$

Repeating the procedure for all nodes, we obtain the following system of equations in the unknowns which are the node-to-reference voltages,

$$
\begin{aligned}
& \left(g_1 + g_2\right) v_{1r} + 0 v_{2r} + 0 v_{3r} - g_4 v_{4r} = j_1 - j_2 \\
& 0 v_{1r} + \left(g_3 + g_4\right) v_{2r} + g_4 v_{3r} - g_3 v_{4r} = j_2 \\
& 0 v_{1r} - g_4 v_{2r} + \left(g_4 + g_5 + g_6\right) v_{3r} - g_5 v_{4r} = 0 \\
& - g_2 v_{1r} + g_3 v_{2r} - g_5 v_{3r} + \left(g_2 + g_3 + g_5\right) v_{4r} = 0
\end{aligned}
\tag{2.34}
$$

The equations are of the form

$$
\begin{bmatrix}
g_1 + g_2 & 0 & 0 & - g_4 \\
0 & g_3 + g_4 & g_4 & - g_3 \\
0 & - g_4 & g_4 + g_5 + g_6 & - g_5 \\
- g_2 & g_3 & - g_5 & g_2 + g_3 + g_5
\end{bmatrix}
\begin{bmatrix} v_{1r} \\ v_{2r} \\ v_{3r} \\ v_{4r} \end{bmatrix}
=
\begin{bmatrix} j_1 - j_2 \\ j_2 \\ 0 \\ 0 \end{bmatrix}
\tag{2.35}
$$

These equations are known as node equations. They are KCL equations in terms of the node-to-reference voltages.

3. ANALOG INTEGRATED CIRCUIT ANALYSIS USING MATLAB

3.1. Bipolar Junction Transistors

The bipolar junction transistor (BJT) is a three-terminal device that contains two 'back-to-back' p-n junctions in the same block of semiconductor material (silicon). The three terminals are connected to three regions of semiconductor material that are named for the function each performs in the transistor. The three regions are named emitter, base and collector. The emitter emits or dispatches charge carriers into the base where control over the carriers is exercised; eventually the carriers are gathered in the collector region. (Kennth R.L.; Willy M.C. S., 1994)

The *NPN* and *PNP* types of BJTs are shown structurally in Fig.3.1, together with their schematic symbols.

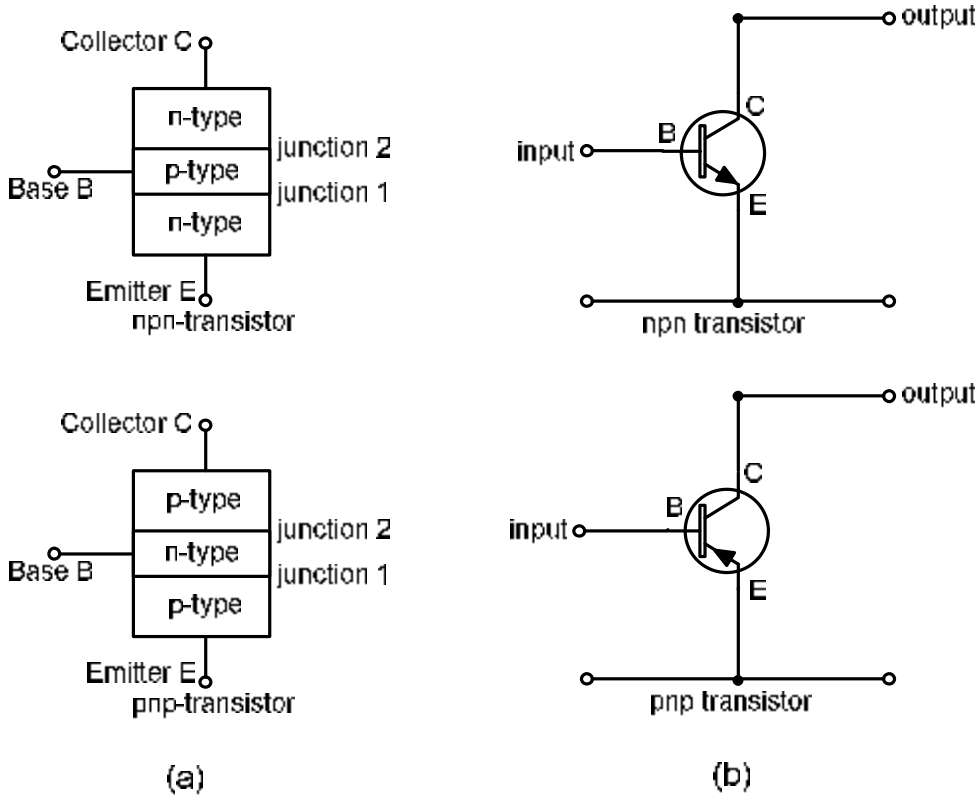


Figure 3.1. *NPN* and *PNP* transistor: (a) structure diagram and (b) schematic symbols.

3.1.1. BJT Static Characteristics

When the transistor is operated as an amplifier. Since the transistor has only three terminals, one terminal must be designated as being common to both input and output. Because of the versatility of the BJT, it can operate with any one of its three terminals as the common terminal. The amplifier configuration is usually named for the common terminal, that is, *common-base* (CB), *common-emitter* (CE), and *common-collector* (CC) or *emitter-follower*.

3.1.1.1. Common-Base Configuration

In the common-base (*CB*) configurations, the input is applied between emitter and base, while the output is taken between collector and base (as illustrated in Fig.3.2 for a *NPN* transistor).

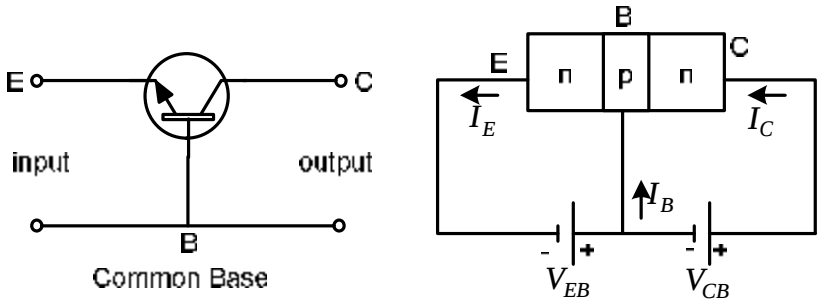


Figure 3.2. *CB* configuration using a *NPN* transistor. For normal operation V_{EB} is negative, V_{CB} is positive, and conventional currents are in the directions shown.

3.1.1.2. Common-Emitter Configuration

In the common-emitter (*CE*) configuration, the input is applied between base and emitter while the output is taken between collector and emitter, as shown in Fig.3.3 for a *NPN* transistor.

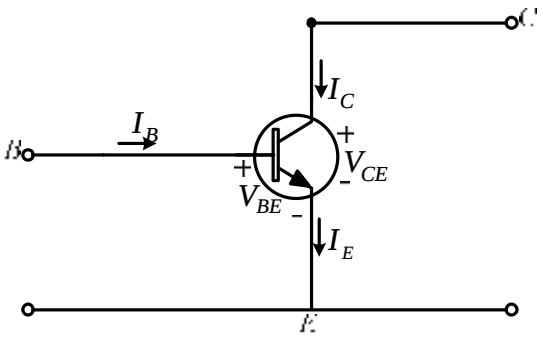


Figure 3.3. *CE* configuration using a *NPN* transistor.

3.1.1.3. Common-Collector Configuration

In the common-collector (*CC*) or emitter follower configuration, the input is applied to the base, while the output is taken from the emitter. The emitter follower (*CC* configuration) may be treated as a special case of the *CE* configuration.

3.1.2. DC Analysis of BJT Circuits

To establish proper operation of the BJT, the base emitter junction must be forward biased and the collector-base junction must be reverse biased.

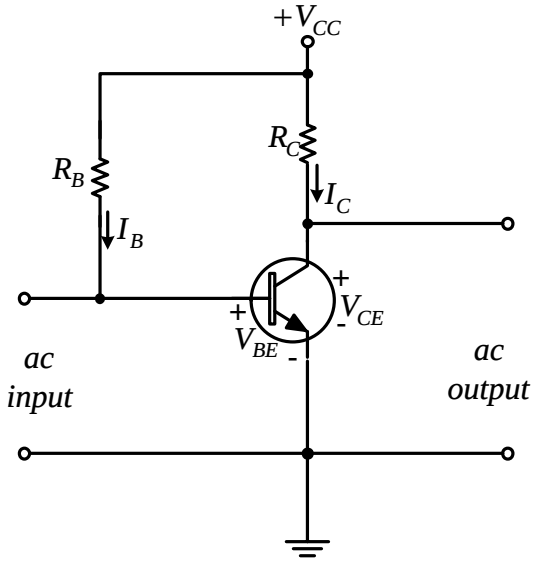


Figure 3.4. Fixed-bias circuit.

The circuit in Fig.3.4 called the fixed-bias circuit, provides the transistor with proper bias for normal operation.

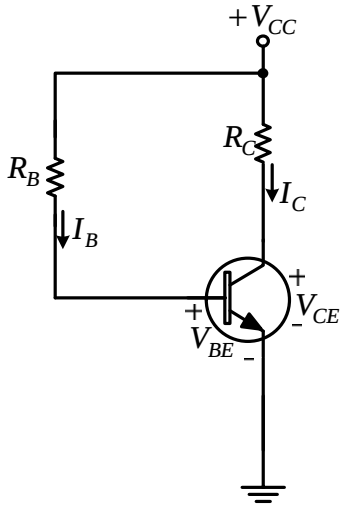


Figure 3.5. DC circuit of fixed-bias.

Taking the summation of voltages from the source V_{CC} and, through R_B, across the base emitter junction to ground, and setting it equal to zero, it is obtained $V_{CC} - I_B R_B - V_{BE} = 0$ which yields.

$$V_{CC} = I_B R_B + V_{BE} \tag{3.1}$$

The base-emitter voltage drop is a forward-biased diode drop. Typically for silicon transistors, this drop is 0.5 to 0.6V ; for germanium, between 0.2 and 0.3V in Eq.(3.1) when V_{BE} of this magnitude is compared V_{CC}, which is typically larger than 10 V, V_{BE} may be justifiably neglected. Thus,

$$V_{CC} \cong I_B R_B \tag{3.2}$$

This is the *bias curve equation*. Because both V_{CC} and R_B are fixed in value, Eq.(3.2) determines the quiescent base current. Therefore,

$$I_{BQ} \cong \frac{V_{CC}}{R_B} \tag{3.3}$$

In a similar manner, we take the summation of voltages in the collector circuit and set it equal to zero to obtain. $V_{CC} - I_C R_C - V_{CE} = 0$ which yields:

$$V_{CC} = I_C R_C + V_{CE} \tag{3.4}$$

This is the *load line equation*. The significance of this name is discussed when graphical techniques is examined for determining the operation point.

It the b of the transistor is known, the quiescent collector current is calculated from the relationship:

$$I_{CQ} = bI_{BQ} \tag{3.5}$$

where I_{BQ} has been determined in Eq.(3.3). Using the value of I_{CQ} thus calculated in Eq.(3.4) the quiescent is determined collector-emitter voltage from the relationship:

$$V_{CEQ} = V_{CC} - I_{CQ} R_C \tag{3.6}$$

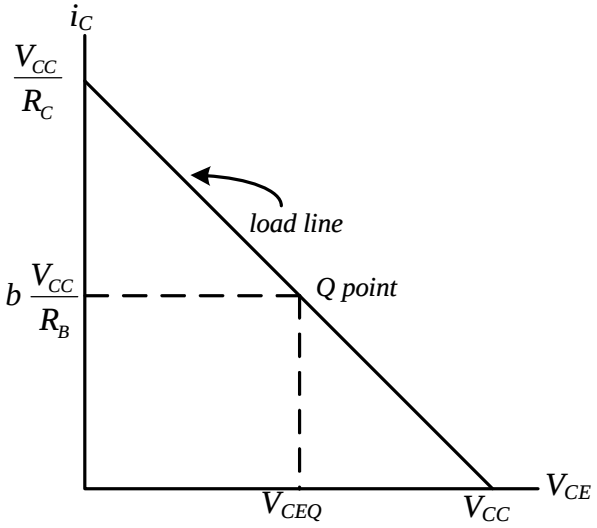


Figure 3.6. DC load line of the circuit.

If the values of the dc supply voltage, the bias resistors, and the transistor *b* are known, it can be seen that the dc operating (quiescent) point for the transistor in Fig.3.6 may be determined in the straight forward manner just indicated.

3.1.3. Hybrid Or *h* Parameters

A two- port network, like one shown in Fig.3.7, may be completely represented by a set of four parameters. The most suitable set of parameters for the BJT is the set of *h* parameters. The defining set of equations for the *h* parameters are

$$\begin{cases} v_1 = h_{11} i_1 + h_{12} v_2 \\ i_2 = h_{21} i_1 + h_{22} v_2 \end{cases} \tag{3.7}$$

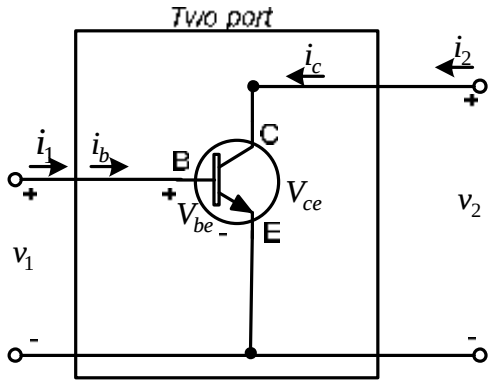


Figure 3.7. The CE configuration as two-port network.

$$h_{11} = h_{i(\ )} \quad h_{12} = h_{r(\ )} \quad h_{21} = h_{f(\ )} \quad h_{22} = h_{o(\ )} \tag{3.8}$$

The second subscript -either e, b or c - denotes whether the emitter, base, or collector terminal is common to the input and the output. For example, in the *CE* configuration

$h_{11} = h_{ie}$ - input impedance (in ohms)

$h_{12} = h_{re}$ - reverse voltage ratio (no units)

$h_{21} = h_{fe}$ - forward current ratio (no units)

$h_{22} = h_{oe}$ - output admittance (in Siemens)

In similar manner, the parameters in the *CB* configuration are : h_{ib}, h_{rb}, h_{fb}, *and* h_{ob} . In the *CC* configuration they are: h_{ic}, h_{rc}, h_{fc}, *and* h_{oc} .

CE h-parameter model : Making the appropriate substitutions in Eq.(3.7) for the CE configuration in Fig.3.8, It is obtained that the defining set of equations for the CE configuration. They are

$$\begin{cases} v_{be} = h_{ie} i_b + h_{re} v_2 \\ i_2 = h_{fe} i_1 + h_{oe} v_2 \end{cases} \tag{3.9}$$

$$h_{ie} = \left.\frac{v_{be}}{i_b}\right|_{V_{CEQ}=0} \quad h_{fe} = \left.\frac{i_c}{i_b}\right|_{V_{CEQ}=0} \quad h_{re} = \left.\frac{v_{be}}{v_{ce}}\right|_{I_{BQ}=0} \quad h_{oe} = \left.\frac{i_c}{v_{ce}}\right|_{I_{BQ}=0} \tag{3.10}$$

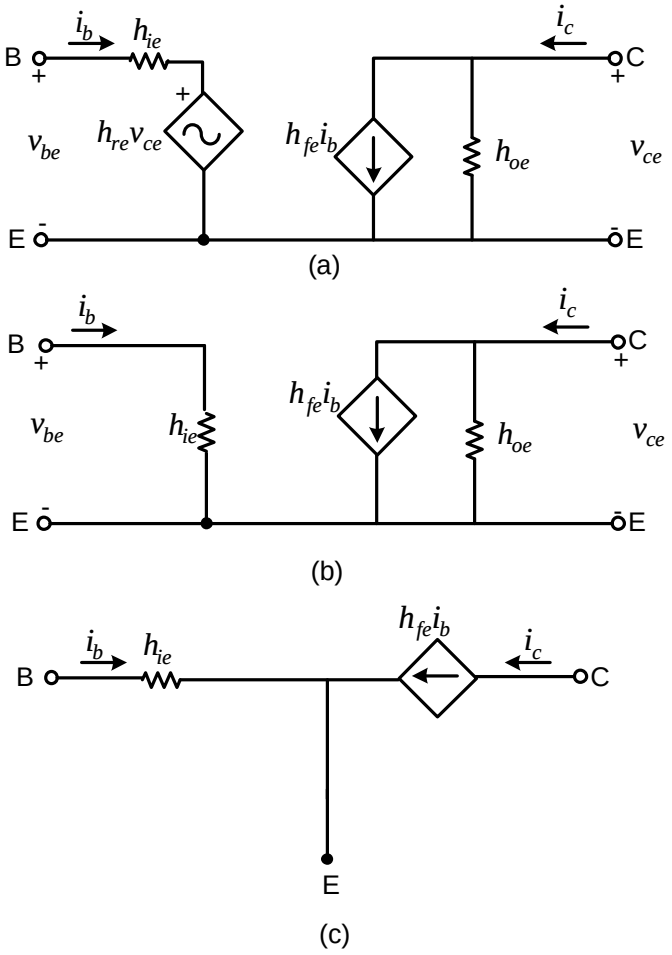


Figure 3.8. CE small-signal transistor model: (a) complete h-parameter model, (b) h_{fe} considered negligible, (c) both h_{re} and h_{oe} considered negligible.

***CB* h-parameter model :** The BJT almost always has a set of h parameters for the *CE* configuration. For completeness, the *CB* and *CC* configurations are mentioned here. The defining set of equations for the *CB* configuration may be seen from Fig.3.9 they are

$$\begin{cases} v_{eb} = -h_{ib} i_e + h_{rb} v_{cb} \\ i_c = -h_{fb} i_e + h_{ob} v_{cb} \end{cases} \tag{3.11}$$

Notice the minus signs in the equations just given. They indicate that the definition of i_1 is in the opposite direction to the actual flow of emitter current in an *NPN* transistor. The *CB* equivalent circuit is shown in Fig.3.9(b). However, in most cases, it is more convenient to use the approximate *CB* transistor model, as shown in Fig.3.9(c).

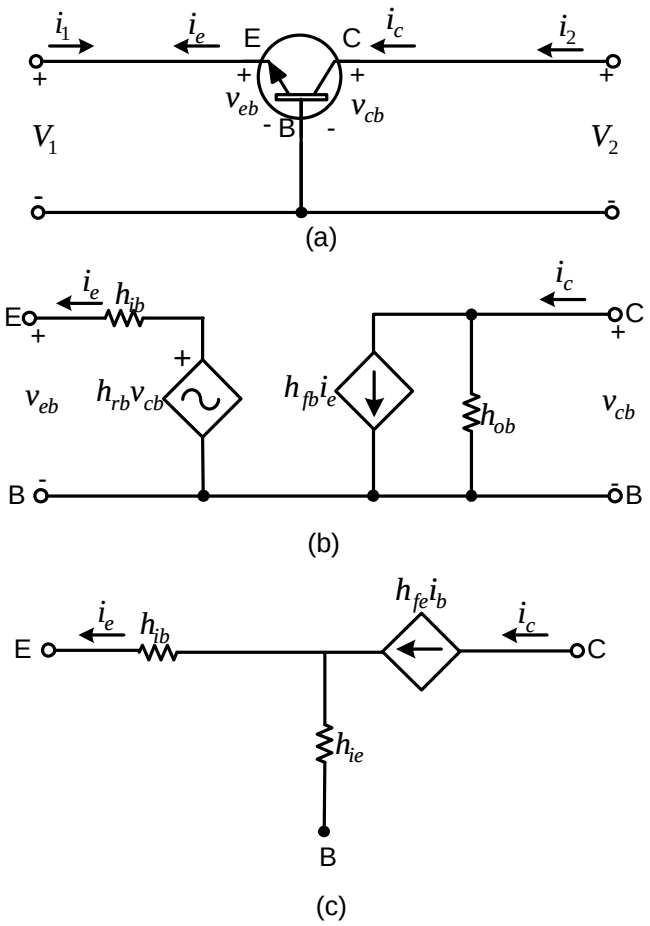


Figure 3.9. *CB* small-signal models: (a) *CB* configuration, (b) complete *CB* *h*-parameter model, (c) approximate *CB* model using *CE* parameters.

***CC* h-parameter model :** The *CC* configuration is illustrated in Fig.3.8 the set of defining equations in this case are

$$\begin{cases} v_{bc} = h_{ic} i_b + h_{rc} v_{ec} \\ -i_e = h_{fc} i_b + h_{oc} v_{ec} \end{cases} \tag{3.12}$$

The BJT model in the *CC* configuration is shown in Fig.3.10(b). As was the case in the CB configuration, however, it is more convenient to use the *CC* approximate model, as depicted in Fig.3.10(c).

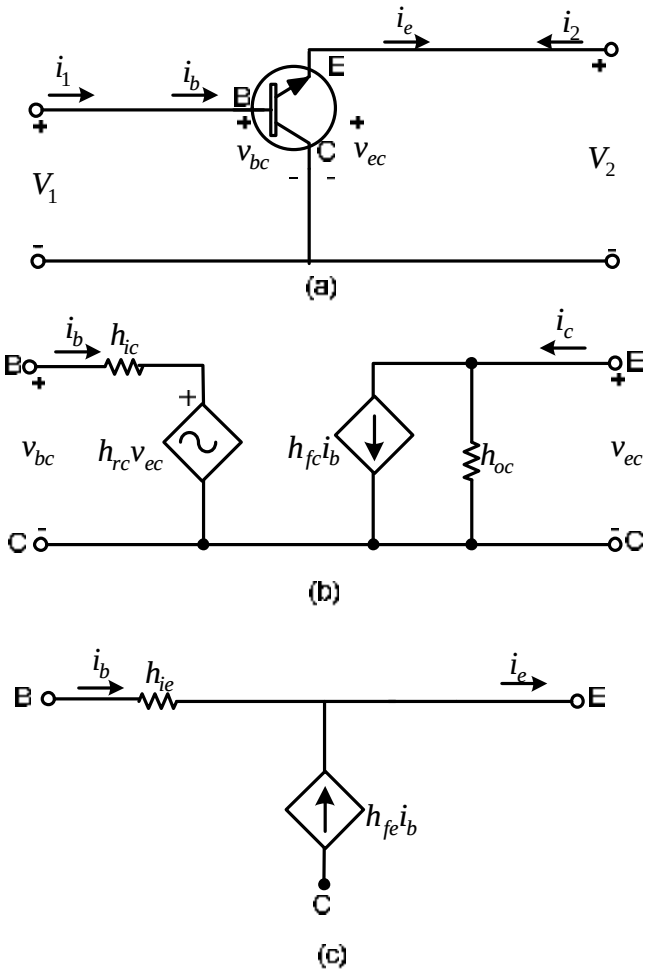


Figure 3.10. *CC* small-signal models: (a) *CC* configuration, (b) complete *CC* *h*-parameter model, (c) approximate *CC* model using *CE* parameters.

3.2. Field- Effect Transistor

Two types of field-effect transistor (FETs) are used in analog integrated circuit. These are the junction field effect transistor (JFET), Fig.3.11(a), and the metal-oxide-semiconductor field-effect transistor (MOSFET). Both devices

approximate the behavior of voltage controlled current sources. (Kennth R.L.; Willy M.C. S., 1994)

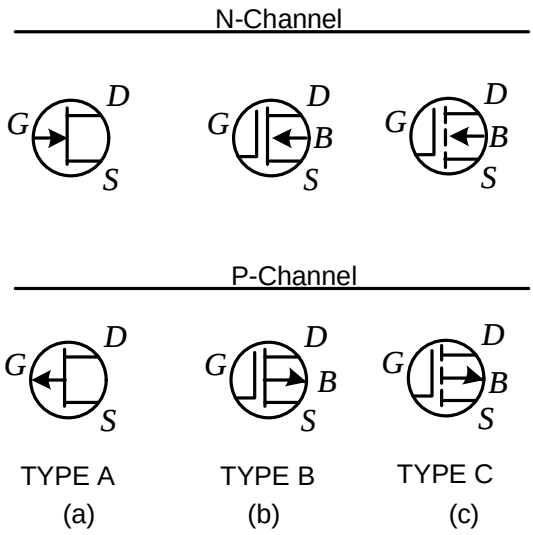


Figure 3.11. Schematic symbols for FET types : (a) JFET type A depletion mode only, (b) MOSFET type B depletion / enhancement mode, (c) MOSFET type C enhancement mode only. NOTE : G = gate, S= source, D=drain, B= bulk.

3.2.1. Junction Field-Effect Transistor

The structure of the two types of depletion mode (type A) JFETs is depicted in Fig.3.12. In Fig.3.12(a), an *N*-type semiconductor is formed and leads are attached to each end. One end is called the source; the other end is called the drain. A very narrow *P*-type region is diffused around the *N*-type semiconductor, forming an *N*-channel. This region of *P*-type semiconductor is called the gate. The third external connection is made to this gate region. Thus, the N-channel JFET consists of the single *PN* junction that is formed by the N type channel and the *P*-type gate. In the *P*-channel JFET pictured in Fig.3.12(b), the channel is *P*-type semiconductor material and the gate is *N*- type.

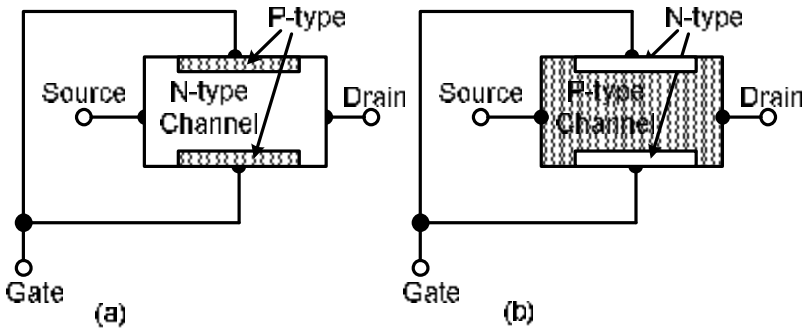


Figure 3.12. Structural representation of JFET : (a) N-channel and (b) P-channel.

3.2.1.1. Biasing The JFET

Self Bias : A JFET self bias circuit is illustrated in Fig.3.13. For this N-channel JFET, the supply voltage V_{DD} is positive in order to set up a positive voltage between

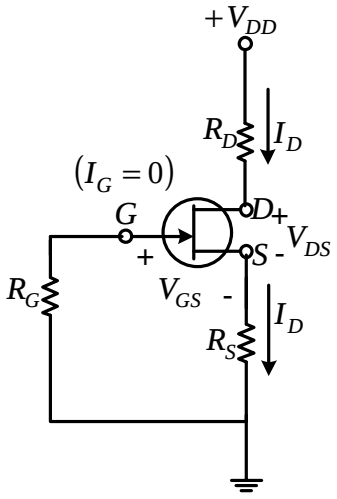


Figure 3.13. N-channel JFET self-bias circuit.

drain and source. Gate bias is accomplished by the voltage drop across R_S caused by the drain current. Equating the voltage supplied (V_{DD}) to the sum of the voltage drops in the output circuit, the load line equation:

$$V_{DD} = I_D(R_D + R_S) + V_{DS} \tag{3.13}$$

Because of the reverse bias between the *P*-type gate and the *N*-type channel, essentially no gate current flows. Thus, in the gate circuit, there is no dc voltage drop across R_G. Adding the voltages in the gate circuit gives the us bias curve equation for the circuit in Fig .3.13:

$$V_{GS} = -I_D R_S \tag{3.14}$$

Voltage Divider Bias : In the bias circuit in Fig.3.14, the voltage divider set up by resistors R_{G1} and R_{G2} makes the voltage from gate to ground positive. In order to reverse bias the gate-source junction, the voltage drop across R_S must be larger than the open-circuit voltage (Thevenin's voltage) across R_{G2}. The open-circuit voltage across R_{G2} is defined as V_{GG} and is determined by Eq.3.15.

$$V_{GG} = V_{DD}\frac{R_{G2}}{R_{G1} + R_{G2}} \tag{3.15}$$

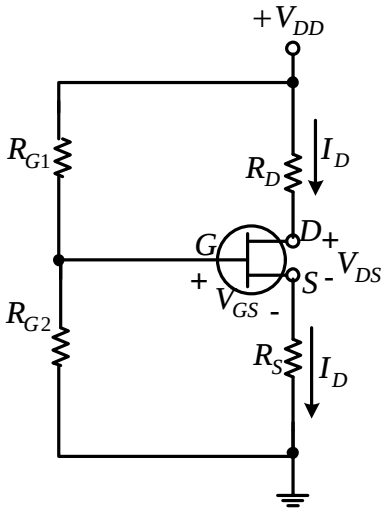


Figure 3.14. Voltage-divider bias circuit for the JFET.

To complete the Thevenization process, the equivalent resistance to left of the gate, labeled R_G, is determined with Eq.3.16.

$$R_G = \frac{R_{G1}R_{G2}}{R_{G1} + R_{G2}} \tag{3.16}$$

The resulting equivalent circuit with the voltage divider replaced by its Thevenin equivalent is illustrated in Fig.3.14. From the output circuit, we obtain the load line equation, Eq.(3.17)

$$V_{DD} = I_D \left(R_D + R_s\right) + V_{DS} \tag{3.17}$$

3.2.2. Biasing The Mosfet

The JFET bias circuit shown in Fig.3.12 may also be used for biasing a MOSFET. As we discussed in the previous section, the enhancement mode MOSFET must have a positive gate-source voltage. Therefore, in the bias circuit of Fig.3.12, the voltage developed across R_S must be somewhat smaller than that developed across R_{G2}. An alternate bias circuit for the enhancement mode MOSFET is indicated in Fig.3.13. This circuit has R_S omitted; therefore, the gate-source voltage is equal to the open-circuit voltage across R_{G2}, which is always positive.

The type B depletion mode MOSFET may be operated without any gate bias or with either a negative or positive gate bias. Both of the JFET bias circuits, Figures 3.13 and 3.14, as well as the enhancement mode MOSFET bias circuit, Fig.3.15, may be used for biasing a depletion mode MOSFET.

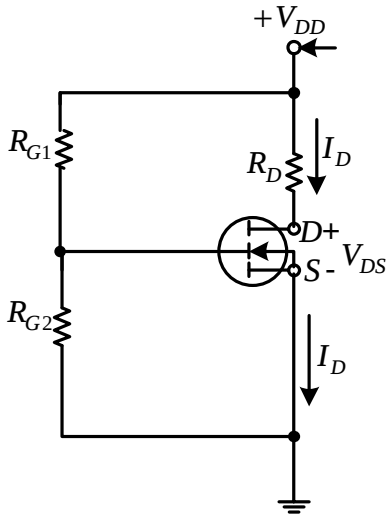


Figure 3.15. An N-channel enhancement mode MOSFET bias circuit.

3.2.3. Small- Signal FET Model

The FET (JFET and MOSFET) may be operated as an amplifier by applying a small time-varying signal to the gate and taking the amplified signal at the drain. The common terminal for both the input and output is the source.

Note that the basic similarity in the operation of the different FETs discussed is indicated by the similarity in their terminal characteristics. As a result, it would be expected that the ac small-signal models for the different FETs would be similar. In fact, the only difference between the ac performances of different FETs is in the slightly different magnitudes of some the parameters.

The low-frequency small-signal model for the FET is shown in Fig.3.14 at the drain terminal, the sum of the currents yields

$$i_d = g_m v_{gs} + \frac{1}{r_{ds}} v_{ds} \tag{3.18}$$

where the FET small-signal parameters g_m and r_{DS} are defined and evaluated from

$$g_m \equiv \textit{transconductance} \equiv \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DSQ}} \tag{3.19}$$

$$r_{DS} \equiv \textit{output resistance} \equiv \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GSQ}} \tag{3.20}$$

It is also useful to define the amplification factor of the FET:

$$m = g_m r_{DS} \tag{3.21}$$

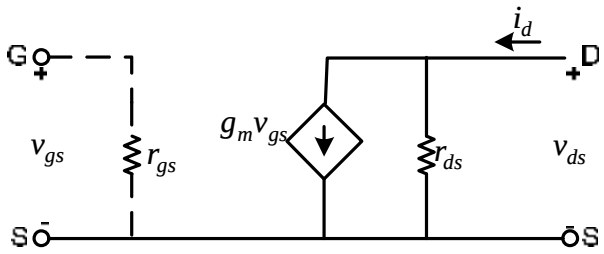


Figure 3.16. FET low-frequency small signal model.

The quantity r_{gs} is the input resistance, which is very hard to measure, especially for a MOSFET where the value may be over 1 tera ohm ($>10^{12}\ \Omega$) This quantity may be replaced by an open-circuit in most applications.

3.3. The Operational Amplifier

The operational amplifier is a voltage amplifier with extremely high gain. Fig.3.17a shows the symbol of the op amp and the power-supply connections to make it work. The inputs, identified by the "-" and "+" symbols, are designated inverting and noninverting. Their voltages with respect to ground are denoted v_N

and v_P, and the output voltage as v_O. The arrow head signifies signal flow from the inputs and output. (Franco S., 2002)

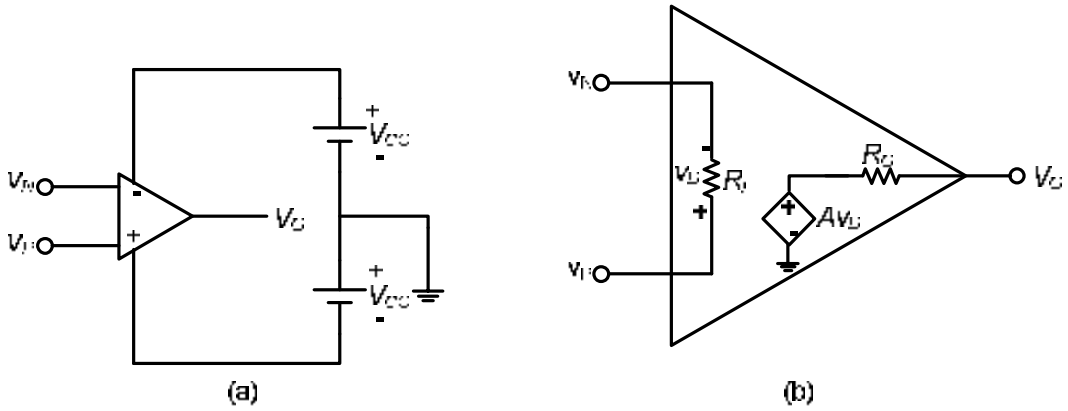


Figure 3.17. (a) Op amp symbol and power-supply connections, (b) Equivalent circuit of a powered op amp.

The difference

$$v_D = v_P - v_N \tag{3.22}$$

is called the differential input voltage and again A is also called unloaded gain. Because in the absence of output loading

$$v_o = Av_D = A(v_P - v_N) \tag{3.23}$$

3.3.1. The Ideal Op Amp

An ideal operational amplifier is differential input, single-ended output amplifier with infinite gain, infinite input resistance and zero output resistance. A conceptual schematic diagram is shown in Fig.3.18. Although assuming an ideal

opamp provides only an approximate analysis, most modern amplifier have such large gains and input impedances that the approximate analysis is a good one

An ideal op amp has following terminal conditions :

- Infinite open-loop gain, $A \approx \infty$.
- Infinite input resistance, $R_i \approx \infty$.
- Zero output resistance, $R_o \approx 0$.

i_P and i_N are the currents drawn by the noninverting and inverting inputs. The currents into both input terminals of an ideal op amp are zero.

$$i_P = i_N = 0 \tag{3.24}$$

The voltage across the input terminals is negligibly small;

$$v_D = v_P - v_N \approx 0 \qquad \text{or} \qquad v_P = v_N \tag{3.25}$$

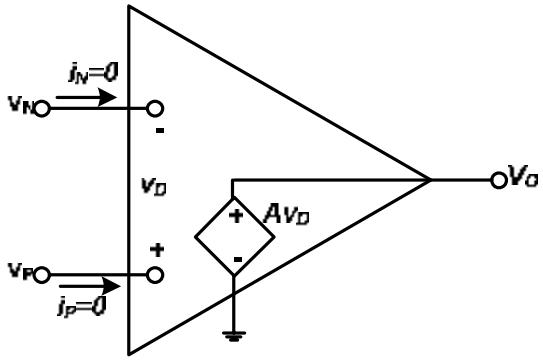


Figure 3.18. Ideal Op Amp model.

3.3.2. Basic Op Amp Configurations

3.3.2.1. The Inverting Amplifier

The inverting amplifier connection is shown in Fig.3.19. In this circuit, the noninverting input is grounded, v_i is connected to the inverting through R_1, and the feedback resistor R_2 is connected between the inverting input and output.

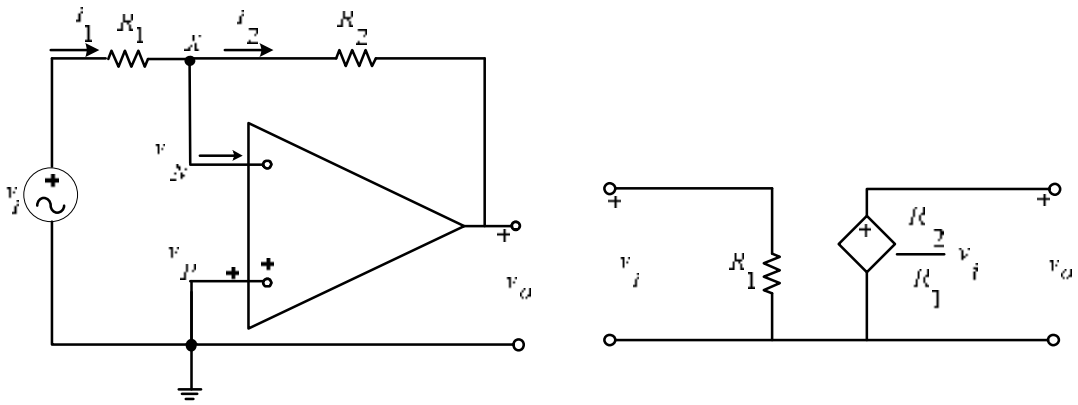


Figure 3.19. Inverting amplifier and its equivalent circuit.

Applying KCL at node X;

$$i_1 = i_2 \qquad \Rightarrow \qquad \frac{v_i - v_N}{R_1} = \frac{v_N - v_O}{R_2} \tag{3.26}$$

For an ideal op amp $v_N = v_P = 0$, the noninverting terminal is grounded

$$\frac{v_i}{R_1} = -\frac{v_O}{R_2} \tag{3.27}$$

or

$$v_O = -\frac{R_2}{R_1} v_i \tag{3.28}$$

for the ratio v_0/v_i and rearranging ,

$$A=\frac{v_0}{v_i}=-\frac{R_2}{R_1} \tag{3.29}$$

This circuit is again an amplifier. However , the gain A is negative, indicating that polarity of v_0 will be opposite to that of v_i to the inverting side of the op amp. Hence the circuit called an inverting amplifier.

3.3.2.2. The Noninverting Amplifier

The noninverting amplifier is shown in Fig.3.20. The input voltage v_i is applied directly at the noninverting input terminal and R_1 is connected between the ground and the inverting terminal. Application of KCL at the inverting terminal gives,

$$i_1 = i_2 \qquad \Rightarrow \qquad \frac{0 - v_N}{R_1} = \frac{v_N - v_O}{R_2} \tag{3.30}$$

But $v_N = v_P = v_i$,

$$-\frac{v_i}{R_1} = -\frac{v_i - v_O}{R_2} \tag{3.31}$$

or

$$v_O = \left(1 + \frac{R_2}{R_1}\right) v_i \tag{3.32}$$

for the ratio v_0 / v_i and rearranging , the voltage gain is

$$A = \frac{v_0}{v_i} = 1 + \frac{R_2}{R_1} \tag{3.33}$$

which does not have a negative sign.

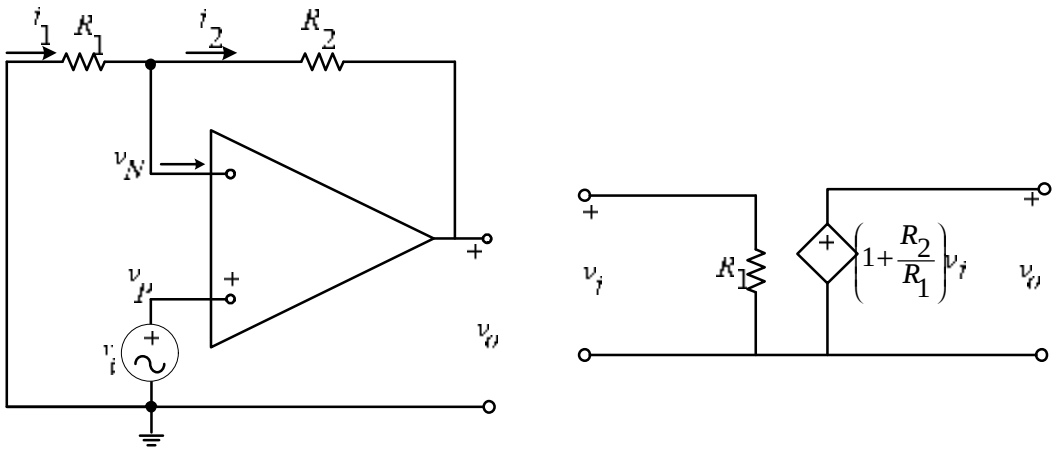


Figure 3.20. Noninverting amplifier and its equivalent circuit.

Notice that if feedback resistor $R_2 = 0$ (short circuit) or $R_1 = \infty$ (open circuit) or both, the gain becomes 1. Under these conditions ($R_2 = 0$ and $R_1 = \infty$), the circuit in Fig.3.20. becomes that shown in Fig.3.21 which is called a voltage follower (or unity gain amplifier) because output follows input. For a voltage follower

$$v_i = v_o \tag{3.34}$$

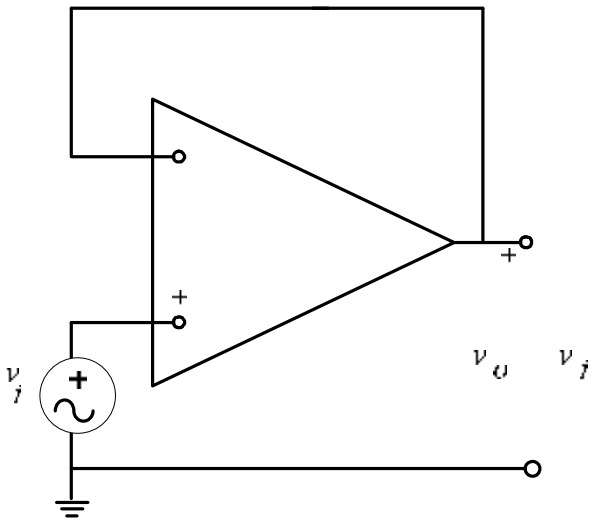


Figure 3.21. The voltage follower.

3.3.2.3.The Summing Amplifier

A summing amplifier is an op amp circuit that combines two or more inputs and produces one output that is the weighted sum of the inputs. The summing amplifier, shown Fig.3.22, is a variation of the inverting amplifier. To obtain a relationship between output and inputs, applying KCL at node *a* gives

$$i = i_1 + i_2 + i_3 \tag{3.35}$$

But

$$i_1 = \frac{v_1 - v_a}{R_1}, \qquad i_2 = \frac{v_2 - v_a}{R_2}$$

$$i_3 = \frac{v_3 - v_a}{R_3}, \qquad i = \frac{v_a - v_o}{R_f} \tag{3.36}$$

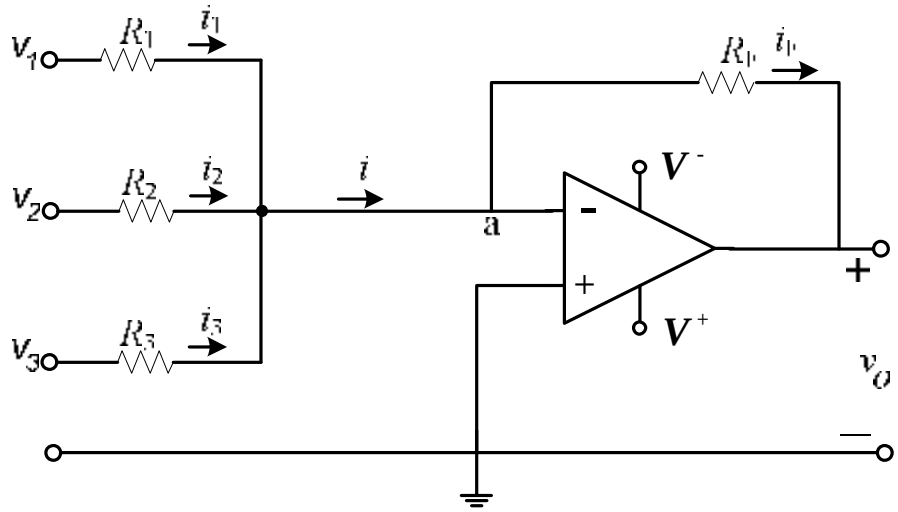


Figure 3.22. Summing Amplifier.

Solving for v_o yields

$$v_o = -\left(\frac{R_F}{R_1} v_1 + \frac{R_F}{R_2} v_2 + \frac{R_F}{R_3} v_3 \right) \tag{3.37}$$

indicating that the output is weighted sum of the inputs (hence the name *summing amplifiers*), with the weights being established be resistance ratios. A popular application of summing amplifiers is audio mixing.

If the Eq.(3.37) yields $R_3 = R_2 = R_1$, then Eq.(3.37) yields

$$v_o = -\frac{R_F}{R_1}\left(v_1 + v_2 + v_3 \right) \tag{3.38}$$

That is, v_o is proportional to the true sum of the inputs. The proportionality constant $-R_F / R_1$ can be varied all the way down to zero by implementing R_F with a variable resistance. If all resistances are equal, the circuit yields the inverted sum of its inputs, $v_o = -\left(v_1 + v_2 + v_3 \right)$.

3.3.2.4. The Difference Amplifier

The difference amplifier is device that the difference between two inputs but rejects any signals common to the inputs. As shown in Fig.3.23, applying KCL to node *a*,

$$\frac{v_1 - v_a}{R_1} = \frac{v_a - v_o}{R_2}$$

or (3.39)

$$v_0 = \left(\frac{R_2}{R_1} + 1 \right) v_a - \frac{R_2}{R_1} v_1$$

Applying KCL to node *b*,

$$\frac{v_2 - v_b}{R_3} = \frac{v_b - 0}{R_4} \tag{3.40}$$

or

$$v_b = \frac{R_4}{R_3 + R_4} v_2 \tag{3.41}$$

But $v_a = v_b$

$$v_0 = \left(\frac{R_2}{R_1} + 1 \right) \frac{R_4}{R_3 + R_4} v_2 - \frac{R_2}{R_1} v_1 \tag{3.42}$$

or

$$v_0 = \frac{R_2}{R_1}\frac{(1+R_1/R_2)}{(1+R_3/R_4)}v_2 - \frac{R_2}{R_1}v_1 \tag{3.43}$$

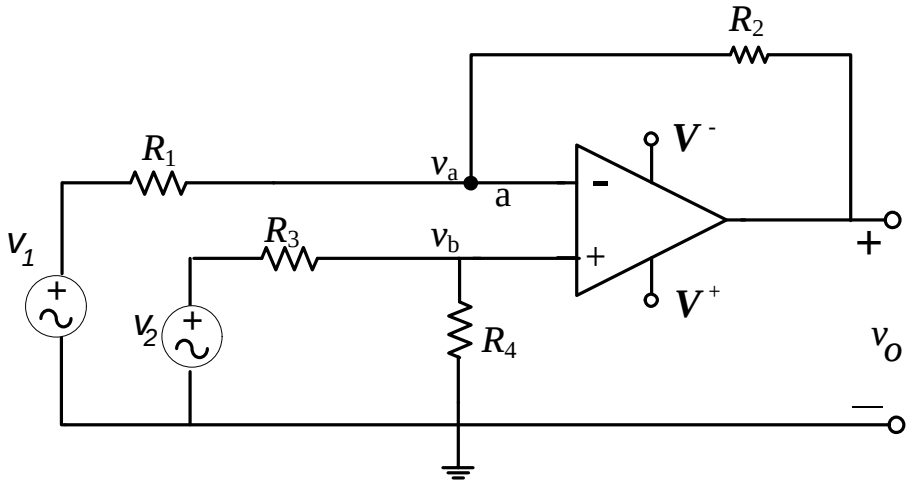


Figure 3.23. Difference amplifier.

An interesting case arises when the resistance pairs in Fig.23 are in equal ratios :

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} \tag{3.44}$$

When this condition is met, the resistances are said to form a balanced bridge, and Eq (3.43) simplifies to

$$v_o = \frac{R_2}{R_1}(v_2 - v_1) \tag{3.45}$$

The output is now proportional to the true difference of the inputs hence the name of the circuit.

3.3.2.5. The Differentiator

To find the input-output relationship for the circuit of Fig.3.24. Imposing $i_C = i_R$ is started. Using the capacitance law and Ohm's law, this becomes .

$$Cd(v_1 - 0)/dt = (0 - v_o)/R, \qquad \text{or} \qquad v_o(t) = -RC\frac{dv_I(t)}{dt} \tag{3.46}$$

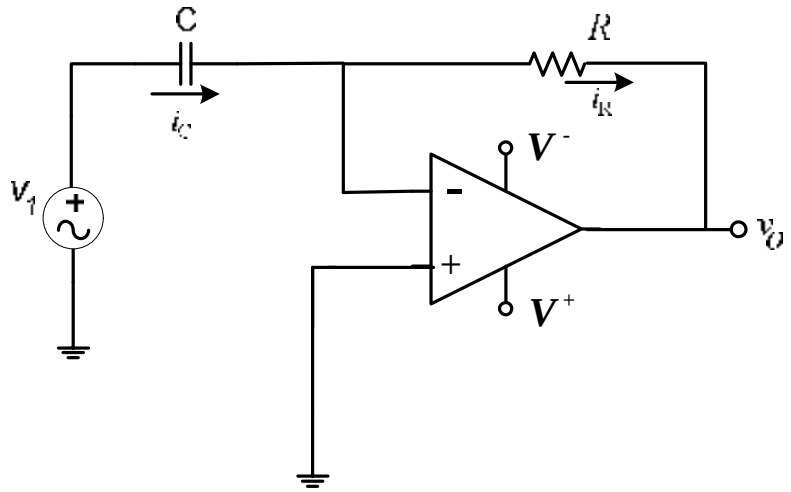


Figure 3.24. The op-amp differentiator.

The circuit yields an output that is proportional to the time derivative of the input-hence the name. The proportionality constant is set by *R* and *C*, and its units are seconds (s).

3.3.2.6.The Integrator

In the case of the integrator, the resistor *R* is used to develop a current i_R which is the proportional input voltage. This current flows into the capacitor *C*, whose voltage is proportional to the integral of the current i_R with respect to the time. Since output voltage is equal to the negative of the capacitor voltage, the output

is proportional to the integral of the input voltage with respect to time. In terms of equations,

$$i_R = \frac{V_1}{R} = i_C \tag{3.47}$$

$$v_o = -\frac{1}{C}\int_0^t i_C dt + v_o(0) \tag{3.48}$$

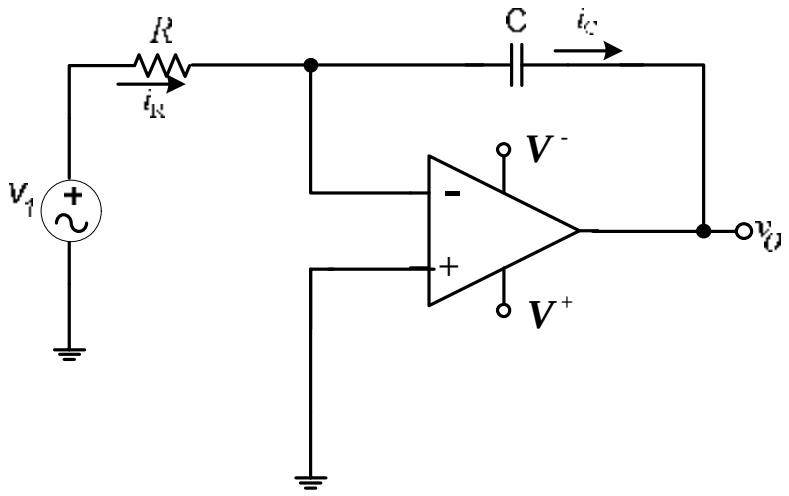


Figure 3.25. The op amp integrator.

Combining Eq.3.47 and Eq.3.48 yields

$$v_o(t) = -\frac{1}{RC}\int_0^t v_1(t)dt + v_o(0) \tag{3.49}$$

where $v_o(0)$ is the value of the output at t=0. This value depends on the charge initially stored in the capacitor.

3.4. The Operational Transconductance Amplifiers (OTA)

An operational transconductance amplifier (OTA) also called transconductance element or a transconductor, is a device that translates voltage inputs to current outputs such that $i_{OUT} = g_m v_{diff}$. The transconductance gain g_m can usually be varied is a filter parameter, I_{ABC} . When g_m is a filter parameter, I_{ABC} can be used to control or to program the characteristics of the filter. This device acts as high-gain voltage-controlled current source (VCCS) and produces an output current from a voltage input.(Franco S, 2002)

3.4.1. The Ideal Model

The circuit symbol for the OTA is shown in Fig.26a. The OTA is seen to be a three input, one output device. The three inputs are voltage signals v_+ ,v_- , and current I_{ABC} ("amplifier bias current") is a DC source used to control g_m , some interesting nonlinear functions can be realized if I_{ABC} is a more general signal. To simplify notation functions can be realized if I_{ABC} is often dropped from the symbol. It is emphasized that dropping I_{ABC} from the symbol is not to imply that I_{ABC} has been eliminated or that it is unimportant. In fact, the control g_m and I_{ABC} is crucial to the use of OTAs in precision filters. In Fig.3.26, the OTA is modeled by an ideal VCCS characterized by the relation,

$$i_O = g_m(v_+ - v_-) \tag{3.50}$$

with infinite input impedance and infinite output impedance, i.e.,

For linear filter applications where I_{ABC} is used to control g_m , it is highly desirable that g_m dependence on I_{ABC} be linear. Hence , the g_m for the ideal OTA is assumed to be

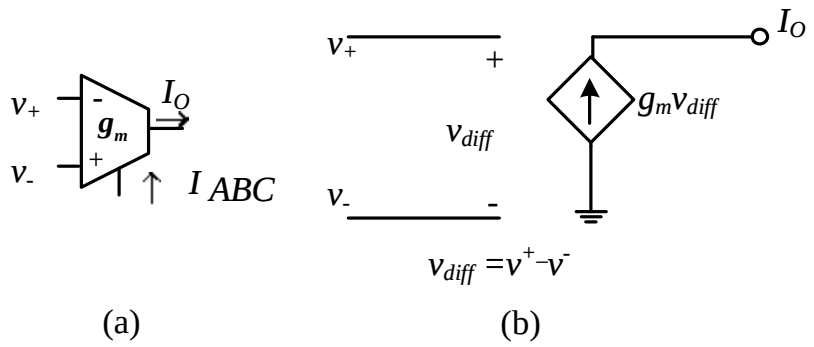


Figure 3.26. The differential OTA (a) symbol, (b) ideal model.

$$g_m = g_m(I_B) = hI_B \tag{3.51}$$

where h is a constant determined by process parameters, temperature, and input device geometries. The linear dependence in Eq. (3.51) occurs when OTA (MOS or bipolar) operates in the weak inversion or low current region.

Example: Find the transfer function of Fig.3.27.

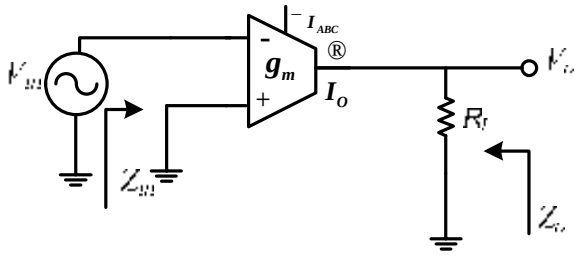


Figure 3.27. OTA example.

$$Z_{in} = \infty \qquad Z_O = R_L$$

$$I_O = g_m(0 - V_{in}) = -g_m V_{in}$$

$$V_O = R_L I_O = -R_L g_m V_{in}$$

$$\frac{V_O}{V_{in}} = -g_m R_L$$

3.4.2. $g_m - C$ Filters

A popular OTA applications is the realization of fully integrated continuous-time filters, where OTAs have emerged as viable alternatives to traditional op-amps. OTA-based filters are referred to as $G_m - C$ filters because they use OTAs and capacitors, but no resistors and no inductors. A popular $G_m - C$ filter example is shown Fig.3.28a. It is analysis proceeds as follows.

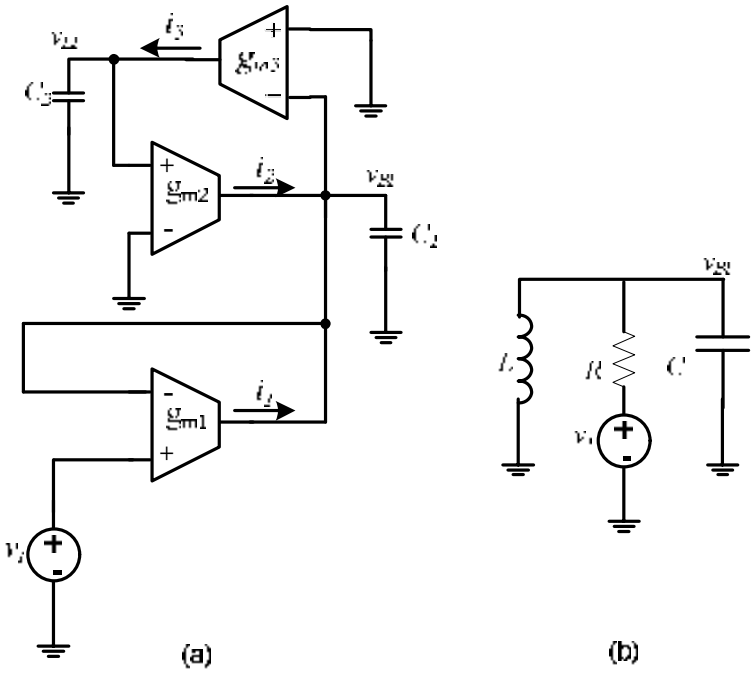


Figure 3.28. $g_m - C$ filter and its *RCL* equivalent.

By Eq.3.50 $i_1 = g_{m1}(v_i - v_{BP})$, $i_2 = g_{m2}\, v_{BP}$, $i_3 = -g_{m3}\, v_{BP}$. By Ohm's law, $v_{LP} = (1/sC_2)i_3$ *and* $v_{BP} = (1/sC_1)(i_1 + i_2)$. Rearranging these equations ,

$$\frac{v_{BP}}{v_{LP}} = \frac{sC_2 g_{m1}/g_{m2}g_{m3}}{s^2 C_1 C_2/g_{m2}g_{m3} + sC_2 g_{m1}/g_{m2}g_{m3} + 1} \tag{3.52}$$

It is readily that this transfer function is the as that of the *RLC* equivalent of Figure 3.28b, provided $C = C_1$, $R = 1/g_{m1}$, *and* $L = C_2 / g_{m2} g_{m3}$. Evidently, g_{m1} simulates a resistance, whereas the combination $g_{m2} - g_{m3} - C_2$ simulates an inductance. Moreover, the circuit provides v_{BP} and v_{LP} simultaneously, a feature not available in its *RLC* counterpart.

3.5. Matlab Programming

3.5.1. Introduction

Computation software for engineering and scientific calculations. The name MATLAB stands for MATRIX LABORATORY. symbolic circuit software package. It was developed by John Little and Cleve Moler of MathWorks, Inc. MATLAB was originally written to provide easy access to the matrix computation software packages LINPACK and EISPACK. (Attia J.O., 1999)

MATLAB is a high-level language whose basic data type is a matrix that does not require dimensioning. There is no compilation and linking as is done in high-level languages, such as C or FORTRAN. Computer solutions in MATLAB seem to be much quicker than those of high-level language such as C or FORTRAN. All computations are performed in complex-valued double precision arithmetic to guarantee high accuracy. (Attia J.O., 1999)

MATLAB has a rich set of plotting capabilities. The graphics are integrated in MATLAB. Since MATLAB is also a programming environment, a user can extend the functional capabilities of MATLAB by writing new modules. (Attia J.O., 1999)

MATLAB has a large collection of toolboxes in a variety of domains. Some example of MATLAB toolboxes are control systems, signal processing, neural network, image processing, and system identifications. The toolboxes consist of functions that can be used to perform computations in a specific domain. At present, there is no MATLAB toolbox for circuit analysis and communication theory. (Attia J.O., 1999)

3.5.2. Graphical User Interface Program

A graphical user interface (GUI) is a graphical display that contains devices, or components, that enable a user to perform interactive tasks. To perform these tasks, the user of the GUI does not have to create a script or type commands at the command line. Often, the user does not have to know the details of the task at hand. Fortunately, most computer users are already familiar with GUIs and know how to use standard GUI components. By providing an interface between the user and the application's underlying code, GUIs enable the user to operate the application without knowing the commands would be required by a command line interface. For this reason, applications that provide GUIs are easier to learn and use than those that are run from the command line. (www.mathworks.com)

The GUI components can be menus, toolbars, push buttons, radio buttons, list boxes, and sliders - just to name a few. In MATLAB, a GUI can also display data in tabular form or as plots, and can group related components. (www.mathworks.com)

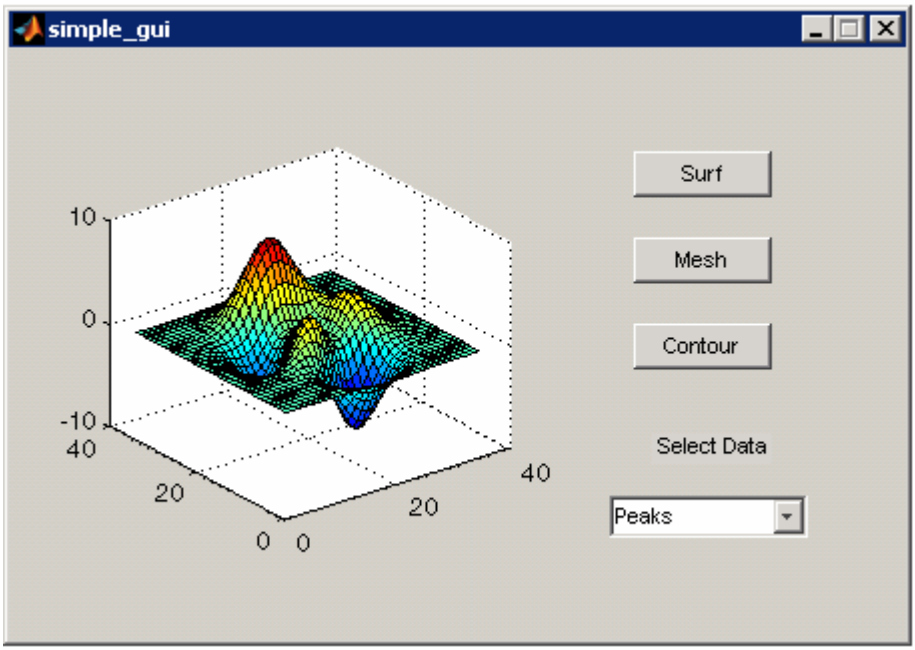


Figure 3.29. A simple GUI is illustrated.
www.mathworks.com

GUIDE Tools Summary The GUIDE tools are available from the Layout Editor shown in the Fig.3.30. The tools are called out in the figure and described briefly below. Subsequent sections show you how to use them.

GUIDE — GUI Development Environment GUIDE, the MATLAB Graphical User Interface development environment, provides a set of tools for creating GUIs. These tools greatly simplify the process of laying out and programming a GUI. This section introduces to GUIDE and the layout tools it provides. When opening a GUI in GUIDE, it is displayed in the Layout Editor, which is the control panel for all of the GUIDE tools. The Layout Editor enables you to lay out a GUI quickly and easily by dragging components, such as push buttons, pop-up menus, or axes, from the component palette into the layout area.

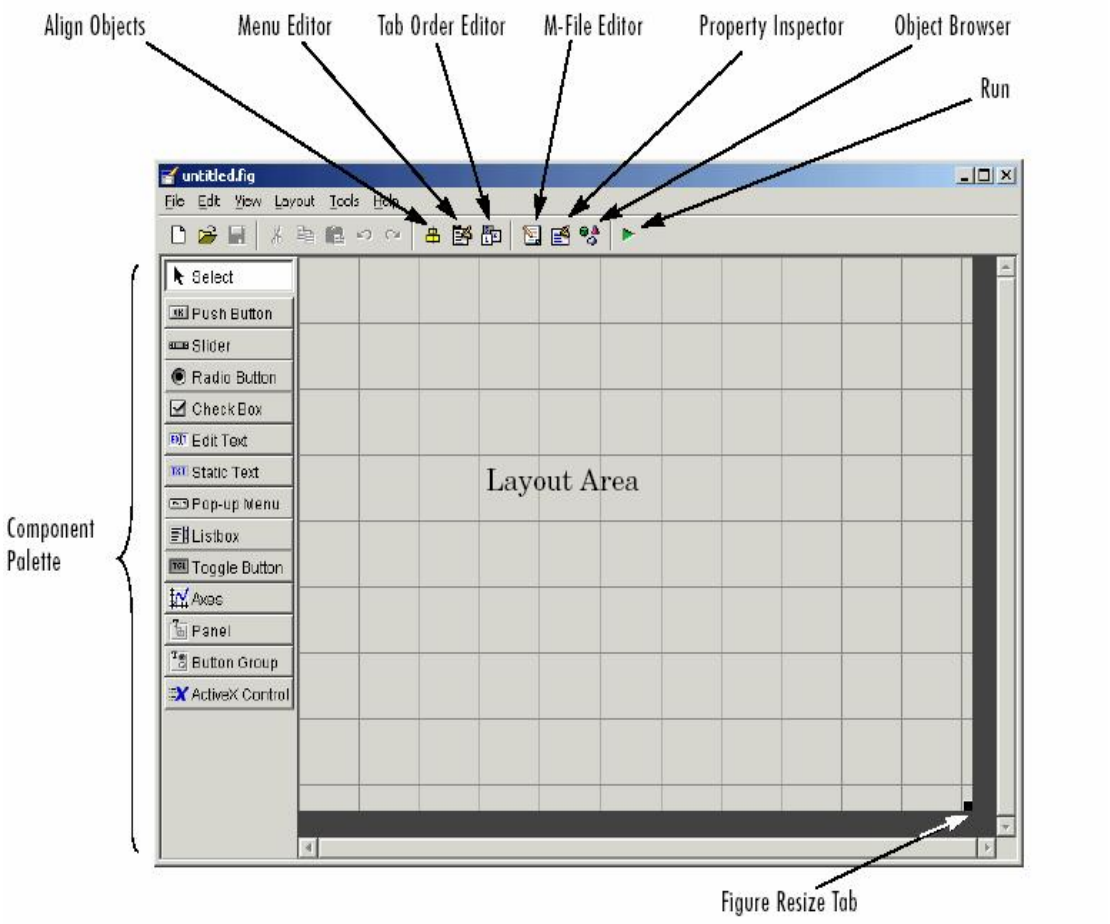


Figure 3.30. The Layout Editor.
www.mathworks.com

3.5.2.1. GUI FIG-Files and M-Files

GUIDE stores GUIs in two files, which are generated the first time saving or running the GUI:

FIG-file — a file with extension .fig that contains a complete description of the GUI figure layout and the components of the GUI: push buttons, menus, axes, and so on. When changes can be made to the GUI layout in the Layout Editor, these changes are saved in the FIG-file.

M-file — a file with extension .m that contains the code that controls the GUI, including the callbacks for its components. This file is referred to as the *GUI M-file*. When first GUI is run from the Layout Editor, GUIDE generates the GUI M-file with blank stubs for each of the callbacks. (www.mathworks.com)

Modal Question Dialog : The modal question dialog template displayed in the Layout Editor is shown in the following figure. From circuit analysis program an example ;

```
answer=questdlg('O.K.?', 'Open text file','Yes','No ','Yes');
if isempty(answer)|answer=='Yes' agree=1; end;
```

Frames : Frames are boxes that enclose regions of a figure window. Frames can make a user interface easier to understand by visually grouping related controls. Frames have no callback routines associated with them and only uicontrols can appear within frames (axes cannot).

List Boxes : List boxes display a list of items and enable users to select one or more items. The String property contains the list of strings displayed in the list box.

Push Buttons : Push buttons generate an action when clicked (e.g., an **OK** button may close a dialog box and apply settings). When clicking the mouse on a push button, it appears depressed; when the mouse is released the mouse, the button appears raised; and its callback executes.

Example from program;

```
function varargout = Close_Callback(h, eventdata, handles, varargin)
close all
```

4. CIRCUIT SIMULATION

4.1. Voltage Controlled Current Source

The voltage-dependent current source (VCCS), as shown in Fig.4.1, is determined by the following equation which introduces one more unknown in the admittance matrix.

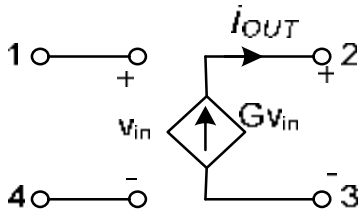


Figure 4.1. Voltage Controlled Current Source.

$$I_{OUT} = G.(V_1 - V_2) \rightarrow V_1 - V_4 - \frac{1}{G} I_{OUT} = 0 \tag{4.1}$$

The new unknown variable I_{OUT} must be considered by the four remaining simple equations.

$$I_1 = 0 \quad I_2 = I_{OUT} \quad I_3 = -I_{OUT} \quad I_4 = 0 \tag{4.2}$$

And in matrix representation this is:

$$\begin{bmatrix} . & . & . & . & 0 \\ . & . & . & . & 1 \\ . & . & . & . & -1 \\ . & . & . & . & 0 \\ 1 & 0 & 0 & -1 & -\frac{1}{G} \end{bmatrix} \bullet \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ I_{OUT} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ 0 \end{bmatrix} \tag{4.3}$$

It can be seen the last row which has been added by the VCCS represents the Determining Eq.4.1 the additional right hand column in the matrix keeps the system consistent.

4.2. Voltage Controlled Voltage Source

The voltage-dependent voltage source (VCVS), as shown in Fig.4.2, is determined by the following equation which introduces one more unknown in the admittance matrix.

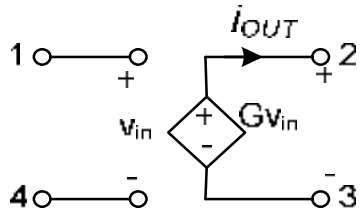


Figure 4.2. Voltage Controlled Voltage Source.

$$V_{in} = V_1 - V_4 \qquad V_2 - V_3 = G(V_1 - V_4) \rightarrow V_1.G - V_2 + V_3 - V_4.G = 0 \qquad (4.4)$$

The new unknown variable I_{OUT} must be considered by the four remaining simple equations.

$$I_1 = 0 \quad I_2 = -I_{OUT} \quad I_3 = I_{OUT} \quad I_4 = 0 \qquad (4.5)$$

And in matrix representation this is:

$$\begin{bmatrix} . & . & . & . & 0 \\ . & . & . & . & 1 \\ . & . & . & . & -1 \\ . & . & . & . & 0 \\ 1 & 0 & 0 & -1 & -\frac{1}{G} \end{bmatrix} \bullet \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ I_{OUT} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ 0 \end{bmatrix} \qquad (4.6)$$

Matlab Code;

```
%VCVS
for j=1:vcvs   % number of voltage controlled voltage sources
  if vv(j,3)
    B(vv(j,3),m0+j)=+1;
    C(m0+j,vv(j,3))=-1;
  end
  if vv(j,4)
    B(vv(j,4),m0+j)=-1;
    C(m0+j,vv(j,4))=+1;
  end
  if vv(j,1)
    C(m0+j,vv(j,1))=+vv(j,5);
  end
  if vv(j,2)
    C(m0+j,vv(j,2))=-vv(j,5);
  end
end
m0=m0+vcvs;
```

4.3. Current Controlled Current Source

The current-dependent current source (CCCS), as shown in Fig.4.3, is determined by the following equation which introduces one more unknown in the admittance matrix.

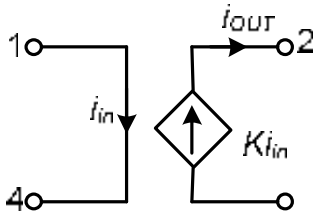


Figure 4.3. Current Controlled Current Source.

$$V_1 - V_4 = 0 \tag{4.7}$$

The new unknown variable I_{OUT} must be considered by the four remaining simple equations.

$$I_1 = +\frac{1}{K} I_{OUT} \quad I_2 = I_{OUT} \quad I_3 = -I_{OUT} \quad I_4 = -\frac{1}{K}.I_{OUT} \tag{4.8}$$

And in matrix representation this is:

$$\begin{bmatrix} . & . & . & . & 0 \\ . & . & . & . & 1 \\ . & . & . & . & -1 \\ . & . & . & . & 0 \\ 1 & 0 & 0 & -1 & -\frac{1}{K} \end{bmatrix} \bullet \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ I_{OUT} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ 0 \end{bmatrix} \tag{4.9}$$

Matlab Code :

```
%CCCS
for j=1:cccs
  if cc(j,1)
    B(cc(j,1),m0+j)=+1;
    C(m0+j,cc(j,1))=-1;
  end
  if cc(j,2)
    B(cc(j,2),m0+j)=-1;
    C(m0+j,cc(j,2))=+1;
  end
  if cc(j,3)
    B(cc(j,3),m0+j)=+cc(j,5);
  end
  if cc(j,4)
```

```
    B(cc(j,4),m0+j)=-cc(j,5);
  end
end
m0=m0+cccs;
```

4.4. Current Controlled Voltage Source

The current-dependent voltage source (CCVS), as shown in Fig.4.4, is determined by the following equations which introduce two more unknowns in the admittance matrix.

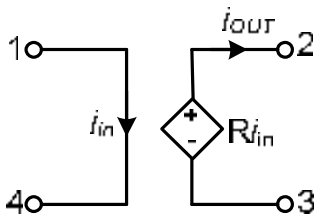


Figure 4.4. Current Controlled Voltage Source.

$$V_1 - V_4 = 0 \tag{4.10}$$

$$V_2 - V_3 = R.I_{in} \rightarrow V_2 - V_3 - R.I_{in} = 0 \tag{4.11}$$

The new unknown variables I_{OUT} and I_{in} must be considered by the four remaining simple equations.

$$V_2 - V_3 = R.I_{in} \rightarrow V_2 - V_3 - R.I_{in} = 0 \tag{4.12}$$

The matrix representation needs to be augmented by two more new rows (for the new unknown variables) and their corresponding columns.

$$\begin{bmatrix} . & . & . & . & 1 & 0 \\ . & . & . & . & 0 & -1 \\ . & . & . & . & 0 & 1 \\ . & . & . & . & -1 & 0 \\ 0 & 1 & -1 & 0 & -R & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 \end{bmatrix} \bullet \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ I_{in} \\ I_{OUT} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ 0 \\ 0 \end{bmatrix} \quad (4.13)$$

Matlab code from program for admittance matrix;

```
%CCVS
for j=1:ccvs
  if cv(j,1)
    B(cv(j,1),m0+2*j-1)=+1;
    C(m0+2*j-1,cv(j,1))=+1;
  end
  if cv(j,2)
    B(cv(j,2),m0+2*j-1)=-1;
    C(m0+2*j-1,cv(j,2))=-1;
  end
  if cv(j,3)
    B(cv(j,3),m0+2*j)=+1;
    C(m0+2*j,cv(j,3))=+1;
  end
  if cv(j,4)
    B(cv(j,4),m0+2*j)=-1;
    C(m0+2*j,cv(j,4))=-1;
  end
end
m0=m0+ccvs;
```

4.5. Operational Amplifier

The ideal operational amplifier, as shown in Fig.4.5, is determined by the following equation which introduces one more unknown in the Nodal Analysis matrix.

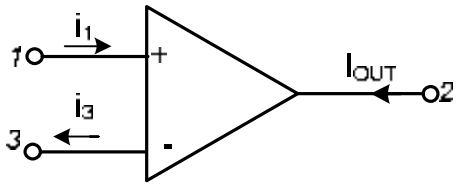


Figure 4.5. Ideal Operational Amplifier.

$$V_1 - V_3 = 0 \tag{4.14}$$

The new unknown variable I_{OUT} must be considered by the three remaining simple equations.

$$I_1 = 0 \quad I_2 = I_{OUT} \quad I_3 = 0 \tag{4.15}$$

And in matrix representation this is:

$$\begin{bmatrix} . & . & . & 0 \\ . & . & . & 1 \\ . & . & . & 0 \\ 1 & 0 & -1 & 0 \end{bmatrix} \bullet \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ I_{OUT} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ 0 \end{bmatrix} \tag{4.16}$$

Matlab Code for op-amps to constitute admittance matrix of circuit;

```
%Op-Amps
for j=1:noa
  if oa(j,3)
```

```
    B(oa(j,3),nvs+j)=1;
  end
  if oa(j,1)
    C(nvs+j,oa(j,1))=+1;
  end
  if oa(j,2)
    C(nvs+j,oa(j,2))=-1;
  end
end
D=zeros(m);
n0=nvs+ncc+nvv;
for j=1:ncv
  D(m0+2*j,m0+2*j-1)=-cv(j,5);
end
```

4.6.Simulation Examples

Example 1:

Simulation Steps :

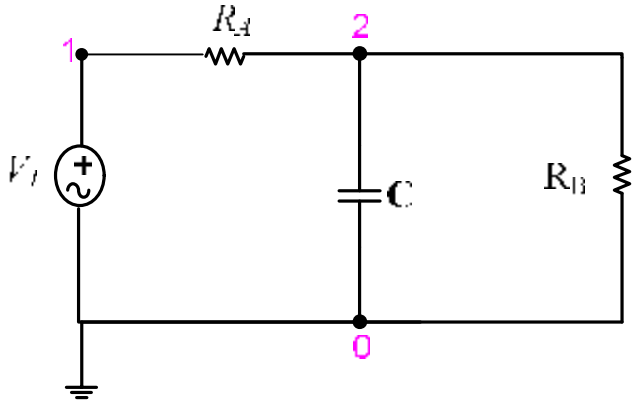


Figure 4.6. Capacitive low-pass filter simulation.

Step 1: Netlist file (*.txt) is loaded.

```
>> fname='clp.txt'
```

fname = clp.txt

>> ahu

Netlist

V1 1 0

RA 1 2

C 2 0

RB 2 0

Solved variables:

[v_1]

[v_2]

[I_V1]

Step 2 : The ratio of required variables is written to find transfer function in s-domain.

>> pretty(v_2/v_1)

Transfer function :

$$\frac{RB}{RB + s\,C\,RA\,RB + RA}$$

It can be written same example given a value for using circuit devices in the circuit:

Netlist

V1 1 0 1

RA 1 2 500

C 2 0 7E-6

RB 2 0 1000

>> eval(v_2/v_1)

```
>> [n,d]=numden(eval(v_2/v_1))

>> mySys=tf(sym2poly(n),sym2poly(d))
```

Transfer function:

```
      2.951e020
-----------------------------
1.033e018 s + 4.427e020
```

Step 3 : Step response and bode diagram are plotted

```
 >> step(mySys)
```

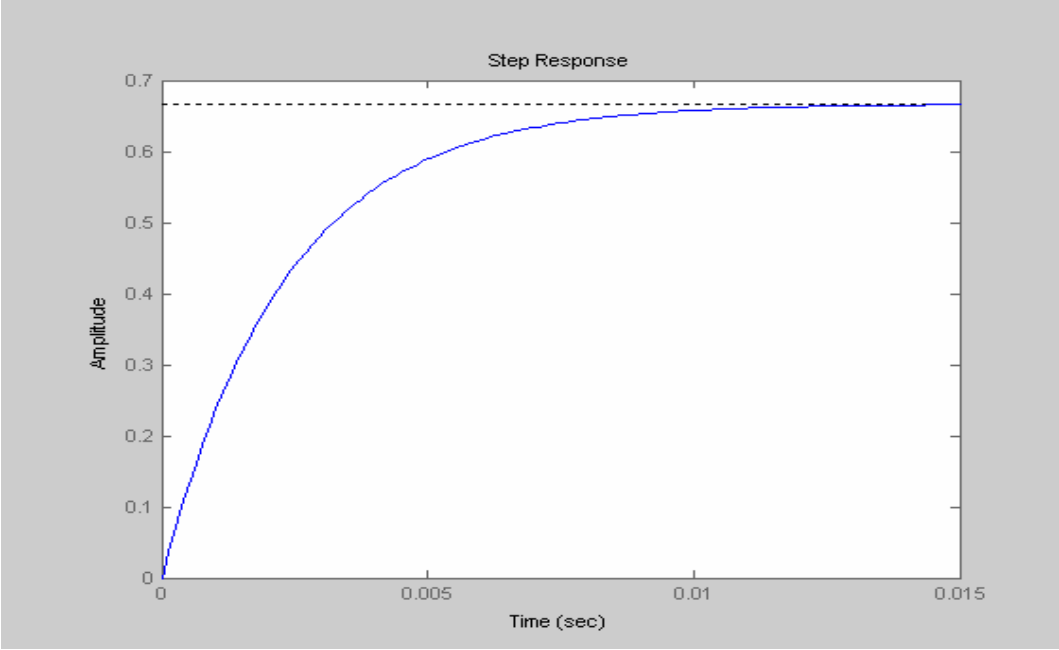


Figure 4.7. Step Response of Fig.4.6.

```
>> bode(mySys)
```

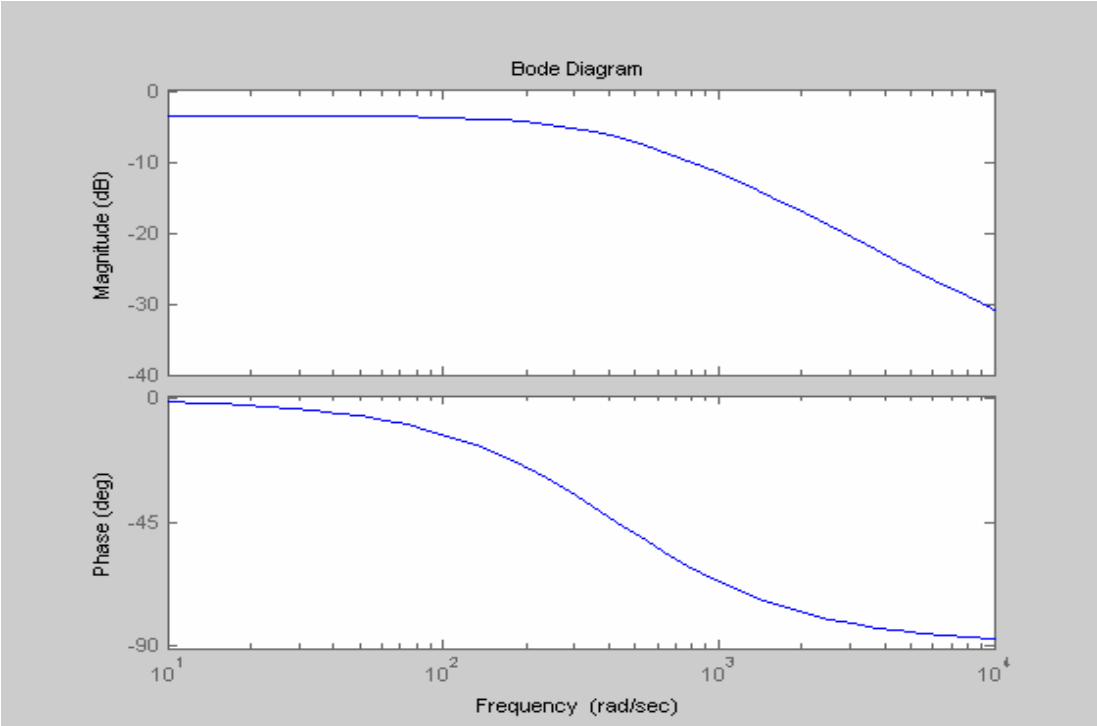


Figure 4.8. Bode Diagram of Fig.4.6.

Example 2 :

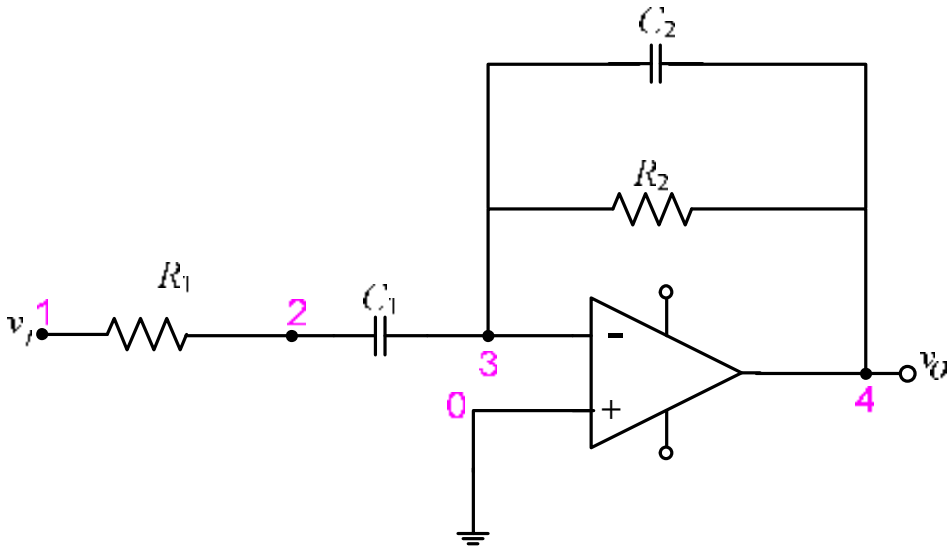


Figure 4.9. An active low pass filter circuit.

```
>> fname='lpf.txt'
fname =  lpf.txt
>> ahu
```

Netlist of an active low pass filter given below:

```
V1 1 0
R1 1 2
C1 2 3
C2 3 4
R2 3 4
Opamp 0 3 4
```

Solved variables:

```
[  v_1]
[  v_2]
[  v_3]
[  v_4]
[ I_V1]
[  I_Opamp]
```

```
>> pretty(v_4/v_1)
```

Transfer Function :

$$-\frac{s\,C1\,R2}{(1 + s\,C1\,R1)\,(s\,C2\,R2 + 1)}$$

Example 3:

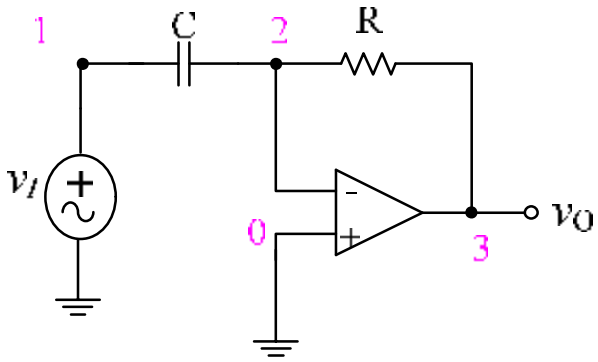


Figure 4.10. Differentiator Circuit.

```
>> fname='diff.txt'
fname =  diff.txt

>> ahu
```

Netlist :

```
    V1 1 0
    C 2 1
    R 3 2
    O 0 2 3
```

Solved variables:

```
[  v_1]
[  v_2]
[  v_3]
[ I_V1]
[  I_O]

 >> pretty(v_3/v_1)

Transfer Function :                -s C R
```

Example 4 :

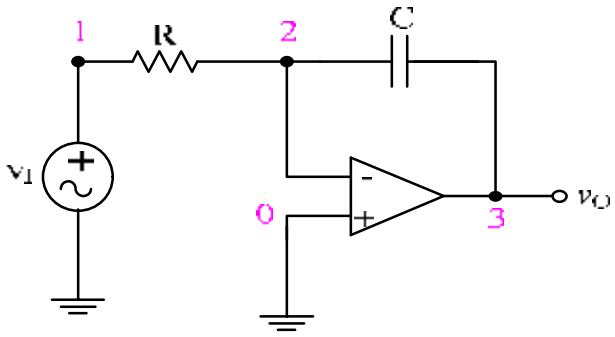


Figure 4.11. Integrator Circuit Simulation.

```
>> fname='int.txt'
fname =  int.txt

>> ahu
```

Netlist :

```
V1 1 0
R 2 1
C 3 2
O 0 2 3
```

Solved variables:

```
[ v_1]
[ v_2]
[ v_3]
[ I_V1]
[ I_O]

>> pretty(v_3/v_1)
```

Transfer Function :

$$\frac{1}{R\,s\,C}$$

```
>> pretty(A)
```

Admittance Matrix of Integrator Circuit in Fig.4.10:

```
[ 1/R      - 1/R          0       1       0]
[                                           ]
[- 1/R     s C + 1/R      -s C    0       0]
[                                           ]
[  0       -s C           s C     0       1]
[                                           ]
[  1       0              0       0       0]
[                                           ]
[  0       -1             0       0       0]
```

5. RESULTS AND CONCLUSION

The goal of this thesis has been to develop a symbolic simulation program for analog circuits. A software package has been written in MATLAB because of its matrix-oriented system.

The Matlab-based program focused on the formulation and reduction of the system of equations of analog integrated circuits, has been described. The MATLAB/GUI models of analog circuit have been constituted. The simulator is designed for the solution of analog circuits. This simulator computes branch voltage and current at each node of the given circuit as symbolic function of the circuit parameters in the frequency *s* domain.

A netlist description of the circuit to be simulated has been written like a txt.file format and its symbolic transfer function, voltage gain, input impedance and two-port parameters have been obtained using this simulation program. Analytical formulas for transfer function of the given circuit have been derived which were obtained by a straightforward application of symbolic techniques without any specific knowledge of the circuit.

The main advantage of symbolic analysis and symbolic simulators is a powerful and time-saving tool for gaining insight in analog circuit behavior. The use of a symbolic simulations is an important complement to traditional numerical simulation. Symbolic simulators is an important component in the process of automating analog circuit design. Several applications depend on the use of symbolic circuit expressions.

Computer-aided circuit analysis and systematic methods are for solving analog circuit problems. This thesis presented the implementation of analog behavioral models within the *Matlab* and showed the various modeling capabilities. It has been shown that by using nodal analysis the procedure for writing symbolic network functions for connected, linear network modeled with RLC elements, VCCS, CCVS and ideal op amps has been significantly simplified. It has been described matrix form of circuit models and illustrated their applications.

The simulation program is presented for the symbolic analysis of analog integrated circuits and generates symbolic expressions for the circuits in s-domain. This yields analytic formulas for transfer functions and impedances. In addition, the expressions can be simplified with a heuristic judgment based on the magnitude of the elements. This yields simple and interpretable formulas, which provide analog designers with insight into the circuit behavior.

In the future, the simulation program will be improved to further reduce the analysis time for large circuits. It will be designed as circuit schematic simulation program. It is possible to model as subcircuits and to assign them schematic symbols.

6. REFERENCES

ATTIA J.O.; 1999, Electronics and Circuits Analysis Using MATLAB, CRC Press LLC.

BALABANIAN N., 1958. Network Synthesis. Prentice-Hall, N.J, 433p.

HASSOUN MARWAN M., LIN P.; April 1995, A Hierarchical Network Approach to Symbolic Analysis of Large=Scale Networks, Volume: 42, pp.201-211.

FRANCO S., 2002, Design With Operational Amplifiers and Analog Integrated Circuits. Mc Graw-HILL, New York, 658p.

HUELSMAN L. P., 1998, Basic Circuit Theory. PRENTICE HALL, N.J, 756p

KENNTH R.L.; WILLY M.C. S., 1994, Desing of Analog Integrated Circuits and Systems. Mc Graw-HILL, New York, 898p.

SOMMER R., HENNIG E., THOLE M., HALFMANN T., WICHMANN T.; 1999, Symbolic Modeling and Analysis of Analog Integrated Circuits, EECTD'99, pp.66-69.

TAN X .- D., SHI C.-J. ; Apr. 2000, Hierarchical Symbolic Analysis of Analog Integrated Circuits via Determinant Decision Diagrams, IEEE Transactions on, Volume: 19, pp.401-412.

WAMBACQ P., DOBROVOLNY P., GIELEN G.G.E., SANSEN W., FELLOW.; Oct. 1998, Symbolic Analysis of Large Analog Circuits Using a Sensitivity-Driven Enumeration of Common Spanning Trees, IEEE Transactions on, Volume: 45, pp. 1342-1350.

WEDEPOHL L.M., JACKSON L.; June, 2000, Modified Nodal Analysis: as essential addition to electric circuit theory and analysis, ESEJ pp.84-92.

YORKE R., 1986, Electric Circuit Theory.Tergamon Press ,Oxford , 393p.

www.mathworks.com

www.allaboutcircuits.com

7. RESUME

Ahu Akçam was born in Niğde, Turkey in 1974. She received B.Sc. degree in Electrical - Electronics Engineering Department from Cukurova University, Adana in 1998. She is working as Electrical Distribution at a company is called TEDAS in Adana about 6 years. She has been studying for MS degree in Electrical - Electronics Engineering Department of Çukurova University, Adana since 2003. She interested in Electrical Circuit.