ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

MSc THESIS

Arzu İŞLER

SYMBOLIC ANALYSIS METHODS FOR SWITCHED CAPACITOR NETWORKS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ADANA, 2010

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We certified that the thesis titled above was reviewed and approved for the award of degree of the Master of Science by the board of jury on 05 /05 /2010.

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ABSTRACT

MSc THESIS

SYMBOLIC ANALYSIS METHODS FOR SWITCHED CAPACITOR NETWORKS

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Supervisor :Asst.Prof.Dr. Murat AKSOY
Year:2010, Pages : 59
Jury :Asst.Prof.Dr. Murat AKSOY
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Symbolic analysis at the circuit level is a formal technique to calculate the behavior or a characteristic of a circuit with the independent variable (time or frequency), the dependent variables (voltages and currents), and (some or all of) the circuit elements represented by symbols.

In this study, we consider the problem of generating simple yet accurate symbolic representation of Switched Capacitor (SC) circuit transfer function and characteristics in terms of circuit parameters for linear(ized) analog integrated circuits. Symbolic modeling and analysis of analog integrated SC circuits are simulated in MATLAB.

Key Words : switched capacitor, symbolic analyses, Matlab

ÖZ

YÜKSEK LİSANS TEZİ

ANAHTARLAMALI KAPASİTÖR DEVRELERİNİN SEMBOLİK ANALİZ METODLARI

Arzu İŞLER

ÇUKUROVA ÜNİVERSİTESİ
FEN BİLİMLERİ ENSTİTÜSÜ
ELEKTRİK-ELEKTRONİK MÜHENDİSLİĞİ ANA BİLİM DALI

Danışman :Yrd.Doç.Dr. Murat AKSOY
Yıl:2010, Sayfa : 59
Jüri :Yrd.Doç.Dr. Murat AKSOY
:Doç.Dr. Turgut İKİZ
:Yrd.Doç.Dr. Mutlu AVCI

Sembolik analiz, bir elektronik devrenin davranışını veya karakteristiğini, bağımsız değişkenler (zaman ve frekans), bağımlı değişkenler (voltaj ve akım) ve devre elemanlarının bazıları veya hepsi ile birlikte ortaya koyan biçimsel bir tekniktir.

Bu tezde, anahtarlamalı kapasitör devrelerinin basit ve geçerli transfer fonksiyonunun ve karakteristiğinin, devre parametreleri açısından oluşturulması amaçlanmıştır. Anahtarlamalı kapasitör devrelerinin sembolik modellenmesi ve analizi MATLAB da benzetimi (simülasyonu) elde edilmiştir.

Anahtar Kelimeler : Sembolik Analiz, Matlab, Anahtarlamalı Kapasitör

ACKNOWLEDGEMENTS

This thesis would not have been possible without the essential and gracious support of my supervisor Assist.Prof.Dr. Murat AKSOY.

I would like to thank my husband also my colleague Erkan İŞLER for his interest and endless encouragement.

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1. INTRODUCTION

1.1. Symbolic Analysis Overview

Symbolic analysis of electronic circuits received much attention during the late 1960s and the 1970s, where a lot of computer-oriented analysis techniques were proposed. Since the late 1980s, symbolic analysis of electronic circuits has gained a renewed and growing interest in the electronic design community (Gielen, Walscharts and Sansen, 1989).

Basically, symbolic analysis calculates the behavior or the characteristics of a circuit in terms of symbolic parameters.

The use of symbolic analysis methods provides considerable insight and flexibility in the design process. It provides a computational tool which allows quickly evaluate different circuit configurations and determine their general suitability for specific design applications.

Symbolic analysis has brought up new issues and opportunities in the electronic circuit design. The nature of the results of this analysis helps the designer to a great extent to get a qualitative insight into the behavior of the circuits under design. The most important advantages of symbolic analysis are based on a number of post processing procedures. These procedures are, e.g. network parameters valuation, sensitivity analysis, evaluation of tolerance, zeros and poles extraction, etc. (Fleischer and Laker,1979).

Symbolic expressions relating the behavior of a system or circuit to its building block characteristics (e.g., design parameters) are useful for several reasons (Hokenek and Moschytz, 1980). First of all, they offer the designer explicit relations that provide insight into the system's overall behavior and characteristics. They can also be used to make decisions about building block and component parameters. Secondly, they provide parameterized, behavioral models which can be used in simulations at higher levels of abstraction or for purposes of synthesis. The fact that these models are symbolic avoids the necessity to recompute them each time a new set of parameter values is introduced (Vanassche, Gielen and Sansen, 2002). This is

This is, for example, useful in performing tradeoff analyses or in circuit optimizations.

A symbolic expression, describing main function, is often required for design any electronic circuit. The symbolic expression contains useful information for optimization of a circuit.

Symbolic analysis is to calculate the behavior or the characteristic of a circuit in terms of symbolic parameters. It offers many advantages than numerical simulation in many applications such as optimum topology selection, design space exploration, behavioral model generation, and fault detection.

In recent years, symbolic network analysis of linearized analog integrated circuits has been a major topic of research. The driving force behind this research is that symbolic analysis can improve the insight into the behavior of analog circuits, and therefore can accelerate the design process of these circuits (Vanassche, Gielen and Sansen, 2002).

The application fields of symbolic analysis techniques (in a close connection with numerical methods) can be divided into the following four main categories, which are essential tasks in the industrial design flow of analog integrated circuits (Sommer, Hennig, Thole, Halfmann and Wichmann,1999):

a. Circuit analysis:
   - determine the influences of element parameters on circuit behavior
   - extraction of dominant circuit behavior in a mathematical and interpretable form (also to be used for circuit sizing)
   - error and tolerance analysis

b. Circuit modeling:
   - support of model generation for analog circuit blocks (on different hierarchical levels)
   - allow for overall circuit simulation by use of behavioral and macro-models

c. Circuit sizing:
   - support manual or computer-aided circuit synthesis
   - derivation of symbolic (generic) sizing formulas for circuit elements as

functions of global circuit specifications

d. Circuit optimization:

- preprocessing of equations by e.g. elimination of variables to allow for an efficient optimization run
- allow for application of optimization algorithms already on system level

Symbolic analysis is a complement to numerical simulation in the design and evaluation of integrated circuits. It provides insight into circuit behaviour that numerical analysis does not. It calculates the behaviour or characteristics of a circuit with the independent variable (time or frequency), the dependent variables (voltages and currents), and some (or all) of the circuit elements being represented by symbols (Sansen, Gielen and Walscharts, 1989).

Symbolic analysis is now a well established technique for use in the design of electronic networks. Network function in symbolic form are the starting point for tolerance analysis, optimization and the calculation of component values.

1.2. Switched Capacitor (SC) Circuits

Fabrication of low frequency active networks arouses the importance of the network size. Heavy and bulky network elements were replaced by small elements like small transistor, capacitors and resistors. In the design of the networks, it is now possible to use thousands of capacitors and transistors but it is not proper to use resistors on chips as well.

During the design, simulation and integration process of the analog networks, it was recognized that the switched capacitor behavior in the network is similar to resistor's behavior. It was then possible to use switched capacitors instead of resistors. In the new technology switched capacitors networks are consist of CMOS transistors and capacitors only. CMOS transistors simply act as switches.

The implementation of switched capacitors in CMOS technology occurred in early 1970's and represented a major step in implementing practical analog circuits and systems in an integrated circuit technology (Allen and Sánchez, 1984).

Advantages of Switched Capacitor Circuits

1- Compatibility with CMOS technology
2- Good accuracy of time constants
3- Good voltage linearity
4- Good temperature characteristics

Disadvantages of Switched Capacitor Circuits

1- Experience clock feed through
2- Require a nonoverlapping clock
3- Bandwidth of the signal must be less than the clock frequency

Switched capacitor circuits have become extremely popular in recent years. The reasons for this are they are fully integratable using MOS technology, and they possess important and useful characteristics such as small size, low power consumption, ease of manufacturing, etc., which are essential in various applications. As the state of the art progresses, it becomes increasingly clear that more detailed analysis to understand the behavior of such circuits is necessary, and algorithms to aid the design of very large-scale circuits using computers need to be developed. A typical process of analyzing a switched-capacitor circuit is illustrated in Figure 1.1. An MOS switched-capacitor circuit consists of periodically operated switches, capacitors, and Op-Amps. These components may be considered ideal or nonideal depending on the physical realization or the purpose of investigation (Liou, Kuo and Clement, 1983).

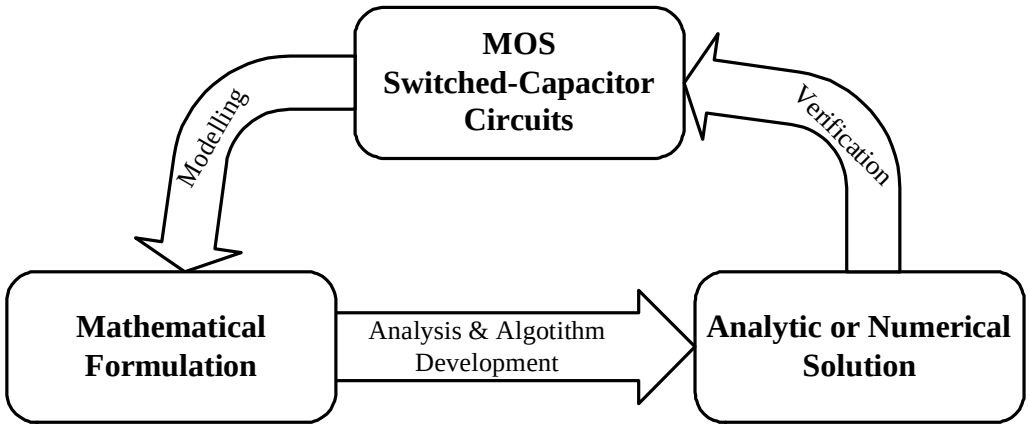


Figure 1.1. A typical process of switched-capacitor circuit analysis

Any passive SC network can be constructed with the six basic building blocks shown in Figure 1.2. The nonswitched shunt capacitor and its dual are the only storage elements in SC networks. Periodically switched capacitors act like resistors, since their memory is destroyed during the closing period of the switch. The ideal switches can be considered as zero-valued capacitors with a switch in parallel. By connecting parallel, serial, and tandem connections of the building blocks in Figure 1.2 , higher order passive SC networks can be obtained.

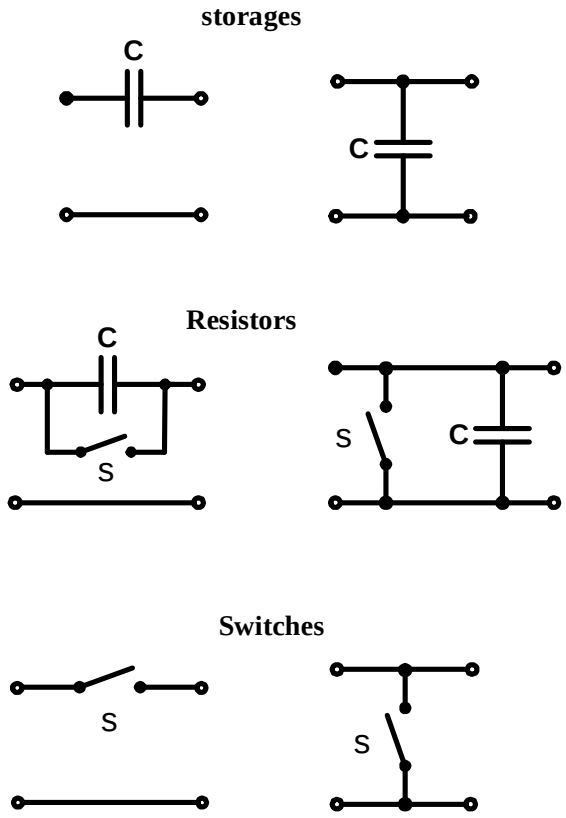


Figure 1.2. The six basic components (building blocks) in SC networks.

1.3. Simulation of Resistors with Switched Capacitors

SC networks are based on the idea of rapidly switching the flow of the current. To explain the principle, look at the Figure 1.3. Switch 1 represents a short circuit

during the first clock period. Switch 2 is short circuit during the second period. We note that two phases are nonoverlapping and that ideally only one switches is closed at any instant of time.

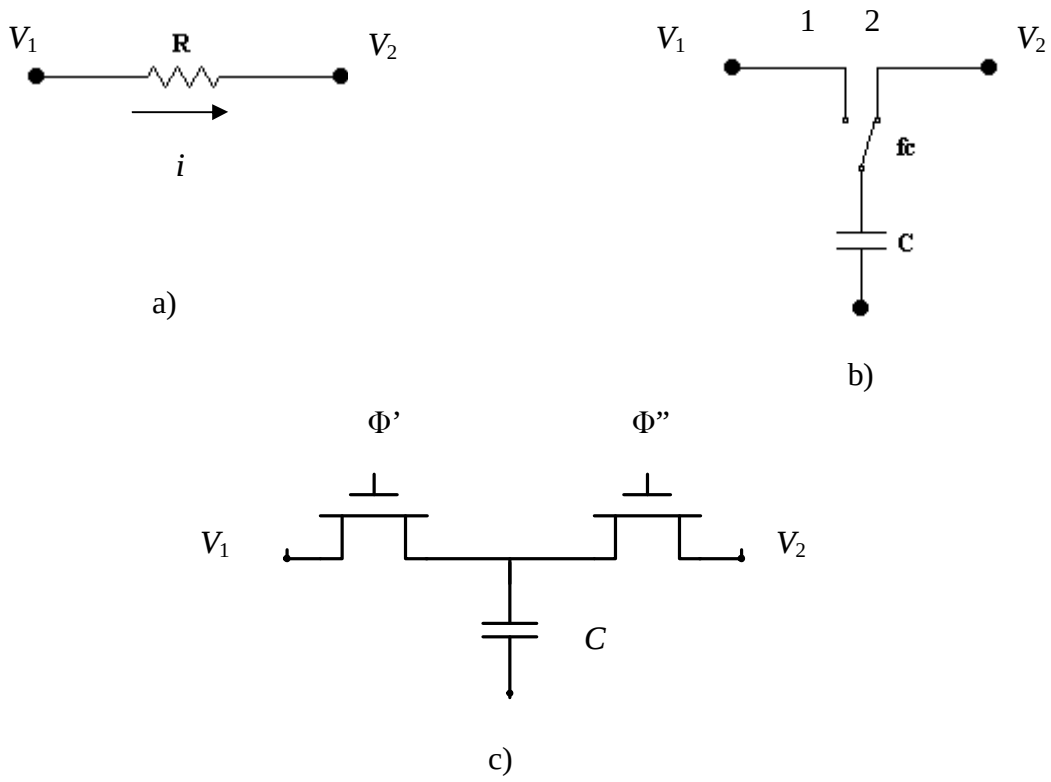


Figure 1.3. (a) A resistor symbol (b) SC simulation of R
(c) SC simulation of R by MOS

Assume that $V_1 > V_2$ in Figure 1.3. When switch 1 closes, voltage V_1 will appear immediately across the capacitor, which will be charge to $Q_1 = CV_1$. In the second phase, with switch 1 open and switch 2 close, the capacitor will immediately lower its voltage to V_2 and the charge on it will be $Q_2 = CV_2$. This will cause charge transfer (charge pump).

The difference of the charges is the net flow of the charge is given by

$$\Delta Q = Q_1 - Q_2 = C(V_1 - V_2) \tag{1.1}$$

The average current flowing over one period will be

$$I_{av} = \frac{\Delta Q}{T_c} = \frac{C}{T_c}(V_1 - V_2) = G(V_1 - V_2). \tag{1.2}$$

where G is replaced by C/T.

The size of an equivalent resistor that yields the same value of current is then

$$R = \frac{(V_1 - V_2)}{i} \cong \frac{T_c}{C} = \frac{1}{Cf_c} \tag{1.3}$$

A simple explanation for the function of an SC is obtained by previous equations.

The value of this resistor decreases with increasing switching frequency or increasing capacitance, as either will increase the amount of charge transferred from V_2 to V_1 in a given time.

For this approximation to be valid, it is necessary that switching frequency f_c be much larger than the frequencies of V_1 and V_2

This, however, is only valid under the assumption that V_1 and V_2 are not affected by the switch closures.

Practically to achieve full integration in silicon chips, MOS (metal oxide semiconductor) may be used in the switched capacitor circuits. MOS technology has the ability to store signal carrying charges at a node for a relatively long period of time, to move the charge between different nodes (under the control of digital clock).

Besides being very accurate, the SC circuit's characteristic can be controlled by a precision digital clock. In addition, absolute capacitance values can be sufficiently reduced while maintaining the same capacitance ratios, resulting in circuits that consume small chip area.

1.4. Overview of The Thesis

This thesis represents symbolic analysis methods of Switched-Capacitor (SC) Networks. This is to be achieved through showing how the switched-capacitor concept can be used as a major step in implementing practical analog circuits and systems in an integrated circuit technology. Switched-Capacitor networks will be constituted and transfer functions of these circuit models will be obtained by a MATLAB simulation. Modified Nodal Analyses (MNA) which is one of the Switched-Capacitor network analysis methods will be used as this simulation core. This will broaden the view of both designer of the networks and electronics technology and engineering undergraduate student (Sanches and Tlelo-Cuautle, 2005) and (Uday and Ajay Bakshi, 2008)

This thesis can be divided into five parts. Chapter 1 is the first part, which presents in detail Symbolic Analysis Background, Switched Capacitor (SC) Circuits, advantages and disadvantages and simulation of resistors with Switched Capacitors. In this chapter also a common used model of SC integrator is examined. In the Chapter 2, general rules of the network analyses and synthesis are given. Especially, the attention is attracted to analysis of circuits with capacitors. This two chapter yields us to the third part Chapter 3, analysis of switched capacitor networks. Behavior of switched capacitor networks is examined firstly by going through the properties of SC networks in the time domain. By Chapter 4, symbolic modeling and analysis of analog integrated SC circuits, is pointing that symbolic analysis provides additional insight into the behavior of SC networks by giving the transfer function. At the end, by several examples using MATLAB, implementation of SC analog behavioral models are presented.

2. NETWORK ANALYSIS

The network analysis means to find a current through or voltage across any branch of the network by using fundamental rules and various simplification techniques.

Electronic devices are described by their nonlinear terminal voltage-current characteristics. Circuits containing electronic devices are analyzed and designed either by utilizing graphs of experimentally measured characteristics or by linearizing the voltage-current characteristics of the devices. The linearized equation set describes the circuit in terms of its interconnected passive elements and independent or controlled voltage and current sources.

2.1. Basic Network Elements

There are there basic linear passive elements; resistance, inductance and capacitance.

The time-stationary (or constant-value) elements of Fig. 2.1. to 2.3 (the resistor, inductor, and capacitor, respectively) are called passive elements, since none of them can continuously supply energy to a circuit. For voltage v and current i, we have the following relationships:

For the resistor, as shown in Fig. 2.1(a),

$$v = Ri \qquad \text{or} \qquad i = Gv \tag{2.1}$$

where R is its resistance in ohms (Ω), Equation (2.1) is known as Ohm's law.

For the inductor as shown in Fig. 2.1(b),

$$v = L\frac{di}{dt} \quad \text{or} \quad i = \frac{1}{L}\int_{-\infty}^{t} v\,dt \tag{2.2}$$

where L is its inductance in henrys (H).

For the capacitor, as shown in Fig. 2.1(c),

$$v = \frac{1}{C}\int_{-\infty}^{t} i\,dt \quad \text{or} \quad i = C\frac{dv}{dt} \tag{2.3}$$

where C is its capacitance in farads (F). If R, L, and C are independent of voltage and current (as well as of time), these elements are said to be linear: Multiplication of the current through each by a constant will result in the multiplication of its terminal voltage by that same constant.

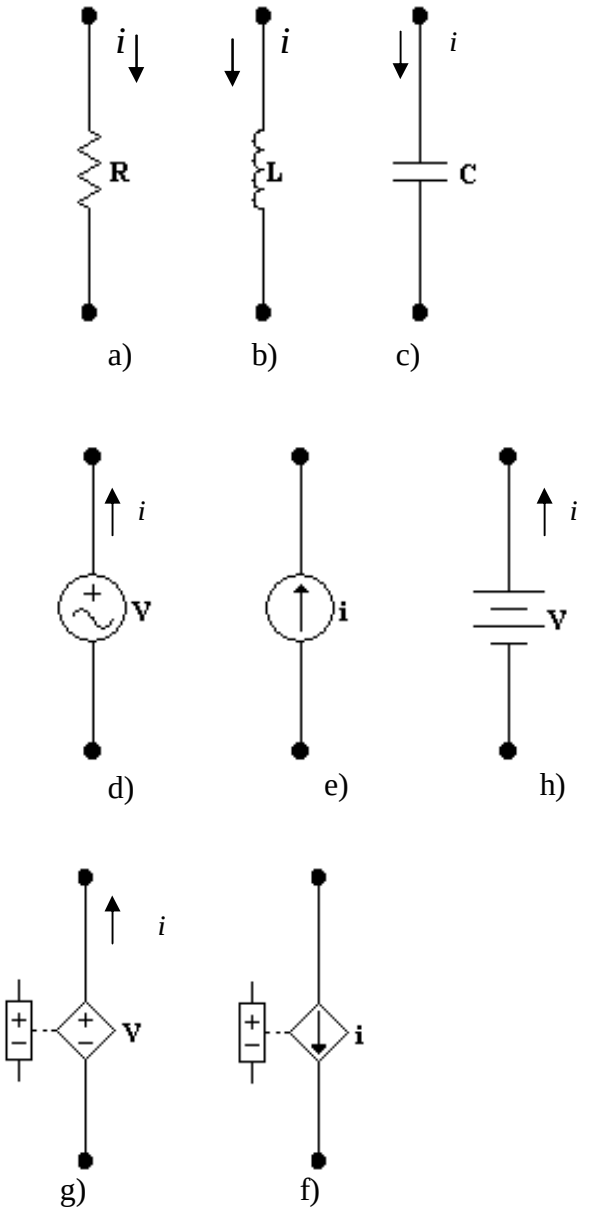


Figure 2.1. Network elements

The elements of Fig.2.1. (d) to (h) are called active elements because each is capable of continuously supplying energy to a network. The ideal voltage source in Fig. 2.1(d) provides a terminal voltage *v* that is independent of the current *i* through it. The ideal current source in Fig.2.1.(e) provides a current *i* that is independent of the voltage across its terminals. However, the controlled (or dependent) voltage source in Fig. 2.1.(f) has a terminal voltage that depends upon the voltage across or current through some other element of the network. Similarly, the controlled (or dependent) current source in Fig. 2.1.(g) provides a current whose magnitude depends on either the voltage across or current through some other element of the network. If the dependency relation for the voltage or current of a controlled source is of the first degree, then the source is called a linear controlled (or dependent) source. The battery or dc voltage source in Fig. 2.1.(h) is a special kind of independent voltage source.

2.2. Circuit Analysis Basics

- **Kirchhoff's Laws:**

These laws help to determine the current in any part of an electrical network for any given applied voltage. These laws are the basic tools of the network analysis.

a. **KCL** (Kirchhoff's Current Law)

In any network the algebraic sum of currents meeting at a point (or node) is always zero. That means the total current leaving a junction is equal to the total current entering that junction.

$$\sum I_{(node)} = 0 \tag{2.4}$$

This law is very helpful to carry out Nodal analysis of a network

b. **KVL** (Kirchhoff's Voltage Law)

In any network, the algebraic sum of all branch voltages around any closed path or closed loop is always zero. This law is very useful in loop analysis of the network.

$$\sum V_{loop} = 0 \tag{2.5}$$

2.3. Circuit Analysis Methods

- **Nodal Analysis**

This method is mainly based on Kirchhoff's Current Law. This method uses the analysis of different nodes of the network. One of the nodes assumed as a reference node whose potential is assumed to be zero. At other nodes the different voltages are to be measured with respect to the reference mode. The equations are to be written for all other nodes by applying KCL. The advantage of this method lies in the fact that we get (n-1) equations when there are n nodes, thus reduces the calculation work.

1. Choose a reference node ("ground")

2. Define unknown voltages (those not fixed by voltage sources)

3. Write KCL at each unknown node, expressing current in terms of node voltages

4. Solve the set of independent equations (N eqn's for N unknown node voltages)

An example for Nodal Analyses is as follows:

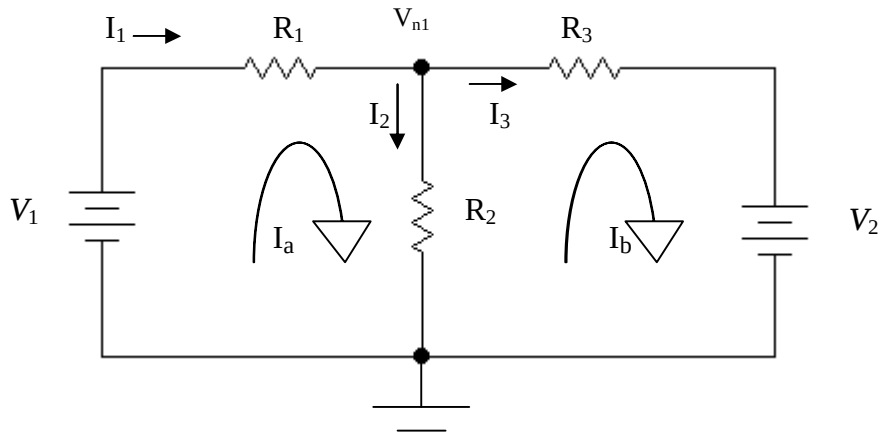


Figure 2.2. A resistive circuit with node voltages and currents

At node 1:

$$I_1 - I_2 - I_3 = 0 \tag{2.6}$$

$$\left[\frac{V_{n1} - V_1}{R_1}\right] - \left[\frac{V_{n1}}{R_2}\right] - \left[\frac{V_2 - V_{n1}}{R_3}\right] = 0 \tag{2.7}$$

$$\left[\frac{V_{n1}}{R_1}\right] - \left[\frac{V_{n1}}{R_2}\right] - \left[\frac{(V_2 - V_{n1})}{R_3}\right] = \frac{V_1}{R_1}$$

- **Loop or Mesh Analysis**

Loop analysis is a method for obtaining loop currents. The technique uses Kirchoff voltage law (KVL) to write a set of independent simultaneous equations. The Kirchoff voltage law states that the algebraic sum of all the voltages around any closed path in a circuit equals zero. The advantage of this method is that for complex networks the number of unknowns reduces which greatly simplifies calculation work.

In loop analysis, the unknowns are the loop currents. Mesh analysis means that we choose loops that have no loops inside them.

Consider again the network shown in Figure 2.2. There are two loops, so assuming two loop currents as I_1 and I_2. While assuming the loop currents, consider the loops such that each element of the network will be included at least once in any of the loops.

Loop Analysis Procedure:

a. Label each of the loop/mesh currents.

b.. Apply KVL to loops/meshes to form equations with current variables.

a. For N independent loops, we may write N total equations using KVL around each loop. Loop currents are those currents flowing in a loop; they are used to define branch currents.

b. Current sources provide constraint equations.

Loop1:

$$I_a R_1 + R_3(I_a - I_b) - V_1 = 0 \tag{2.9}$$

$$I_a(R_1 + R_3) - I_b R_3 = V_1 \tag{2.10}$$

Loop2:

$$R_3(I_b - I_a) + R_2 I_2 - V_2 = 0 \tag{2.11}$$

$$-I_a R_3 + I_b(R_2 + R_3) = V_2 \tag{2.12}$$

The matrix form of Equation (2.10) and (2.12) is as follows:

$$\begin{bmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{bmatrix} \begin{bmatrix} I_a \\ I_b \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.13}$$

2.4. Laplace Transform Analysis Directly from the Circuit Diagram

The solution of most electrical problems can be reduced ultimately to the solution of differential equations and the use of Laplace transforms provides an alternative method to those used previously. Laplace transforms provide a convenient method for the calculation of the complete response of a circuit.

The Laplace transform of the Resistor Equation is:

$$V(s) = RI(s) \tag{2.14}$$

It is important that $V(s)$ merely means that it is the Laplace transform of v and $I(s)$ is the Laplace transform of i. Whenever the Laplace transform of the functions is taken it is referred to as 's-domain' as opposed to the time domain.

If an inductor has no initial current, $i = 0$ at time $t = 0$ the normal equation is $v = L(di/dt)$ where L is the inductance.

The Laplace transform of the Inductor Equation is:

$$Z(s) = \frac{V(s)}{I(s)} = sL \tag{2.15}$$

If the capacitor has no initial voltage, $v = 0$ at time $t = 0$ the normal equation is $i = C(dv/dt)$

The Laplace transform of the Inductor Equation is:

$$Z(s) = \frac{V(s)}{I(s)} = \frac{V(s)}{sCV(s)} = \frac{1}{sC} \tag{2.16}$$

Summarizing, in the time domain, the circuit elements are R, L and C and in the s-domain, the circuit elements are R, sL and $(1/sC)$.

3. ANALYSIS OF SWITCHED CAPACITOR NETWORKS

The full frequency behavior of switched capacitor networks can in general be obtained by solving a set of linear equations obtained by analysis methods that will be analyzed in this chapter.

3.1. Properties of SC Networks in the Time Domain

The network in Fig 3.1. consists of a toggle switch and three capacitors. If the switches are placed between capacitors, the topology of the network is being changed every τ seconds and at the same time charge is being instantaneously exchanged between capacitors.

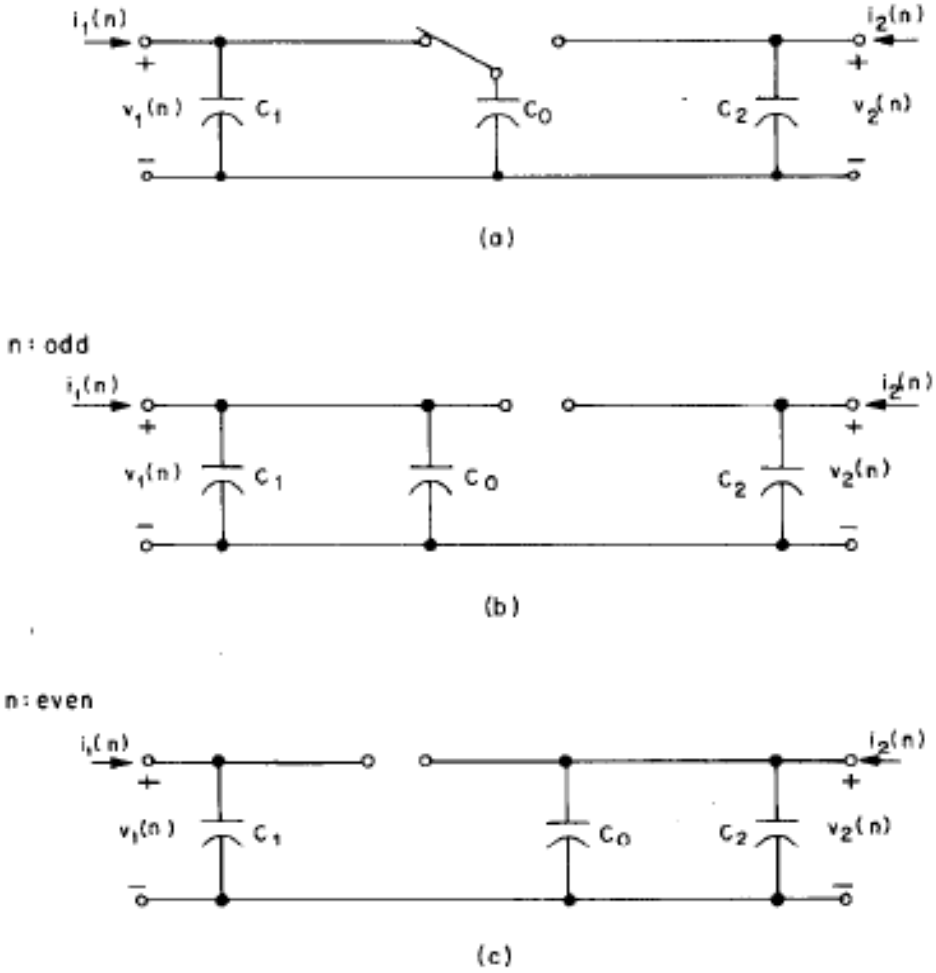


Figure 3.1. SC with two-port

The general charge equations for an SC network will have time-variant coefficients and the general matrix equation will have the form

$$i(n) = [C(n)] \times v(n) - [C(n-1)] \times v(n-1) \tag{3.1}$$

Assuming that at odd times of n, the switch is on the left, one obtains the network shown in Fig. 3.1 (b). Applying the charge equations to the network in this state results in the matrix equation

$$\begin{bmatrix} i_1(n) \\ i_2(n) \end{bmatrix} = \begin{bmatrix} (C_1 + C_0) & 0 \\ 0 & C_2 \end{bmatrix} \times \begin{bmatrix} v_1(n) \\ v_2(n) \end{bmatrix} - \begin{bmatrix} C_1 & C_0 \\ 0 & C_2 \end{bmatrix} \times \begin{bmatrix} v_1(n-1) \\ v_2(n-1) \end{bmatrix} \tag{3.2}$$

Similarly, for even times n, the network has the topology shown in Figure 3.1 (c) and the charge equations become

$$\begin{bmatrix} i_1(n) \\ i_2(n) \end{bmatrix} = \begin{bmatrix} C_1 & 0 \\ 0 & (C_2 + C_0) \end{bmatrix} \times \begin{bmatrix} v_1(n) \\ v_2(n) \end{bmatrix} - \begin{bmatrix} C_1 & 0 \\ C_0 & C_2 \end{bmatrix} \times \begin{bmatrix} v_1(n-1) \\ v_2(n-1) \end{bmatrix} \tag{3.3}$$

Depending on which time n is considered, Equation (3.3) will have different elements in its matrices. Our objective is now to combine equations of the kind given by (3.2) and (3.3) into one, such that it will be valid both for even and odd n, in short, for all times n. The charge equations (3.2) and (3.3) describing Figure 3.1 differ because capacitor *C*, is connected to node 1 for odd, and to node 2 for even times. This time-variant topology can be taken into account by introducing the following two time-dependent “switching functions”

$$A^e(n) = \frac{1 + (-1)^n}{2} = \begin{pmatrix} 1 & \text{for n even} \\ 0 & \text{for n odd} \end{pmatrix} \tag{3.4}$$

$$A^0(n) = \frac{1 - (-1)^n}{2} = \begin{pmatrix} 1 & \text{for n even} \\ 0 & \text{for n odd} \end{pmatrix} \tag{3.5}$$

With these switching functions, the two Equations (3.2) and (3.3) can be combined into the form of Equation (3.1) (Kurth and Moschytz,1979),

$$\begin{bmatrix} i_1(n) \\ i_2(n) \end{bmatrix} = \begin{bmatrix} C_1 + A^0(n)C_0 & 0 \\ 0 & C_2 + A^e(n)C_0 \end{bmatrix} \times \begin{bmatrix} v_1(n) \\ v_2(n) \end{bmatrix} - \begin{bmatrix} C_1 & A^0(n)C_0 \\ A^e(n)C_0 & C_2 \end{bmatrix} \times \begin{bmatrix} v_1(n-1) \\ v_2(n-1) \end{bmatrix} \quad (3.6)$$

Equation (3.6) is the time-variant matrix equation required to describe the network of Fig. 3.1 (a). As will be seen later any SC network can be described by a matrix equation of this kind, where the time variance is expressed by the switching functions $A^{o}(n)$ and $A^{e}(n)$.

As a result, SC networks can be described using the analysis methods of sampled-data systems with timevariant coefficients, whereby a similarity exists to the nodal analysis of resistive networks.

3.2. Properties of SC Networks in the z – Domain

Symbolic analysis provides additional insight into the behavior of SC networks by giving the transfer function in terms of the variable z, other words in the z domain. Because the phases need not have equal time slots, it is necessary, in general, to generate the transfer functions from the source in any given clock phase to the output in all phases. (J.Vlach, Singhal, and M. Vlach, 1984)

Switched-capacitor networks are not discrete systems. If the signal is sampled and held before it is applied to the network, the voltages of the network are piecewise constant. The nodal charge equations are used to describe the behavior of a time-discrete network. They are based on the charge conservation principle, similar to Kirchhoff's current law, which says, the algebraic sum of charges leaving any node in any phase is zero. The indefinite nodal capacitance matrix, C_n, can be set up merely by inspection of the network

$$C_n V_n = Q \quad (3.7)$$

Let us consider a capacitor embedded in an SC network with n nodes and assume a nonoverlapping clock with two phases, Φ' and Φ'' shown in Figure 3.2.

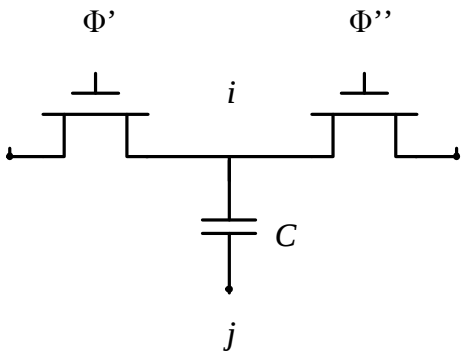


Figure 3.2. Capacitor

we need to set up one charge equation for each node in each clock phase

$$\left.\begin{aligned} C\left(v_i'-v_j'\right) - C\left(v_i''-v_j''\right)z^{-1} &= 0 \\ C\left(v_j'-v_i'\right) - C\left(v_j''-v_i''\right)z^{-1} &= 0 \end{aligned}\right\}\Phi' \qquad \left.\begin{aligned} C\left(v_i''-v_j''\right) - C\left(v_i'-v_j'\right)z^{-1} &= 0 \\ C\left(v_j''-v_i''\right) - C\left(v_j'-v_i'\right)z^{-1} &= 0 \end{aligned}\right\}\Phi'' \tag{3.8}$$

or written in matrix form

$$\begin{pmatrix} C & -C & -C/z & C/z \\ -C & C & C/z & -C/z \\ -C/z & C/z & C & -C \\ C/z & -C/z & -C & C \end{pmatrix}\begin{pmatrix} v_i' \\ v_j' \\ v_i'' \\ v_j'' \end{pmatrix} = 0 \tag{3.9}$$

As shown in the Figure 3.3 in a switched capacitor circuit, the switching operation is used to charge capacitors in one switch position and deliver the charged capacitor voltage in a different switched position.

Switched capacitor circuits have several applications. Switched capacitor filters are one of them. The other applications are Low pass filters, signal processing and communication applications, analog to digital, digital to analog converters.

A basic building block of SC circuits is switched capacitor integrator in Figure 3.3. and 3.4

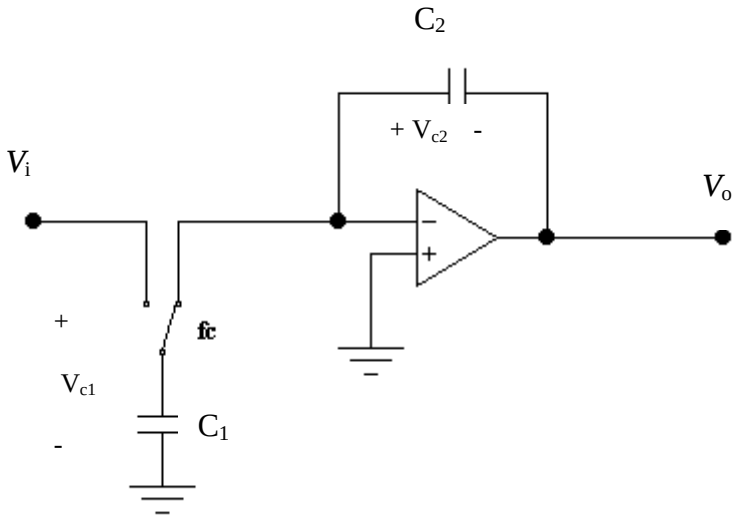


Figure 3.3. SC Integrator

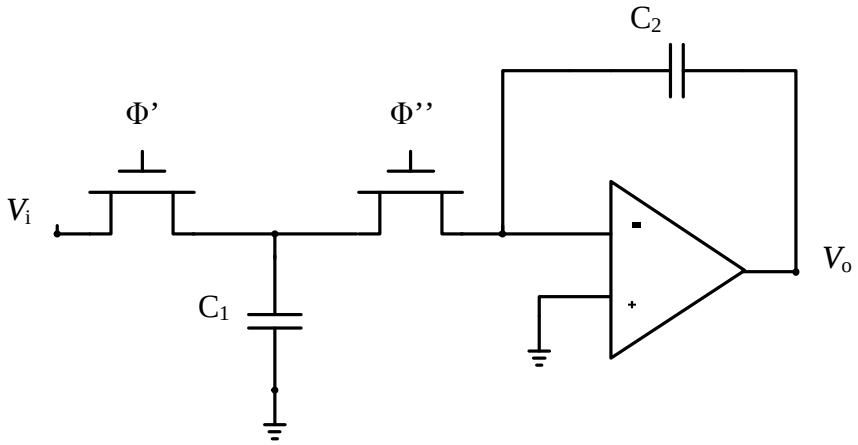
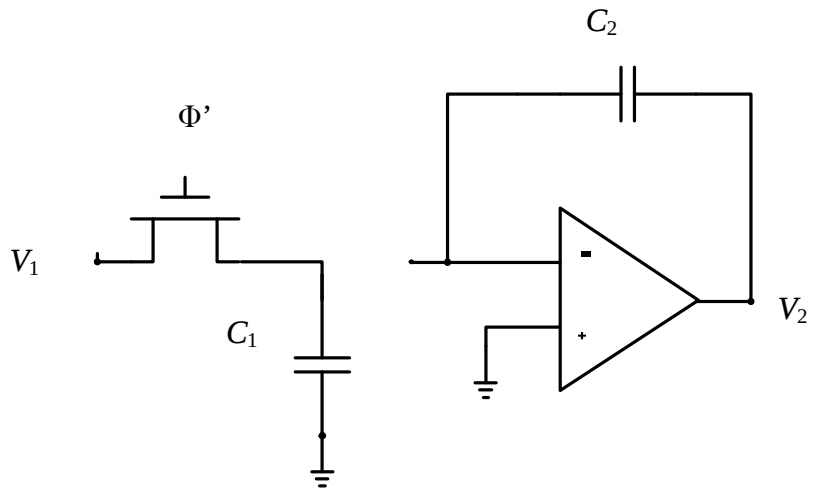


Figure 3.4. SC integrator by MOS implementation

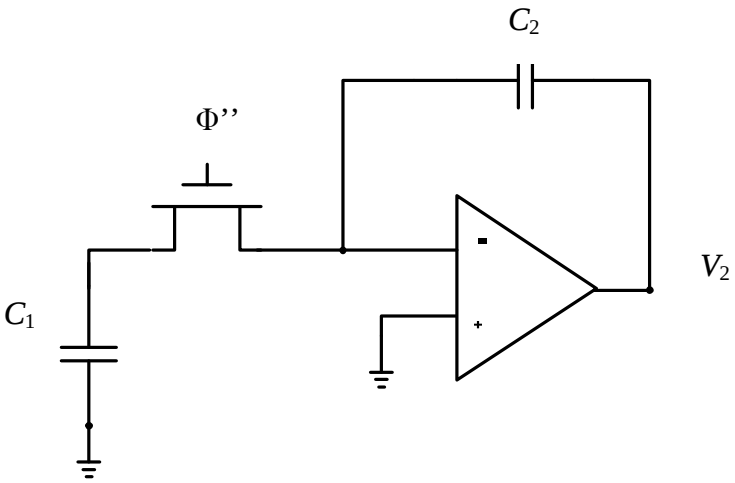
Working Principle of SC Integrator:

Φ' phase, C_1 charged to V_1



a)

Φ'' phase, charge transferred from C_1 to C_2.



b)

Figure 3.5. SC Integrator working principle

The effective resistance of a switched capacitor can be used to make an active integrator as shown in Fig.3.5 (a). Its operation is identical to an active RC integrator. In the switched-capacitor integrator, the sampled charge during one clock

phase is transferred to the integrating capacitor during another clock phase. Until the next sampling point, the integrator output has a one full sampling clock delay. Therefore, the following charge relation holds at two sampling points n and n+1.

$$V_2(n+1) = V_2(n) - \frac{C_1}{C_2} V_1(n) \tag{3.10}$$

By taking the z-transform of the equation (3.10), we can get the transfer function in the z-domain.

$$zV_2(z) = V_2(z) - \frac{C_1}{C_2} V_1(z)$$

$$\frac{V_2}{V_1}(z) = -\frac{C_1}{C_2}\frac{1}{z-1} = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} \tag{3.11}$$

The function of 1/(z-1) is called direct discrete-time integrator (DDI)

Basically the procedure for finding out the transfer function of an SC integrator is as follows:

- Write difference equation, that relates output sequence to input sequence

$$V_o(nT_s) = V_i\left[(n-1)T_s\right] - \ldots \tag{3.12}$$

- Use delay operator Z -1 to transform the recursive realization to algebraic equation in Z domain

$$V_o(Z) = Z^{-1}V_i(Z)\ldots \tag{3.13}$$

3.3. Properties of SC Networks in the Frequency - Domain

When the signals are not sampled, the z-domain solution is no longer valid, a complete frequency-domain solution needed.

Symbolic analysis is the procedure that generates the network function H(x) with respect to the complex frequency variable x as the ratio of two polynomials:

$$H(x) = \frac{N(x)}{D(x)} = \frac{f_0(p) + xf_1(p) + \ldots\ldots + x^n f_n(p)}{g_0(p) + xg_1(p) + \ldots\ldots + x^m g_m(p)} \tag{3.14}$$

The coefficients f_i, i = 0,1, . . , n and g_j , j = 0,1 . . , m of each power x are symbolic polynomial functions expressed in sum of product (SOP) format in the circuit elements p. The complex frequency variable x can be either s for continuous time or z for discrete-time circuits like SC networks.

One of the most important building blocks in a continuous-time active-RC filter is the inverting analog integrator, which is illustrated in Figure 3.6. It is assumed that all the op-amps used in this work are ideal—that is, dc-offset-free, with infinite gain and bandwidth, powered by sufficient supply voltages and so on.

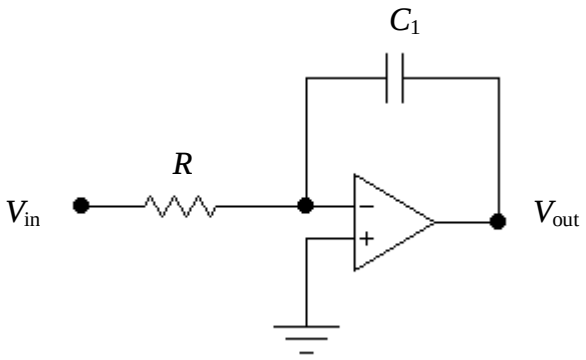


Figure 3.6. Active-RC integrator

The time-domain expression of the circuit is given by

$$V_{out}(t) = -\frac{1}{RC_1}\int_{-\infty}^{t} v_{in}(t)dt \tag{3.15}$$

Utilizing the Laplace-transform, we obtain the s-domain transfer function of the active-RC integrator as follows:

$$H(s)=\frac{V_{out}(s)}{V_{in}(s)}=-\frac{1}{sRC_1} \tag{3.16}$$

As shown in the Figure 3.7, the simplest way to realize an SC integrator is to replace the resistor *R* in the active-RC integrator with one of the SC simulations introduced in the previous section.

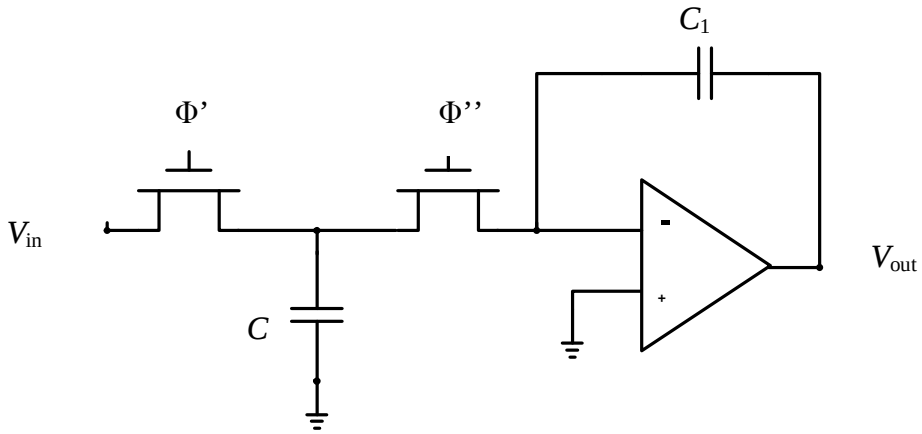


Figure 3.7. Active-SC integrator

4. INTRODUCTION OF SYMBOLIC ANALYSIS METHODS FOR SC NETWORKS

The nature of the results of symbolic analysis helps the designer to a great extent to get a qualitative insight into the behavior of the circuits under design. The most important advantages of symbolic analysis are based on a number of post processing procedures. These procedures are, e.g. network parameters valuation, sensitivity analysis, evaluation of tolerance, zeros and poles extraction, etc. Independently of these features, it has shown that symbolic analysis offers the possibility of analysis of switched-capacitor (SC) networks (Fleischer and Laker, 1979). These circuits have largely dominated analog signal processing during the last years. SC circuits ease the realization of numerous transfer functions determined by stable sampling frequency and precise capacitor ratios (Fleischer and Laker, 1979).

A great deal of importance has been given on the formulation methods for SC networks. This is because of the formulation methods represent a very important aspect of the entire analysis process.

4.1. Nodal Approach

The analysis of all-capacitor networks will first be reviewed by using the concept of nodal charge equations. After the inclusion of switches, it is demonstrated that in all cases, charge equations similar to Kirchhoff's current equations apply except that the storage properties of the capacitors must be taken into account. This leads to the description of SC networks as time-variant sampled-data networks. (Kurth and Moschytz, 1979)

Consider the capacitor C shown in Fig. 4.1. The incremental charge q(t) stored at any given time t can be expressed by the current i(t) and the voltage v(t), namely where v(0) represents the voltage across C at time t = 0.

$$q(t) = \int_0^t i(t)dt = C \cdot v(t) - C \cdot v(0) \tag{4.1}$$

expressed in matrix form:

$$[q(t)] = \left[\int_0^t i(t)dt\right] = [C]\cdot[v(t)] - [C]\cdot[v(0)] \tag{4.2}$$

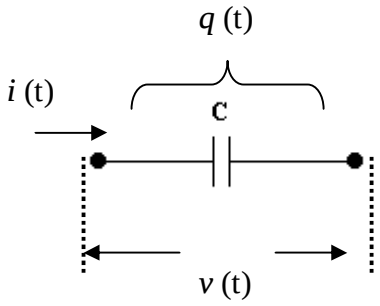


Figure 4.1. Charges and voltages on a capacitor

Note that when describing the capacitor network in terms of charges and voltages, the matrix [C] contains only real-valued time-invariant elements
The nodal charge equations become:

$$q(n) = [i(n)] = [C]\cdot[v(n)] - [C]\cdot[v(n-1)] \tag{4.3}$$

Solving for the currents *i*(n) we obtain

$$i(n) = [C]\cdot v(n) - [C]\cdot v(n-1) \tag{4.4}$$

where *i*(n) and *v*(n) are vectors.

The matrix equation (4.4) corresponds to Kirchhoff's current law as applied to an all-capacitor network with sampled input currents. These equations will be referred to as nodal charge equations.

An example for a nodal approach is as follows:

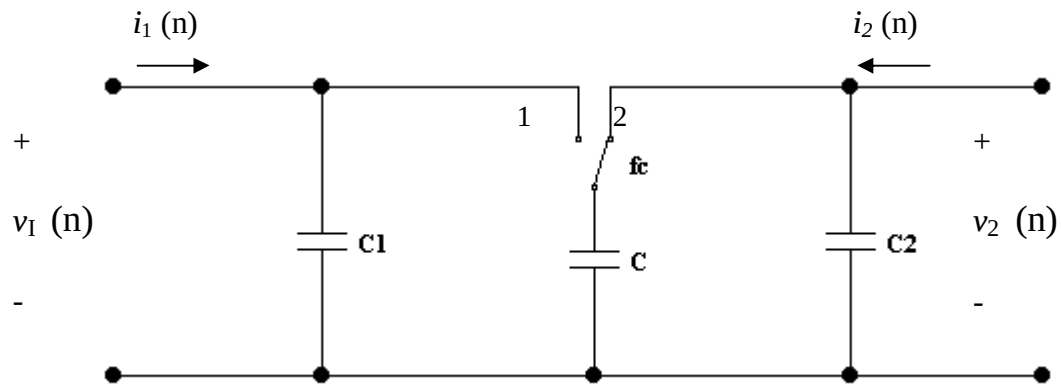


Figure 4.2. A SC network

When the Switch is in position 1 and 2, the current equations in the matrix form is given in Equation (4.5) and (4.6), respectively

$$\begin{bmatrix} i_1(n) \\ i_2(n) \end{bmatrix} = \begin{bmatrix} (C_1 + C) & 0 \\ 0 & C_2 \end{bmatrix} \cdot \begin{bmatrix} v_1(n) \\ v_2(n) \end{bmatrix} - \begin{bmatrix} C_1 & C \\ 0 & C_2 \end{bmatrix} \cdot \begin{bmatrix} v_1(n-1) \\ v_2(n-1) \end{bmatrix} \quad (4.5)$$

Switch is in position 2:

$$\begin{bmatrix} i_1(n) \\ i_2(n) \end{bmatrix} = \begin{bmatrix} C_1 & 0 \\ 0 & (C_2 + C) \end{bmatrix} \cdot \begin{bmatrix} v_1(n) \\ v_2(n) \end{bmatrix} - \begin{bmatrix} C_1 & 0 \\ C & C_2 \end{bmatrix} \cdot \begin{bmatrix} v_1(n) \\ v_2(n-1) \end{bmatrix} \quad (4.6)$$

4.2. Equivalent Circuit Approach

An equivalent circuit, by definition, is indistinguishable from its original circuit when measured from its external terminals. Because of its simplicity in circuit representation, it can often be used to as a simple approach for circuit analyses. This is especially true for the case of switched-capacitor equivalent circuits. An insight can be gained into the SC functions.

The basic concept is the development of switched-capacitor equivalent circuits is the modeling of the time-varying switched-capacitor circuits by coupled time invariant circuit models. Since the time-varying nature of the switched-capacitor circuit is caused by the periodic switching elements in the circuit, the circuit can be considered to be equivalent to having a finite number of time-invariant circuit models cycling from one to another. The initial condition of each model is determined by the state of the previous model. This finite number of models corresponds to the number of switching phases of the circuit (Liou, Kuo and Clement,1983).

In the frequency-domain, switched-capacitor equivalent circuit representations are not unique, although many of them are formulated using time domain nodal charge or two port equations. Based on the different choices of circuit variables, signal constraints, circuit complexities, existing computer-aided analysis programs, etc., many different switched-capacitor equivalent circuits model have been developed.

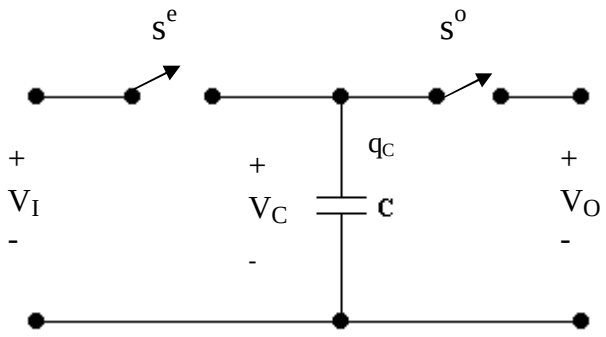


Figure 4.3. A parallel switched-capacitor circuit

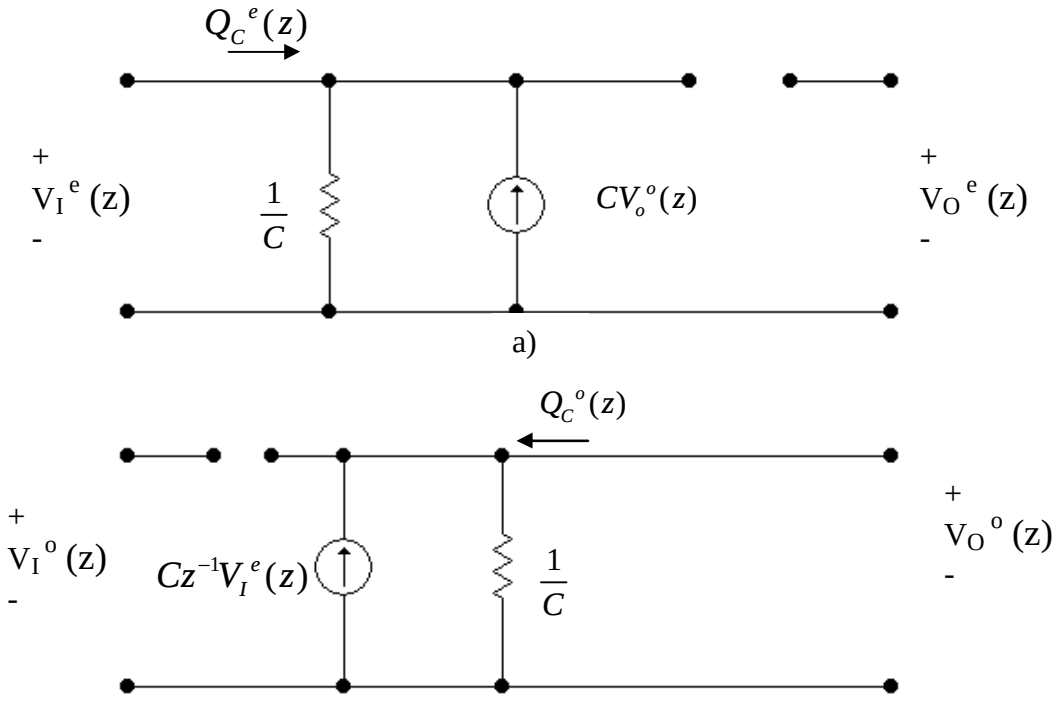


Figure 4.4. An equivalent circuit of a Fig. 4.3 (a) when s^e is closed, (b) when s^o is closed

Referring to Fig. 4.3, let q_c(t) and v_c(t) be the injected charge and voltage across a capacitor of capacitance C. At the end of switching subintervals Δ_1 and Δ_2, τ =T/2 and the injected charge is given by the following charge Equations (4.7) and (4.8).

$$q_c(nT+t) = C\left[v_c(nT+t) - v_c(nT)\right]$$
and
$$q_c(nT) = C\left[v_c(nT) - v_c((n-1)T+t)\right] \tag{4.7}$$

The z-transforms of (4.7) are, respectively,

$$Q_c^{\,e}(z) = C\left[V_c^{\,e}(z) - V_c^{\,o}(z)\right]$$
and
$$Q_c^{\,o}(z) = C\left[V_c^{\,o}(z) - z^{-1}V_c^{\,e}(z)\right] \qquad (4.8)$$

An example for Equivalent Circuit Approach is as follows:

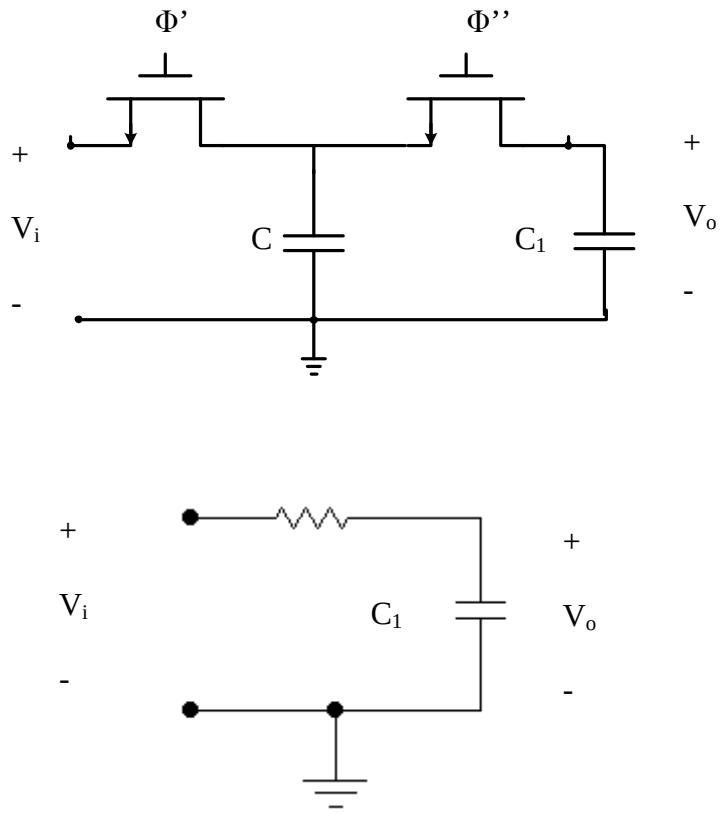


Figure 4.5 RC filter and its SC model

Φ’ phase:

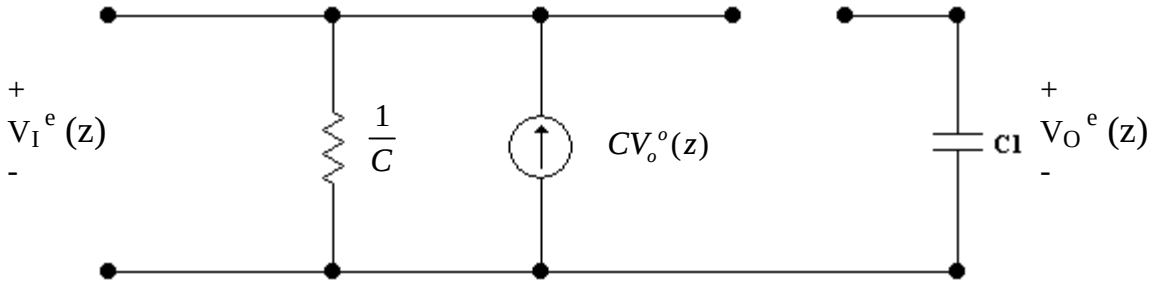


Figure 4.6. An equivalent circuit of a Fig. 4.5. for Φ’ phase

Φ’’ phase:

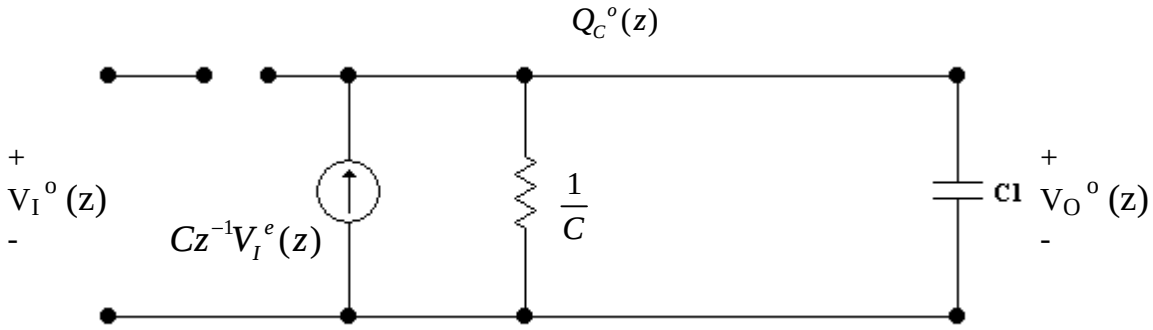


Figure 4.7. An equivalent circuit of a Fig. 4.5. for Φ’’ phase

The z-domain representations are,

$$Q_c^e(z) = C\left[V_c^e(z) - V_c^o(z)\right]$$

and

$$Q_c^o(z) = C\left[V_c^o(z) - z^{-1}V_c^e(z)\right] + C_1\left[V_c^o(z)\right] \tag{4.9}$$

4.3. Modified Nodal Approach (MNA)

The modified nodal formulation of switched-capacitor circuits differs from the nodal formulation in that the “charge flows” of the voltage sources (independent and controlled) and possibly of the “closed” switches are also included (in addition to the node voltages) in the network formulation. Therefore, the size of the network equation is increased. However, the network coefficient matrix is generally sparse, and sparse-matrix techniques can be efficiently employed for computer solutions. In this thesis, because of these advantages and its compatibility to switched capacitor networks, this approach will be used to analyses and simulate the SC networks ((Liou, Kuo and Clement,1983).

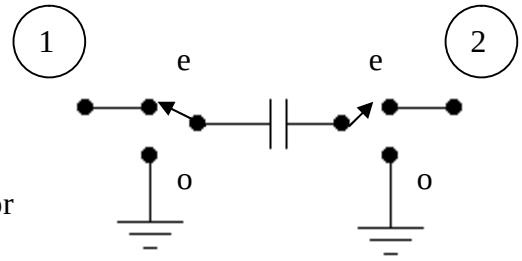
The basic switched-capacitor element is considered as a two port charge transfer admittance expression in the z-domain. This transfer admittance is defined as:

$$Y(z) = \frac{\Delta Q(z)}{V(z)} \tag{4.10}$$

where ΔQ(z) is the z-transformation of the output instantaneous charge increment at time t = nT_c *(n = 1, 2, 3 . . ..)* and *V(z)* is the z-transformation of the terminal voltage. One may note that ΔQ(z) can be treated as the current *i(s)* in the s-domain and sample frequency $f_c = 1/T_c$.

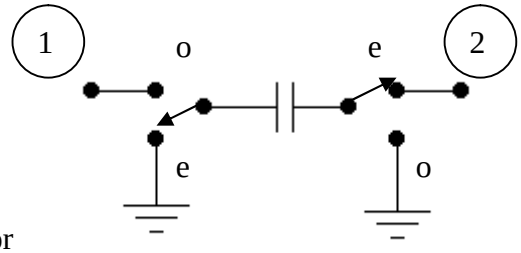
Fig. 4.8. shows an overview of the four basic SC elements together with its corresponding stamps for MNA analysis. (Zivkovic, Petkovi and Milovanovi,1998)

SC invertor



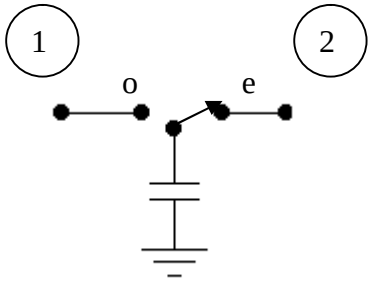
	V_1^e	V_2^e
1^e	C	-C
2^e	-C	C

SC noninvertor



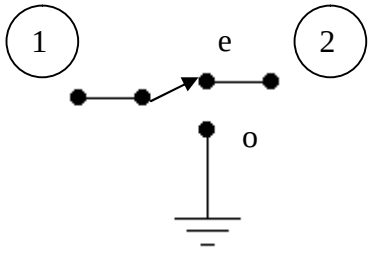
	V_1^e	V_2^e
1^e	C	Cz^{-1}
2^e		

Delay admittance



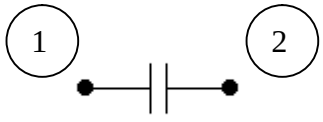
	V_1^e	V_2^e
1^e	C	$-Cz^{-1}$
2^e		

Simple switch



	V_1^e	V_2^e
1^e		
2^e		
N.E	1	-1

capacitor



	V_1^e	V_2^e
1^e	$C(1-z^{-1})$	$-C(1-z^{-1})$
2^e	$-C(1-z^{-1})$	$C(1-z^{-1})$

Figure 4.8. Basic SC building blocks and their stamps for MNA z-domain analysis

The contribution of capacitors for z-domain analysis is also shown in Figure 4.8. Note that 'e' denotes even while 'o' denotes odd phase of clock, respectively. N.E. means new equation, i.e. that element increases the size of the circuit matrix.

Once a formulation technique is adopted, the time-, z-, and frequency-domain analyses can be proceed.

In following chapter 5, some examples will be given by using MNA method.

5. MATLAB PROGRAMMING

5.1. MATLAB Symbolic Simulation Levels

Nowadays, most scientists and engineers rely on computer simulations to analyze, design, and prototype complex systems. Scientific and engineering system models are implemented in a variety of simulation environments (Bastos, Monti, 2005).

In the simulation examples that are given in the chapter 6 are examined using a MATLAB symbolic simulation program. This simulation program basically solves the electronic circuits with MNA method that mentioned previous chapters.

MNA is often preferred for larger systems of equations than the other methods, but it is easier to implement algorithmically on a computer which is a substantial advantage for automated solution. To use modified nodal analysis you write one equation for each node not attached to a voltage source (as in standard nodal analysis), and you augment these equations with an equation for each voltage source. To be more specific, the rules for standard nodal analysis are shown below:

Node Voltage Method:

To apply the node voltage method to a circuit with n nodes (with m voltage sources), perform the following steps.

1. Selective a reference node (usually ground).
2. Name the remaining n-1 nodes and label a current through each passive element and each current source.
3. Apply Kirchoff's current law to each node not connected to a voltage source.
4. Solve the system of n-1-m unknown voltages.

The difficulty with this method comes from having to consider the effect of voltage sources. Either a separate equation is written for each source, or the supernode method must be used.

The rules for modified nodal analysis are given by:

Modified Nodal Analysis (MNA):

To apply the node voltage method to a circuit with n nodes (with m voltage sources), perform the following steps.

1. Selective a reference node (usually ground) and name the remaining n-1 nodes. Also label currents through each current source.
2. Assign a name to the current through each voltage source. We will use the convention that the current flows from the positive node to the negative node of the source.
3. Apply Kirchoff's current law to each node. We will take currents out of the node to be positive.
4. Write an equation for the voltage each voltage source.
5. Solve the system of n-1 unknowns.

As an example consider the circuit below

Step 1 and Step 2 (currents through the voltage sources with current from positive node to negative node) is applied to the circuit given in Figure 5.1.

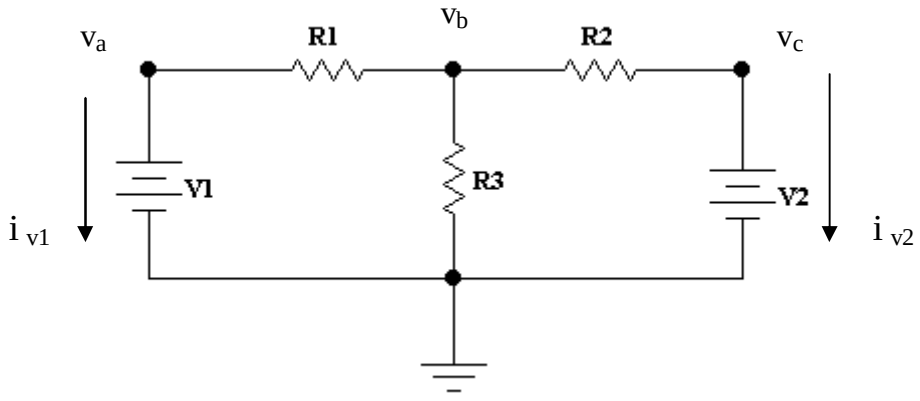


Figure 5.1. A resistive network

Apply step 3 (with positive currents out of the node):

$$\text{Node a}: \quad i_{v1} + \frac{v_a - v_b}{R_1} = 0 \tag{5.1}$$

$$\text{Node b}: \quad \frac{v_b - v_a}{R_1} + \frac{v_b}{R_3} + \frac{v_b - v_c}{R_2} = 0 \tag{5.2}$$

$$\text{Node c}: \quad i_{v2} + \frac{v_c - v_b}{R_2} = 0 \tag{5.3}$$

Apply step 4:

$$V_a = V_1 \tag{5.4}$$

$$V_c = V_2 \tag{5.5}$$

Step 5 is the combination of the above Equations.

The matrix form of the equations above is as follows:

$$\begin{bmatrix} \frac{1}{R_1} & -\frac{1}{R_1} & 0 & 1 & 0 \\ -\frac{1}{R_1} & \frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3} & -\frac{1}{R_2} & 0 & 0 \\ 0 & -\frac{1}{R_2} & \frac{1}{R_2} & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \\ i_{v1} \\ i_{v2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ V1 \\ V2 \end{bmatrix} \tag{5.6}$$

Now all that is left is to solve the 5x5 set of equations (recall that the nodal analysis method resulted in just 1 equation, though we did some substitutions along the way). Solving the 5x5 equation is difficult by hand, but not so with a computer.

Observations about MNA:

If you examine the matrix equations that resulted from the application of the MNA method, several patterns become apparent that we can use to develop an algorithm. All of the circuits resulted in an equation of the form.

$$Ax = z \tag{5.7}$$

This circuit had 3 nodes and 2 voltage sources (n=3, m=2). The resulting matrix is shown below.

$$\begin{bmatrix} \frac{1}{R_1} & 0 & 0 & -1 & 0 \\ 0 & \frac{1}{R_2}+\frac{1}{R_3} & -\frac{1}{R_2} & 1 & 0 \\ 0 & -\frac{1}{R_2} & \frac{1}{R_2} & 0 & 1 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \\ i_{v1} \\ i_{v2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ V1 \\ V2 \end{bmatrix} \tag{5.8}$$

Note that the grey highlighted portion of the A matrix is 3x3 (in general nxn), and includes only known quantities, specifically the values of the passive elements (the resistors). In addition the highlighted portion of the A matrix is symmetric with positive values along the main diagonal, and only negative (or zero) values for the off-diagonal terms. If an element is connected to ground, it only appears along the diagonal; a non-grounded (e.g. R_2) appears both on and off the diagonal). The rest of the terms in the A matrix (the non-highlighted portion) contains only ones, negative ones and zeros. Note also that the matrix size is 5x5 (in general (m+n)x(m+n)). For

all of the circuits we will analyze (i.e., only passive elements and independent sources), these general observations about the A matrix will always hold.

Now consider the x matrix, the matrix of unknown quantities. It is a 1x5 matrix (in general 1x(n+m)). The topmost 3 (in general n) elements are simply the node voltages. The bottom 2 (in general m) elements are the currents associated with the voltage sources.

This brings us to the z matrix that contains only known quantities. It is also a 1x5 matrix (in general 1x(n+m)). The topmost 3 (in general n) elements are either zero, or the sum of independent current sources. The bottom 2 (in general m) elements are the independent voltage sources.

To summarize:

MNA applied to a circuit with only passive elements (resistors) and independent current and voltage sources results in a matrix equation of the form Ax=z

For a circuit with n nodes and m independent voltage sources:

- The A matrix:
  - is (n+m)x(n+m) in size, and consists only of known quantities.
  - the *n*x*n* part of the matrix in the upper left:
    - has only passive elements
    - elements connected to ground appear only on the diagonal
    - elements not connected to ground are both on the diagonal and off-diagonal terms.
  - the rest of the **A** matrix (not included in the *n*x*n* upper left part) contains only 1, -1 and 0 (other values are possible if there are dependent current and voltage sources.
- The **x** matrix:
  - is an (*n*+*m*)x1 vector that holds the unknown quantities (node voltages and the currents through the independent voltage sources).
  - the top *n* elements are the *n* node voltages.

  - the bottom *m* elements represent the currents through the *m* independent voltage sources in the circuit.
- The **z** matrix:
  - is an (*n*+*m*)x1 vector that holds only known quantities
  - the top *n* elements are either zero or the sum and difference of independent current sources in the circuit.
  - the bottom *m* elements represent the *m* independent voltage sources in the circuit.

The circuit is solved by a simple matrix manipulation:

$$x = A^{-1}z \tag{5.9}$$

Though this may be difficult by hand, it is straightforward and so is easily done by computer.

Notational Convention:

This simulation program cannot simply read a schematic diagram so we need to develop a method for representing a circuit textually. This can be done using a device called a netlist that defines the interconnection between circuit elements. If you have used SPICE (Simulation Program with Integrated Circuit Emphasis) this is a familiar concept. (http://www.swarthmore.edu/NatSci/echeeve1/Ref/mna/MNA3.html)

Obviously, the notation used does not change the solution. However the convention described below will make it quite easy to develop the matrices necessary for solution of the circuit.

- Ground is labeled as node 0.
- The other nodes are labeled consecutively from 1 to *n*.
- We will refer to the voltage at node 1 as v_1, at node 2 as v_2 and so on.
- The naming of the independent voltage sources is quite loose, but the names must start with the letter "V" and must be unique from any node names. For our purposes we will require that independent voltage sources have no

underscore ("_") in their names. So the names Va, Vsource, V1, Vxyz123 are all legitimate names, but V_3, V_A, Vsource_1 are not.

- The current through a voltage source will be labeled with "I_" followed by the name of the voltage source. Therefore the current through Va is I_Va, the current through VSource is I_VSource, etc...
- The naming of the independent current sources is similar; the names must start with the letter "I" and must no underscore ("_") in their names. So the names Ia, Isource, I1, Ixyz123 are all legitimate names, but I_3, I_A, Isource_1 are not.

These rules are somewhat restrictive but they make development of the algorithm easier while still allowing quite a bit of freedom.

These rules are easily explained with an example.

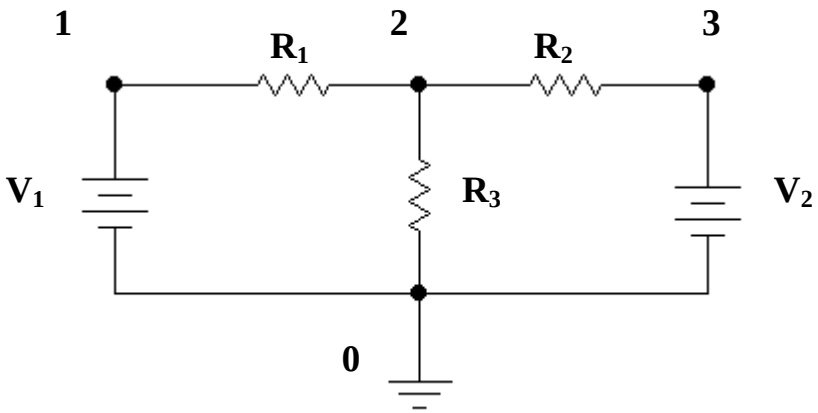


Figure 5.2. A resistive network with nodes

The circuit shown in the Figure 5.2. is labeled according to the guidelines above. Ground is node 0 and the other two nodes are labeled 1 and 2.

All possible sequences of simulation steps are shown in Figure 5.3.

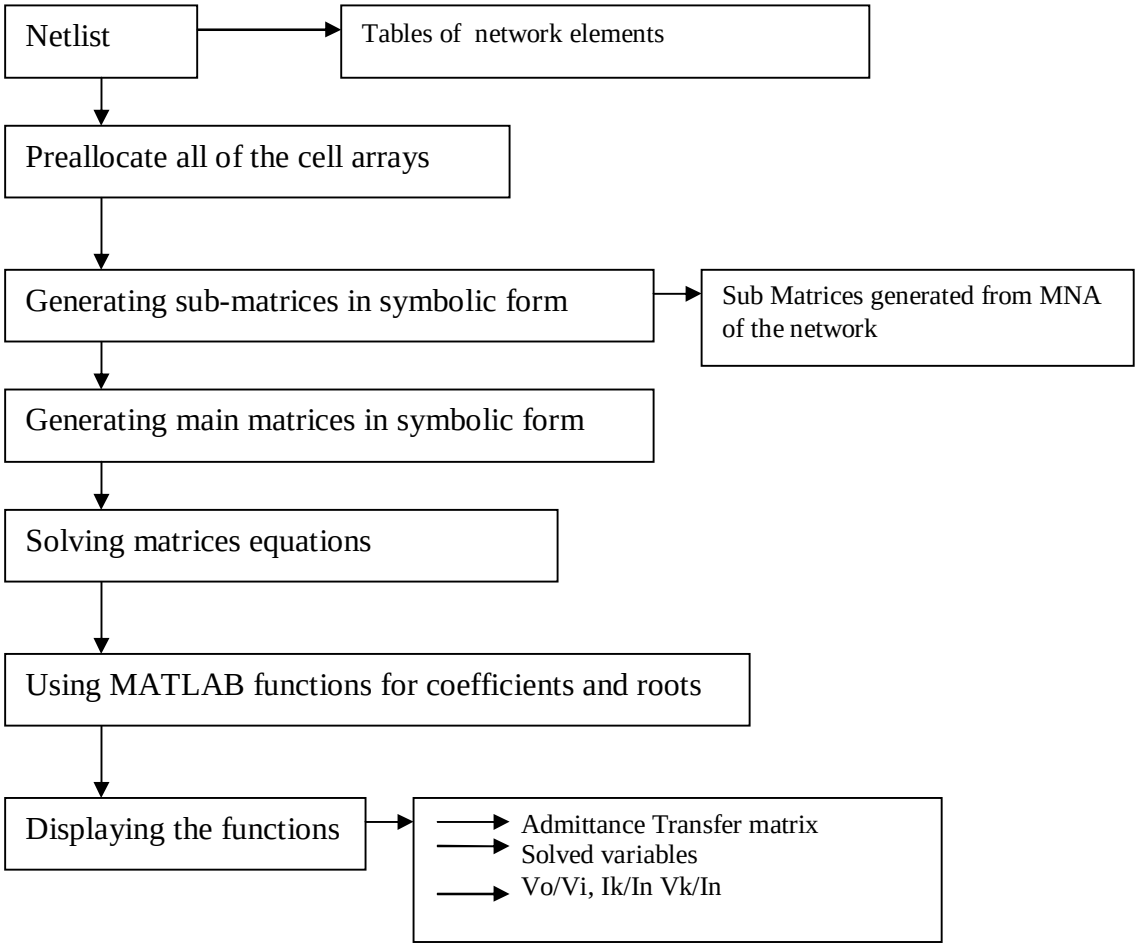


Figure 5.3. Flow chart of simulation

6. CIRCUIT SIMULATION EXAMPLES

Throughout the following examples, SC circuits are analysed and its behavior is observed by getting their transfer functions and by using a simulation program in MATLAB, which is mentioned in the previous section.

Example 1: A voltage divider circuit with SC is given in Figure 6.1. and the solution of its Matlab simulation is obtained.

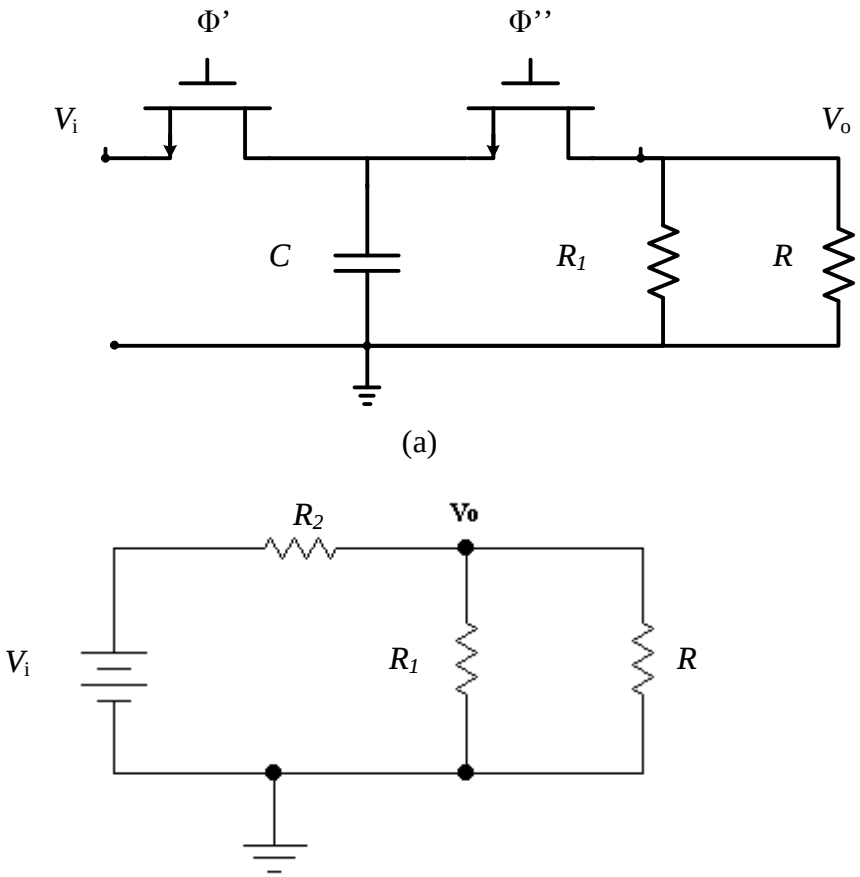


Figure 6.1. (a) A voltage divider circuit with SC (b) A voltage divider circuit equivalent

Analytic Solution:

$$R_{eq} = \frac{R \times R_1}{R + R_1} \tag{6.1}$$

$$R_2 = \frac{1}{Cf_s} \qquad \text{where } f_s \text{ is the switch frequency} \tag{6.2}$$

Then the transfer function will be:

$$\frac{Vo}{Vi} = \frac{R_{eq}}{\frac{1}{Cf_s} + R_{eq}} \tag{6.3}$$

Matlab Solution:

% Symbolic analyses program:
>> analizson

% Network Specifications:

Netlist
```
V1   1 0
R2   1 2  *
R1   2 0
R    2 0
```

Solved variables:

```
[V1 ]
[V2 ]
[IV1]
```

% Calculation of transfer function:

Enter symbol to make analysis :V2/V1

Transfer Function :

$$\frac{R\,R1}{\frac{R1}{f\,C} + \frac{R}{f\,C} + R\,R1}$$

Example 2: A SC low pass filter is given in Figure 6.2 and the solution of its Matlab simulation is obtained.

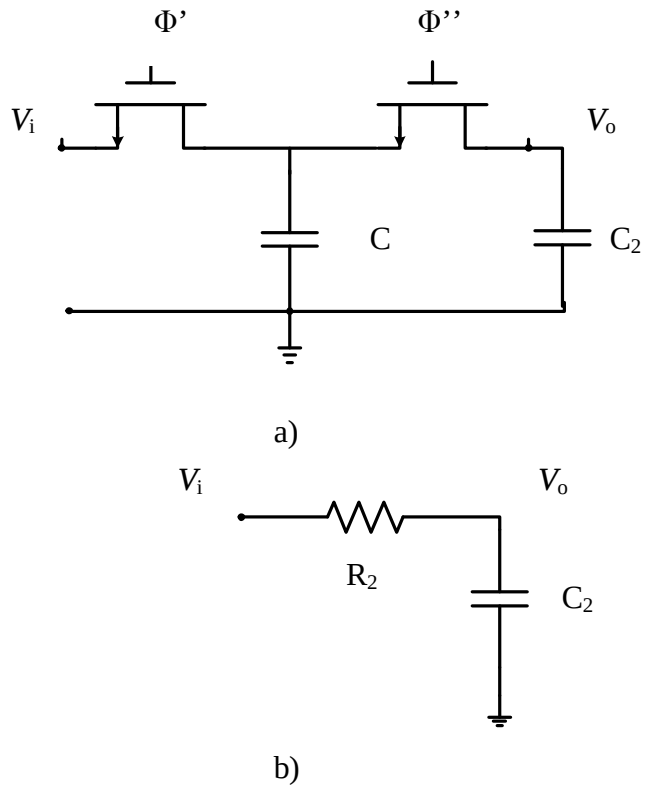


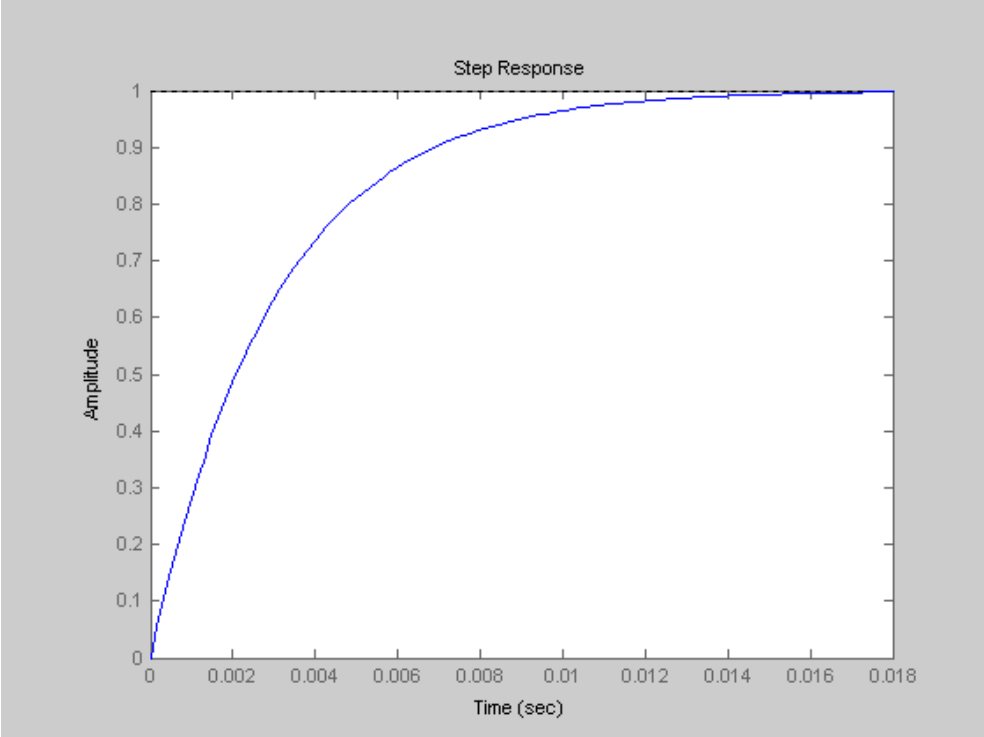
Figure 6.2. (a) Switched-capacitor low-pass filter (b) RC Low pass filter

Matlab Solution:

```
>> analizson
% Network  Specifications:
Netlist
    V1   1  0
    R2   1  2  *
    C2   2  0
Enter symbol to make analysis :V2/V1

Transfer Function:                    1
                                ----------------
                                      s C2
                                1 + ------------
                                      f C

>> syms C2,f,C
>> H=1/(1+(s*C2)/(f*C))
>> C=1E-6, C2=3E-6, f=1000
>> [n,d]=numden(eval(H))
>> mySys=tf(sym2poly(n),sym2poly(d))

Transfer function:
      7.379e2
-----------------------
2.214s + 7.379e2
```

In the following Figures, Step Response and Bode Diagram of Fig 6.2. are given. As it is seen from the Step Response Figure, the time it takes for the capacitor to charge is 5τ which is 0.018 sec. for the given values above. The cut-off frequency for the given values is seen from the Bode Diagram.

```
>> step(mySys)
```



>> bode(mySys)

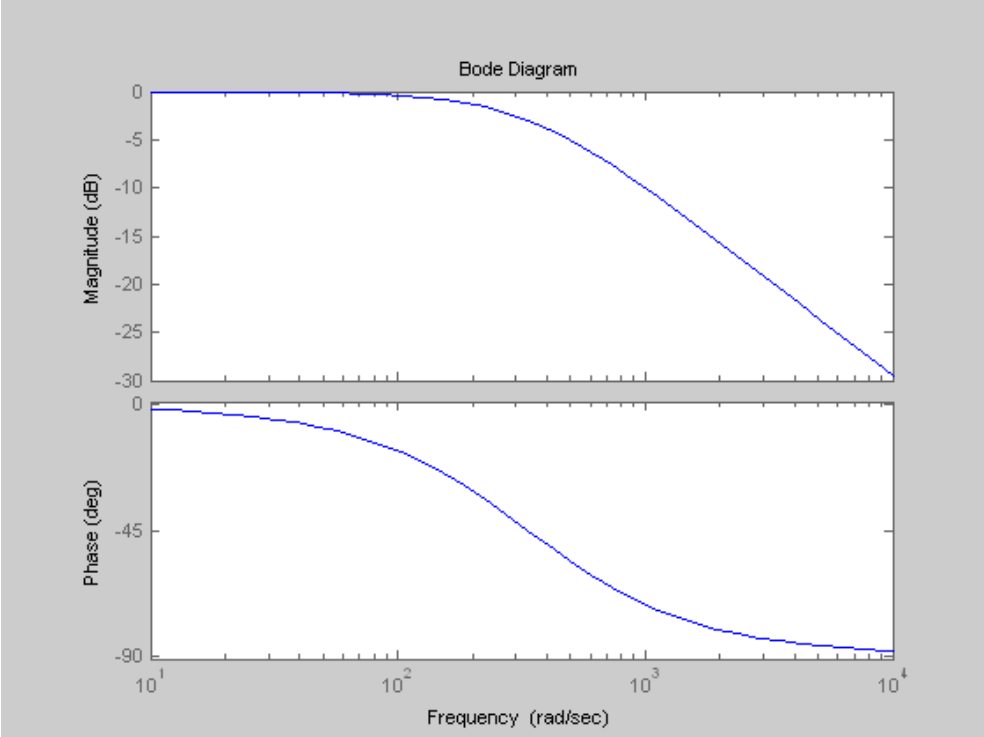
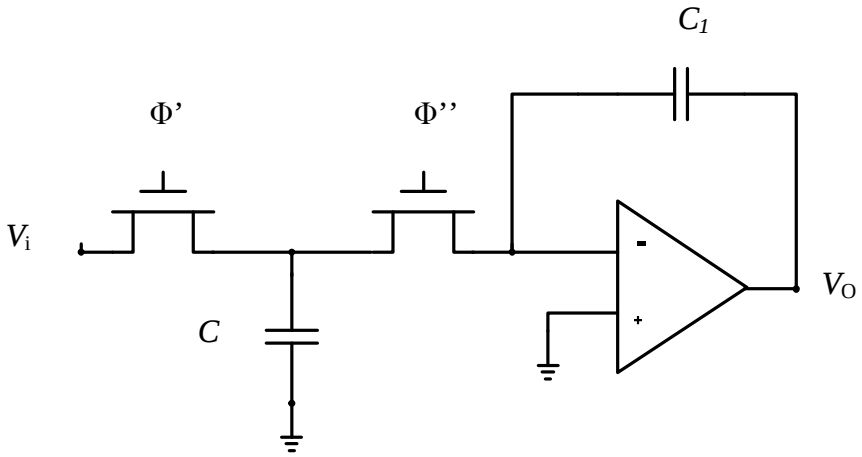
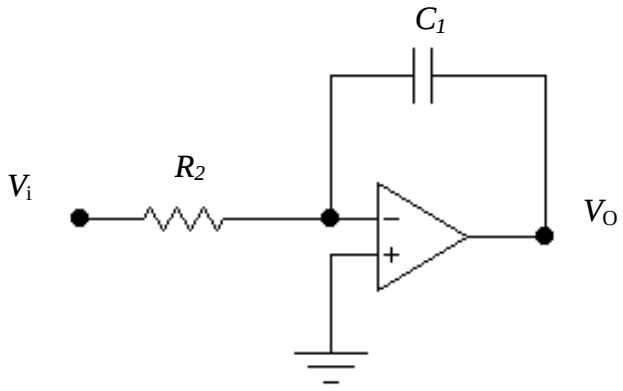


Figure 6.3. Step Response and Bode Diagram of Fig 6.2.

Example 3: A SC integrator is given in Figure 6.3. and the solution of its Matlab simulation is obtained.



a)



b)

Figure 6.4. SC integrator

Analytic Solution:

$$\frac{V_{out}}{V_{in}} = f_s \times \frac{C}{sC_1} \tag{6.4}$$

Matlab Solution:

% Symbolic analyses program:

>> analizson

% Network Specifications:

Netlist

V1 1 0

R2 1 2 *

C1 2 3

OAmp 0 2 3

Solved variables:

v_1

v_2

v_3

I_V1

I_OAmp

% Calculation of transfer function:

>> v_3/v_1

Transfer Function:

$$-\frac{f\,C}{s\,C1}$$

7. RESULTS AND CONCLUSION

In this study, symbolic analyzing of general SC networks methods is presented. And also, a MATLAB simulation is used for symbolic analysis of SC network using specially designed examples. Examples results showed that symbolic analyses provide us with a general equivalent circuit and additional insight in the capabilities of SC networks. Also symbolic calculations and simulations for exploring circuit properties and for checking hand calculations, serves as a supporting tool for designers.

The simulation program used in this thesis cannot simply read a schematic diagram so a method is developed for representing a circuit textually. This can be done by a netlist that defines the interconnection between circuit elements so that the symbolic simulator reads netlist as its input. This simulation program basically solves the electronic circuits with MNA method in the s-domain. MNA often results in larger systems of equations than the other methods, but is easier to implement algorithmically on a computer which is a substantial advantage for automated solution. MNA is a method that is widely established approaches in circuit analysis.

This simulation starts with a netlist (very similar to spice) and generates and solves the resulting circuit equations. The symbolic results, by handling resistors, capacitors, inductors and op-amps, can be evaluated to give numeric results if desired.

In this thesis, basic SC networks are analyzed by several methods and sample networks are simulated by using the main approach that is switched capacitor behavior in the network is similar to resistor's behavior. It is observed from the simulation results, too. Switch capacitor behavior can be obtained when the switching frequency is much higher than the maximum signal frequency.

Such an analysis would provide fruitful ground for further research in symbolic analysis of SC networks. One of the challenges for future symbolic analyzing is increasing the complexity of circuits, while keeping the interpretability of results. The symbolic analysis of large SC networks is the focus of intense attention in the last years and will continue to be of interest in the future.

These analysis methods would also yield to the new, more efficient algorithms; applications are being amplified within fields such as automatic design of SC integrated circuits, together with the development of symbolic analysis techniques for more complex and non-traditional characteristics.

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RESUME

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