INTEGRATION OF CHIPS BY FLIP-CHIP BONDING TECHNIQUES

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
MATERIALS SCIENCE AND NANOTECHNOLOGY

By
Mehmet Halit Öztürk
May 2023

Integration of Chips by Flip-Chip Bonding Techniques
By Mehmet Halit Öztürk
May 2023

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Mehmet Yılmaz(Advisor)

Emine Yegan Erdem

Burhanettin Erdem Alaca

Approved for the Graduate School of Engineering and Science:

Orhan Arıkan
Director of the Graduate School

ABSTRACT

INTEGRATION OF CHIPS BY FLIP-CHIP BONDING TECHNIQUES

Mehmet Halit Öztürk
M.S. in Materials Science and Nanotechnology
Advisor: Mehmet Yılmaz
May 2023

Integration and packaging of MEMS devices are necessary for designing operational, independent and mobile products. Flip-chip bonding (FCB) has been recognized as an important technology to meet some of the integration and packaging needs. To assemble a probe for photoacoustic imaging (PAI), integration of ASIC chips with a CMUT chip and integration of the CMUT chip with a PCB is required, where various FCB techniques may be employed for integration. Thermo-sonic FCB was the most suitable for the ASIC-CMUT integration. Gold stud bumps (GSBs) were used for the TSFCB. Therefore, the fabrication of GSBs was optimized for 25.4 µm and 17.5 µm diameter gold wires. Also, to flatten the top surface of the GSBs and to level the height of the GSBs, a novel displacement-controlled coining (DCC) process is developed. The height and bonding surface area of the GSBs can be tailored for flip-chip bonding (FCB) processes. Furthermore, using the lumped-capacitance modeling approach, a heat energy transfer based, experimentally validated analytical model is developed for the thermo-sonic flip-chip bonding process (TSFCB). The developed analytical model is used to estimate TSFCB process parameters for ASIC-CMUT FCB integration. Successful TSFCB process trials are completed in this study at a wide range of process temperatures ($T_{process}$) of 24 °C, 25 °C, 40 °C, 150 °C, and 375 °C. Two ASIC chips are successfully integrated with a CMUT chip via the TSFCB. Another FCB process combines stacked GSBs and isotropic conductive adhesive (ICA) material optimized for the integration of CMUT-PCB. Surface-mount device (SMD) and a through-hole component of the PCB are soldered and fabrication of the integrated electronic systems of the probe is completed. Finally, the design and fabrication of the probe are presented. The probe is assembled using integrated electronic systems for PAI imaging.

Keywords: Flip-chip bonding, thermo-sonic, ultrasonic, gold stud bump,

displacement-controlled coining, analytical modeling, conductive paste.

ÖZET

TERS YONGA ENTEGRASYON TEKNIKLERI ILE YONGALARN ENTEGRE EDILMESI

Mehmet Halit Öztürk
Malzeme Bilimi ve Nanoteknoloji, Yüksek Lisans
Tez Danışmanı: Mehmet Yılmaz
Mayıs 2023

Çalışan, bağımsız ve mobil ürünler tasarlamak için MEMS cihazlarının entegrasyonun yapılması ve paketlemesinin tamamlanması gerekmektedir. Ters yonga entegrasyon tekniği (FCB) entegrasyon ve paketleme ihtiyacını karşılayabilecek önemli bir teknolojidir. Ters yonga entegrasyon teknolojisi ile, ASIC yongalarının bir CMUT yongası ile entegrasyonu ve CMUT yongası ile baskı devre kartının (PCB) entegrasyonu yapılarak fotoakustik görüntüleme (PAI) yapabilen prob üretimi mümkün hale gelmektedir. ASIC ve CMUT yongalarının entegrasyonu için termo-sonik ters yonga entegrasyonu (TSFCB) en uygun yöntem olarak belirlenmiştir. TSFCB prosesinde altın topçuklar kullanılır. Bu sebeple, altın topçukların üretimi 25.4 µm ve 17.5 µm altın teller için optimize edilmiştir. Ayrıca, altın topçukların üst yüzeyini düzleştirmek, düzleştirilen yüzeyin yüzey alanını kontrol etmek ve altın topçukların yüksekliğini dengelemek için yeni bir yer değiştirme kontrollü düzleştirme (DCC) işlemi geliştirilmiştir. Bu yer değiştirme kontrollü düzleştirme işlemi ile, altın topçukların yüksekliği ve birleştirme yüzey alanı, ters yonga entegrasyonu (FCB) için uygun hale getirilebilir. Ayrıca, lumped capacitance modelleme yaklaşımı kullanılarak termo-sonik FCB prosesi (TSFCB) için ısı enerjisi transferine dayalı, deneysel olarak doğrulanmış bir analitik model geliştirilmiştir. Geliştirilen analitik model, ASIC-CMUT FCB entegrasyonunda TSFCB işlem parametrelerini tahmin etmek için kullanılır. Bu çalışmada başarılı TSFCB proses denemeleri, 24 °C, 25 °C, 40 °C, 150 °C ve 375 °C'lik çok çeşitli proses sıcaklıklarında ($T_{process}$) tamamlanmıştır. İki ASIC yongası, TSFCB aracılığıyla bir CMUT yongasıyla başarıyla entegre edilmiştir. İstiflenmiş altın topçuklar ve izotropik iletken yapışkan (ICA) malzemesini birleştiren bir FCB işlemi, CMUT-PCB'nin entegrasyonu için optimize edilmiştir. PCB'nin komponentlerinin lehimlenerek, probun entegre elektronik sistemlerinin imalatı tamamlanır. Son olarak, probun tasarımı ve üretimi sunulmuştur. Prob, PAI

görüntüleme için entegre elektronik sistemler kullanılarak monte edilmiştir.

Anahtar sözcükler: Ters yonga entegrasyonu, ultrasonik, termosonik, altın topçuk, yer değiştirme kontrollü düzleştirme, analitik modelleme, iletken epoksi malzeme.

Acknowledgement

I would like to sincerely thank Dr. Mehmet Yılmaz, my advisor, for allowing me to work in an exceptional research environment. His unwavering support, guidance, and encouragement have been valuable to me. I am incredibly appreciative of the life experiences and professional attitude he has instilled in me that goes beyond academia. I am thankful for all the opportunities he has given me and will carry the knowledge gained from them throughout my life.

I want to express my sincere gratitude to Dr. Fikret Yıldız for his scientific mentoring and advice throughout my research. I learned a lot from him while working with him on experiments and under his guidance.

I am deeply thankful to Prof. Dr. Abdullah Atalar for his help on our research project. I have extensively benefited from his extensive knowledge of PCB fabrication.

I would like to thank Asst. Prof. Dr. E. Yegan Erdem for dedicating her time to evaluate my thesis.

I would like to thank Prof. Dr. Erdem Alaca for dedicating his time to evaluate my thesis.

I would like to thank my precious family who loved and supported me during my master's degree and in every moment of my life. I would like to thank my father Ahmet Öztürk for being a wonderful father, my mother Nalan Öztürk for being a wonderful mother, my brother İbrahim Öztürk for being a legendary brother and my sister Zeynep İrem Öztürk for being a legendary sister. I am very proud to be your son and your big brother. We will accomplish many more things in the future.

I want to thank Melike Aygün Tutan, my love, for changing my life and making me a better man. I want to thank you for your love, support, and wise advice throughout my research. We will accomplish many more things in the future.

Next, I want to thank my dear friends and colleagues. Rashid, Merve, Ahmad, Habibe, Samet, Umut, Doğukan, Muhammad Ali, Amir. Thank you guys for giving me this endless friendship, great support, and wise advice. I was lucky to work with you.

I want to express my gratitude to Can Güven who immensely helped me during my research. I want to thank Halil İbrahim Şener and Hazal Vural for their support and cooperation during my research.

Finally, I want to thank all the staff of UNAM for their constant support and help. UNAM is a great place because of you.

We gratefully acknowledge the financial support of the Scientific and Technological Research Council of Turkey (TUBITAK) via project number 118S041.

We gratefully acknowledge Ioan Dan, Thomas Müller, and all the relevant staff of Finetech GmbH & Co. KG. for their help, and technical support in calibrating the flip-chip bonder and providing our technical needs via their technical design services and technical consulting services. I still owe you sütaş ayran and köfte.

Contents

1 Introduction **1**

2 Fabrication Process **6**

2.1 Design Considerations of ASIC-CMUT Flip-Chip Bonding (FCB) 6

2.2 Design and Fabrication of Pseudo Chips 12

2.3 Fabrication of Gold Stud Bumps (GSBs) 16

2.4 Displacement-Controlled Coining (DCC) Process 18

2.4.1 Aluminum Mold Design & Fabrication 20

2.4.2 Borosilicate Glass 22

2.4.3 Displacement-controlled coining (DCC) process steps . . . 23

2.4.4 Displacement-controlled coining (DCC) process trials . . . 26

2.5 Thermo-sonic Flip-Chip Bonding Process (TSFCB) 43

2.5.1 Performing the TSFCB 43

2.5.2 Analytical Modelling of the thermo-sonic flip-chip bonding process (TSFCB) 46

2.5.3 TSFCB Process of Real ASIC and Real CMUT 62

2.5.4 Underfill and Parylene C Coating Processes 64

2.6 CMUT - PCB Integration 71

2.6.1 Design and fabrication of the PCB 71

2.6.2 Design and fabrication of the pseudo-PCB 72

2.6.3 FCB process design for CMUT – PCB integration 73

2.6.4 Selection, characterization, and application of the ICA material (EPO-TEK H20E Conductive Paste) 77

2.6.5 Fabrication of the stacked GSBs 80

2.6.6 Force-controlled coining of the stacked GSBs 81

2.6.7 FCB integration trial of the pseudo-CMUT and pseudo-PCB 84

2.6.8 FCB integration of a real CMUT and a real PCB 87

2.7 PCB Component Soldering and Wire Bonding of the Device Layer 91

2.7.1 The Prototype PCB for alignment control 91

2.7.2 Time-pressure dispenser (TPD), the Solder material, and the Soldering Station 92

2.7.3 Soldering of the PCB components 93

2.7.4 Wire Bonding of the device layer 96

2.8 Probe Assembly 97

2.8.1 Design and Fabrication of the Probe 97

2.8.2 Assembling a Test Probe to Validate Water Tightness and to Observe the Effects of the Compression Forces 101

2.8.3 Assembling the real Probe 104

3 Conclusion **106**

A Supplementary **124**

B Supplementary **129**

List of Figures

2.1 Design and fabrication of the pseudo-ASIC chips and the pseudo-CMUT chips. 13

2.2 Design of the pseudo-ASIC chip and the pseudo-CMUT chip and 2-probe measurement technique that is used for this study. (a) Design of the pseudo-ASIC chip and partial view from the array of bonding pads of the pseudo-ASIC chip, (b) Design of the pseudo-CMUT chip, design of the bonding pads of the pseudo-CMUT chip and partial view from the array of bonding pads of the pseudo-CMUT chip, (c) Aligned pseudo-ASIC chip on the pseudo-CMUT chip after the FCB process, (d) 2-probe measurement method to measure resistances of the GSBs. 14

2.3 Fabrication steps of a GSB. (a) Step-1: Performing bond1, (b) Step-2: Performing loop z direction, (c) Step-3: Performing loop y direction, (d) Step-4: Performing bond2, (e) Step-5: Capillary tool moves up, (f) Fabricated GSB, (g) Anatomy of a GSB. 17

2.4 The aluminum mold. (a) Design of the aluminum mold and fabricated aluminum mold, (b) Laterally on the left and longitudinally on the right, parallelism measurement between cavity bottom surface and mold top surface. 20

2.5 3.30 mm thick, Borosilicate glass. 22

2.6 Steps of the DCC process, (a) Placing the pseudo-ASIC chip inside the selected mold cavity, (b) Placing the Borosilicate glass on top of the aluminum mold, (c) Placing another aluminum piece on top of the Borosilicate glass and application of compressive force to coin the GSBs. 24

2.7 ImageJ measurements. (a) Measuring height of a GSB, (b) Measuring the surface area of a GSB by selecting the foreground pixel area encapsulated inside the yellow-colored closed curve. 25

2.8 Gold stud bump properties before and after the DCC process. (a) Anatomy of a coined gold stud bump, (b) Mean values of the GSBs before the DCC process, (c) Mean values of the GSBs after the FCFC process trials. h: Height, d: Diameter, th: Tail height, MC: Mold cavity, SD: Standard deviation 27

2.9 Results of the DCC process. (a) Mean height values of the GSBs and standard deviation of the height values of the GSBs after the DCC process (the y-axis on the right indicates the mold cavities with orange triangle markers.), (b) Optical microscope images of the pseudo-ASIC chip before and after the DCC process, (c) Scanning electron microscope images of the pseudo-ASIC chip before and after the DCC process. 29

2.10 Surface area of the GSBs after the coining process. (a) Average pressure/bump (MPa) vs average surface area/bump (mm^2/bump) after the DCC process, (b) Optical microscope images of the surface area of the GSBs after coined by 550 µm, 540 µm, 530 µm mold cavities, respectively. 31

2.11 Resistivity measurements of the GSBs after the FCB processes. (a) Resistivity of the GSBs pairs after the TSFCB, (b) FCB structures after the TSFCB processes. 32

2.12 Comparison of 0.25 N/bump, 0.5 N/bump, and 0.75 N/bump coining processes. Mean height value vs compressive force/bump plot (on the left) shows that height of the GSBs decreases with increasing compressive force/bump. Average surface area/bump vs compressive force/bump plot (on the right) shows that average surface area increases with increasing compressive force/bump value. . . 34

2.13 SEM (a), and optical microscope (b) images of the GSBs after 0.25 N/bump (b-left), 0.5 N/bump (b-middle), 0.75 N/bump (b-right) coining processes, respectively. In b-left and b-middle images, a red circle highlights an uncoined GSB. The GSBs are all coined in the b-right image. 36

2.14 Pseudo-ASIC31 is coined with 1N/bump and 2N/bump to study effects of the high compressive forces. Height value decreases with increasing the compressive force/bump as shown in the plot on the left. Also, average surface area/bump value increases with increasing the compressive force/bump as shown in the plot on the right. 38

2.15 Pseudo-ASIC31 is coined with 1N/bump and 2N/bump to study effects of the high compressive forces. Optical microscope and SEM images are shown after the coining processes. 40

2.16 Comparison of the coining processes performed by the DCC process and the FCC capability of an FCB tool. 42

2.17 The TSFCB Process steps. (a) Clamping of the pseudo-CMUT chip, (b) Design of the die collet, (c) Alignment between the pseudo-ASIC chip and the die collet (top) and Alignment between the pseudo-ASIC chip and the pseudo-CMUT substrate (bottom), (d) The TSFCB process. 45

2.18 An example ultrasonic power-ultrasonic time plot from a TSFCB process. 47

2.19 TSFCB process trials for Pyrex pseudo-ASICs. Increasing T_m% increases deformation of GSB and misalignment. 53

2.20 TSFCB process trials for Silicon pseudo-ASICs. Beneath 46 % T_m, nonconductive GSB connections observed. 54

2.21 TSFCB process plots. (a) TSFCB process at 150 °C and 19 N. Total process takes 87 seconds. Ultrasonic power is applied at 60^{th} second (shown in red dashed line), (b) TSFCB process at 24 °C and 19 N. Total process takes 15 seconds. Ultrasonic power is applied at 9^{th} second (shown in red dashed line). 57

2.22 Estimation of bump deformation during the TSFCB process. (a) Location of the 8 GSBs in the array, (b) Bump height estimation and measurement values, (c) SEM images of the trials. 59

2.23 (a) Multiple pseudo-ASIC chips are bonded on the same pseudo-CMUT substrate, (b) Two Pyrex pseudo-ASIC chips are bonded very close to each other. The shortest distance between the two pseudo-ASIC chips is 520 µm. 60

2.24 (a) Optical and SEM images of ASIC-1, (b) Optical microscope and SEM images of ASIC-2. 62

2.25 (a) Bonded ASIC chips on the CMUT surface after the TSFCB process, (b) The CMUT chip after the TSFCB process. 63

2.26 SEM images of ASIC-1 and ASIC-2 after the TSFCB processes. Connections of ASIC-1 and ASIC-2 are fully integrated with the CMUT chip. 64

2.27 Underfill dispensing trial using the TPD tool. (a) Dispensed underfill dots on the silicon wafer surface, (b) Dispensed dot diameter vs. time plot. 66

2.28 Underfill dispensing to the FCB structure. (a) The underfill material is dispensed using the route ("L" shape) highlighted by the red arrows, and 4 dots are dispensed to the edge of the pseudo-ASIC chip, (b) Optical microscope images of the FCB structure after the dispensing process. 67

2.29 SEM images of the FCB structure after underfill dispensing and curing are completed. 67

2.30 Dicing Tape covering of the PCB bonding pads of the CMUT chip before the Parylene C coating. 69

2.31 The CMUT chip after the Parylene C coating and removal of the masking tape. 69

2.32 Design of the PCB. 71

2.33 Fabricated real PCB. 72

2.34 Design of the pseudo-PCB. (a) The structure of the top and the bottom layer is the same. (b) Alignment of the CMUT chip bonding pads and pseudo-PCB bonding pads. 73

2.35 Fabricated pseudo-PCBs. 74

2.36 (a) Regression analysis after viscosity measurement of the H20E ICA material (at room temperature), (b) Viscosity (mPa.s) vs shear rate (1/s) graph of H20E. 78

2.37 TPD optimization of H20E. (a) TPD Trial with various pressure and time value on a Pyrex surface, (b) H20E bump material height measurement via Keyence VKX-100 confocal microscope, (c) H20E bumps on the bonding pads of the pseudo-PCB. 79

2.38 Change in the average bump height according to the change in the TPD dispensing parameters. 79

2.39 SEM images of stacked GSB. (a) Stacked GSB on the PCB pads of the pseudo-CMUT chip, (b) A stacked GSB structure image. . 80

2.40 (a) Standard die collet (SDC), (b) force-controlled coining of the stacked GSB. 82

2.41 Stacked GSB on the PCB bonding pads of the CMUT chip. (a) Stacked GSBs before the coining process, (b) Stacked GSBs after the coining process. 83

2.42 Subjecting pseudo-FCB structure to 80 °C temperature. (a) Pseudo-FCB structure is on the pseudo-PCB during the heating process, (b) Resistance values of the pseudo-FCB structure before and after subjecting to high temperature. 84

2.43 Pseudo-CMUT pseudo-PCB FCB process. (a) FCB process at 1 N force, 120 °C curing temperature for 15 minutes, (b) Pseudo-CMUT pseudo-PCB structure after the FCB process, (c) Alignment between the bonding pads after the FCB process. 86

2.44 Soldering of pseudo-PCB. (a) Inserting copper wires into through holes and dispensing the solder material, (b) Reflowed solder materials. 86

2.45 Stacked GSBs on the PCB pads of the real CMUT chip. 87

2.46 (a) The real PCB with soldered SMD components prior to FCB integration, (b) Conductive paste bumps were dispensed by a paintbrush on the PCB bonding pads. 88

2.47 Alignment between the real CMUT chip and the real PCB after the FCB process. 89

2.48 CMUT-PCB integrated structure. (a) Front side of the PCB, (b) Back side of the PCB. 89

2.49 The prototype PCB is assembled into the probe, and the alignment of the PCB components is checked. 92

2.50 (a) The TPD and a syringe that contains SAC 305 solder material, (b) YIHUA 853AAA+ solder station. 93

2.51 Photo of the real PCB after soldering work is completed. The PCB is integrated with the ASIC chips - the CMUT chip structure and components are soldered. 95

2.52 Wire bonding connection between the PCB ground pad and the device layer of the CMUT chip. 96

2.53 The design of the Probe. (a) The assembled probe, (b) The 3D printed holder part, (c) The outer aluminum part, (d) The bottom aluminum part. 98

2.54 The bottom aluminum part. (a) the bottom aluminum part with PCB, (b) the nest for the 7x2 IDC connector through-hole legs, (c) the Cross section of the bottom aluminum part. O-ring 1 and O-ring 2 locations are shown with red arrows. 99

2.55 (a) The cross-section view of the probe, (b) The inner aluminum part 1, (c) The inner aluminum part 2, (d) The cross-sectional view of the internal aluminum parts, the CMUT chip, the PCB, and the fiber assembled. 100

2.56 Test probe assembly. (a) The test PCB is placed on the bottom part, and the ASIC-CMUT flip-chip bonded structure is placed on top of the test PCB, (b) 2 inner aluminum parts are placed on the PBC, (c) The bottom part of the test probe, (c) Assembled test probe. 102

2.57 (a) The ASIC-CMUT structure on the test PCB after the experiment, (b) Average resistance value before and after the test assembly. 103

2.58 (a) The test probe inside the water, (b) The ASIC-CMUT structure on the test PCB after the experiment. The broken corner is shown. No water penetrated into the probe, (c) The average resistance values before and after the experiment. 104

2.59 Real Probe assembly. (a) The PCB is placed on the bottom aluminum part, (b) The inner aluminum parts are placed atop the PCB with a 15 cN.m torque value, (c) The bottom part of the probe after the assembly, where ASIC-CMUT structure is visible. 105

.1 (a) Anatomy of a GSB, (b) An example ultrasonic power-ultrasonic time plot, (c) T_{int} calculation for a TSFCB process. 131

.2 The US die collet attached to the placer arm. 134

.3 Ultrasonic calibration plot after the calibration. 135

.4 Ideal clamping of the substrate with the spring. 137

.5 Alignment of the top chip and the substrate chip. (a) Alignment of the right side, (b) Alignment of the left side, (c) A good alignment. 140

.6 FCB Process model (Simulink). 144

.7 The SDC die collet touches the CMUT chip from the middle of the CMUT chip. 147

.8 A good alignment between the CMUT and the PCB. 149

List of Tables

2.1 SBB process parameters for 17.5 µm and 25.4 µm gold wire. . . . 17

2.2 Properties of GSBs of the Pyrex pseudo-ASIC chips after the DCC process. h: Height, SD: Standard deviation, D: Diameter, SA: Surface area, GSB: Gold stud bump, Avg: Average. 46

2.3 Properties of GSBs of the Silicon pseudo-ASIC chips after the DCC process. h: Height, SD: Standard deviation, D: Diameter, SA: Surface area, GSB: Gold stud bump, Avg: Average. 46

2.4 Thermal conductivities of relevant materials. 51

2.5 TSFCB process trials of Pyrex pseudo-ASICs. 51

2.6 TSFCB process trials of Silicon pseudo-ASIC. 51

2.7 Resistance measurement results of Pyrex trials. 55

2.8 Resistance measurement results of Silicon trials. 55

2.9 GSB properties of ASIC-1 and ASIC-2 after the displacement-controlled coining process. 62

2.10 TSFCB parameters of ASIC-1 and ASIC-2. The parameters are calculated by the developed analytical model. 63

2.11 Properties of 353 ND underfill material. 65

2.12 Properties of H20E ICA material. 77

2.13 Stud bump bonding parameters of the Stacked GSB. 81

2.14 The PCB component list. 94

2.15 Wire bonding parameters of the PCB ground pad and the device layer of the CMUT chip. 97

A.1 Resistance results of the TSFCB trials at Fig. 2.11. 125

A.2 Measured values table of Pseudo ASIC 32 after 0.25 N/bump, 0.5 N/bump, 0.75 N/bump coining processes. MC: Mold cavity, h: Height, SD: Standard deviation, SA: Surface area, CF: Compressive force. 126

A.3 Values of the GSBs after 1 N/bump and 2 N/bump DCC processes. MC: Mold cavity, h: Height, SD: Standard deviation, SA: Surface area, CF: Compressive force. 127

A.4 Values of GSBs after the FCC and the DCC processes. h: Height, SD: Standard deviation, SA: Surface area, Avg: Average. 128

Chapter 1

Introduction

A Capacitive Micromachined Ultrasound Transducer (CMUT) is a MEMS device that transduces ultrasonic waves to electronic signals. Such electronic signals can be processed, and photoacoustic imaging (PAI) can be formed. Microfabrication techniques can be used to fabricate CMUTs, and CMUT chips can be used for PAI imaging. A CMUT chip comprises CMUT cells with a vibrating top layer and a fixed bottom layer. Interaction between the ultrasound wave and CMUT top layer vibrates the top layer, and due to the capacitance effect, a signal is produced. Each CMUT chip can have multiple CMUT cells that work as a pixel for PAI imaging. Multiple CMUT cells can be fabricated in a 2D array [1]. Fabricated CMUTs must be integrated with electronics to process signals from the CMUT transducer cells. An application-specific integrated circuit (ASIC) can process signals generated by the CMUT cells, and flip-chip bonding techniques can integrate ASIC and CMUT [2]. A printed circuit board (PCB) can connect CMUT cells to conventional electronics [2]. Then, the integrated CMUT-ASIC-PCB structure can be assembled into a probe for PAI imaging purposes [3, 4].

Kerem Enhoş worked on designing and fabricating CMUT arrays (256 CMUT cells) and integrating the CMUT chip to a PCB via the thermo-sonic flip-chip technique in 2019 at Bilkent University [5]. Later, Talha Masood Khan worked on designing and fabricating CMUT arrays during his Ph.D. studies in 2020

at Bilkent University [6]. Furthermore, Yusuph Abubakar Abhoo worked on designing and fabricating CMUT array (256 CMUT cells) in 2021 at Bilkent University [7].

To design and fabricate a PAI probe, an interdisciplinary and collaborative project between Bilkent University UNAM, Bilkent University, Hakkari University, and Ankara University has been initiated. In this PAI probe, a CMUT chip comprises 256 CMUT cells in a 2D array designed and fabricated on Pyrex substrate. The bottom electrode of the CMUT chip was Ti/Pt/Au metal stack, and the top layer of the CMUT chip was a silicon-on-insulator (SOI) wafer bonded by an anodic wafer bonding technique [8]. Furthermore, a trans-impedance amplifier ASIC chip is designed with 128 inputs to amplify and process the CMUT cell signals. The design of the trans-impedance amplifier ASIC chip was done by graduate student Cem Bülbül and his thesis adviser Prof. Dr. Abdullah Atalar. The designed ASIC chip was manufactured on silicon substrates by AMS in Austria. A PCB is designed by Prof. Dr. Abdullah Atalar and manufactured at PCBWay company with glass fabric composite (FR4) material. Finally, a prototype probe is designed by undergraduate student summer intern Halil İbrahim Şener and Dr. Mehmet Yılmaz and fabricated from aluminum material with conventional manufacturing techniques, and 3D polymer printing techniques.

In this integration of chips by flip-chip bonding techniques thesis study, fabricated CMUT chips, ASIC chips, and PCBs are integrated using two different flip-chip bonding techniques. Components of the integrated PCB structure are soldered and the CMUT-PCB ground connection is completed by wire bonding. The integrated ASIC-CMUT-PCB is then assembled into a prototype probe. The design and fabrication of the probe are also proposed.

A suitable flip-chip bonding technique for ASIC-CMUT integration is selected based on the process capability of the used cleanroom facility and the material compatibility of the ASIC and the CMUT. Thermo-sonic flip-chip bonding with gold stud bumps is the selected flip-chip bonding technique. Chapter 2.1 describes the design considerations of ASIC-CMUT flip-chip bonding (FCB). There were a limited amount of ASIC and CMUT chips. Therefore, pseudo-ASIC chips

and pseudo-CMUT chips, which are geometrical replicas of the ASIC and CMUT chips, are designed and fabricated to use them for flip-chip process development. The cost and psychological stress of flip-chip bonding process development is significantly decreased by using pseudo chips for unit process development without wasting very valuable real ASIC and real CMUT chips. Also, unique connections between bonding pads are designed to measure the electrical resistance of the structure after the flip-chip bonding process. Creating specific connections allows us to measure the resistance of the bonded structure and observe the success of the developed flip-chip bonding process. Chapter 2.2 describes details of the design and fabrication of pseudo chips.

Thermo-sonic flip-chip bonding uses gold stud bumps (GSBs) to integrate the chips. Chapter 2.3 describes the fabrication of the gold stud bumps. Fabrication of the gold stud bumps is optimized for 25.4 µm diameter gold wire and 17.5 µm diameter gold wire. The heights of the gold stud bumps show variations after the fabrication. These height variations can be detrimental to thermo-sonic flip-chip bonding. Also, the top surface of the gold stud bumps is not flat after the stud bump fabrication. Therefore, heights of the gold stud bumps must be equalized and surface areas of the gold stud bumps must be flattened by a process known as coining in the literature. In chapter 2.4, different than what has been proposed and done in the literature so far, a novel coining process called displacement-controlled coining process is developed and experimentally studied. An aluminum mold which contains an array of cavities with known and pre-defined depth values is designed to control bump deformation and displacement during the coining process. A double side polished and thick Borosilicate glass substrate is used as a flat surface which transfers the applied displacement-controlled deformation force to the stud bumps. The height and bonding surface area of the gold stud bumps can be tailored for flip-chip bonding processes. The proposed technique can be used to simultaneously coin arrays of stud bumps with high precision, providing an alternative, cost-effective, precise, time-efficient, R&D and mass fabrication suitable processing of stud bumps prior to FCB applications. The displacement-controlled coining is also compared to the traditional coining technique (force-controlled coining).

Chapter 2.5 describes thermo-sonic flip-chip bonding (TSFCB) process developments via pseudo chips. A heat energy transfer-based novel analytical model, which is based on lumped-capacitance model, is developed for the thermo-sonic flip-chip bonding process. The analytical model shows that when the interface temperature (temperature between the flat top surface of the gold stud bump and the bonding pad) reaches 46-70 % of the melting temperature of the gold, 100 % conductive flip-chip bonded structures can be obtained. Using this model, GSBs fabricated with both 25.4 µm and 17.5 µm gold wire are experimentally successfully bonded.

To increase the interface temperature, ultrasonic time and ultrasonic power parameters are more significant than the process temperature ($T_{process}$). $T_{process}$ comes from the heated stage of the flip-chip bonder located beneath the substrate chip (in our case, the CMUT chip). Thus, although the process temperature is decreased to room temperature, successful flip-chip bonding is performed by compensating the temperature loss by the ultrasonic time and the ultrasonic power. The analytical model shows and experimentally proves that thermo-sonic flip-chip bonding at room temperature is possible. Successful TSB trials are completed in this study at process temperatures of 24 °C, 25 °C, 40 °C, 150 °C, and 375 °C. The developed model can calculate the interface temperature (T_{int}) and estimate process parameters prior to the TSFCB process. The process parameters can be adjusted depending on the desired process temperature, the mass and specific heat capacity of GBSs, the amount of ultrasonic energy, and the amount of ultrasonic time. Furthermore, a mechanical deformation model from the literature is integrated with the developed analytical model to calculate the deformation of the gold stud bumps during the thermo-sonic flip-chip bonding process. Using the mechanical deformation model and the developed process model together can estimate bump deformation during the TSB processes with less than 2 µm accuracy.

Thermo-sonic flip-chip bonding of real ASIC chips to a real CMUT chip is described in Chapter 2.5.3. Underfilling process for a flip-chip bonded structure is proposed. Parylene C coating of the ASIC-CMUT flip-chip bonded structure is proposed. The underfilling process and Parylene C coating process are described

in Chapter 2.5.4.

CMUT-PCB integration is described in Chapter 2.6. Stacked gold stud bumps and isotropic conductive adhesive is selected for the integration of CMUT and PCB. The selected flip-chip bonding technique allows the integration of CMUT and PCB at low temperatures and low bonding force. Chapter 2.6 starts by describing the design and fabrication of the PCB. A pseudo PCB which is a geometrical replica of the real PCB, is designed and fabricated to decrease the flip-chip process development cost. Afterward, the flip-chip bonding process design for CMUT-PCB integration is discussed. Selection criteria, characterization, and application of the isotropic conductive adhesive material are proposed. Fabrication of the stacked gold stud bumps and coining of the stacked gold stud bumps are optimized and described. Flip-chip bonding trial is presented using a pseudo-PCB and pseudo-CMUT. The flip-chip bonding process of a real CMUT and a real PCB is then presented.

Chapter 2.7 presents the soldering of the PCB components and wire bonding of the device layer-PCB ground connection. A prototype PCB is fabricated to control the alignment of the component and position inside the probe before the real PCB fabrication. Time-pressure dispenser tool is introduced. Soldering material and the soldering station are also presented. Components of the PCB are given, and the soldering process is described. Wire bonding of the device layer-PCB ground connection is optimized and proposed.

Chapter 2.8 starts by describing the design and fabrication of the probe. A test probe is assembled using a pseudo-ASIC pseudo-CMUT flip-chip bonded structure and a test PCB. The effects of the forces generated during the test probe assembly on the FCB structure were investigated. The water tightness of the probe was also tested by assembling the test structure. Finally, the assembly of the real probe is presented.

Chapter 2

Fabrication Process

2.1 Design Considerations of ASIC-CMUT Flip-Chip Bonding (FCB)

There are three 1^{st} level interconnection techniques used for IC/MEMS packaging. Wire bonding, Tape-automated bonding (TAB), and flip-chip bonding (FCB) [9]. Wire bonding is still dominant technique used for the packaging of IC/MEMS due to established infrastructure and low-cost substrate availability. However, as functionality of chips is increasing and total foot-print area is decreasing, FCB becomes preferred technique due to area array I/O pad design ability and smaller foot-print packaging capability [10].

Variety of bumping techniques are developed for FCB. Solder bumping, and stud bump bonding (SBB) are two of these varieties. Solder bumping is the main technique used today for FCB packaging. Solder bumping uses solder material as interconnect materials between chips. At the beginning, lead based solder materials were used, but high reflow temperatures (i.e. over 300 °C) were too high for most of the materials used in IC/MEMS packaging and therefore ceramic based materials could only be used. Later, eutectic solder (reflow temperature 220 °C) materials are developed as interconnect materials to decrease reflow temperatures

and to utilize organic substrates for FCB packaging [11].

SBB is the second bumping technique. Gold and copper bumps are fabricated by modifying process sub-steps of the wire bonding process. Wire bonding wires are cut when the first ball is bonded and mushroom-like shaped bumps are fabricated on each bonding pad one by one [12]. Thermo-compression FCB (TCB) process and thermo-sonic FCB (TSFCB) process are used to integrate chips by SBB. There are some advantages of SBB over solder bumping listed below.

I. Lower set-up cost and process cost: The infrastructure is the same with wire bonding infrastructure and is already available. No additional equipment is needed. Less process steps and faster work-in-progress [13] is possible.

II. Finer pitch bonding (less than 100 µm) [14].

III. Ability to bump individual dies makes it helpful for R&D purposes and MEMS studies [15, 16].

IV. No need for under bump metallization (UBM). Variety of bonding pad material can be used (i.e. Au and Al). Eliminates gold pad dissolution [15, 17, 18].

V. Higher electrical conductivity and more reliable metallurgical joining [16, 19].

VI. Using Lower process parameters (time, pressure, temperature) and eliminating contamination (no flux requirement) are possible [18, 19].

Due to these advantages, SBB FCB process is extremely helpful for high energy physics (HEP) detectors R&D studies [20], MEMS, MOEMS, and surface acoustic wave (SAW) studies [14], chip-on-glass display applications, prototyping of multi-chip modules (MCMs), optoelectronic studies, low cost FCB packaging [18], and system in package (SIP) applications [17]. Moreover, the thermo-sonic flip-chip bonding (TSFCB) process is preferred for flexible substrates due to low temperature processing [21, 22]. Currently, SBB is also used for mass production regularly [23].

TCB uses force and temperature and TSFCB uses force, temperature and ultrasonic energy to integrate chips [17]. There is also ultrasonic FCB (USB) which uses force and ultrasonic energy to integrate chips [24]. Gold stud bump (GSB) studies show that 250 °C – 350 °C temperature is needed for TCB [25], around 150 °C temperature is needed for TSFCB [26] and room temperature to 150 °C for USB [27]. TSFCB contains USB and hereafter TSFCB will be used to mean on FCB process with ultrasonic energy. TSFCB is mostly preferred over TCB due to desired lower temperature processing [28], low bonding forces, and ability to work with non-rigid substrates [29]. GSB is the most common used bump material for TSFCB.

Longitudinal and transverse application of ultrasonic vibration are the two techniques used in TSFCB. Ultrasonic vibration is applied vertical to the bonding interface at longitudinal TSFCB and is applied parallel to the bonding interface at transverse TSFCB. Tomioka et al. concluded that longitudinal TSFCB creates stronger bonding than transverse TSFCB [30]. Also, longitudinal TSFCB offers better die collet co-planarity than transverse TSFCB [31]. However, longitudinal TSFCB may damage the chips by applying too much ultrasonic energy and this is known as hammering effect [32]. Thus, amount of ultrasonic energy must be controlled carefully when working with longitudinal TSFCB and sufficient co-planarity must be ensured when working with transverse TSFCB.

TSFCB is a solid-state bonding technique that enable the advantages listed above [33]. Therefore, many efforts have been put into optimization and modelling of the process. Staiculescu et al. conducted a design of experiments (DOE) study for GSB TSFCB process and they concluded that substrate thickness between 250 µm - 635 µm is insignificant [34]. Hizukuri et al. investigated the strain and chip damage during the USB process and they concluded that by applying sufficient bonding force, average strain on the bumps becomes more compressive which avoids chip damaging [35].

Wang et al. studied the effects of ultrasonic power, ultrasonic time, and bonding force on the TSFCB process. They concluded that bonding strength is increased with increased ultrasonic power (up to 3.5 W) and time (up to 200 ms),

but bonding strength is decreased with excessive ultrasonic power and excessive ultrasonic time. Only moderate ultrasonic energy should be used to obtain high bonding strength. They also concluded that moderate bonding force (up to 360 g/bump) increases bonding strength but excessive bonding force decreases the bonding strength [36]. Luu et al. concluded that successful bonding at 50 °C is obtained for TSFCB process with GSBs [37].

Wang et al. created a dynamic finite element model of the TSFCB process to optimize. They concluded that moderate bonding force (80 g/bump), moderate ultrasonic amplitude (1 µm) is needed to obtain high bonding strength. They also accepted a bonding interface temperature of 600 °C instead of a temperature of 160 °C used for the study to accommodate heating effects of the ultrasonic energy. They used a constitutive relation equation which will also be discussed in this study [38].

Ultrasonic energy effects on the bonding interface are not fully understood and are still a research topic. Li et al. concluded that ultrasonic energy increases dislocation density at the bonding interface. Dislocations promote atom diffusion by increased dislocation lines which lead a metallurgical bonding [39]. Kang et al. studied acoustic softening effect created by ultrasonic energy during the TSFCB process. The conclusion is that ultrasonic energy creates similar microstructural effects with heating. They achieved successful bonding at 180 °C [40].

Huang et al. studied GSB formation via 3-D finite element model. They concluded that bonding pressure is the most effective process parameter to create bonding. Another conclusion is that increasing height of the GSB leads to a more reliable bonding [41].

McLaren et al. developed a computer model to control the TSFCB process. They concluded that co-planarity of the die collet is an important factor for reliable bonding. Leveling the height of the GSBs via a coining process was not employed and deformation variation was observed between the bumps which can lead to unsuccessful bonding [42].

Lawyer et al. optimized TSFCB process. They concluded that with introducing ultrasonic energy, bonding force and bonding temperature can be decreased. When optimum bonding force and ultrasonic energy is applied, contact area can be increased to 100 %. 120 g/bump, 8 W and 200 ms bonding parameters were found to be optimum between Au-Au [43].

Chuang et al. investigated effects of the bonding parameters for TSFCB process. They concluded that bonding strength and contact area increases with increasing ultrasonic power and bonding force. 40 g/bump bonding force is insufficient to create bonding. Thus, bonding force ensures the contact between GSB and bonding pad during the TSFCB [44]. Rohwer et al. concluded that the TSFCB process is possible at 150 °C temperature with 20 N bond force via GSB and gold bonding pad [26].

Wang et al. created a finite element model of the TSFCB process. They concluded that at 160 °C bonding temperature, it is possible to obtain good bonding by applying 2 W ultrasonic power, 100 ms ultrasonic time, and 30 g/bump bond force. However, when ultrasonic power is increased to 2.2 W, over bonding is observed [45]. Jun-hui et al. suggested that ultrasonic power that is more than 5 W results in slippage and rotation problems. Ultrasonic power between 1 W – 5 W should be used to obtain reliable TSFCB bonding [46].

In Ref [47], a model of the plane strain for the GSB TSFCB process was developed. Interface slip was increased by ultrasonic energy and the bonding interface was heated up, which created bonding. The friction coefficient was found to be 0.347 for 392 MPa bonding force and 200 °C bonding temperature.

It is understood from these studies that optimization and modelling of TSFCB is highly critical for reliable bonding. In this thesis study, a novel heat energy transfer based analytical model is developed for the TSFCB process and the developed model is studied experimentally for GSBs fabricated via both 25.4 µm and 17.5 µm gold wires on gold bonding pads. Bonding interface temperature (T_{int}) is calculated analytically from applied ultrasonic energy and applied temperature during the TSFCB process. The TSFCB process was successfully performed at

temperatures from room temperature to 375 °C with the parameters calculated by the developed analytical model. Effects of bonding force and pressure are discussed and amount of deformation is calculated by combining the analytical model and constitutive relation equations developed for gold wire bonding wires [48]. Optical microscope imaging was used to observe misalignment and SEM imaging was used to observe the FCB structures after the TSFCB processes. The 2-probe resistivity measurement technique was used for measuring the resistance of the FCB structures after the TSFCB processes.

2.2 Design and Fabrication of Pseudo Chips

In this thesis study, using microfabrication techniques, pseudo-ASIC chips, and pseudo-CMUT chips, which are cheaper geometrical replicas of the real ASIC chips and real CMUT chips, are designed and microfabricated for development and modelling of the TSFCB process to reduce the process development costs and to confirm the validity of the developed processes.

There are two kinds of pseudo-ASIC chips used in this study. One pseudo-ASIC chip group is made of Pyrex (7740) substrate with 500 µm ± 25 µm thickness and the other pseudo-ASIC chip group is made of silicon substrate with 500 µm ± 25 µm thickness, that also has 300 nm thick silicon nitride deposited on the silicon substrate surface. The pseudo-ASIC chip has 143 bonding pads. Dimensions of the pseudo-ASIC chip are 6.17 mm x 1.43 mm x 0.5 mm (thickness) (**Fig. 2.1a**). The pseudo-CMUT chip, only made of Pyrex material, is the substrate with 16.75 mm x 16.75 mm x 0.5 mm (thickness) dimensions (**Fig. 2.1a**). Dimensions of the bonding pads are 90 x 90 µm with 130 µm pitch distance for both the pseudo-ASIC chips and the pseudo-CMUT chips.

Followed wafer-scale microfabrication approach for Pyrex type pseudo-ASIC chips, Pyrex type pseudo-CMUT chips and silicon type pseudo-ASIC chips are the same. The microfabrication of all of the pseudo-chips starts with spin coating of HMDS adhesion layer (MicroChemicals GmbH). The wafers are put on a hot plate for 30 mins at 150 °C. Spin coating of 2 µm thick AZ5214E image reversal photoresist (MicroChemicals GmbH) on the wafer surfaces is performed after. UV exposure with a photomask is completed by applying a 45 mJ/cm^2 dose. Exposed wafers are put on the hot plate for reversal bake for 2 minutes at 120 °C. A flood exposure is performed without any photomask by applying 250 mJ/cm^2 dose. Exposed wafers are put in DI water diluted AZ400K developer solution (MicroChemicals GmbH) for approximately 2 minutes (**Fig. 2.1b**). Wafers that have developed photoresist after photolithography steps are transferred into inductively coupled plasma (ICP) equipment chamber to process by oxygen plasma for 15 seconds to remove photoresist residuals from the photoresist

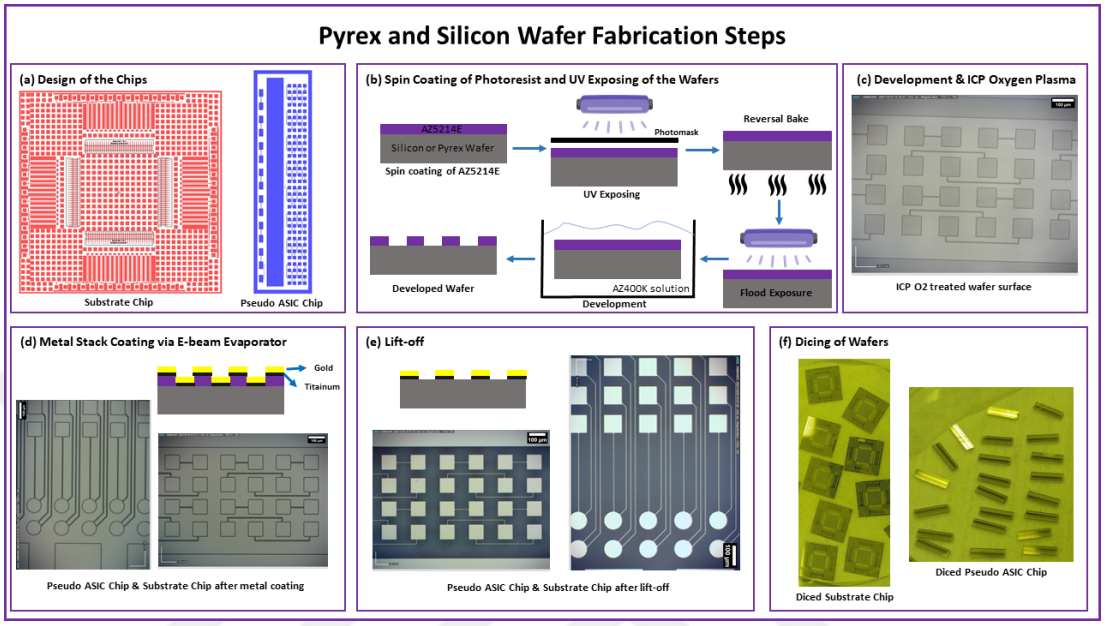


Figure 2.1: Design and fabrication of the pseudo-ASIC chips and the pseudo-CMUT chips.

developed regions, if any (**Fig. 2.1c**).

A metal stack of 100 nm titanium and 500 nm gold is deposited by e-beam evaporation process as wires, bonding pads, and touch pads, for electrical measurements (**Fig. 2.1d**). Thickness of the bonding pads are critical both for GSB fabrication by stud bump bonding, and for the TSFCB process. Tomioka et al. investigated the effects of the substrate bonding pad plating thickness on die-shear strength. They used gold material for bonding pads and concluded that die-shear strength increases with increasing gold plating thickness until 910 nm. Beyond 910 nm thickness, die-shear strength is saturated [49]. Kang et al. used a metal stack of 20 nm titanium and 600 nm gold for their study on the TSFCB process [50]. Therefore, the metal stack used in this study is suitable for the TSFCB process and is sufficient to obtain good bonding while keeping the cost low. After metal deposition, lift-off process is completed by putting and keeping wafers in pure acetone for long enough time to remove the photoresist and metal stack on photoresist mask, completely (**Fig. 2.1e**). Finally, dicing saw processing is used to dice the wafers into chips as shown in **Fig. 2.1f**.

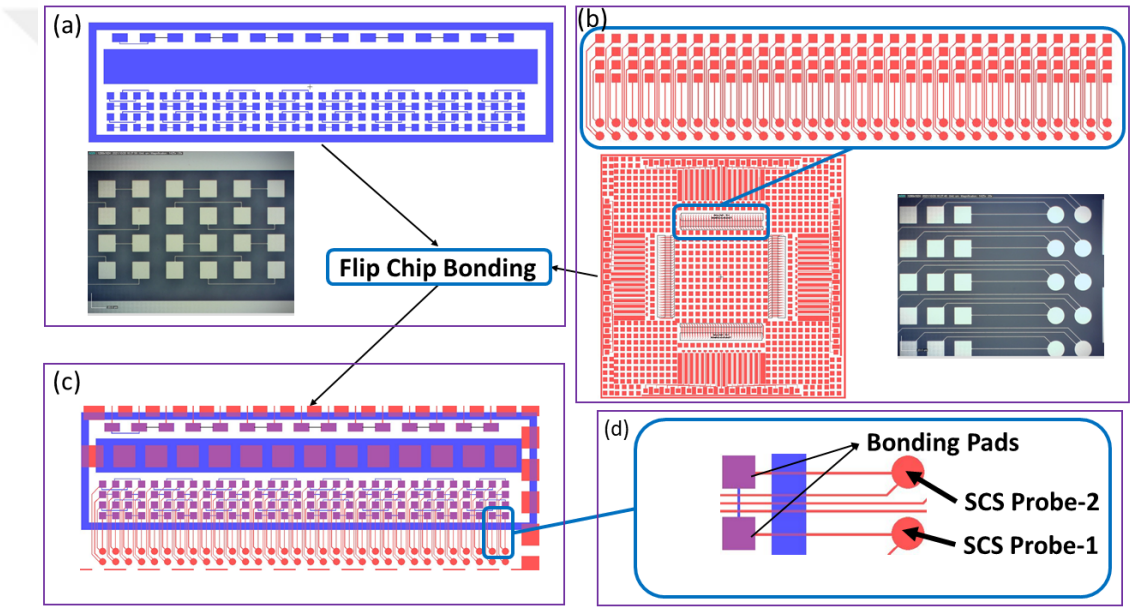


Figure 2.2: Design of the pseudo-ASIC chip and the pseudo-CMUT chip and 2-probe measurement technique that is used for this study. (a) Design of the pseudo-ASIC chip and partial view from the array of bonding pads of the pseudo-ASIC chip, (b) Design of the pseudo-CMUT chip, design of the bonding pads of the pseudo-CMUT chip and partial view from the array of bonding pads of the pseudo-CMUT chip, (c) Aligned pseudo-ASIC chip on the pseudo-CMUT chip after the FCB process, (d) 2-probe measurement method to measure resistances of the GSBs.

To form bonds between pseudo-ASIC chips and pseudo-CMUT chips, TSFCB process is used. A semiconductor characterization system (KEITHLEY 4200-SCS) is used to measure electrical resistance of the bonded regions after the TSFCB process using the 2-probe resistivity method. To be able to measure the conductivity of the bonded regions, specific connections are designed between bonding pads of the pseudo-ASIC chip (**Fig. 2.2a**) and bonding pads of the pseudo-CMUT chip (**Fig. 2.2b**). Probes of the semiconductor characterization system are in contact with corresponding circle features on the pseudo-CMUT chip as shown in **Fig. 2.2d**. Electrical resistance of the bonded regions are measured after TSFCB trials. Since the 2-probe measurement method (rather than 4-probe measurement method) is used, probe resistances and wire resistances are also included in the measurement results.

2.3 Fabrication of Gold Stud Bumps (GSBs)

GSBs are fabricated using 25.4 µm gold wire (Heraeus Au HA3) for some pseudo-ASIC chips and 17.5 µm gold wire (Heraeus Au HA3) for other chips. This thesis study uses a TPT HB16 semiautomatic wire bonder machine (TPT Wire Bonder GmbH & Co KG) to fabricate GSB. The parameters of the fabrication of the GSBs are given in **Table 2.1** for both wire types. GSBs are fabricated via the stud bump bonding process. The process starts with selecting a suitable capillary tool according to the gold wire chosen (**Table 2.1**). Electronic flame-off (EFO) is used to create a free-air ball (FAB) at the edge of the capillary tool. A capillary tool with a FAB at the tip of the capillary tool is pressed against a bonding pad on a chip to bond FAB to the bonding pad. During the **bond1** step, a known amount of ultrasonic energy (i.e. ultrasonic energy = ultrasonic power x ultrasonic time) is applied to locally heat the contact sides of FAB and bonding pad for the bonding to happen between FAB and bonding pad, while the chip containing the bonding pads is kept preheated at a predefined temperature to help the interface bonding between contact sides of FAB and the bonding pad (**Fig. 2.3a**). After the **bond1** step is completed, the capillary tool moves up according to the **loop z** direction (**Fig. 2.3b**) and then moves in the y direction according to the **loop y** direction (**Fig. 2.3c**). During the **bond2** step, a predetermined amount of force is applied, and the gold wire is compressed between the capillary tool and the gold ball (**Fig. 2.3d**). **Bond2** deforms the gold wire that is attached to the gold ball. Capillary moves up and breaks the gold wire at a region within the heat-affected zone (HAZ) (**Fig. 2.3e**). Thus, a GSB is created on the bonding pad with a mushroom-like shape with a sharp tail (**Fig. 2.3f**). This entire process is repeated as many times as needed to form the needed amount of gold stud bumps [12].

The anatomy of a GSB is shown in **Fig. 2.3g**. Since the gold wire breaks within the HAZ region, GSBs have variable tail lengths. To eliminate the varying tail lengths and sharp tails, a process called "coining" is necessary before the flip-chip bonding. Details of the coining process will be discussed in Chapter 2.4.

	17.5 µm Gold Wire		25.4 µm Gold Wire	
	Bond1	**Bond2**	**Bond1**	**Bond2**
Ultrasonic Power (mW)	200	0	200	0
Ultrasonic Time (ms)	200	30	200	30
Force (mN)	250	5	250	5
Temperature (°C)	120	120	120	120
EFO (%)	40	N/A	40	N/A
UPCO (µm)	N/A	400	N/A	375
Loop z-axis (µm)	120	N/A	120	N/A
Loop y-axis (µm)	20	N/A	50	N/A
Capillary Tip	SPT - SBB-23090		SPT - UTS-35FE	

Table 2.1: SBB process parameters for 17.5 µm and 25.4 µm gold wire.

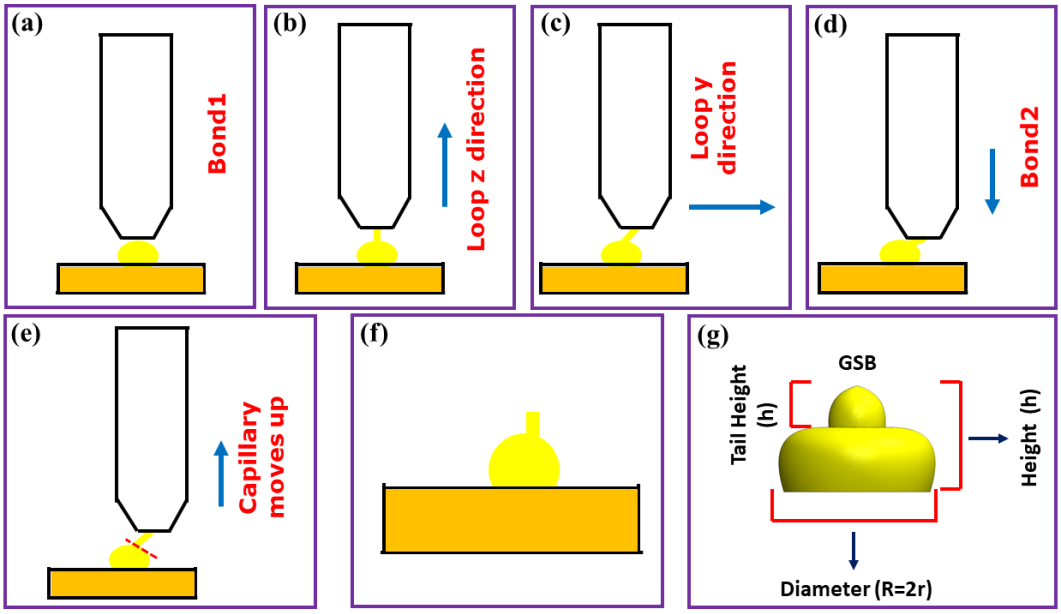


Figure 2.3: Fabrication steps of a GSB. (a) Step-1: Performing bond1, (b) Step-2: Performing loop z direction, (c) Step-3: Performing loop y direction, (d) Step-4: Performing bond2, (e) Step-5: Capillary tool moves up, (f) Fabricated GSB, (g) Anatomy of a GSB.

2.4 Displacement-Controlled Coining (DCC) Process

There are a variety of bumps used on chips for FCB and TAB applications. GSB is one of these varieties. Currently, GSB is used at production stage regularly [23].

GSBs are fabricated by a modified wire bonding process. Stud bump fabrication via a wire bonder offers an economical and reliable bumping method for FCB applications. Also, it is very suitable for research and development studies because researchers may need to change the design of substrates and stud bump dimensions any time [51].

Due to the ultrasonic welding process during stud bump formation, heat affected zone (HAZ) occurs in the wire at a region of the wire that is close to the FAB. Upward motion of the capillary tool breaks the wire randomly from a region within HAZ. Therefore, GSBs have variable tail lengths after the stud bumping process. Variable tail length with large standard deviation is not suitable for FCB and TAB applications because large height differences between tails of GSBs can lead to unsuccessful bonding due to uneven distribution of pressure per stud bump, which causes misalignment during FCB and TAB processes. To minimize the deviation in the variable tail length, the upward motion of the capillary tool during breaking the wire and ball connection may be done in a specified upward motion trajectory. Furthermore, a flat surface on top of the GSB is preferred for reliable bonding. A process called "coining" is used for leveling heights of the GSBs. According to the literature, height level variations of ± 5 µm or less may be required for reliable FCB and TAB applications [16]. Considering that more than two decades of time has passed since the publication of the information in reference [16] and there are significant technological advancements in the FCB process needs, we should be able to state that the FCB, and coining requirements are getting stricter, including the requirements for minimal height level variations.

Usually, a polished and flat plate with uniform thickness, made of glass, silicon, or ceramic is used for the coining process, and around 1 N/bump force is applied to level GSBs [20, 30, 52, 53]. Also, flip chip bonders can be used for the coining process [54, 55]. GSBs are used in applications of thermo-sonic FCB [13, 14, 21, 30, 34, 36, 38, 40, 44, 45, 49], thermo-compression FCB [25, 56], and conductive adhesive FCB [55, 57]. Coining process equalizes heights of the GSBs, and creates flat surfaces with uniform surface areas on top of the GSBs. The flat surface areas for GSBs are especially a critical requirement in conductive adhesive FCB applications such as anisotropic conductive adhesive (ACA), and dip coating isotropic conductive adhesive (ICA). Therefore, studies on conductive adhesive FCB have also been focused on the coining process [17, 58, 59, 60].

To perform the coining process, different than what has been proposed and done in the literature so far, a displacement-controlled coining (DCC) process is developed for GSB arrays. Furthermore, for thermo-sonic FCB applications, using the tail height regions of the GSB for compressive pressure adjustments by DCC, is also implemented. An aluminum rigid mold which contains an array of cavities with controlled depth values is designed and manufactured to control the displacement of deformation during the coining process. Moreover, a double side polished, relatively thick (3.3 mm) Borosilicate glass is used as a flat surface which transfers applied displacement and force to the stud bumps.

GSBs are fabricated via stud bump bonding process that is explained in detail in Chapter 2.3. For DCC process trials, GSBs fabricated by 25.4 µm diameter gold wire (Au-HA 3) from Heraeus is used. 143 GSBs with 75 µm to 83 µm diameters and 50 µm to 60 µm ball heights are fabricated for every pseudo-ASIC chip.

Coining process is required before the FCB processes to flatten the contact surface, and nominally equalize the heights, of the GSBs. As aforementioned, around 1 N/stud bump has been recommended for the coining process in the published literature. This recommendation suggests that 143 N of force is needed for coining the GSBs on the pseudo ASIC chips. However, flip chip bonder used in this study (Fineplacer Matrix Ma, Finetech GmbH) is capable of applying force

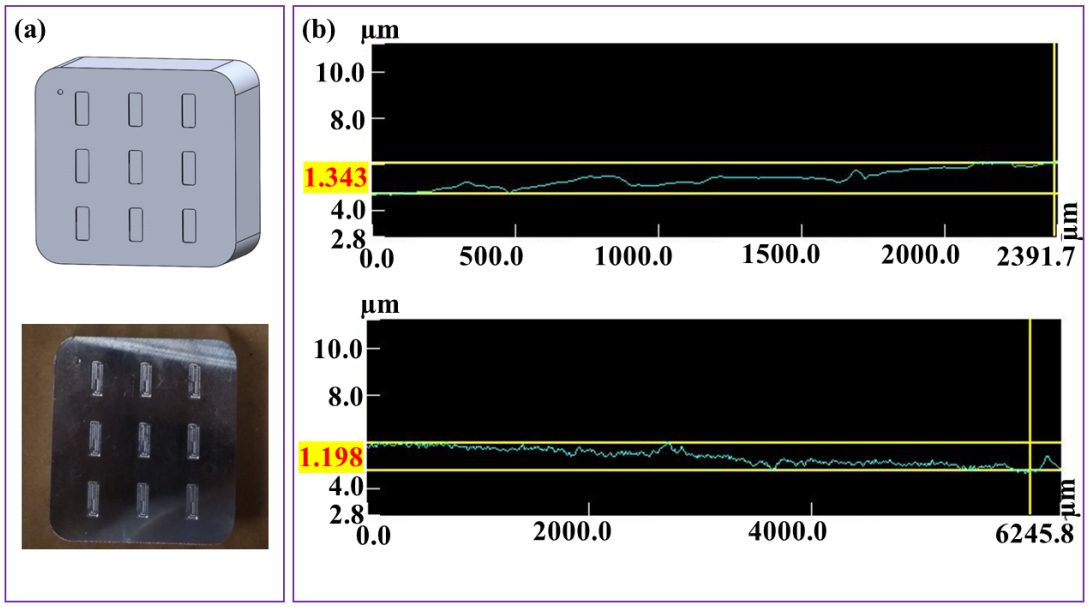


Figure 2.4: The aluminum mold. (a) Design of the aluminum mold and fabricated aluminum mold, (b) Laterally on the left and longitudinally on the right, parallelism measurement between cavity bottom surface and mold top surface.

values only up to 20 N. Thus, another novel solution was needed for coining of the GSBs before FCB processes.

2.4.1 Aluminum Mold Design & Fabrication

An aluminum mold with 3x3 array of 9 mold cavities is designed and manufactured as shown in **Fig. 2.4a**. By design, each mold cavity in the array has a defined depth value. The aluminum mold cavity with known depth is used as a nest for the pseudo ASIC chip and also is used for displacement-controlled deformation of GSBs on the pseudo ASIC chips during the coining process. Dimensions of the rigid molds are 40 mm x 40 mm x 20 mm, where 20 mm is the thickness of the mold. Width and length dimensions of the rigid mold cavities are 6.80 mm x 2.65 mm with 0.5 mm radius curves at the corners. The aluminum mold is fabricated by CNC milling (HSC 55 CNC Milling Machine, DMG MORI) process.

Designed depth values of the 9 mold cavities are 515 µm, 520 µm, 525 µm, 530 µm, 535 µm, 540 µm, 545 µm, 550 µm, and 560 µm, respectively. Furthermore, after CNC milling manufacturing, confocal microscope (Keyence VKX-100) measured depth values of the 9 mold cavities are 515 µm, 516 µm, 525 µm, 528 µm, 534 µm, 545 µm, 547 µm, 550 µm, and 558 µm, respectively. Here, it is very important to emphasize that 5 µm depth movement is a more sensitive value than the movement resolution limits of the CNC milling machine that is used for the fabrication of the aluminum molds. Therefore, due to the CNC movement resolution limits, some cavities have different measured depth values than designed depth values.

After determining the actual depth of each mold cavity with depth measurement capability of a confocal microscope (i.e. Keyence VKX-100) or a surface profilometer, one can use any mold cavity that is known to have the appropriate depth value for the coining process. Parallelism between cavity bottom surface and mold top surface is measured. The parallelism measurement is performed by accepting the profile of the mold top surface as a flat reference. The deviation is then measured on the cavity bottom surface with a confocal microscope (Keyence VKX-100). The average deviation between the parallelism of the cavity bottom surface and the mold top surface, as measured longitudinally and laterally, are 1.198 µm, and 1.343 µm, respectively (**Fig. 2.4b**). Furthermore, CNC milling machines with higher movement resolution and higher precision may be employed for studies that may need higher precision for height values of the coined stud bumps.

Since pseudo-ASIC chips have approximately 500 µm thickness values, expected GSB heights after the coining process are approximately 15 µm, 16 µm, 25 µm, 28 µm, 34 µm, 45 µm, 47 µm, 50 µm, and 58 µm, respectively. Furthermore, usually, 4-inch diameter wafers are produced with a ± 25 µm thickness variation. This is the usual thickness variation value given by the wafer manufacturers or wafer suppliers when wafers are purchased from wafer manufacturers or wafer suppliers. However, based on our personal experience, the actual measured wafer thickness variations are usually less than ± 5 µm across the same Si wafer. Hence, chips fabricated from the same wafer, may have different thickness values



Figure 2.5: 3.30 mm thick, Borosilicate glass.

within ± 5 µm variation. On the other side, different wafers can have different thickness values within ± 25 µm variation. One should measure the actual thickness of the chip before performing the coining process and select suitable mold cavity according to the measured thickness value. This way, even with different chip thickness, same bump height can be achieved by using DCC process.

2.4.2 Borosilicate Glass

Double side polished Borosilicate glass is used as a flat surface which is responsible for flattening of the coined surfaces of the GSBs by applying limited displacement to the stud bumps that are inside the mold cavities. An image of the Borosilicate glass is given in **Fig. 2.5**. Thickness of the Borosilicate glass is 3.30 mm. Thickness of the Borosilicate glass is important to have a high bending stiffness value to prevent undesired bending of the glass. High bending stiffness ensures that there will be limited or no bending on the Borosilicate glass during the coining process, depending on the magnitude of the applied uniformly distributed force.

2.4.3 Displacement-controlled coining (DCC) process steps

A pseudo-ASIC chip is placed inside an aluminum mold cavity (**Fig. 2.6a**). Depth of the mold cavity is selected based on desired height value for the GSBs. A pseudo ASIC chip with uncoined stud bumps is placed inside the nest. The Borosilicate glass is then placed on top of the aluminium mold (**Fig. 2.6b**). Another aluminum piece with the same dimensions and thickness as the first aluminum mold is placed on top of the Borosilicate glass. A cleanroom wiping tissue can be placed on top of the Borosilicate glass before placing the top aluminum piece to protect the Borosilicate glass from scratches. A compression force, the magnitude of which can be measured with a digital balance, is applied by human hand to the top of the aluminum piece to perform the first part of the coining process. Here, it is important to emphasize that, in order to minimize the coined stud bump height variations caused by the inclination of the mold cavity shown in **Fig. 2.4b**, the same pseudo-ASIC chip is removed from the mold cavity, rotated 180° (without being flipped upside down) with respect to its initial position, and replaced into the same mold cavity nest for the second part of the coining process. Then, the same compression force, the magnitude of which is again measured with the digital balance, is applied by human hand to the top of the aluminum piece to complete the second (which is also the last) part of the coining process (**Fig. 2.6c**).

In this approach, aluminum mold cavity depth is used as a displacement-controlled barrier during the coining of the stud bumps, and a safe nest for the pseudo-ASIC chip to prevent excessive deformation of the stud bumps and pseudo-ASIC chip. Borosilicate glass is used as a flat surface to ensure uniform deformation on the stud bumps, and co-planarity between Borosilicate glass surface and coined surfaces of stud bumps. Since the displacement of the Borosilicate glass is controlled (i.e. limited), GSBs are deformed to a defined height all together at the same time. Assuming that all the structures (i.e. aluminium molds, Borosilicate glass, pseudo ASIC chip) are rigid except the initial state of the prepared GSBs, final height of the GSBs are expected to become the same as height

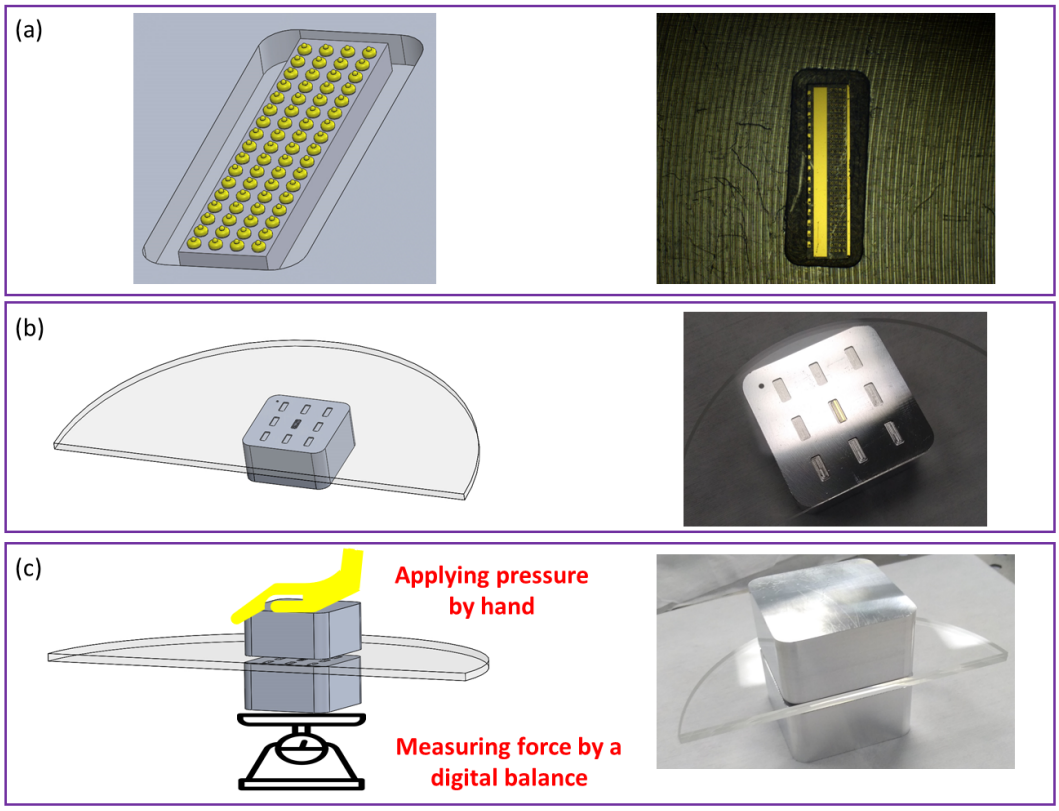


Figure 2.6: Steps of the DCC process, (a) Placing the pseudo-ASIC chip inside the selected mold cavity, (b) Placing the Borosilicate glass on top of the aluminum mold, (c) Placing another aluminum piece on top of the Borosilicate glass and application of compressive force to coin the GSBs.

of the mold cavity, after the coining process.

Although we do not need to measure with very high precision the compressive force that is deforming the GSBs, we approximately applied at least 1 N/bump force for GSBs made from 25.4 µm diameter wires. The mold, the Borosilicate glass, and the aluminum piece are put on a digital balance to track the applied compressive force during the coining process (**Fig. 2.6c**).

ImageJ software and image processing techniques are used to measure the height, tail height, diameter, and surface area of all 143 stud bumps in order to quantitatively evaluate the performance of the DCC process.

In order to obtain SEM images for geometrical measurements of the coined stud

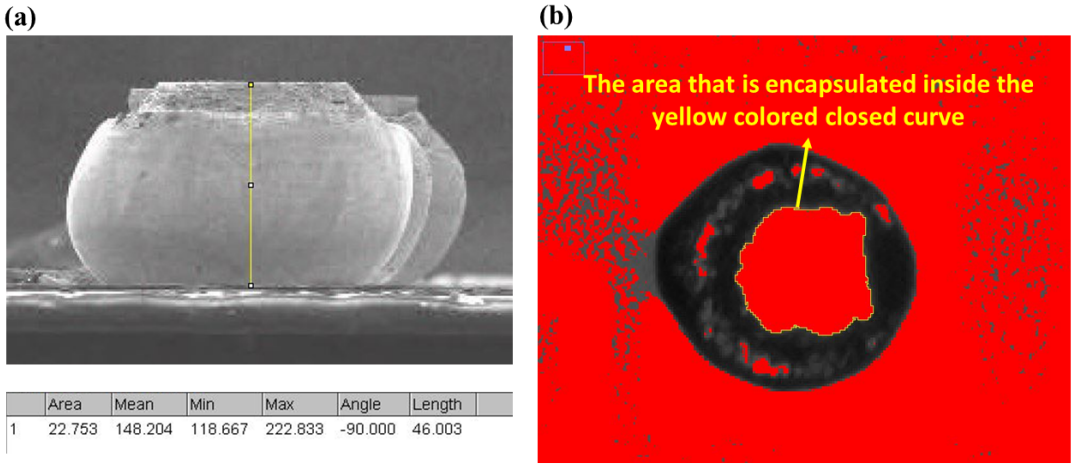


Figure 2.7: ImageJ measurements. (a) Measuring height of a GSB, (b) Measuring the surface area of a GSB by selecting the foreground pixel area encapsulated inside the yellow-colored closed curve.

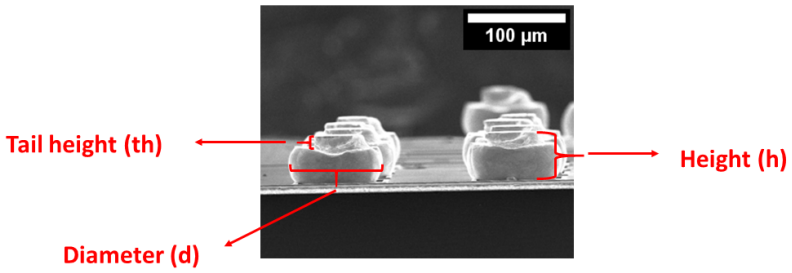
bumps, both before and after the coining process, individual pseudo-ASIC chips were placed horizontally on vertical SEM stubs. Vertical placement eliminates the measurement angle during SEM measurements. To use SEM images for geometrical measurements, ImageJ is employed to manually measure the height, tail height, and diameter of the GSBs (**Fig. 2.7a**). After DCC processes, optical microscope images of the coined surfaces of the samples were also taken. The images were converted to 8-bit format. Using ImageJ's threshold function, images were separated into pixels representing the foreground and the background. The surface areas on top of the GSBs were then calculated by selecting the foreground pixel regions (**Fig. 2.7b**).

2.4.4 Displacement-controlled coining (DCC) process trials

Initial GSB properties before the DCC process are given below in **Fig. 2.8b**. Initially, there are large variations of stud bump heights and tail heights of the GSBs due to the nature of the wire bonding process, because the wire is separated from the bonded ball randomly in the HAZ region after ball bump bonding (**Fig. 2.9c**). Mean standard deviation of GSB heights is 11.5 µm which is more than maximum allowable variance of 5 µm for FCB processes according to the literature [16]. Therefore, for our TSFCB application with 25.4 µm diameter gold wires, the coining process must be done on the stud bumps before the FCB process. 15 coining processes are tried with pseudo-ASIC chips. 2 of the coining processes are tried with 545 µm depth mold cavity, 3 of the coining processes are tried with 547 µm depth mold cavity, and 9 of the coining processes are tried with 550 µm depth mold cavity. Mold cavity depths are selected with respect to the initial GSB properties and desired GSB properties after the coining process. 143 N (1 N/bump) of compressive force is applied manually (**Fig. 2.6c**), for every coining trial.

Before the coining process, tail heights of the GSBs vary significantly due to breakage of the gold wire randomly within the HAZ during the wire bonding process. Sharp tails are observed after the wire bonding process in scanning electron microscope imaging (**Fig. 2.9c**). Standard deviations of the tail heights also vary significantly again due to breakage of the gold wire randomly within the HAZ during the wire bonding process. The tail parts of the GSBs seem in darker color before the coining process during optical microscope imaging because of the scattering of light in different directions. Coining process flattens tops of the tails. Coined tails of the GSBs seem in yellowish color during the optical microscope imaging (**Fig. 2.9c**) because of the flattened yellowish gold surface after coining process. Although heights and standard deviations of the tails still vary, values are limited to a narrower range. Furthermore, in this application, instead of the tail height values, total height values of the GSBs are critical for FCB processes. Therefore, mean height values of the GSBs are measured after each trial as shown

(a)



(b)

ASIC Chip	Mean Height Value (µm)	Mean Standard Deviation of Height (µm)	Mean Diameter Value (µm)	Mean Tail Height Value (µm)	Mean Standard Deviation of Tail Height (µm)
Pseudo ASIC	50 to 60	11.5	75 to 83	10 to 30	10.3

(c)

Trial	ASIC chip	Depth of MC (µm)	Mean h (µm)	SD h (µm)	Mean d (µm)	Mean th (µm)	SD th (µm)
1	Pseudo ASIC 1	545	46.6	0.814	78.1	13.5	4.799
2	Pseudo ASIC 2	547	48.8	0.909	81.5	12.2	2.82
3	Pseudo ASIC 3	547	47.1	2.28	75.8	10.8	3.102
4	Pseudo ASIC 4	550	52.4	0.986	82.4	16.4	1.778
5	Pseudo ASIC 5	550	51.9	0.656	79.5	14.2	1.422
6	Pseudo ASIC 6	550	52.1	0.737	81.2	16.2	3.715
7	Pseudo ASIC 7	550	50.0	1.008	81.8	13.8	2.033
8	Pseudo ASIC 8	550	50.2	1.135	80.4	13.7	5.52
9	Pseudo ASIC 9	550	49.8	1.018	83.5	13.7	5.587
10	Pseudo ASIC 10	550	50.8	0.809	82.6	14.3	4.377
11	Pseudo ASIC 11	547	47.6	1.096	78.5	11.5	1.906
12	Pseudo ASIC 12	545	46.1	0.797	77.7	13.5	3.541
13	Pseudo ASIC 13	550	49.7	1.382	78.3	14.9	3.843
14	Pseudo ASIC 14	550	49.8	1.733	81.0	16.1	2.964

Figure 2.8: Gold stud bump properties before and after the DCC process. (a) Anatomy of a coined gold stud bump, (b) Mean values of the GSBs before the DCC process, (c) Mean values of the GSBs after the FCFC process trials. h: Height, d: Diameter, th: Tail height, MC: Mold cavity, SD: Standard deviation

in **Fig. 2.8c** and plotted in **Fig. 2.9a**. Trial-15 is performed with 547 µm mold cavity and a silicon wafer is used as a flat surface. Details of trial-15 is given on page 32.

After the coining process is initiated, once the surface of the aluminum mold is in contact with the Borosilicate glass, the movement of the Borosilicate glass stops. Thus, displacement of the Borosilicate glass is controlled and the GSBs are deformed to the same height of the mold cavity depth. Moreover, standard deviations of height of the GSBs are important to examine the suitability of the GSBs for the FCB processes after the coining process. Standard deviation values are low enough to be suitable for the FCB process used in this application.

Another important point is that, the surface areas of the coined tails of the GSBs are narrower than the coined surface areas in the "body" part of the GSBs, if the coining process is completed in the tail height part of the ball bumps.

Due to the relation between pressure, force, and surface area (P=F/A), when the surface area, A, of the coined surface is narrower, the total pressure, P, value at the coined surface area increases for the same amount of applied force, F, value during the FCB process.

Furthermore, pressure per bump value increases even for the same force per bump value during the FCB process by utilizing smaller surface areas for coined surfaces (i.e. in the tail region of the ball bump).

Pressure per bump value is a more descriptive process parameter for FCB processes, compared to force per bump value, since the total pressure, P_t, value that is applied to the coined total bonding interface area, A_t, can significantly change for the same total force, F_t, value depending on the available total surface area (i.e. bonding interface area), A_t, value.

Since the total amount of coined surface area can be controlled by the DCC process, the total surface area of the GSBs (especially at the tail part of the stud bumps) can also be manipulated to increase or decrease the total pressure value needed for successful FCB processes.

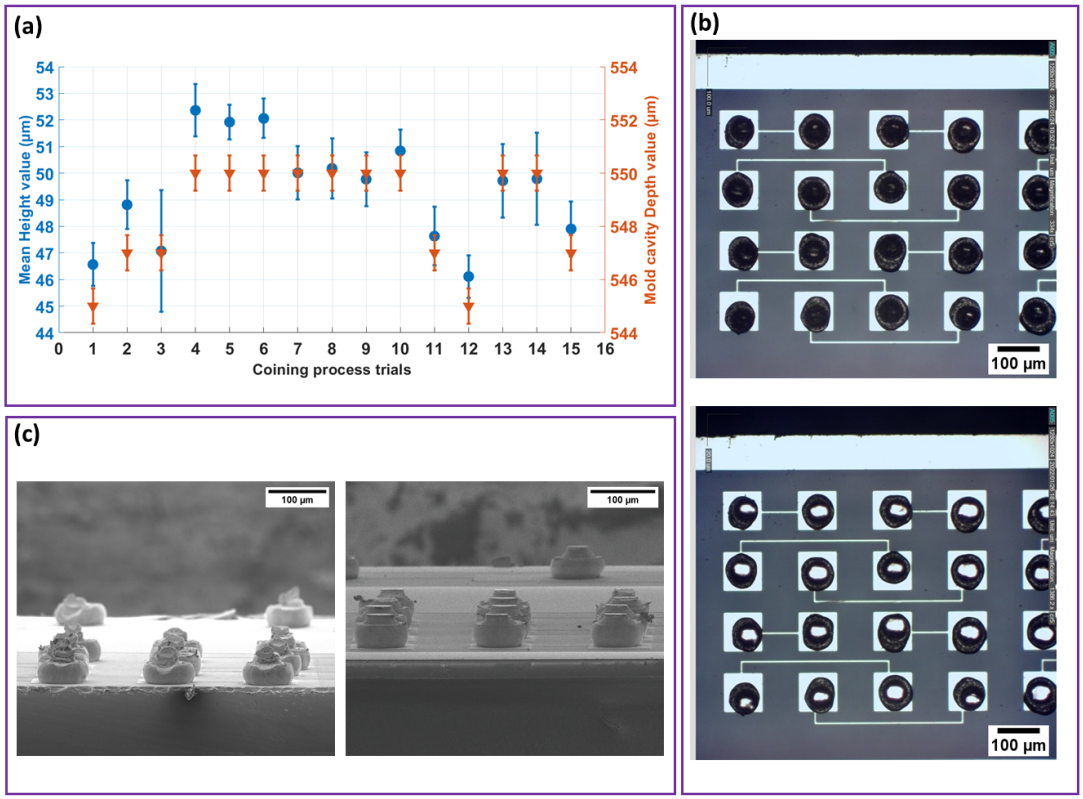


Figure 2.9: Results of the DCC process. (a) Mean height values of the GSBs and standard deviation of the height values of the GSBs after the DCC process (the y-axis on the right indicates the mold cavities with orange triangle markers.), (b) Optical microscope images of the pseudo-ASIC chip before and after the DCC process, (c) Scanning electron microscope images of the pseudo-ASIC chip before and after the DCC process.

For example, one can use a deeper mold cavity to deform the GSB surface areas for less for smaller surface areas at the tail regions after coining. Thus, pressure per bump value during the FCB process will be higher for the same amount of applied force.

To demonstrate our capability of manipulating the coined surface areas starting from tail region to the body region of the stud bumps, a test chip is coined within 550 µm, 540 µm, and 530 µm deep mold cavities, as shown in **Fig. 2.10b**. Pressure per bump values that would be applied at the FCB interface, and average surface area per bump values that would be used as bonding interface during the FCB processes are calculated after each coining process with respect to 19 N force value for 143 bumps that may be applied during a FCB process. As can be seen in **Fig. 2.10a**, pressure per bump value that can be applied during FCB process significantly decreases (from left to right in the graph) when larger coined surface area values are obtained by working with shorter mold cavities.

Thermo-sonic FCB (TSFCB) processes have been used to integrate pseudo-ASIC chips to pseudo-CMUT chips after the DCC process. 1 W to 3 W ultrasonic power range, 0.9 s to 1.2 s ultrasonic time range, 24 °C to 375 °C temperature range, and 19 N fixed force process parameters are used for the trials. Details of the TSFCB process is proposed in Chapter 2.5. Electrical connectivity and mechanical connectivity of the bumps have been measured via the 2-probe resistance measurement method described in Chapter 2.1., and as shown in **Fig. 2.2d**. 100 % successful electrical connectivity results have been obtained for multiple FCB process trials (**Fig. 2.11a** & **Table A.1**). The 2-probe resistance measurement method used in our measurements, results in somewhat high standard deviations for measured resistance values. We believe that there are four major components in these standard deviations. We believe that the first part of this variation is due to using 2-probe resistance measurement method, while the second part of the variation may be coming from having different lengths (hence, resistances) for different electrical measurement paths passing through the bonded interfaces [61]. A third possible reason for the variation between the resistances may be due to the initial variation in the surface areas of individual coined surfaces (i.e. variation from coin to coin) before the FCB process is actually done. A fourth

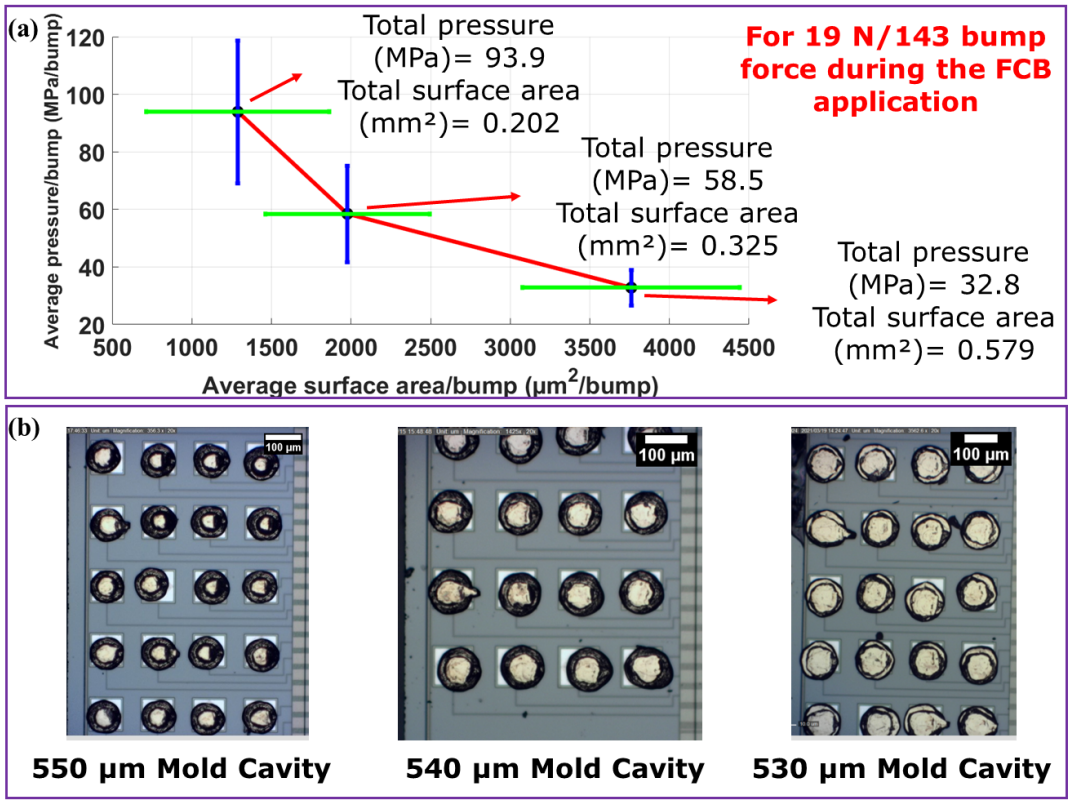


Figure 2.10: Surface area of the GSBs after the coining process. (a) Average pressure/bump (MPa) vs average surface area/bump (mm^2/bump) after the DCC process, (b) Optical microscope images of the surface area of the GSBs after coined by 550 μm, 540 μm, 530 μm mold cavities, respectively.

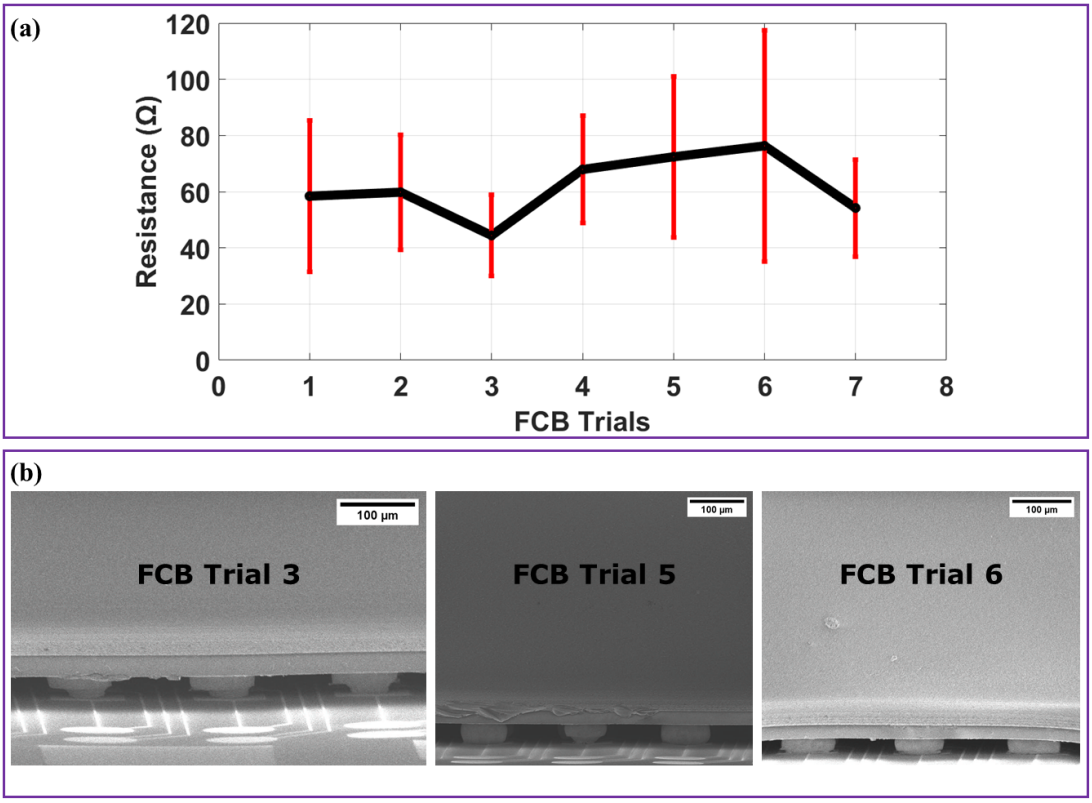


Figure 2.11: Resistivity measurements of the GSBs after the FCB processes. (a) Resistivity of the GSBs pairs after the TSFCB, (b) FCB structures after the TSFCB processes.

possible reason we can think of for the variations between the resistances may be due to post-coining surface quality and/or "before FCB" cleanliness of the bonding pad surfaces [62]. SEM images of FCB bonded structures after thermo-sonic FCB are shown in **Fig. 2.11b**.

The DCC technique described in this study allows for a bump height variation of 1.09 µm on average, with the bump geometries and 25 µm wire diameter we used in this study. After thermo-sonic FCB experiments using pseudo ASIC chips coined by this technique, completely conductive FCB structures are obtained.

Height and surface area values of the GSBs can be tailored according to the FCB process needs by adjusting the height of the mold cavity (**Fig. 2.10**).

Height of the mold cavity, applied compressive force and the high bending stiffness of the polished flat surface that is used for coining (in our case, Borosilicate glass) are the most important parameters for the DCC process. The bending stiffness of the flat coining surface material must be high enough to have high precision coining process.

To investigate if the polished surface of a standard and approximately 500 µm thick, 4-inch diameter, silicon wafer may be used as the coining surface, a DCC process (Trial-15) is performed by using a 526.4 ± 1.9 µm thick silicon wafer as the polished flat surface between the aluminum mold pieces. 547 ± 0.66 µm deep mold cavity is used for the experiment. 1 N/bump (i.e. a total of 143 N for 143 bumps) force is applied during the coining process. The coining process results in an average height value of 47.9 µm and a standard deviation of 1.04 µm for the coined stud bumps. Trial-15 at **Fig. 2.9a** depicts the mean height and standard deviation of the GSBs. This experiment indicates that the polished surface of a 526.4 ± 1.9 µm thick silicon wafer (i.e. standard, 4-inch diameter, Si wafer) can serve as a coining surface, when supported by a thick aluminum block as shown in **Fig. 2.6c**.

Applied compressive force value is systematically varied and experimentally studied in order to understand the effects of the applied compressive force on the DCC process. A pseudo ASIC chip (named as Pseudo ASIC 32) is coined with 0.25 N/bump, 0.5 N/bump and 0.75 N/bump, respectively, to study low compressive force values. Because of the initial height variations in the tail length or body length of the stud bumps (i.e. due to variations in GSB process), and because the contact between the flat surface of the Borosilicate glass, and the top

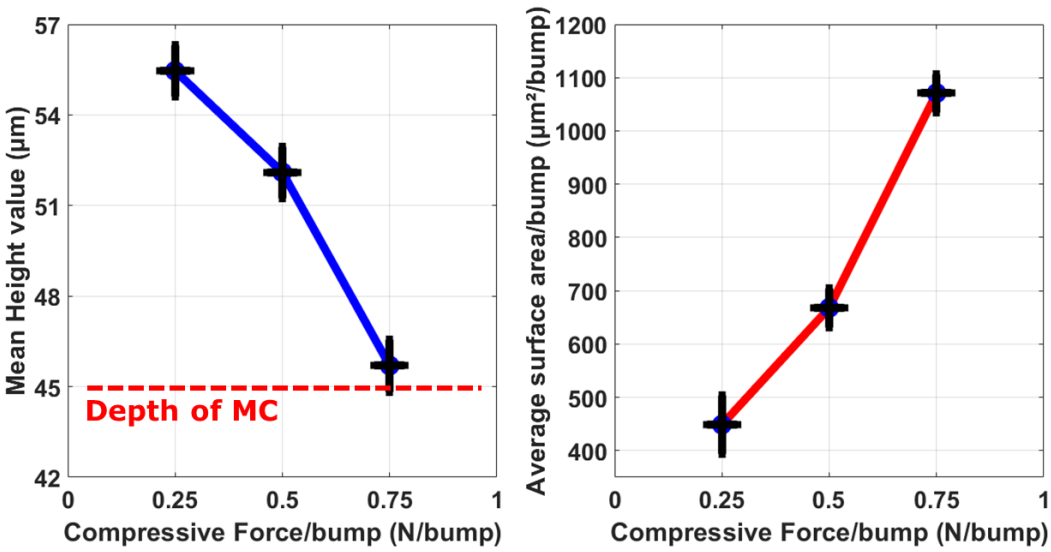


Figure 2.12: Comparison of 0.25 N/bump, 0.5 N/bump, and 0.75 N/bump coining processes. Mean height value vs compressive force/bump plot (on the left) shows that height of the GSBs decreases with increasing compressive force/bump. Average surface area/bump vs compressive force/bump plot (on the right) shows that average surface area increases with increasing compressive force/bump value.

surface of the aluminum cavity mold may be poorer at low compressive force values, 13 GSBs could not be coined after 0.25 N/bump trial, and 4 GSBs could not be coined after 0.5 N/bump trial. All GSBs were coined after 0.75 N/bump trial (Details about 0.25 N/bump, 0.5 N/bump, and 0.75 N/bump trials are given in **Table A.2**). Changes in the average height value and average surface area/bump value are shown in **Fig. 2.12**. Average height value decreases, and average surface area/bump value increases with increasing compressive force/bump value.

If the coining processes would have not been performed inside the known depth mold cavities and would have not been performed under displacement-controlled experimental setup, 627.2 MPa (for 0.25 N/bump), 785.7 MPa (for 0.50 N/bump), and 719.2 MPa (for 0.75 N/bump) total pressure values would have been instantaneously applied to the deformed surface areas of the coined stud bumps during these coining process trials. Because these high pressure values are larger than the compressive yield stress of GSBs (compressive yield stress of the GSB is 127.7

MPa according to the publication of Wang et al. [38]), the stud bumps would obviously be plastically deformed under compression, till a force balance is obtained as the surface area of the coined stud bumps become larger and larger, if there were no displacement controlled mold cavity. In other words, even if compressive pressure values that are more than the compressive yield strength of gold are used for these coining trials, the displacement of the flat coining surface of the Borosilicate glass is stopped at the top surface of the mold cavities and the deformation is displacement-controlled, successfully. A set of experiments that is supporting the information explained in this paragraph (comparison of force-controlled coining (FCC) process using a flip-chip bonder tool and the DCC process) is also explained in **Fig. 2.16**, and the paragraph that is referring to **Fig. 2.16** on page 40-41.

For each DCC experiment, mean height values, total surface area values, and total pressure values of stud bumps are measured, after each coining process. SEM images are used to show the change in the height of the stud bumps, and optical microscope images are used to show change in the coined surface areas of the stud bumps, in **Fig. 2.13a**, and **Fig. 2.13b**, respectively.

Also, using the displacement-controlled approach, a pseudo-ASIC chip (named as pseudo-ASIC 31) is coined with 1 N/bump and 2 N/bump, respectively, to study compressive forces that are higher than the recommended value (1 N/bump) as shown in **Fig. 2.14** (Details about 1 N/bump, 2 N/bump trials are given in **Table A.3**).

Pseudo-ASIC31 is coined with 1 N/bump at first. All of the GSBs are coined. Final height of the GSBs is very close to the depth of mold cavity which means the displacement is controlled during the coining process. Also, total surface area of the pseudo-ASIC31 after 1 N/bump is almost the same with the total surface area of 0.75 N/bump coined pseudo-ASIC32.

2 N/bump compressive force is applied for the second coining process. After 2 N/bump compressive force is applied, final average height of the GSBs is approximately 2 µm below the top surface of the mold cavity. Insufficient (i.e. low) local

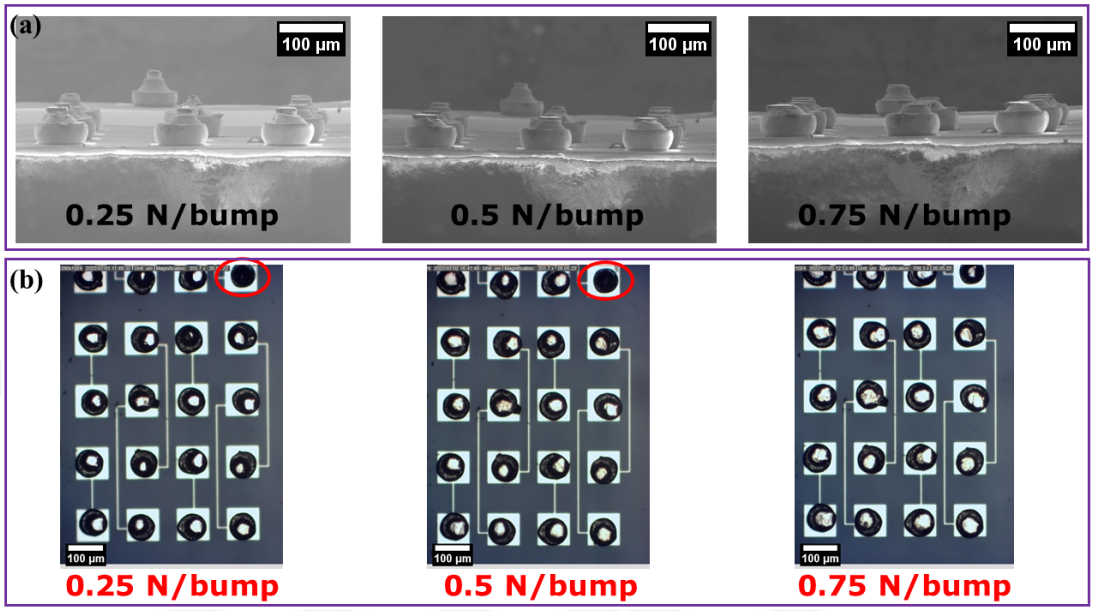


Figure 2.13: SEM (a), and optical microscope (b) images of the GSBs after 0.25 N/bump (b-left), 0.5 N/bump (b-middle), 0.75 N/bump (b-right) coining processes, respectively. In b-left and b-middle images, a red circle highlights an uncoined GSB. The GSBs are all coined in the b-right image.

bending stiffness and relatively low Young's Modulus value of the Borosilicate glass or the aluminum mold may be the reasons for the final average height value of the stud bumps that is approximately 2 µm below the top surface of the mold cavity.

Although the compressive force is increased 100 % (i.e. from 1 N/bump to 2 N/bump) for the second DCC process, the mean height has only decreased 5 % and total coined surface area has only increased 19 % compared to 1 N/bump coining process. This suggests that the displacement of the Borosilicate glass plate is still controlled, but the local bending stiffness of Borosilicate plate is not stiff enough to maintain flat Borosilicate surface in the mold cavity region, for 2 N/bump compressive force value.

Optical microscope images show amount of change of the surface area after the coining processes (**Fig. 2.15**). SEM images show the change in the height of the GSBs after the coining processes (**Fig. 2.15**). As a result of DCC rather

than FCC, the surface area increased lesser and the height decreased lesser than predicted by the 2 N/bump applied compressive force. The deformation was still within needed standard deviation for successful coining process, for our application. If a coining plate with a higher bending stiffness value is used, the 2 N/bump trial might have given higher mean height values compared to depth of mold cavities. Due to higher Young's Modulus values compared to Borosilicate or aluminium, flat plates with flat coining surfaces made from titanium or steel materials can be used as flat surfaces and molds to increase the precision capability of the DCC process.

Low and high compressive force coining process trials in this specific experimental setup of this study suggest that 0.75 N/bump to 1 N/bump should be used for the DCC process of stud bumps obtained from 25.4 micrometer diameter gold wires, in order to have a strong enough contact between the flat surface of the Borosilicate glass and the top surface of the aluminum mold that is in contact with the Borosilicate glass. Furthermore, we should always keep in mind that if we have smaller diameter wires (i.e. 17.5 microns, or 12 microns, or even smaller) for GSB formation, these 0.75 N/bump to 1 N/bump force values that are needed for 25.4 micrometer diameter wires will be more than needed because the surface areas that can be flattened become smaller and smaller, for smaller diameter wires.

In DCC, tail heights and surface areas of the tails of the GSBs may be tailored by the depth of the mold cavity without using excessive amount of compressive force in order to obtain properly coined ASIC chips.

If a DCC process is of interest for industrial applications, the work can be converted to applying the pressure or force with a meter rather than manually by human hand to very precisely control the force needed for coining process.

The DCC process is very suitable for both R&D studies, and may be very suitable for mass manufacturing due to array type designed aluminum mold, especially when the expensive tools for larger coining force needs are not available.

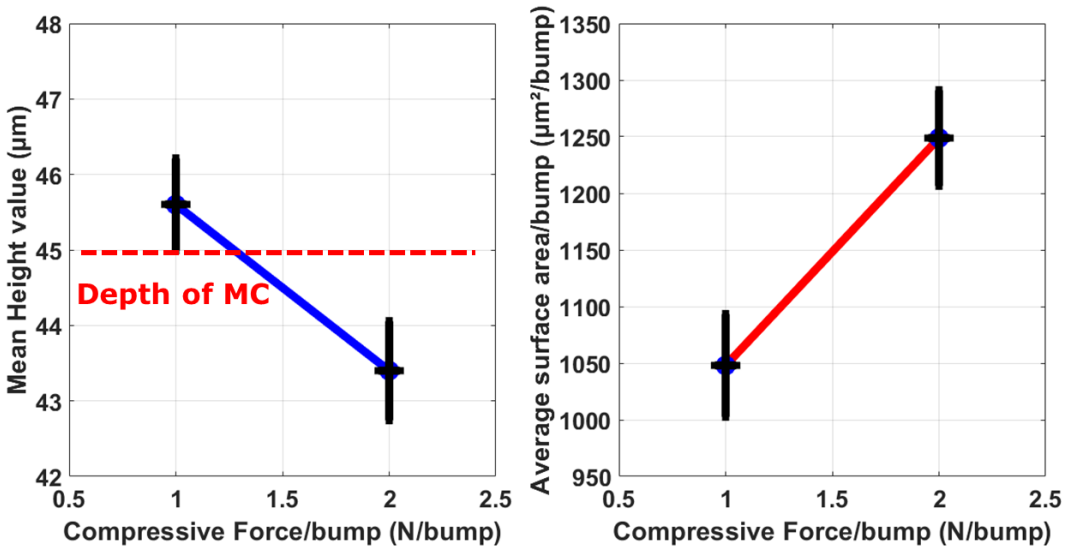


Figure 2.14: Pseudo-ASIC31 is coined with 1N/bump and 2N/bump to study effects of the high compressive forces. Height value decreases with increasing the compressive force/bump as shown in the plot on the left. Also, average surface area/bump value increases with increasing the compressive force/bump as shown in the plot on the right.

One can design mold cavities with different depth values to optimize FCB processes for R&D purposes and one can design mold cavities with the same depth values to perform coining process for multiple chips simultaneously. Also, with this approach, an expensive and high-tech FCB tool with high force output may not be needed for coining processing. Thus, FCB tool would not be busy performing coining processes which saves significant process time. Furthermore, if FCB tool is used for the coining process, co-planarity of the die collet may become very critical parameter which may affect success of the coining process. One can avoid co-planarity problems by having the DCC process performed in a mold cavity, assuming that the manufactured mold cavity satisfies the co-planarity requirements for the specific coining process. Local co-planarity, and global co-planarity of the coined GSBs are satisfied by the manufacturing capabilities of the CNC tool. If very high precision local co-planarity, and very high precision global co-planarity are needed, ultra-precision state-of-the-art CNC machines or electrical discharge machines (EDMs) may be used for preparation of the coining molds.

There are fabricated coining tools designed for wire bonders for coining individual stud bumps [12]. Stud bumps can be coined individually using these coining tools. Although these coining tools are effective tools for coining, using these individual coining tools can be time-consuming, particularly for large arrays. Time-wise, the displacement-controlled array coining method may be more efficient compared to using coining tools that are designed for individual stud bump coining.

Another advantage would be that, if there are capabilities to conduct the stud bumping and coining processes in inert environmental conditions, without being exposed to oxidizing environmental conditions, materials that are oxidized in ambient environmental conditions (i.e. aluminum, and copper) can also be coined by this approach. Oxidation of the materials must be prevented for electrical conductivity.

It is important to emphasize that, it may be necessary to consider the interfacial reactions between the flat coining surface (i.e. the Borosilicate glass) and the

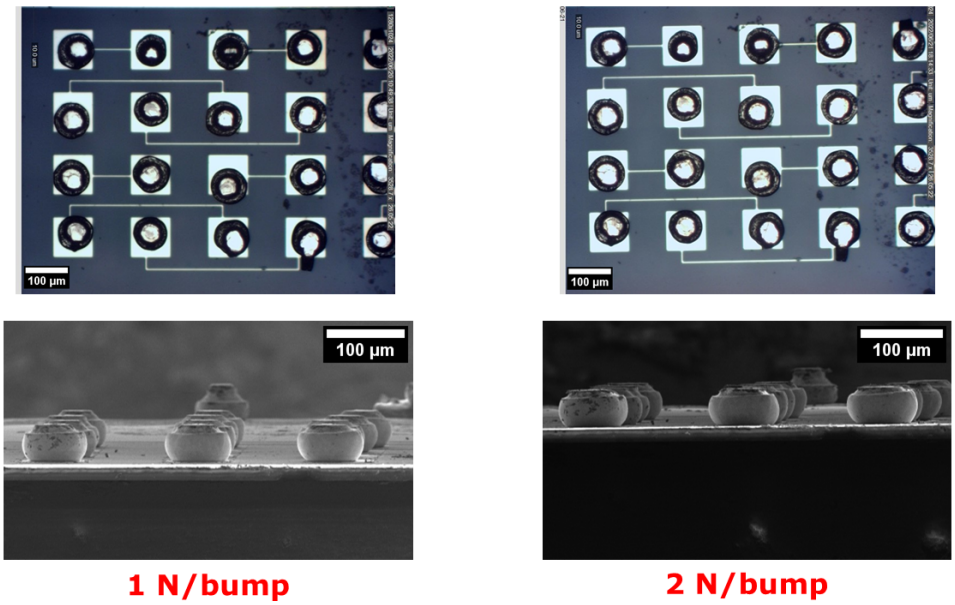


Figure 2.15: Pseudo-ASIC31 is coined with 1N/bump and 2N/bump to study effects of the high compressive forces. Optical microscope and SEM images are shown after the coining processes.

stud bumps (i.e. GSB) before the coining process. At room temperature, there is no interfacial reaction between gold, Borosilicate glass, and aluminum. However, for example, due to adhesive nature of indium metal, when indium may be used as a bump material, there may be an interfacial reaction between indium and the flat coining surface. To prevent such interfacial reactions between the materials that are in mechanical contact, a surface functionalization step may be carried out to prevent the reactions, or a suitable combination of materials may need to be selected to prevent adhesion or reaction possibilities between two contact surfaces before coining on the flat surface.

In this coining study, although we demonstrated high precision DCC using GSBs made from 25 micrometer diameter gold wires, DCC can be extended to smaller diameter wires (for more compressive pressure values with same compressive force values) as well as larger diameter wires that can be used for stud bump formation.

In **Fig. 2.16**, FCC process using a FCB tool and DCC process are compared.

For force-controlled case, 5 different chips, where each chip has 8 bumps, are used for coining experiments. For force-controlled case, 8 bumps/chip is selected because of the 20 N maximum force limitation of the available FCB tool. For displacement-controlled case, chips with 143 bumps are used, results of which are already presented in **Fig. 2.12**, and **Fig. 2.14**. 0.25 N/bump to 2 N/bump forces are applied in 5 different trials for each coining technique. It is concluded that the surface areas of the GSBs increase more and heights of the GSBs decrease more when coining is performed by the FCC with the FCB tool even when the same amount of force/bump is applied for both coining techniques. This mechanical deformation bias in the FCC case must be related to the fact that these is no "displacement-controlled stopper" during the FCC case. **Fig. 2.16** depicts more decrease in the height values and more increase in the surface area values for FCC process using an FCB tool. Both methods provide an accurate coining process, but DCC approach can be preferred when the maximum force value of an FCB tool is insufficient to coin large arrays of stud bumps (Details of **Fig. 2.16** is given in **Table A.4**).

Finally, pseudo ASIC chips that are made of silicon material are used for DCC process. There is no significant difference between Pyrex pseudo ASIC chips and silicon pseudo ASIC chips after the DCC process which suggests that silicon chips can be coined by the method presented in this study.

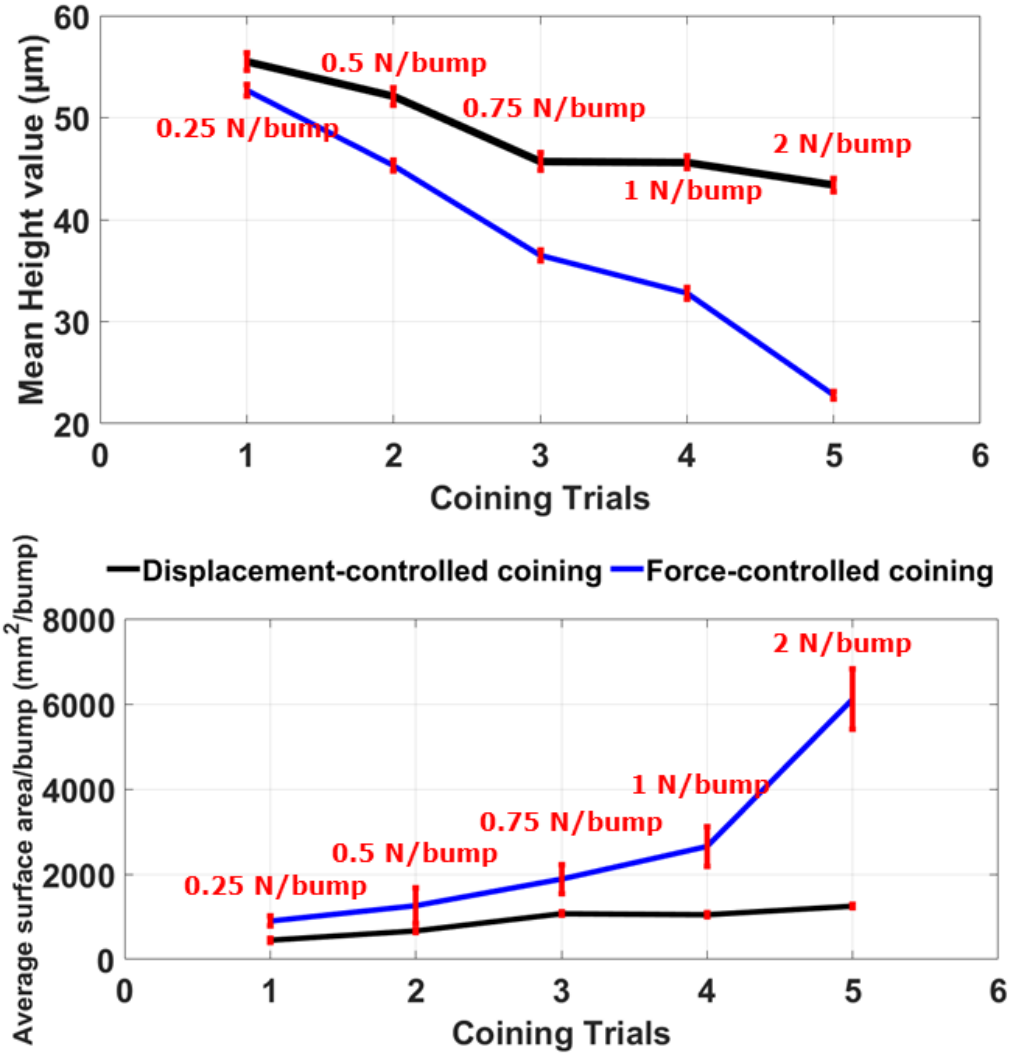


Figure 2.16: Comparison of the coining processes performed by the DCC process and the FCC capability of an FCB tool.

2.5 Thermo-sonic Flip-Chip Bonding Process (TSFCB)

2.5.1 Performing the TSFCB

In this thesis study, all TSFCB processes were carried out by a transverse arm designed flip-chip bonder (Fineplacer Matrix Ma, Finetech GmbH). A pseudo-CMUT chip is placed on the heated stage of the flip-chip bonder. There is a custom design mechanical fixer positioned on the heated stage. The pseudo-CMUT chip is clamped between the notch and the spring of the mechanical fixer mechanically and is also clamped via vacuum of the heated stage as shown in **Fig. 2.17a**.

Usually, a bonding tool is used for the TSFCB process to hold top dies via vacuum. The bonding tool is called die collet. Ultrasonic energy is transmitted to the bonding interface by the vibrations of the die collet. Therefore, design of the die collet is highly critical to obtain optimum transducer performance [63]. Furthermore, it is known that co-planarity of the die collet is very critical in transverse systems to distribute ultrasonic energy homogeneously throughout the bonding interface [64]. The die collet is attached to the transducer by a set screw and distance between the screw and the edge of the die collet is known as tool drop distance (TDD). Kang et al. concluded that TDD affects ultrasonic vibration amplitude of the die collet [65]. Therefore, optimum TDD distance should be chosen to avoid undesired ultrasonic energy loss during the TSFCB process. Moreover, in their another study, Kang et al. observed that increasing the mass of the die collet decreases the ultrasonic vibration amplitude. A TSFCB process with 1000-I/Os is possible by designing a die collet with a suitable TDD and mass values [66]. Li et al. studied a chip-press model where top die was not clamped by the die collet. They studied two different die collets. One was smaller than the top die and the other was bigger than the top die. They concluded that using bigger die collet eliminated slippage and rotation problems during the TSFCB process. Thus, a die collet that has greater area than the top die is

recommended for the TSFCB process [67].

Taking all this information into account, a four-side tungsten carbide die collet is designed by Finetech GmbH & Co. KG in Germany for the pseudo-ASIC chips and the real ASIC chips of this thesis study. The designed die collet is manufactured by Micro-Mechanics in Singapore, shown in **Fig. 2.17b**. Total length of the die collet is 36.83 mm and shaft diameter is 3.17 mm. According to our measurements, mass of the die collet is 3.6 grams. According to our characterization, TDD value of 13 mm is selected which offers the highest ultrasonic power value during the calibration step of the flip-chip bonding process. Same die collet with the same TDD value is used for all of the TSFCB processes in this study.

A pseudo-ASIC chip that has the coined GSBs is placed on a Gel-Pak (GBSs are in contact with the Gel-Pak.). The die collet is aligned with the pseudo-ASIC chip as shown in **Fig. 2.17c**. The die collet holds the pseudo-ASIC chip via partial vacuum suction (50 – 70 %). Since the nest depth of the die collet is 0.24 mm with inclined internal side walls of the nest, all the bottom side corners of the pseudo-ASIC chip are in mechanical contact with the die collet which helps with efficient transferring of the applied ultrasonic energy.

The pseudo-ASIC chip and the pseudo-CMUT chip are aligned by using the optical beam splitter of the flip-chip bonder tool. Top side image in **Fig. 2.17c** shows the alignment before the TSFCB process. When the alignment is completed, the TSFCB process starts by initial contact between the chips to be bonded. Compression force (hence, calculated compression pressure) is applied by the die collet and the temperature is applied by the heated stage. When a predetermined compression force (hence, calculated compression pressure) value and predetermined temperature value are reached during the process, a predetermined amount of ultrasonic process power is applied throughout a predetermined ultrasonic process time by the die collet via ultrasonic vibration motion at 60 kHz frequency (**Fig. 2.17d**). After the ultrasonic vibration is completed, temperature is decreased to room temperature and lastly the compression force is removed from top of the bonded chip pair. The die collet moves up and the TSFCB process is completed. Bottom image in **Fig. 2.17c** shows the alignment

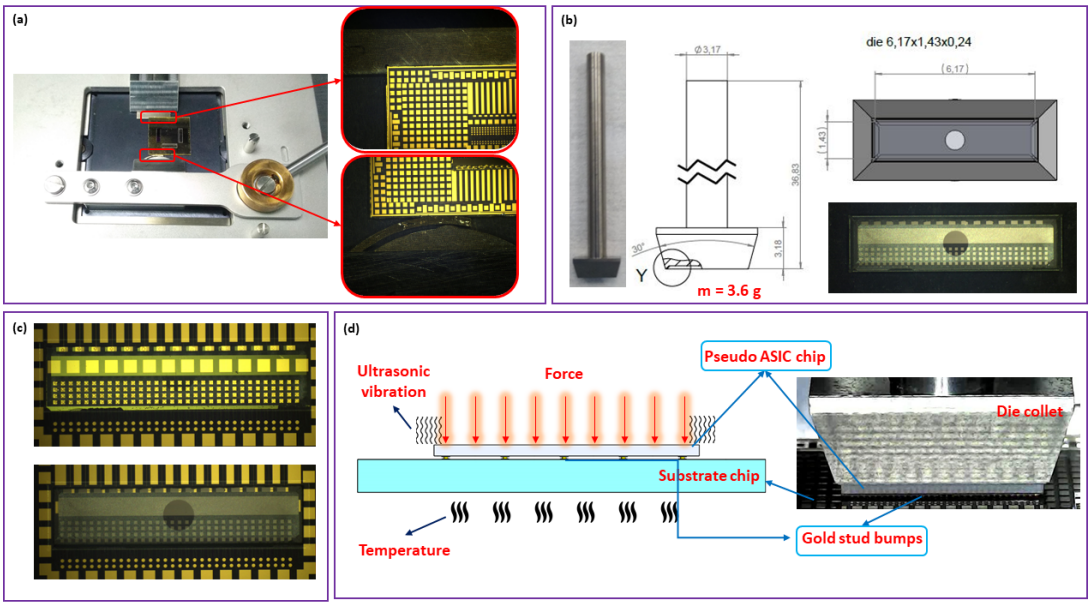


Figure 2.17: The TSFCB Process steps. (a) Clamping of the pseudo-CMUT chip, (b) Design of the die collet, (c) Alignment between the pseudo-ASIC chip and the die collet (top) and Alignment between the pseudo-ASIC chip and the pseudo-CMUT substrate (bottom), (d) The TSFCB process.

after the TSFCB process.

After the completion of the TSFCB process, because Pyrex is an optically transparent material, optical microscope imaging is used to quantify the amount misalignment between the bonded chips. SEM imaging is used to observe the bonding between the GSBs and the gold bonding pads and to check the stand-off distance after the TSFCB process. 2-probe resistivity method, described in **Fig. 2.2**, is used to measure the electrical resistance of the bonded structures after each TSFCB process trial.

No	Trial	Gold Wire D (µm)	Mean h (µm)	SD h (µm)	Mean D (µm)	Total SA (mm2)	No of GSB
1	Pyrex-1	25.4	48.8	0.91	81.5	0.08	143
2	Pyrex-2	25.4	45.2	0.66	81.9	0.21	143
3	Pyrex-3	25.4	43.6	0.60	80.5	0.22	143
4	Pyrex-4	25.4	45.4	0.44	82.0	0.19	143
5	Pyrex-5	25.4	52.4	0.99	82.4	0.12	143
6	Pyrex-6	25.4	51.9	0.66	79.5	0.10	143
7	Pyrex-7	25.4	45.9	1.06	82.8	0.21	143
8	Pyrex-8	25.4	45.2	0.79	81.4	0.17	143
9	Pyrex-9	25.4	47.1	2.28	75.8	0.10	143
10	Pyrex-10	25.4	50.0	1.01	81.8	0.15	143
11	Pyrex-11	25.4	52.1	0.74	81.2	0.14	143
12	Pyrex-12	25.4	40.7	0.76	93.8	0.02	8
13	Pyrex-13	25.4	46.6	0.81	78.1	0.07	143
14	Pyrex-14	25.4	44.1	0.49	80.3	0.22	143
15	Pyrex-15	25.4	47.1	2.07	81.2	0.18	143
	Avg		47.1	0.95	81.6	0.14	

Table 2.2: Properties of GSBs of the Pyrex pseudo-ASIC chips after the DCC process. h: Height, SD: Standard deviation, D: Diameter, SA: Surface area, GSB: Gold stud bump, Avg: Average.

No	Trial	Gold Wire D (µm)	Mean h (µm)	SD h (µm)	Mean D (µm)	Total SA (mm2)	No of GSB
1	Silicon-1	25.4	36.0	0.54	87.6	0.02	8
2	Silicon-2	25.4	45.6	0.81	81.6	0.17	143
3	Silicon-3	25.4	36.9	0.97	85.2	0.02	8
4	Silicon-4	17.5	37.6	0.49	63.4	0.08	143
5	Silicon-5	25.4	37.8	0.55	90.0	0.06	30
6	Silicon-6	25.4	45.0	0.71	81.3	0.19	143
7	Silicon-7	17.5	39.0	0.74	60.8	0.03	143
8	Silicon-8	25.4	37.1	0.43	88.5	0.02	8
	Avg		39.4	0.65	79.8	0.07	

Table 2.3: Properties of GSBs of the Silicon pseudo-ASIC chips after the DCC process. h: Height, SD: Standard deviation, D: Diameter, SA: Surface area, GSB: Gold stud bump, Avg: Average.

2.5.2 Analytical Modelling of the thermo-sonic flip-chip bonding process (TSFCB)

An analytical model, based on lumped-capacitance model in heat transfer engineering, capable of calculating the bonding interface temperature (T_{int}) is developed. The applied ultrasonic energy, process temperature, and properties (specific heat capacity and approximate geometrical dimensions) of GSBs are used in the analytical model to determine the T_{int}. Calculating the T_{int} makes it possible to estimate the success of the TSFCB process. Height, and diameter of each GSB is measured after the DCC process. Average height and average diameter values are calculated after the measurements (**Table 2.2** & **Table 2.3**).

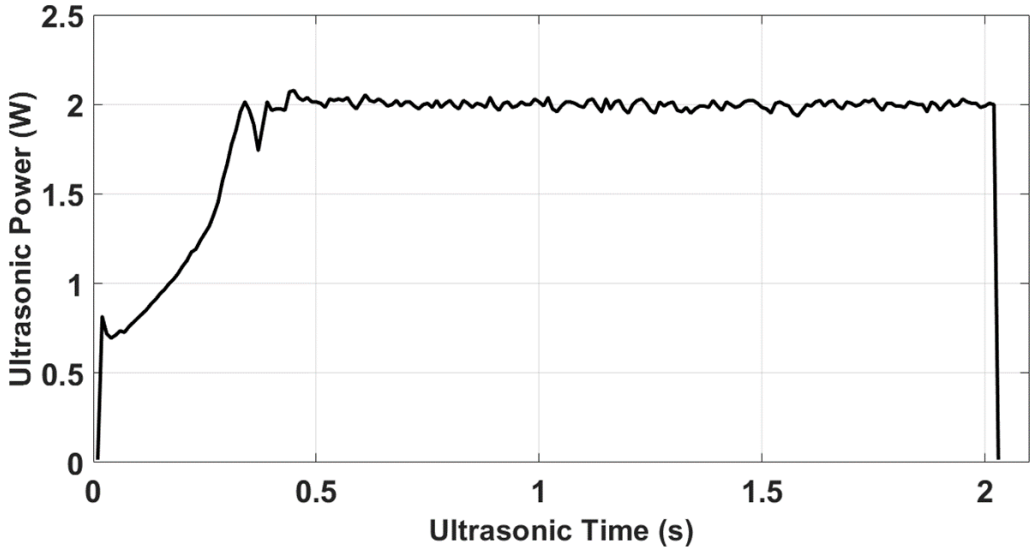


Figure 2.18: An example ultrasonic power-ultrasonic time plot from a TSFCB process.

Each GSB can be assumed as a cylinder. **Fig. 2.3g** shows anatomy of a GSB. At step 1, by using average height (h) and average diameter (R=2r), average volume (V) of a GSB can be calculated (**Equation 2.1**). Then average volume is multiplied with the density of gold (ρ= 19300 kg/m^3) to find average mass of each GSB (m) (**Equation 2.2**). Number of the gold stud bumps (N) is multiplied by the average mass value to find the total mass of the GSBs (M) in the array (**Equation 2.3**).

$$V = \pi r^2 h \tag{2.1}$$

$$m = \rho V \tag{2.2}$$

$$M(kg) = m(kg)N \tag{2.3}$$

During the TSFCB process, ultrasonic energy is partially transferred from the vibrating transducer to the bonding interface. Effects of the ultrasonic energy on the bonding interface is similar to heating [40]. Therefore, it may be assumed that applied ultrasonic energy helps to increase the temperature of the bonding interface via vibration motion and friction between the bonding surfaces. The TSFCB process can be assumed as the heat energy transfer problem. **Equation 2.4** shows the first rule of thermodynamics. ΔU represents the change in internal energy of the system and Q represents the heat added to the system, and W represents the work done by the system. During the TSFCB process, the system performs no significant mechanical work, suggesting that work is negligible (dW = 0). As a result, the change in internal energy (ΔU) equals the heat added to the system (**Equation 2.5**). The effects of the ultrasonic energy can now be transferred to heat.

$$\Delta U = Q - W \tag{2.4}$$

$$\Delta U = Q \tag{2.5}$$

Mayer et al. determined that less than 2 % of the ultrasonic energy that is generated by the vibrating transducer is used at the bonding interface [68]. Ultrasonic power starts to increase when ultrasonic process time begins. However, it takes some time to reach the input ultrasonic power value. **Fig. 2.18** is an example ultrasonic power-ultrasonic time plot obtained from the flip-chip bonder sensor data. The area beneath this ultrasonic power-ultrasonic time plot indicates the total ultrasonic energy (Q) applied by the transducer. Based on the assumption from Ref [68], for this study it is assumed that 2 % of the generated ultrasonic energy quantity is used for bonding and the amount can be calculated by **Equation 2.6**. 2 % of the generated total ultrasonic energy can be divided by the multiplication of the total mass of GSBs (M) and specific heat of the gold (c=129 J/kg°C) to find change in the temperature (ΔT) of the bonding interface (ΔT in **Equation 2.7**). If heating is applied from the heated stage, it is the

process temperature ($T_{process}$). Summation of $T_{process}$ and ΔT gives the interface temperature (T_{int}) (**Equation 2.8**). Using the percentage calculation, the proportion of the melting temperature ($T_m\%$) that is the T_{int} can be computed (**Equation 2.9**).

$$Q(J) = P(W)t(s)0.02 \tag{2.6}$$

$$Q(J) = M(kg)c(J/kg^{\circ}C)\Delta T(^{\circ}C) \tag{2.7}$$

$$Tint(^{\circ}C) = Tprocess(^{\circ}C) + \Delta T(^{\circ}C) \tag{2.8}$$

$$Tm(\%) = 100x\frac{Tint(^{\circ}C)}{Tm(^{\circ}C)} \tag{2.9}$$

As the FCB equipment transducer vibrates, it is known that the local temperature of the bonding interface rises, due to friction generated heat. This suggest that TSFCB can be considered as a heat generation (or in general, heat transfer) process.

A single GSB can be considered as a unit in the analysis of this heat transfer process. Since there is transient heat generation at the bonding interface and transient heat conduction to the GSB during the application of the ultrasonic energy, difference between temperature at the bonding interface and the temperature of the GSB must be considered.

Lumped-capacitance model (LCM) is evaluated for the TSFCB process. LCM assumes that temperature of the solid unit, in our case GSBs, is spatially uniform at any instant during the transient process. Therefore, temperature gradients within the GSB unit are negligible. LCM suggests that the resistance to conduction inside the GSB unit is small compared to heat transfer between the

unit and its surroundings. . In the TSFCB process case, initially (before the initiation of the vibration of the transducer) the GSBs are surrounded by (room temperature or hot) still air from the curved sides of the GSBs. Furthermore, the top side and bottom side of the GSBs are surrounded (i.e. mechanically compressed) by chip substrates. In our applications, the chip substrates are made from silicon or Pyrex. Hence, the GSBs are entirely surrounded by significantly lower thermal conductivity materials compared to the thermal conductivity GSBs that are made from gold. Hence, GSBs can be assumed as completely confined in a thermally insulating environment. Furthermore, once the approximately 60 kHz frequency vibrations of the TSFCB transducer are initiated, the amplitude of the vibrations of the die collet tip are approximately on the order of several micrometers. Hence, once the approximately 60 kHz frequency vibrations of the TSFCB transducer are initiated, the still air that is in the close vicinity of the die collet tip and close vicinity of the GSBs is not still for the short amount of US vibration time of the die collet. Therefore, it may be assumed that there is confined volume forced convection within the close vicinity (approximately within the vibration amplitudes of the die collet and GSBs) of the GSBs. In addition, it is assumed that after the confined volume forced convection vicinity of the GSBs, the air immediately becomes "still air" again. Hence, after the forced convection vicinity of the GSBs, the GSBs are again surrounded by still air that has low thermal conductivity.

With several critical experimental unknowns (i.e. exact vibration amplitude of the die collet, and exact forced convection value of the confined volume surrounding air) that we have in the experimental setup, it is very difficult to explain all these details with mathematical formulations within the scope of this study. These critical experimental unknowns will be studied in future research studies in more detail.

Because the GSBs and the vicinity of the GSBs are surrounded by low thermal conductivity materials compared to thermal conductivity of GSB, LCM assumptions are valid for the GSBs of the TSFCB process. Consequently, it is safe to infer that the temperature of GSBs is the same as that of the bonding interface (T_{int}) during the ultrasonic bonding time interval of the bonding process.

Material	Thermal Conductivity (W/mK)
Air	0.01-0.047 [69]
Pyrex	1.143 [70]
Silicon	75.5-147.6 [71]
Gold	367.1-392.8 [69]

Table 2.4: Thermal conductivities of relevant materials.

No	Trials	Force (N)	Total pressure (MPa)	$T_{process}$ (°C)	US power (W)	US time (s)	Tm%
1	Pyrex-1	19	130.8	375	2.5	0.9	46.9
2	Pyrex-2	19	91.7	375	1	1	47.04
3	Pyrex-3	19	85.6	150	2	1	47.25
4	Pyrex-4	19	99.4	24	2.4	1.2	47.54
5	Pyrex-5	19	145.8	375	2.5	1.1	51.05
6	Pyrex-6	19	150.5	375	3	1	52.5
7	Pyrex-7	19	88.8	150	2.5	1	53.24
8	Pyrex-8	19	114.3	150	2	1.2	58.27
9	Pyrex-9	19	118.2	375	2.5	0.9	61.35
10	Pyrex-10	19	125.7	375	2.5	1.1	63.27
11	Pyrex-11	19	138.9	375	5	1	64.45
12	Pyrex-12	2	120.0	25	0.7	0.3	67.61
13	Pyrex-13	19	125.8	375	5	1	80.24
14	Pyrex-14	19	86.4	150	2	2	102.2
15	Pyrex-15	19	103.2	375	10	1	179.5

Table 2.5: TSFCB process trials of Pyrex pseudo-ASICs.

The **Table 2.5** and **Table 2.6** pseudo-ASIC chips are used to perform the TSFCB process. All trials are performed on pseudo-CMUT substrates made of Pyrex. The TSFCB process parameters for Pyrex trials are listed in **Table 2.5** and silicon trials are listed in **Table 2.6**. The trials are sorted from minimum to maximum T_m%.

Pyrex trials at **Table 2.5** starts by 46 % T_m at first trial and end at 179 % T_m interface temperature. $T_{process}$ of minimum 24 °C and maximum 375 °C is

No	Trials	Force (N)	Total pressure (MPa)	$T_{process}$ (°C)	US power (W)	US time (s)	Tm%
1	Silicon-1	3.2	186.3	24	0.8	0.2	39.03
2	Silicon-2	19	111.5	150	1.5	1	41.19
3	Silicon-3	2.5	165.0	150	0.6	0.2	46.82
4	Silicon-4	19	229.5	150	1.5	0.9	55.3
5	Silicon-5	13.5	226.4	150	1	0.5	57.66
6	Silicon-6	19	102.4	150	2	1.2	58.49
7	Silicon-7	6.5	189.0	150	1.1	1	60.44
8	Silicon-8	3.2	196.5	40	0.6	0.3	69.97

Table 2.6: TSFCB process trials of Silicon pseudo-ASIC.

used. Ultrasonic power and ultrasonic time are selected to obtain a target T_m% value and calculated prior to TSFCB process by described equations (**Equation 2.1-2.9**).

Due to the technical configuration of the flip-chip bonder, because we were limited in terms of the maximum amount of applicable compressive force by the flip-chip bonder, the compressive force is kept constant for trials with 143 GSBs. For Pyrex-12 trial which has 8 GSBs, 2 N of force is applied. Main reason behind the specific amount of compressive force selection is to have similar compressive pressure values for all process trials. Since the coined surface areas of GSBs vary from chip to chip, compressive pressure values also vary from chip to chip.

Although, various $T_{process}$ values (24 °C, 25 °C, 150 °C and 375 °C) are implemented, TSFCB processes performed between 46 % and 70 % of T_m interface temperature shows complete conductivity. Beyond 80 % T_m value, nonconductive GSB connections are observed. There are 2 nonconductive GBS connections for 80 % T_m (Pyrex-13), 15 nonconductive GSB connections for 102 % T_m (Pyrex-14) and 143 nonconductive GSB connections for 179 % T_m (Pyrex-15). SEM and optical microscope images are taken after TSFCB process trials and are showed in **Fig. 2.19** along with number of unbonded GSB connection and T_m% relation plot. As shown in **Fig. 2.19**, increasing the interface temperature (as $T_{int} = T_m$%) increases deformation of GSBs, misalignment between the chips, number of nonconductive GSB connections and eventually leads to unsuccessful bonding.

Silicon trials at **Table 2.6** starts by 39 % T_m at first trial and end at 69.9 % T_m interface temperature. $T_{process}$ of minimum 24 °C and maximum 150 °C is used. Ultrasonic energy and ultrasonic time are selected to obtain a target T_m% value and calculated prior to TSFCB process by described equations (**Equation 2.1-2.9**).

Although, various $T_{process}$ values of 24 °C and 150 °C are implemented, TSFCB processes performed between 46 %-69.9 % T_m interface temperature shows complete conductivity. Below 46 % T_m value, nonconductive GSB connections

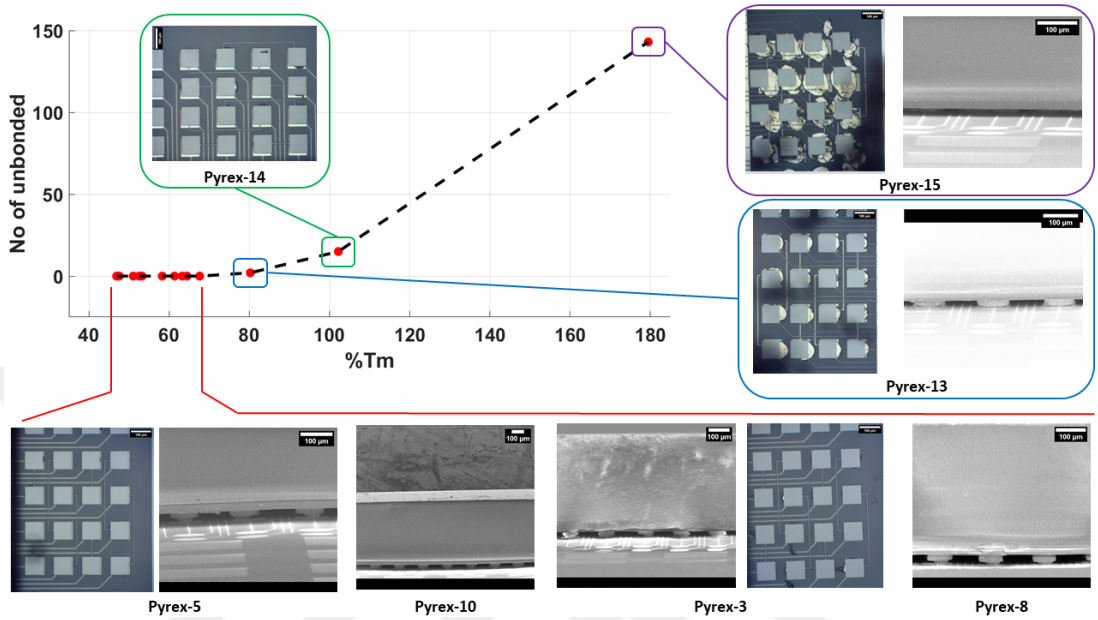


Figure 2.19: TSFCB process trials for Pyrex pseudo-ASICs. Increasing T_m% increases deformation of GSB and misalignment.

are observed. There are 2 nonconductive GBS connections for 39 % T_m (Silicon-1) and 30 nonconductive GSB connections for 41 % T_m (Silicon-2). SEM and optical microscope images are taken after TSFCB process trials and are showed in **Fig. 2.20** along with number of unbonded GSB connection and T_m% relation plot. As shown in **Fig. 2.20**, decreasing interface temperature (T_m%) below 46 % T_m, decreases deformation of GSBs and poor contact between the GSB and the bonding pad leads to unsuccessful bonding.

Silicon-4 trial and Silicon-7 trial are completed by using GSBs fabricated by 17.5 µm diameter gold wire. Volume of the gold stud bumps is smaller and therefore to reach interface temperature value of 55-60 % T_m, less ultrasonic energy is required. 1.5 W ultrasonic power and 0.9 s ultrasonic time is used for Silicon-4 trial to reach 55 % T_m and 1.1 W ultrasonic power and 1.0 s ultrasonic time is used for Silicon-7 trial to reach 60 % T_m. When GSBs fabricated by 25.4 µm gold wire are used, volume (hence, mass) of the GSBs are larger and to reach the same T_m% value, 2 W ultrasonic power and 1.2 s ultrasonic time is used for Silicon-6 trial to reach 58 % T_m. Silicon-4, Silicon-7 and Silicon-6 TSFCB process trials are completed at 150 °C $T_{process}$, but significantly less ultrasonic energy was

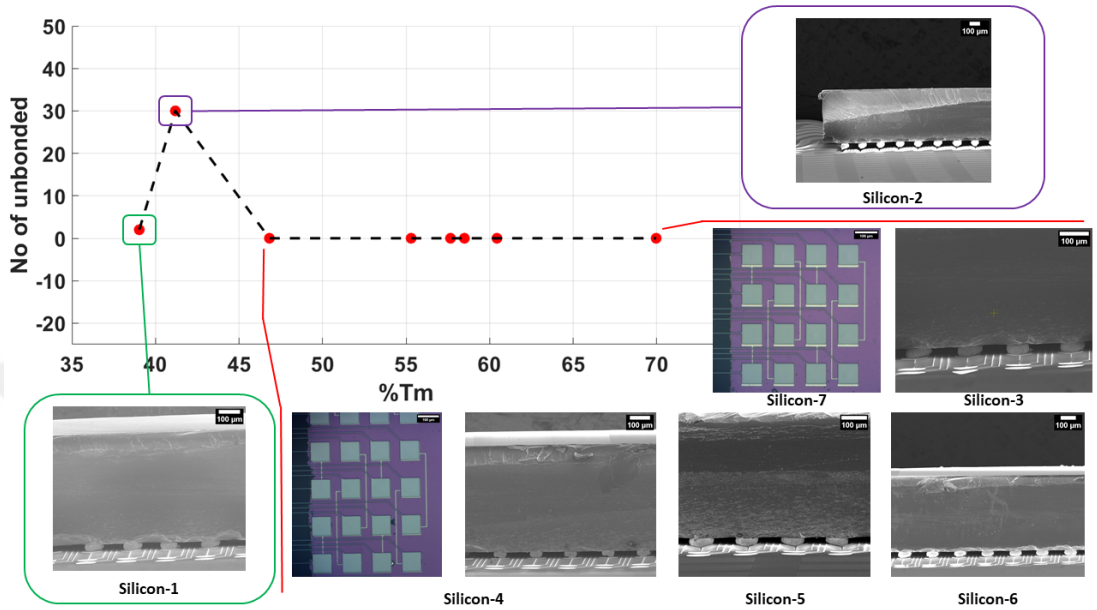


Figure 2.20: TSFCB process trials for Silicon pseudo-ASICs. Beneath 46 % T_m, nonconductive GSB connections observed.

sufficient to integrate GSBs fabricated from 17.5 µm gold wire.

Resistance of the GSB connections are measured by 2-probe resistivity measurement technique. Resistance of Pyrex trials are given in **Table 2.7** and resistance of Silicon trials are given in **Table 2.8**.

A heat energy transfer based analytical model for the TSFCB process is developed. The developed model can calculate the interface temperature (T_{int}). T_{int} can be manipulated by the amount of total mass of GSBs, $T_{process}$, ultrasonic process power and ultrasonic process time. The developed analytical model is tested using silicon and Pyrex chips that have GSBs. TSFCB process parameters are estimated prior to the TSFCB process by the analytical model and calculated after the TSFCB process by taking the raw data from the flip-chip bonder tool.

Trials with a T_m% value between 46 % and 70 % of the T_m were completely conductive for both Pyrex chips and Silicon chips. This suggests that both Silicon and Pyrex chips can successfully bond at a T_{int} between 46 % and 70 % of the T_m. This also suggests that low thermal conductivity substrate materials

No	Trails	Avg. Resistance (Ω)	SD of Resistance (Ω)	No of unbonded
1	Pyrex-1	58.4	27.01	0
2	Pyrex-2	69.2	17.1	0
3	Pyrex-3	55.1	26.7	0
4	Pyrex-4	68.1	33.3	0
5	Pyrex-5	44.4	14.5	0
6	Pyrex-6	98.9	92	0
7	Pyrex-7	174.9	81.3	0
8	Pyrex-8	55.1	21.1	0
9	Pyrex-9	59.8	20.4	0
10	Pyrex-10	76.3	41.2	0
11	Pyrex-11	72.4	28.6	0
12	Pyrex-12	42.8	0.55	0
13	Pyrex-13	119.6	95.8	2
14	Pyrex-14	90.2	38.8	15
15	Pyrex-15	1.0E+09	0	143

Table 2.7: Resistance measurement results of Pyrex trials.

No	Trails	Avg. Resistance (Ω)	SD of Resistance (Ω)	No of unbonded
1	Silicon-1	71.3	31.4	2
2	Silicon-2	66.4	20.9	30
3	Silicon-3	42.3	0.31	0
4	Silicon-4	55.1	25.9	0
5	Silicon-5	61	23.1	0
6	Silicon-6	45.1	16.2	0
7	Silicon-7	49.1	25.7	0
8	Silicon-8	40.2	0.28	0

Table 2.8: Resistance measurement results of Silicon trials.

such as Pyrex (Thermal conductivity of Pyrex: 1.143 W/mK) and silicon (Thermal conductivity of silicon is strongly temperature dependent, and the thermal conductivity of silicon decreases as temperature increases [72]) have a negligible effect on the interface temperature because the LCM assumptions for the TSFCB process are valid.

GSBs made from 25.4 µm or 17.5 µm have different amounts of total masses, for the same number of GSBs. Because the amount of GSB mass also affects T_{int}, smaller masses of the same material require less ultrasonic energy to reach the same T_{int}. If a small amount of ultrasonic energy is required due to the vulnerability of a substrate, the amount of ultrasonic energy required to achieve successful TSFCB integration can be decreased by working with smaller stud bump masses.

The analytical model can be used to tailor process parameters according to the requirements and restrictions prior to actual bonding process. T_{int} can be tailored for various $T_{process}$. 100 % conductive FCB structures are obtained in this study by the TSFCB processes at $T_{process}$ temperatures of 24 °C, 25 °C, 40 °C, 150 °C, and 375 °C. If there is a $T_{process}$ limit due to delicate substrates, one can decrease $T_{process}$, and to compensate for the loss from $T_{process}$, one can increase the ultrasonic power and/or time, and the same T_{int} value can be obtained. The total integration process time can be shortened by performing TSFCB integration at low temperatures or even at room temperature. The target temperature is where TSFCB process begins. The integration process requires more time if the target temperature is high because it takes longer to reach the target temperature. At 150 °C, the TSFCB process takes 90 seconds to complete; while, at 24–25 °C, it takes only 6–15 seconds (**Fig. 2.21**). The throughput can be increased by cutting the total process time. If total process time decreases, cost can also be decreased.

The developed analytical model can be integrated with deformation models to estimate bump deformation during the TSFCB process. Liu et al. developed constitutive relation equations for a 25.4 µm diameter gold bonding wire [48]. The constitutive relation equations developed for the 25.4 µm gold wire and

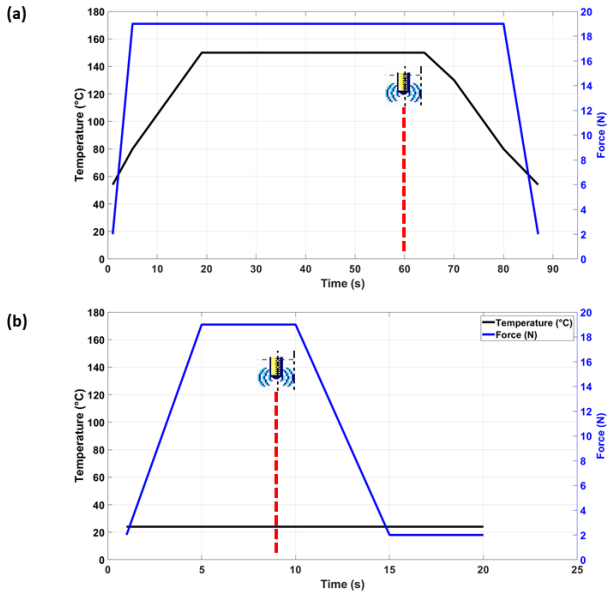


Figure 2.21: TSFCB process plots. (a) TSFCB process at 150 °C and 19 N. Total process takes 87 seconds. Ultrasonic power is applied at 60^{th} second (shown in red dashed line), (b) TSFCB process at 24 °C and 19 N. Total process takes 15 seconds. Ultrasonic power is applied at 9^{th} second (shown in red dashed line).

listed below.

$$\sigma = E_0(1 - e^{-\alpha\varepsilon}) + E_1\varepsilon(1 - T^*) \tag{2.10}$$

$$E_0(T) = 228.9908 - 0.0778T - 0.00015269T^2,\ T : {}^\circ C \tag{2.11}$$

$$\alpha(T) = 606.0641 - 0.7032T + 0.001215T^2,\ T : {}^\circ C \tag{2.12}$$

$$E_1 = 360 \tag{2.13}$$

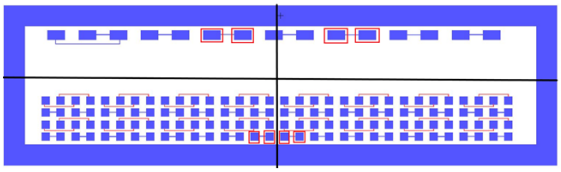
$$T^* = \frac{T - T_{room}}{T_{melt} - T_{room}},\ T_{room} : 24\,{}^\circ C\ and\ T_{melt} : 1064\,{}^\circ C \tag{2.14}$$

In the above equations, T refers to T_{int}. T_{int} can be calculated by the developed analytical model. Then, using above equations, deformation of GSBs and final height of the GSBs after the TSFCB process can be calculated.

Pyrex-12, Silicon-3, and Silicon-1 trials are performed to study the estimation of bump deformation. In order to deform the GSBs more, lesser amount of GSBs are placed on the pseudo-ASIC chips to increase force/bump and pressure/bump values during the TSFCB processes. All three pseudo-ASIC chips have eight GSBs fabricated by 25.4 µm gold wire. The eight GBSs are placed with their centers of gravity approximately in the middle of the pseudo-ASIC chip shown in red rectangular markers **Fig. 2.22a**. Pressure, T_{int}, initial bump heights, estimated final bump heights, measured average bump heights, and deviation values are given in **Fig. 2.22b**. T_{int} is calculated by the developed analytical model and bump deformation is calculated by taking T as T_{int} in **Equations 2.10-2.14**. T_{int} equals to the temperature of the GSBs due to LCM assumptions. Thus, deformation of the GSB is calculated at the T_{int} temperature. Deviation, which is the difference between the estimated final bump height value and the measured average final bump height value, is calculated after SEM imaging is completed for each trial shown in **Fig. 2.22c**. The deviation values are less than 2 µm showing that integrating the developed analytical model and the deformation model [48] can be used to estimate the bump deformation between GSBs and gold bonding pads. The deviation can be decreased by calculating the exact amount of ultrasonic energy transferred from the die collet and creating constitutive equations (**Equations 2.10-2.14**) specifically for the gold wire that is used. Estimating and controlling the bump deformation may be helpful to control the stand-off distance between the chips. The stand-off distance is an important parameter during the underfilling process and can be tailored according to underfilling process needs [73].

T_{int} value was 39 % for Silicon-1 trial. Although high pressure value is applied during the TSFCB process, 2 GSBs are nonconductive. Thus, even if high pressure is applied during the bonding process, T_{int} value of 39 % is not enough to create bonding between Au-Au interface. Furthermore, using low pressure/bump value is not enough to create bonding between Au-Au interface. It is observed

(a)



(b)

	Pressure (MPa)	%Tint	Initial bump height (µm)	Estimated final bump height (µm)	Measured average final bump height (µm)	Deviation (µm)
Silicon-1	186.3	39.03	36.0	33.36	31.65	1.71
Silicon-3	164.7	46.82	36.9	34.52	32.80	1.72
Pyrex-12	120.0	67.61	40.7	31.86	31.93	0.07

(c)

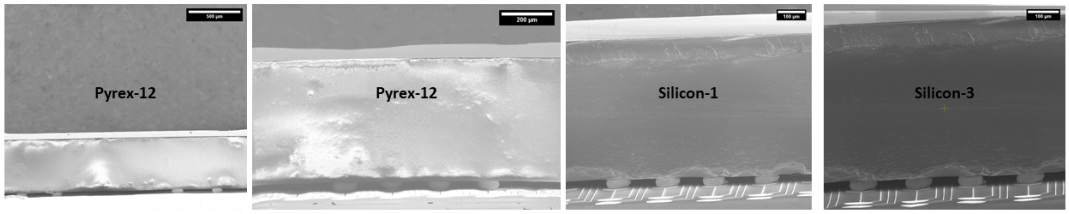


Figure 2.22: Estimation of bump deformation during the TSFCB process. (a) Location of the 8 GSBs in the array, (b) Bump height estimation and measurement values, (c) SEM images of the trials.

that TSFCB processes that used less than 80 MPa pressure value failed in this study. It can be inferred that sufficient amount of T_{int} and pressure/bump value is needed to obtain successful Au-Au bond.

Multiple pseudo-ASIC chips are sequentially and successfully bonded to the same pseudo-CMUT substrates using the developed analytical model to estimate the process parameters of the TSFCB processes shown in **Fig. 2.23a**. Furthermore, to test the possibility of bonding two pseudo-ASIC chips with a distance that is shortest for our die collet geometry, two Pyrex pseudo-ASIC chips are bonded on the same pseudo-CMUT substrate. The shortest distance between the two Pyrex pseudo-ASIC chips is 520 µm which is the shortest possible with the die collet used in this study and SEM image of the structure is shown in **Fig. 2.23b**. Thus, using the TSFCB process, multi-chip packaging and high-density packaging is possible.

There are some assumptions made for the developed model in order to engineer the TSFCB process. The developed analytical model works by accepting the

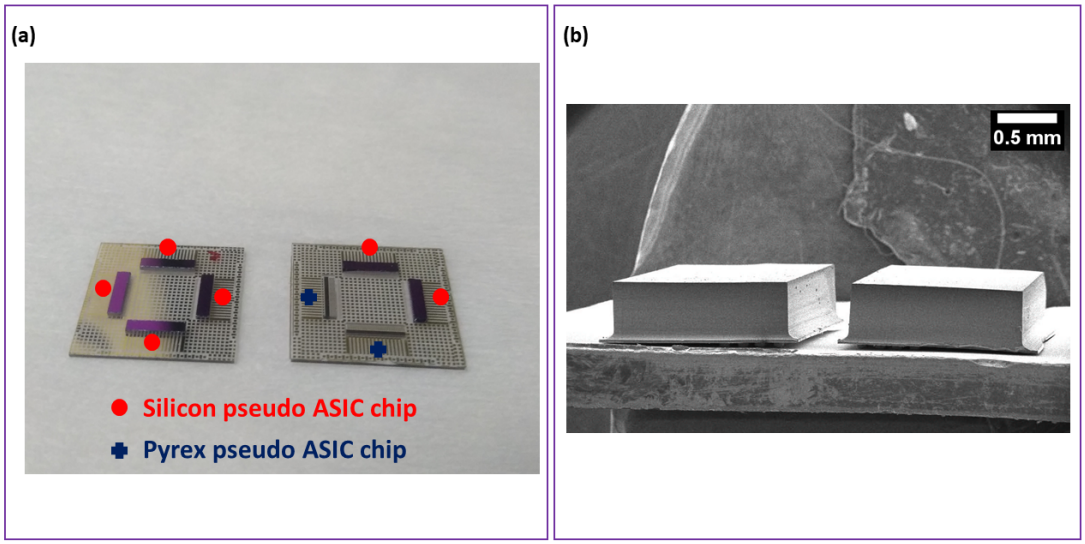


Figure 2.23: (a) Multiple pseudo-ASIC chips are bonded on the same pseudo-CMUT substrate, (b) Two Pyrex pseudo-ASIC chips are bonded very close to each other. The shortest distance between the two pseudo-ASIC chips is 520 µm.

assumptions listed below:

I. The model accepts that the TSFCB process is a solid-state welding joining process that takes place below the melting point of the stud bump materials. The TSFCB process was designed as a solid-state process back in the 1970s [33].

II. The model accepts that 2 % of the ultrasonic energy is used for interface bonding [68].

III. The model assumes that 2 % of the ultrasonic energy is given off in a very short time (ultrasonic time) that is supporting our assumptions allowing us to work with LCM equations.

IV. The model is only experimentally tested between the same bonding materials. In this study, only GSBs and gold bonding pads are experimentally studied. The bonding between different materials (i.e. Au-Al or Au-Pt) was not studied.

V. The model assumes that LCM assumptions are valid for the TSFCB process

suggesting that the difference between temperature of GSBs and temperature of the bonding interface is negligible.

VI. The model assumes that the temperature of the heating stage is the initial temperature of the interface temperature.

VII. Time for diffusion is not considered.

No	ASICs	Gold Wire D (µm)	Mean h (µm)	SD h (µm)	Mean D (µm)	Total SA (mm^2)	No of GSB
1	ASIC-1	17.5	33.6	1.02	67.1	0.067	143
2	ASIC-2	17.5	33.7	0.74	68.8	0.075	143

Table 2.9: GSB properties of ASIC-1 and ASIC-2 after the displacement-controlled coining process.

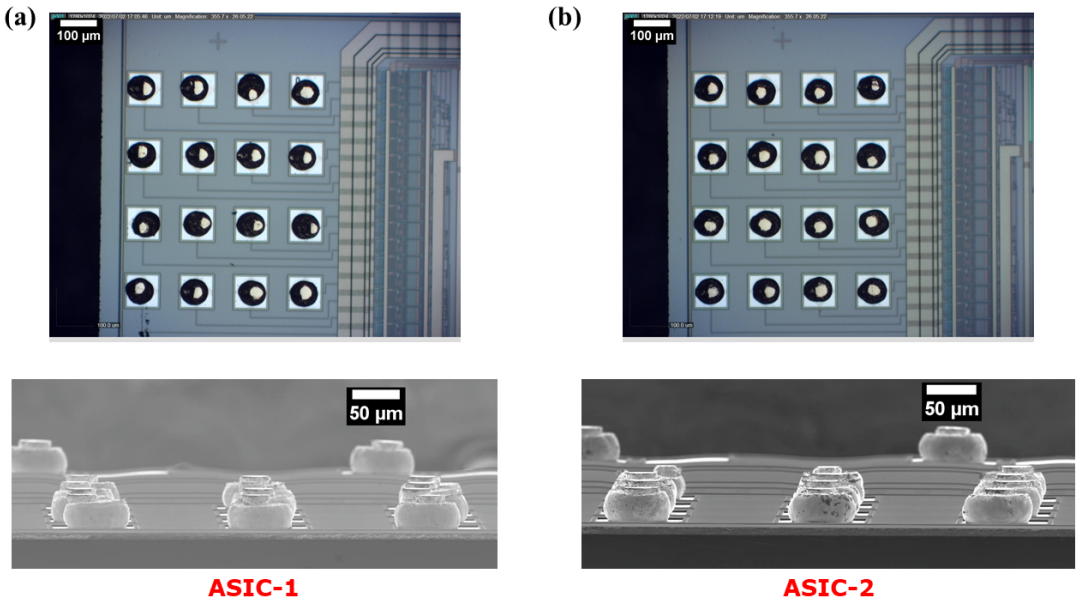


Figure 2.24: (a) Optical and SEM images of ASIC-1, (b) Optical microscope and SEM images of ASIC-2.

2.5.3 TSFCB Process of Real ASIC and Real CMUT

After optimizing the TSFCB unit process, it is time to integrate real ASIC chips and a real CMUT chip. GSBs are fabricated by the SBB process described in Chapter 2.3. 17.5 µm diameter gold wire is used for the stud bump fabrication. Then, the DCC is performed for 2 real ASIC chips (ASIC-1 and ASIC-2). GSB properties after the DCC process are given in **Table 2.9**. Optical microscope and SEM images are shown in **Fig. 2.24**.

TSFCB process parameters are calculated by the developed analytical model (**Table 2.10**). 50-70 % T_m value is targeted by the analytical model and is obtained during the TSFCB process (**Table 2.10**). TSFCB process of ASIC-1 is performed first. Then, TSFCB process of ASIC-2 is performed. Bonded ASIC chips on the CMUT chip are shown in **Fig. 2.25a**. By completing TSFCB

No	ASICs	Force (N)	Total pressure (MPa)	Tprocess (°C)	US power (W)	US time (s)	Tm%
1	ASIC-1	12.5	186.5	150	1.6	1.1	52.42
2	ASIC-2	14.5	193.3	150	1.9	1.1	65.03

Table 2.10: TSFCB parameters of ASIC-1 and ASIC-2. The parameters are calculated by the developed analytical model.

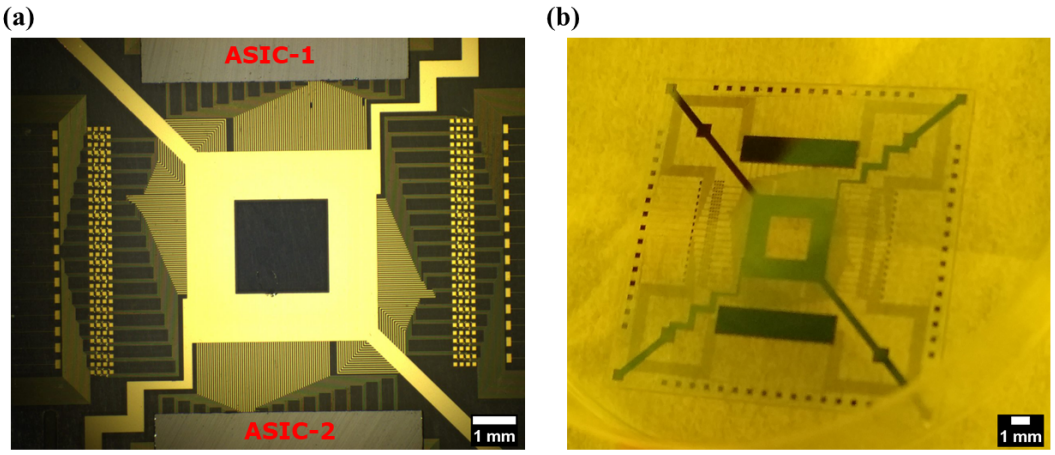


Figure 2.25: (a) Bonded ASIC chips on the CMUT surface after the TSFCB process, (b) The CMUT chip after the TSFCB process.

processes, 2 ASIC chips are integrated with the CMUT chip, as shown in **Fig. 2.25b**.

The SEM tool is used to image the FCB structure (**Fig. 2.26**). All 143 connections/ASIC of both ASIC chips are in contact with the bonding pads, suggesting that a total of 256 CMUT cells are integrated with the ASIC circuits. Therefore, signals from all CMUT cells (256 cells) can be processed by the ASIC chips when the yield of CMUT array cells is 100 % [8]. These TSFCB processes also prove again that 50-70 % T_m value can integrate the GSBs to gold bonding pads successfully.

The FCB-integrated CMUT chip is now ready for the CMUT–PCB integration process. Before integrating with the PCB, selected regions of the FCB structure will be coated with a Parylene material. Details of the Parylene C coating are

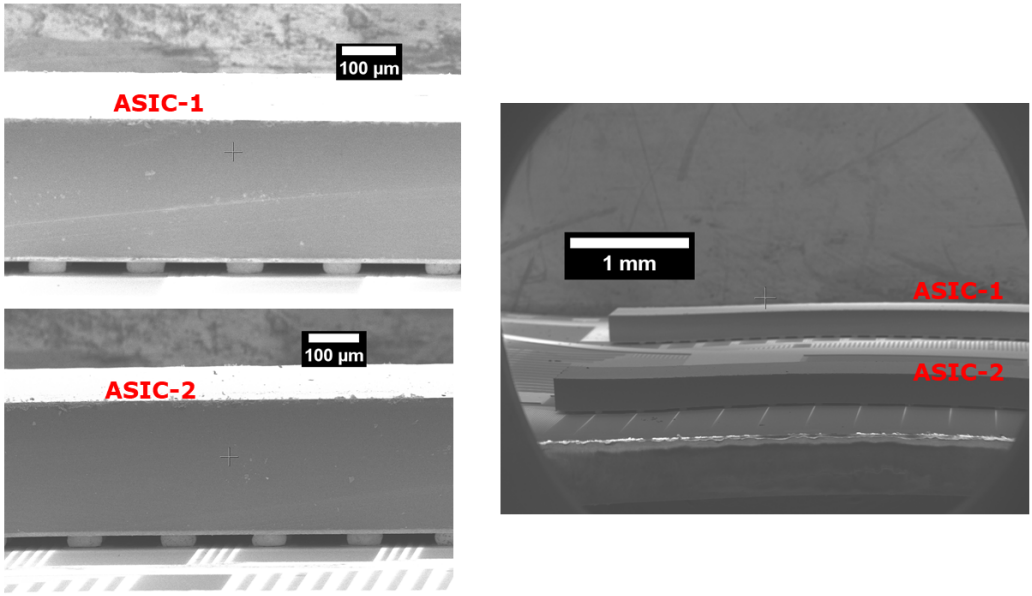


Figure 2.26: SEM images of ASIC-1 and ASIC-2 after the TSFCB processes. Connections of ASIC-1 and ASIC-2 are fully integrated with the CMUT chip.

given in the next chapter.

2.5.4 Underfill and Parylene C Coating Processes

Underfill materials are electrically nonconductive and non-Newtonian epoxy materials [74]. The underfill materials are used to improve the reliability of bump connections of FCB structures [75]. A controlled amount of underfill material is dispensed into the gap of the FCB structure to increase reliability and reduce thermal expansion and stresses [76]. Dispensed underfill material fills the gap by capillary flow [77]. Usually, dispensing of underfill is performed in either an "I" shape or an "L" shape [78]. It is known that the "L" shape dispensing decreases the filling time of the gap more than the "I" shape dispensing by 1.4 times [79]. "I" shape dispensing means dispensing an underfill to one side of the FCB structure. "L" shape dispensing means dispensing an underfill to two sides of the FCB structure.

Suitable underfill materials from many candidates are found at EPO-TEK

Property	353 ND
Pot life (hours)	3
Biocompatibility	Yes
Low outgassing	Yes, NASA approved
Conductivity (ohm-cm)	N/A
Viscosity (cP.s)	3000-5000
Maximum operating temperature (°C)	250
Curing Schedule-1	150 °C - 1 minute
Curing Schedule-2	120 °C - 5 minutes
Curing Schedule-3	100 °C - 10 minutes
Curing Schedule-4	80 °C - 30 minutes
Curing Schedule-5	25 °C - 3 days

Table 2.11: Properties of 353 ND underfill material.

company. 353 ND underfill material is chosen for underfilling the ASIC-CMUT FCB structure due to the underfilling capability of the FCB structure, biocompatibility, low outgassing, maximum operating temperature, and available low-temperature curing schedules. **Table 2.11** shows the properties of the 353 ND underfill material [80].

The 353 ND underfill material must be applied on the edge of an ASIC chip that is FCB bonded on a CMUT chip. It is decided that a time-pressure dispenser (TPD) can be used to dispense the 353 ND underfill material to the gap of the ASIC-CMUT integrated structure. The TPD parameter optimization is performed for the underfill material. The TPD trials were carried out by Fluidmatic 1000T time-pressure dispenser machine. Details about the machine are given in Chapter 2.7.2.

A G21 needle, 1.5 bar pressure, and various time values are used to optimize the amount of underfill material dispensed. The underfill material is first dispensed on a silicon wafer surface (**Fig. 2.27a**). 1.5 bar pressure and 0.4-1.0 seconds time values are used for the dispensing tests (**Fig. 2.27b**). The diameter of the dispensed underfill dots is measured via a Keyence VKX-100 confocal microscope. It is clear from **Fig. 2.27b** that decreasing dispensing time decreases the volume of the underfill material.

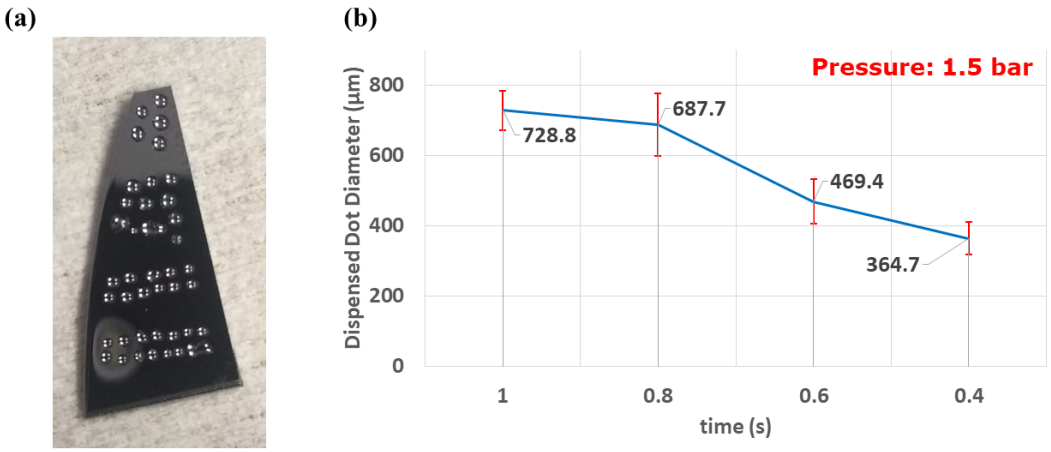


Figure 2.27: Underfill dispensing trial using the TPD tool. (a) Dispensed underfill dots on the silicon wafer surface, (b) Dispensed dot diameter vs. time plot.

An underfill process trial on a pseudo-ASICs pseudo-CMUT FCB structure is performed using 1.5 bar and 0.6 seconds as the TPD parameters. A G21 needle is used for the trial. Four dots, with the "L" shape approach, are dispensed to the edge of the pseudo-ASIC chip from the longer side and shorter side, as shown in **Fig. 2.28a**. The underfill material flowed through the gap due to the capillary effects and reached the other side of the pseudo-ASIC chip. **Fig. 2.28b** depicts optical microscope images after completing the underfill dispensing and capillary flow. The FCB structure is left for 3 days in the cleanroom in order to cure the underfill material at room temperature. Then, the FCB structure is also examined via SEM imaging. **Fig. 2.29** shows SEM images of the FCB structure, and the gap between the chips is filled with the underfill material.

The electrical resistance of the FCB structure was known prior to underfilling and is measured by the SCS tool after the underfill process. Before the experiment, the average resistance value was 45.4 $\pm$ 13 Ω. After the experiment, the average resistance value was 76.8 $\pm$ 24 Ω. All of the 143 GSB connections were found to be conductive. Underfilling the FCB structure is understood to be possible with TPD dispensing, and the underfill fills the gap between the chips via

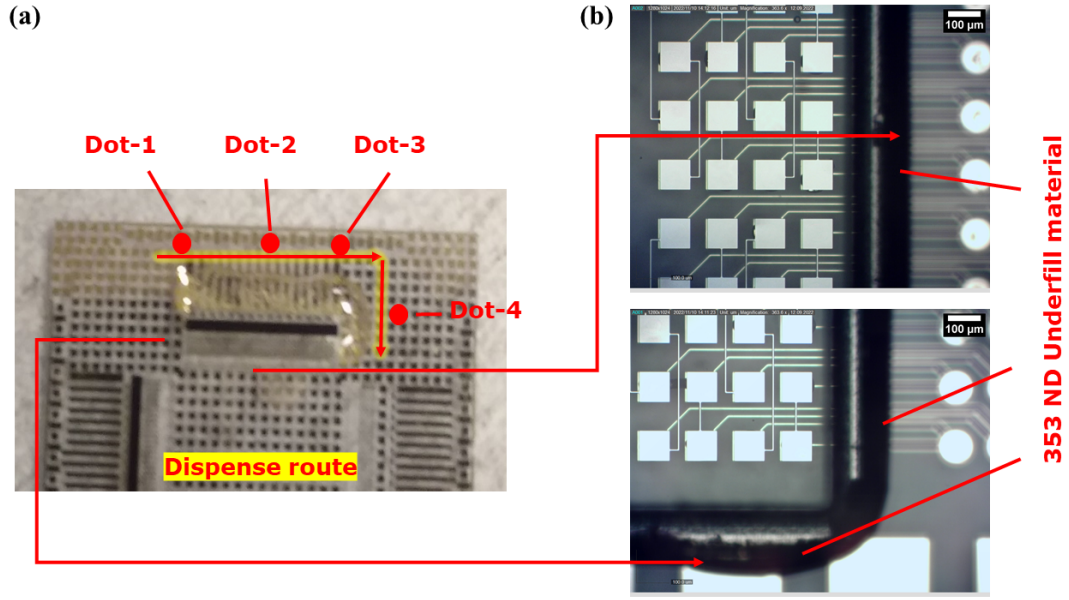


Figure 2.28: Underfill dispensing to the FCB structure. (a) The underfill material is dispensed using the route ("L" shape) highlighted by the red arrows, and 4 dots are dispensed to the edge of the pseudo-ASIC chip, (b) Optical microscope images of the FCB structure after the dispensing process.

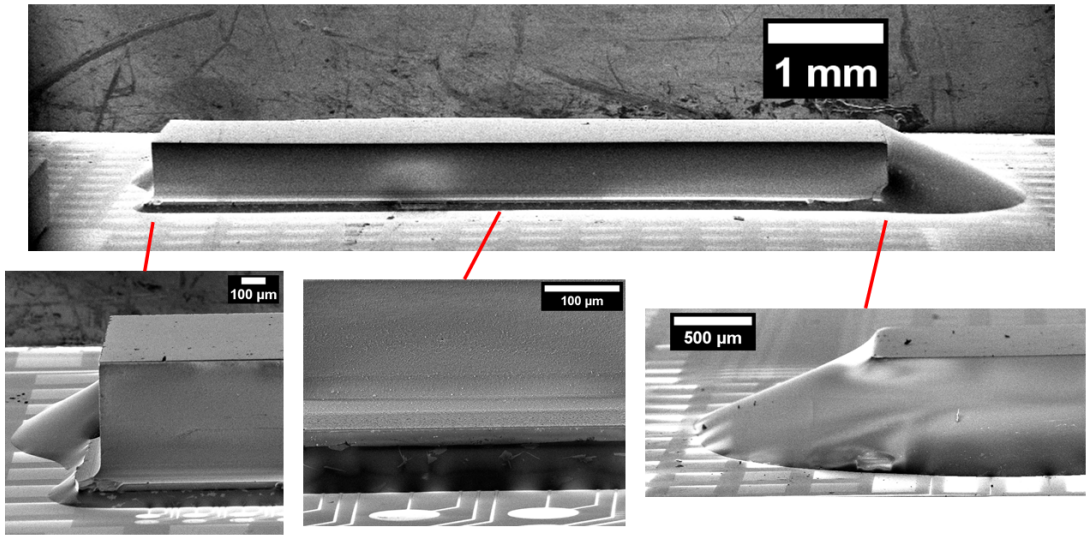


Figure 2.29: SEM images of the FCB structure after underfill dispensing and curing are completed.

capillary flow. It is also possible to cure the underfill material at room temperature. The FCB structure was 100 % conductive before and was also 100 % conductive after the underfill process.

Parylene C coating is another technique to protect the FCB structure from external effects. Parylene is a polymer, biocompatible, and non-conductive material [81]. The Parylene C coating is a conformal coating applied by a vapor deposition system under vacuum at room temperature and encapsulates all exposed surfaces [82].

The real ASIC-CMUT FCB structure comprises 2 ASIC chips bonded by the TSFCB process and a Pyrex CMUT chip. The Pyrex CMUT chip comprises a Si device layer (of an SOI wafer) and a Pyrex bottom substrate. An anodic wafer bonding process bonds the Si device layer of an SOI wafer to the bottom Pyrex substrate. There are metal wiring features on the bottom Pyrex substrate. Due to the existence of the metal features, the anodic wafer bonding process cannot seal the CMUT chips. Thus, there is air inside the gaps of the CMUT chips. The air must be evacuated, and the CMUT cells must be sealed under the vacuum to operate. Since the Parylene C coating encapsulates the whole surface under vacuum conditions, the gap of a CMUT cell can be sealed and the ASIC-CMUT FCB structure can be encapsulated simultaneously with the Parylene C coating. Therefore, the Parylene C coating is selected to seal the CMUT cells and to protect the FCB structure simultaneously at one step.

Since Parylene C encapsulates the whole surface, PCB pads and the back side of the CMUT must be protected during the coating. To protect the PCB pads and the back side of the CMUT chip, a dicing tape (Adwill-D-628, UV curable dicing tape) is attached to the PCB pads and the back side of the CMUT chip before the Parylene C coating (**Fig. 2.30**). The Parylene C coating is performed at METU MEMS Lab.

When the coating is completed, the dicing tape on the PCB pads and the back side is removed after applying UV light with a dose of 300 mJ/cm^2 to the dicing tape.

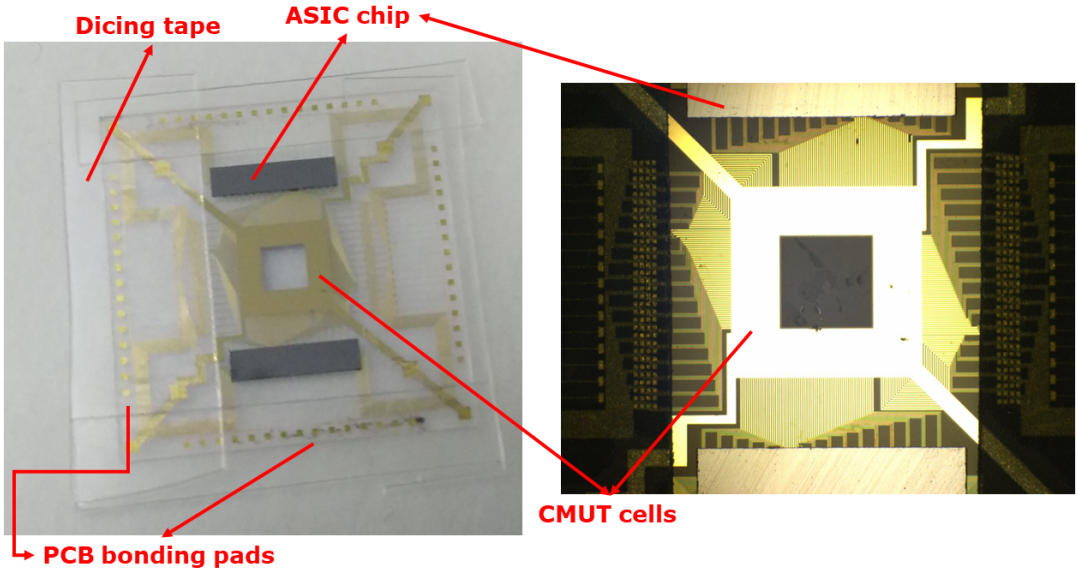


Figure 2.30: Dicing Tape covering of the PCB bonding pads of the CMUT chip before the Parylene C coating.

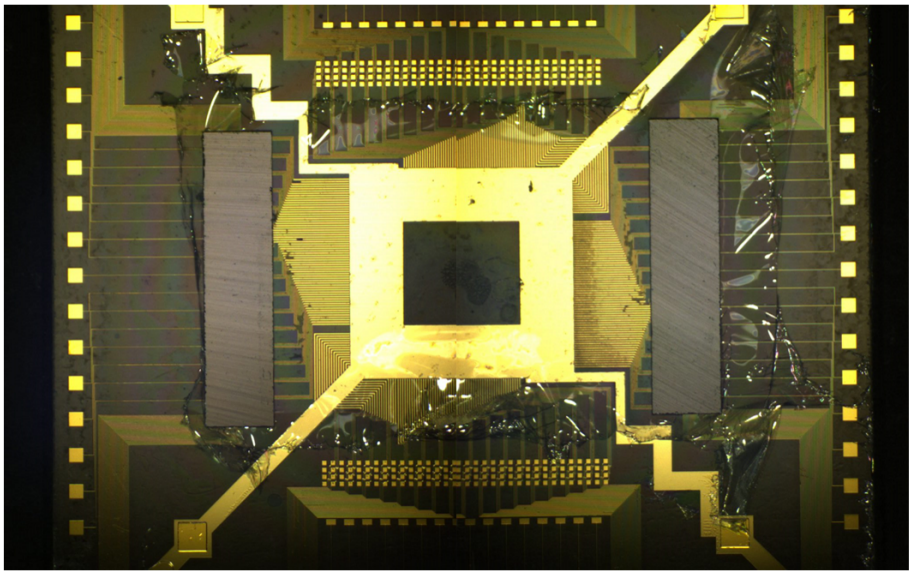


Figure 2.31: The CMUT chip after the Parylene C coating and removal of the masking tape.

Fig. 2.31 depicts the CMUT chip and the Parylene C coating. Parylene material is located on the CMUT cells and the ASIC chips. There is no Parylene C material on the PCB bonding pads. This suggests that the CMUT cells are sealed. The ASIC-CMUT FCB structure is protected. The CMUT-PCB integration is possible due to uncoated PCB bonding pads.

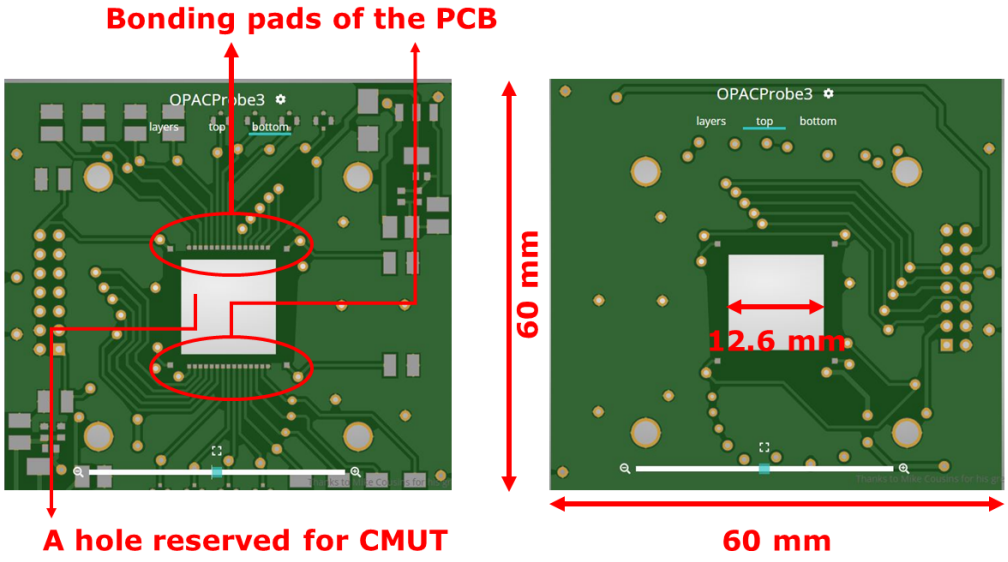


Figure 2.32: Design of the PCB.

2.6 CMUT - PCB Integration

2.6.1 Design and fabrication of the PCB

A PCB is designed by Prof. Dr. Abdullah Atalar to supply energy to ASIC-CMUT integrated structures and to process generated signals at the CMUT cells. Dimensions of the PCB are 60 x 60 x 0.6 (thickness) mm. The PCB has two layers. A square hole in the middle of the PCB is reserved for CMUT chips. The dimensions of the hole are 12.6 x 12.6 mm. A green solder mask covers the PCB; the surface finish is hot air solder leveling (HASL). The components of the PCB and the soldering process details are given in Chapter 2.7.

There are 30 HASL surface-finished bonding pads reserved for CMUT bottom layer integration. There are 4 HASL surface-finished bonding pads reserved for CMUT top-layer integration. PCB bonding pads of the CMUT chips and the 30 HASL bonding pads have the exact dimensions (300 x 300 µm). A flip-chip bonding process will integrate the PCBs and the CMUT chips. The design of the PCB is shown in **Fig. 2.32**.

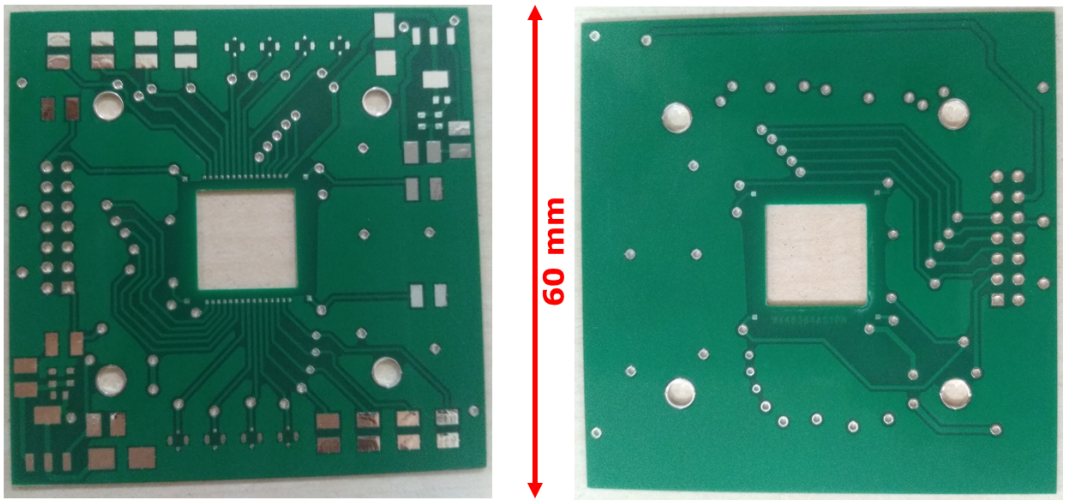


Figure 2.33: Fabricated real PCB.

The PCB is fabricated at PCBWay company in China from FR-4 material (glass fabric composite material) with a glass transition temperature (Tg) of 150 °C. The fabricated PCB is shown in **Fig. 2.33**.

2.6.2 Design and fabrication of the pseudo-PCB

In this thesis study, using milling techniques, pseudo-PCBs which are cheaper geometrical replicas of the real PCBs, are designed and fabricated to develop the CMUT-PCB integration process to reduce development costs and confirm the validity of the developed method. This very similar strategy was also followed during the ASIC-CMUT TSFCB process development. To fabricate the pseudo-PCB, a double-side copper-coated FR-4 material is used. The design of the PCB is completed by using L-edit software. Dimensions of the pseudo-PCB are the same as the real PCB, and the design is shown in **Fig. 2.34a**. Dimensions of the bonding pads of the pseudo-PCB are the same as the real PCB and the real CMUT chip. The alignment between the CMUT chip and the pseudo-PCB is shown in **Fig. 2.34b**, the alignment is tested and confirmed before the

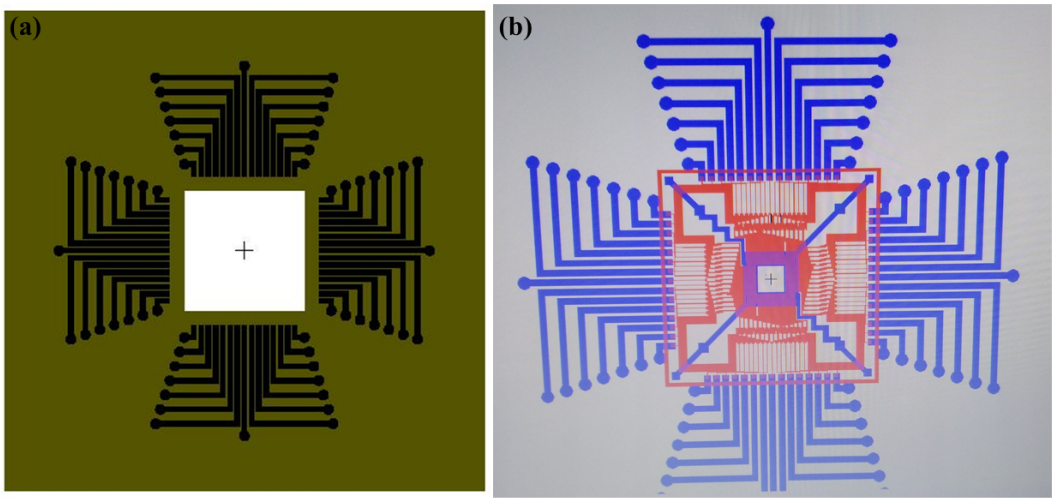


Figure 2.34: Design of the pseudo-PCB. (a) The structure of the top and the bottom layer is the same. (b) Alignment of the CMUT chip bonding pads and pseudo-PCB bonding pads.

fabrication.

Features of the CMUT chips are located on the front side. When a CMUT chip is flip-chip bonded to a PCB, the features of the CMUT chips and the features of the PCB will be on different surfaces. Therefore, the pseudo-PCB has 2 layers. Bonding pads of the pseudo-PCB are connected to through vias by copper traces. It is possible to connect the bottom and the top layer electrically by the through vias. The connection between the top and the bottom layer will be ensured by soldering copper wires inside through vias. The pseudo-PCBs are fabricated by LPKF S62 milling machine, and fabricated pseudo-PCBs are shown in **Fig. 2.35**.

2.6.3 FCB process design for CMUT – PCB integration

To integrate CMUT chips onto PCBs, a suitable flip-chip bonding technique must be selected. Two ASIC chips are already bonded to a CMUT chip until this step

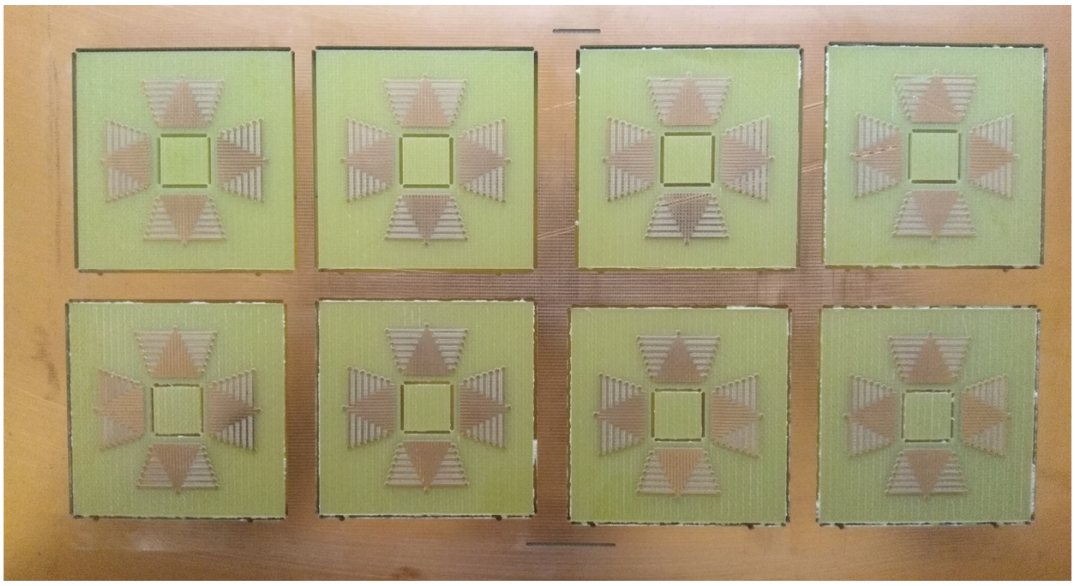


Figure 2.35: Fabricated pseudo-PCBs.

via the TSFCB technique. Therefore, during the CMUT-PCB integration, bonding between the ASIC and the CMUT must be preserved. Also, the anodic wafer bonding of the CMUT chip must be maintained as well to protect the functionality of the CMUT. Below is the list of the process requirements of CMUT-PCB integration:

I. Although the ASIC-CMUT bonding interface is protected by underfill epoxy material or Parylene C material, applying high force during the CMUT-PCB integration may damage the bonding of ASIC-CMUT. Low-force processing capability is needed.

II. Applying high temperatures may damage the ASIC-CMUT bonding interface. Low-temperature processing capability is needed.

III. Applying ultrasonic energy may damage the ASIC-CMUT bonding interface. In addition, a specifically designed die collet must be required for the top die to perform the TSFCB process. During this study, there is no specifically designed die collet for the CMUT chip. Thus, performing a TSFCB is impossible and unsuitable to bond the CMUT chip onto the PCB.

IV. Bonding pads of the CMUT is gold, and the bonding pad of the PCB is HASL solder material. Thus, the metallurgy of these bonding pads is different. A conductive interface material suitable for bonding different metallurgical surfaces must be selected.

Considering the abovementioned requirements, flip-chip bonding using isotropic conductive adhesive (ICA) is one of the most suitable techniques for integrating CMUT chips onto PCBs. ICA is a composite material comprised of a polymer epoxy resin and conductive fillers [83]. Conductive fillers are dispersed in the epoxy resin matrix. To ensure conductivity, the weight percentage of the conductive filler material must exceed the critical percolation limit. The percolation theory states that when the conductive filler material exceeds the critical percentage weight limit, fillers create a 3D network within the polymer matrix [57]. Therefore, isotropic electrical conductivity occurs. ICAs are thixotropic, shear thinning, and non-Newtonian materials [84]. The thixotropy comes from aggregation of the suspended conductive fillers [85]. ICAs contain 80 % weight or more conductive fillers to exceed the critical percolation limit to have conductivity [58]. The viscosity behavior of ICA is usually compatible with the Herschel-Bulkley fluid model [86]. Therefore, ICAs have yield stress. Below the yield stress, ICAs do not flow and behave like a solid [87]. Due to the non-Newtonian behavior of ICAs, it is very difficult to model the flow of ICAs [88]. A summary of the models developed for the fluid dispensing of non-Newtonian fluids can be found in Ref. [89]. Instead of working on modeling the fluid dispensing of ICAs, an empirical modeling approach could be more useful [90].

Usually, they are sold in two separate boxes that contain resin and hardener. Long pot life, good conductivity, viscosity behavior of the material, low outgassing, biocompatibility, maximum operating temperature, and curing temperatures are critical parameters that need to be considered to choose [91].

ICAs are lead-free alternative replacements of solder materials developed for thermally sensitive components. They have applications on chip-on board, chip-on glass, multi-chip modules, and flip-chip bonding [92]. FCB with ICAs offers low force [93] and low-temperature [94, 95] processing. ICAs also benefit the

bonding of different metallurgical surfaces. Usually, GSB is used for the top chip, and the GSBs are embedded into the ICA epoxy material. After the top chip and the bottom chip are brought into contact by GSB and ICA, curing of the ICA is performed. As a result, embedded GSB into the ICA are bonded permanently. Haberland et al. used an ICA and coined GSBs to perform an FCB process. GSBs are dipped into the ICA material prior to the FCB process [59]. Haberland et al. suggest that the ICA can be dispensed on the bonding pad [59].

Reinert et al. used coined GSBs and ICA material to perform an FCB process, and they concluded that the GSBs and ICA combination is very suitable for R&D and small series production [60]. Zhong et al. combined coined GSBs and a silver-filled ICA by dip transfer to integrate chips by an FCB process at 120 °C and concluded that increasing the height of the GSBs increases the tolerance of the FCB process [55]. Clayton et al. worked on GSB and ICA combination to perform an FCB process at 80 °C. They observed that the amount of ICA is critical to avoid short connections, and the height of GSB is essential to creating good contact with the ICA. To increase the height of GSBs, they decided to work with stacked GSBs. Increasing the total height is helpful to avoid short connections and ensures good contact between ICA and GSB. According to Clayton et al., the minimum ICA dot size that can be fabricated by a time-pressure dispensing (TPD) is 125 µm [96]. According to Wong et al. FCB with ICA is well suited for multilevel FR4 substrates in combination with surface-mount devices (SMDs), and ICAs can work with large material combinations [91]. Ref. [97] suggests that a time-pressure dispenser (TPD) can dispense ICAs to PCB pads.

It is understood from the literature that ICA and GSB combination can be used to perform FCB of CMUT and PCB. Low temperature and low force possibilities are well suited for protecting the CMUT chip and the ASIC-CMUT FCB interface. A time-pressure dispenser can dispense the ICA to the PCB bonding pads, or even the ICA can be applied manually by a paintbrush to the PCB bonding pads due to having relatively large, 300 x 300 µm bonding pads. Stacked GSB fabrication can be performed on the CMUT PCB bonding pads. A selected ICA can bond GSBs to HASL PCB bonding pads. Therefore, it is decided to work with the ICA-GSB combination for the CMUT-PCB FCB integration process.

Property	H20E
Pot life (days)	2.5
Biocompatibility	Yes
Low outgassing	Yes, NASA approved
Conductivity (ohm-cm)	0.0004
Viscosity (cP.s)	2200-3200
Maximum operating temperature (°C)	200
Curing Schedule-1	175 °C - 45 seconds
Curing Schedule-2	150 °C - 5 minutes
Curing Schedule-3	120 °C - 15 minutes
Curing Schedule-4	100 °C - 2 hours
Curing Schedule-5	80 °C - 3 hours

Table 2.12: Properties of H20E ICA material.

2.6.4 Selection, characterization, and application of the ICA material (EPO-TEK H20E Conductive Paste)

Suitable ICA material from many candidates is found at EPO-TEK company. H20E ICA material is chosen for CMUT-PCB integration due to its superior pot life, good conductivity, low outgassing, biocompatibility, maximum operating temperature, and available low-temperature curing schedules. **Table 2.12** shows the properties of the H20E [98].

To validate the viscosity behavior, the viscosity of the H20E is measured at room temperature by a rheometer (MCR-301 Anton Paar). Regression analyses are completed to model the viscosity behavior of the H20E. In **Fig. 2.36a**, it is shown that the best regression is the Herschel-Bulkley model for the H20E, and the yield stress is 85.6 Pa. It is also observed in **Fig. 2.36b** that the viscosity decreases with increasing shear rate and confirms that the H20E shows shear thinning.

When the external force exceeds the yield strength, the H20E will flow. Therefore, applying too much pressure can lead to the overflow of the material and can create electrical shorts between adjacent bonding pads.

H20E must be selectively applied only on the bonding pads of the PCB. There

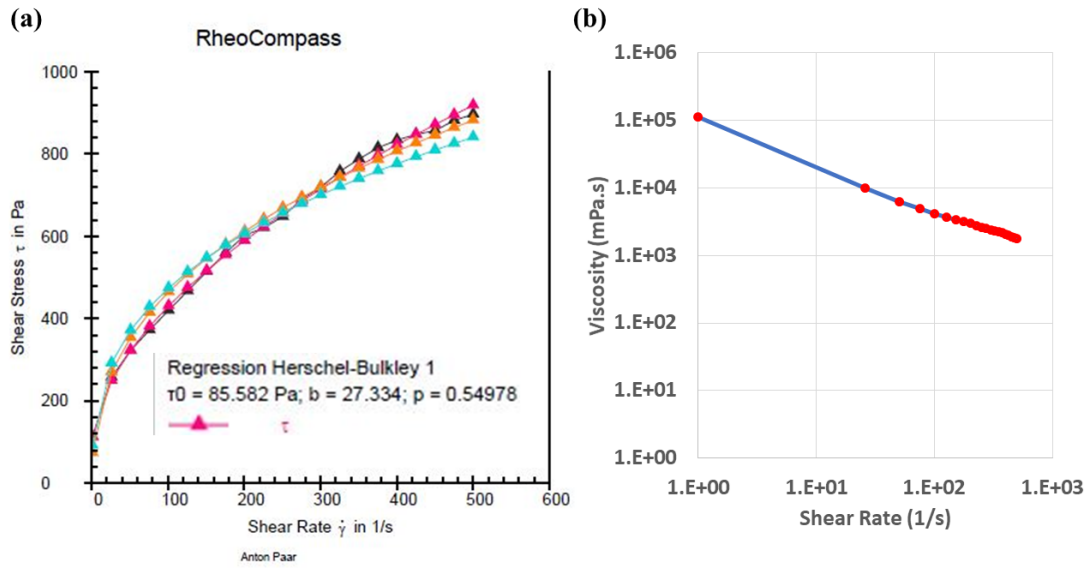


Figure 2.36: (a) Regression analysis after viscosity measurement of the H20E ICA material (at room temperature), (b) Viscosity (mPa.s) vs shear rate (1/s) graph of H20E.

are two ways to dispense selectively. One uses a time-pressure dispenser (TPD), and the other uses a paintbrush.

The TPD trials were carried out by Fluidmatic 1000T time-pressure dispenser machine. Details about the machine are given in Chapter 2.7.2. Dispensing experiments with various pressure and time parameters were performed on a Pyrex surface to optimize the TPD of the H20E (**Fig. 2.37a**). A G27 needle was used for all dispensing trials. 1 bar 0.5 s, 1 bar 0.4 s, 1 bar 0.3s, 1 bar 0.2 s, 1 bar 0.1s, and 1.5 bar 0.3 s TPD parameters were used, and 10 H20E bumps were created with the TPD parameters. The height of the H20E bumps was measured using a Keyence VKX-100 confocal microscope (**Fig. 2.37b**).

It is observed that decreasing time value decreases the average height of the H20E bumps. In addition, for the same time value, increasing the pressure value increases the average H20E bump height. The change of the H20E bump height according to TPD dispensing parameters is shown in **Fig. 2.38**.

The TPD machine is located outside of the used cleanroom facility. It is

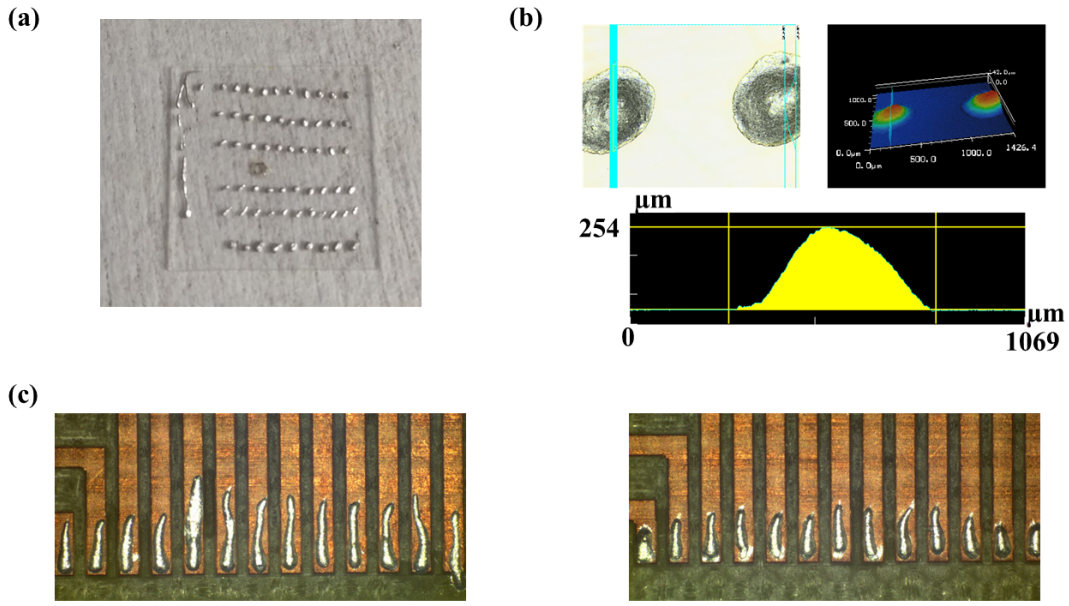


Figure 2.37: TPD optimization of H20E. (a) TPD Trial with various pressure and time value on a Pyrex surface, (b) H20E bump material height measurement via Keyence VKX-100 confocal microscope, (c) H20E bumps on the bonding pads of the pseudo-PCB.

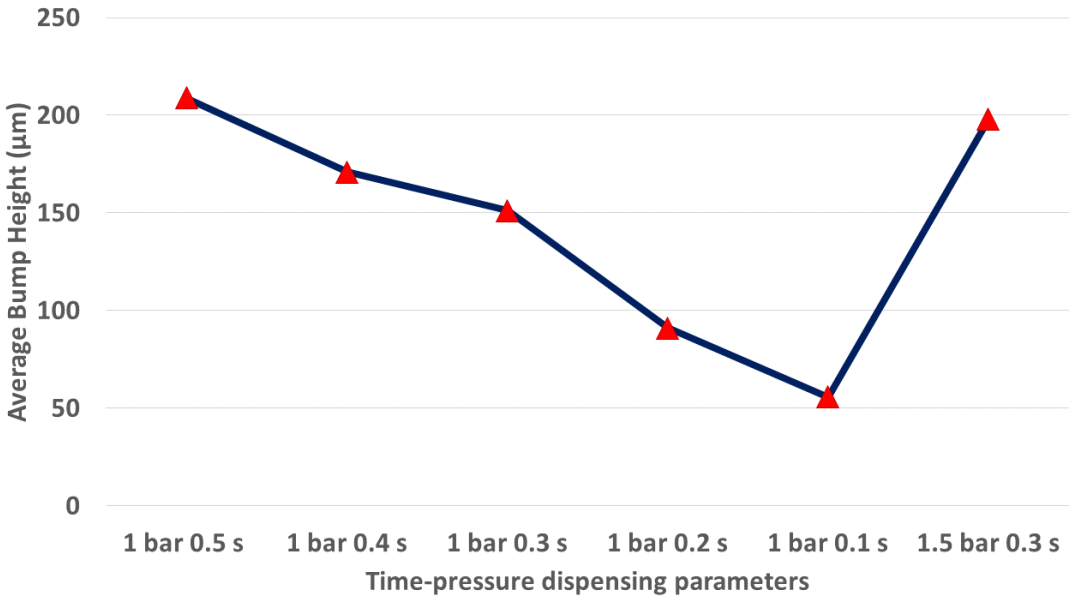


Figure 2.38: Change in the average bump height according to the change in the TPD dispensing parameters.

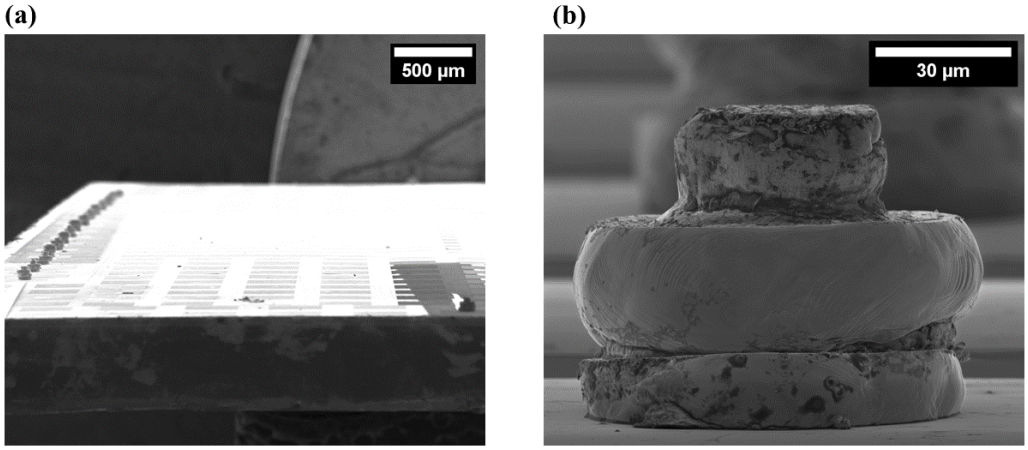


Figure 2.39: SEM images of stacked GSB. (a) Stacked GSB on the PCB pads of the pseudo-CMUT chip, (b) A stacked GSB structure image.

decided that a paintbrush can also be used to dispense H20E bumps inside the cleanroom to avoid contamination.

2.6.5 Fabrication of the stacked GSBs

Since the CMUT chip bonding pads are gold, GSB can be formed via the stud bump bonding technique. GSB can be embedded into ICA material to simultaneously create electrical connections and strong mechanical connections. GSB can also work as a mechanical stopper/displacement limiter during the FCB process. GSB can avoid the overflow of the ICA material by controlling the stand-off distance between the CMUT chip and the PCB. It is decided that a stacked GSB can have a higher height value and be more secure during the FCB process to avoid the overflow of the ICA material. The stud bump bonding technique can fabricate the stacked GSB. After forming the first GSB, another can be formed on top of the prior one.

Stacked GSBs are fabricated using the parameters in **Table 2.13** with the

	GSB1		GSB2	
	Bond1	Bond2	Bond1	Bond2
Ultrasonic Power (mW)	200	0	200	0
Ultrasonic Time (ms)	200	0	200	0
Force (mN)	250	5	250	5
Temperature (°C)	120	120	120	120
EFO (%)	40	N/A	40	N/A
UPCO (µm)	N/A	375	N/A	375
Loop up (µm)	120	N/A	120	N/A
Loop y-axis (µm)	50	N/A	50	N/A

Table 2.13: Stud bump bonding parameters of the Stacked GSB.

same wire bonder (TPT HB16). SEM images of the stacked GSBs on the PCB pads of a pseudo-CMUT chip are shown in **Fig. 2.39a**. A close SEM image of a stacked GSB structure is also given in **Fig. 2.39b**.

Stacked GSB will be embedded in the ICA material during the FCB process. An increased contact area between the ICA material and the stacked GSB is critical for successful mechanical and electrical integration. Therefore, a coining process can flatten the surface area on top of the stacked GSB before the FCB process to increase the contact surface area for better mechanical and electrical integration with the ICA material.

2.6.6 Force-controlled coining of the stacked GSBs

Displacement-controlled coining process approach is not preferred this time due to the presence of the ASIC chips on the CMUT chip. The thickness of the ASIC chip is 500 µm. The expected stacked GSB height is around 60-100 µm. The stacked GSB is shorter than the ASIC chip. When a flat surface is used for the coining, the flat surface will be in contact with the ASIC chip rather than the stacked GSB. Thus, to perform a coining process on the stacked GSB, a force-controlled coining process is selected.

Standard die collet (SDC), shown in **Fig. 2.40a**, is selected to hold the CMUT

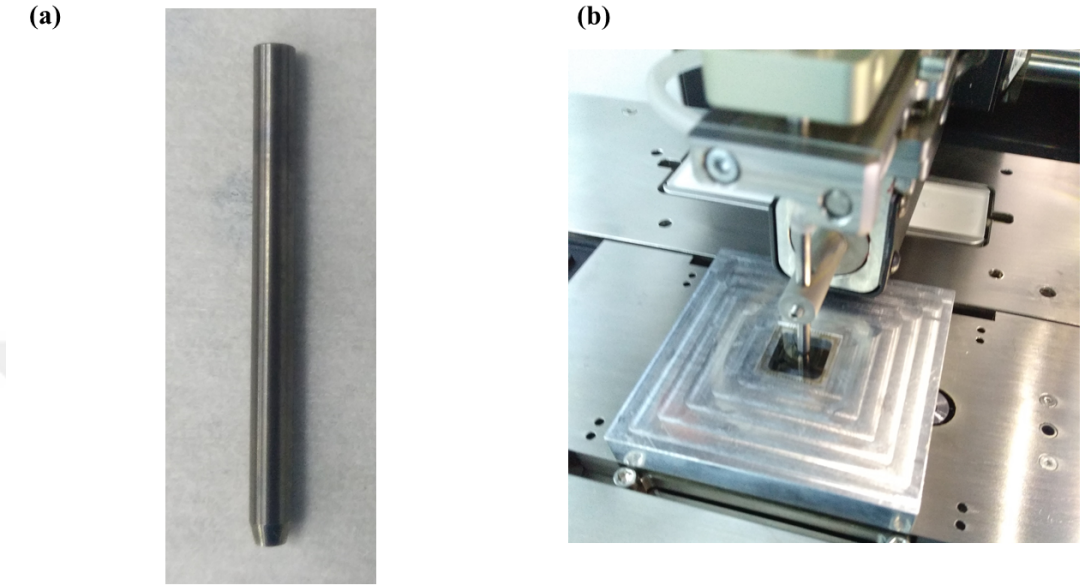


Figure 2.40: (a) Standard die collet (SDC), (b) force-controlled coining of the stacked GSB.

chip. SDC is made of stainless steel material. The height of the SDC is 36.85 mm. The diameter of the SDC is 3.15 mm. The SDC holds the CMUT chip with a vacuum hole with a diameter of 400 µm.

A 66 x 66 mm aluminum part with a 9 mm thickness is selected as a flat surface for the force-controlled coining process. There is a 12.6 x 12.6 mm hole in the middle of the aluminum part, which is suitable for the position of the ASIC chips on the CMUT chip. The hole avoids contact of the ASIC chips with the flat aluminum surface and ensures that only stacked GSBs will be in contact with the flat surface.

In this thesis study, to perform the force-controlled coining process, the stacked GSBs on the PCB bonding pads of the CMUT chip are pressed with 10 N normal force against an aluminum part, as shown in **Fig. 2.40b**.

Optical microscope images of the stacked GSBs are shown in **Fig. 2.41**. Before the coining process, no flat surface was on top of the stacked GSBs (**Fig. 2.41a**). After coining, flat surfaces are created on top of the stacked GSBs (**Fig.**

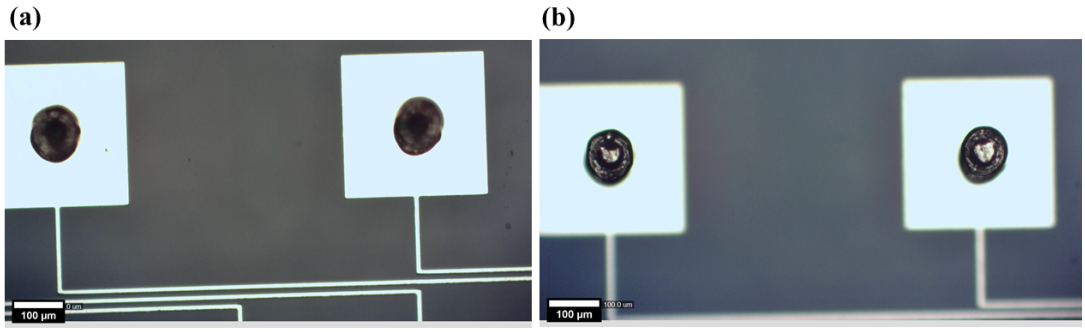


Figure 2.41: Stacked GSB on the PCB bonding pads of the CMUT chip. (a) Stacked GSBs before the coining process, (b) Stacked GSBs after the coining process.

2.41b).

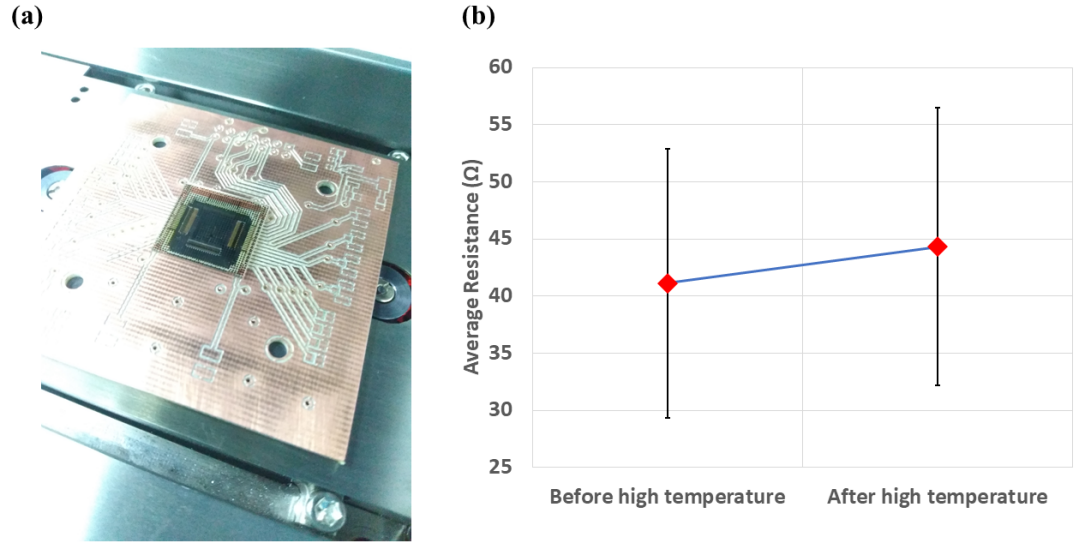


Figure 2.42: Subjecting pseudo-FCB structure to 80 °C temperature. (a) Pseudo-FCB structure is on the pseudo-PCB during the heating process, (b) Resistance values of the pseudo-FCB structure before and after subjecting to high temperature.

2.6.7 FCB integration trial of the pseudo-CMUT and pseudo-PCB

As mentioned earlier in Chapter 2.6.1, the Tg value of the PCB is 150 °C. However, the maximum service temperature of ASIC – CMUT flip-chip bonding is unknown. To test the behavior of the flip-chip bonding of pseudo-ASIC and pseudo-CMUT at high temperatures, a thermo-sonic flip-chip bonded pseudo-ASIC pseudo-CMUT structure is subjected to an 80 °C temperature for 3 hours. The structure is put on a pseudo-PCB, and the pseudo-PCB is heated by the heated stage of the flip-chip bonder from the bottom (**Fig. 2.42a**). Resistance of the structure before subjecting to high temperature was 41 ± 11 Ω. The structure's resistance after the high temperature was 44 ± 12 Ω (**Fig. 2.42b**). The resistance values are very similar and suggest no significant effect of 80 °C temperature on the flip-chip bonded pseudo-ASIC and pseudo-CMUT structure.

The TPD machine was used to dispense H20E bumps on the PCB bonding pads

of a pseudo-PCB (**Fig. 2.37c**). 1 bar, 0.3 s, and G27 needle TPD parameters were used. The average height of the H20E bumps was 111 µm, measured via Keyence VKX-100 confocal microscope. Furthermore, stacked GSBs were bonded on the PCB bonding pads of a pseudo-CMUT chip with no ASIC chip. The stacked GSBs were coined by the force-controlled coining approach. 10 N normal force is applied during the coining process. The average height of the stacked GSBs was 68 ± 3 µm and was measured via SEM imaging.

The flip-chip bonder aligned the pseudo-CMUT chip and the pseudo-PCB. The pseudo-CMUT chip was put on the pseudo-PCB by the SDC tool. After the initial contact, the FCB process was completed by applying 1 N of normal force at 120 °C curing temperatures for 15 minutes (**Fig. 2.43a**). The integrated structure of pseudo-CMUT and pseudo-PCB is shown in **Fig. 2.43b**. There was no misalignment or electrical short connections due to the overflow of the H20E ICA material (**Fig. 2.43c**). It was observed that the pseudo-CMUT chip was attached to the pseudo-PCB mechanically. To measure the electrical conductivity, connections between the top and the bottom layer must be soldered.

Copper wires were inserted into each through holes. SAC 305 alloy (Indium Corporation) solder material was dispensed using the TPD tool to the top and bottom through hole entries. The solder material is reflowed with a soldering station (YIHUA 853AAA+) to complete the soldering of the pseudo-PCB. Details of soldering are given in Chapter 2.7.

To measure the electrical conductivity, the 2-Probe resistivity measurement technique was used. SCS tool performed the measurement. The average resistance value was 93.3 ± 34.3 Ω. All of the connections were conductive.

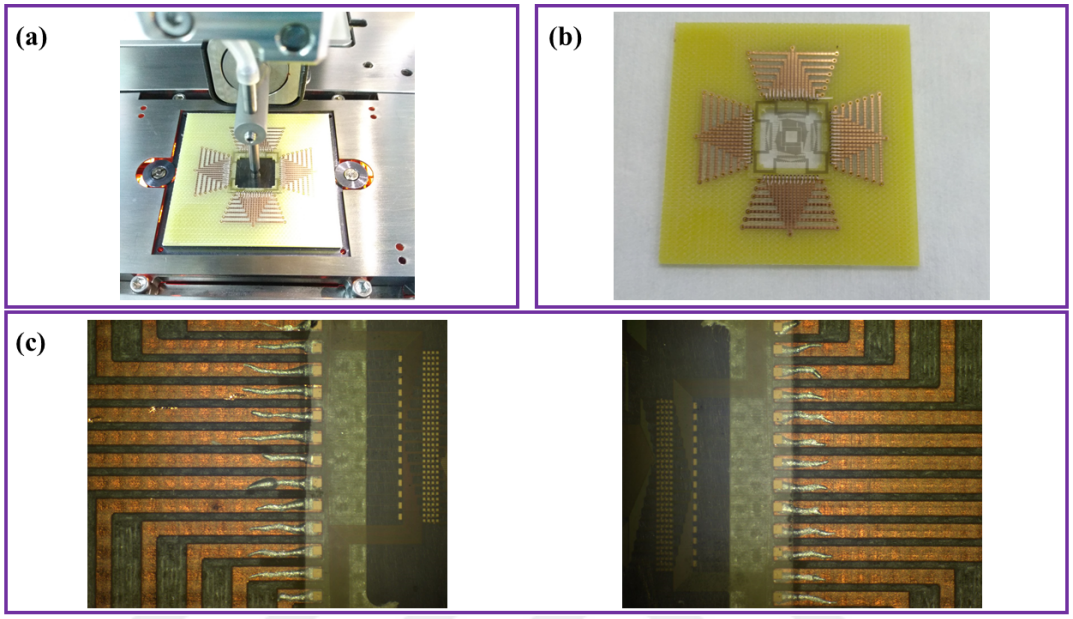


Figure 2.43: Pseudo-CMUT pseudo-PCB FCB process. (a) FCB process at 1 N force, 120 °C curing temperature for 15 minutes, (b) Pseudo-CMUT pseudo-PCB structure after the FCB process, (c) Alignment between the bonding pads after the FCB process.

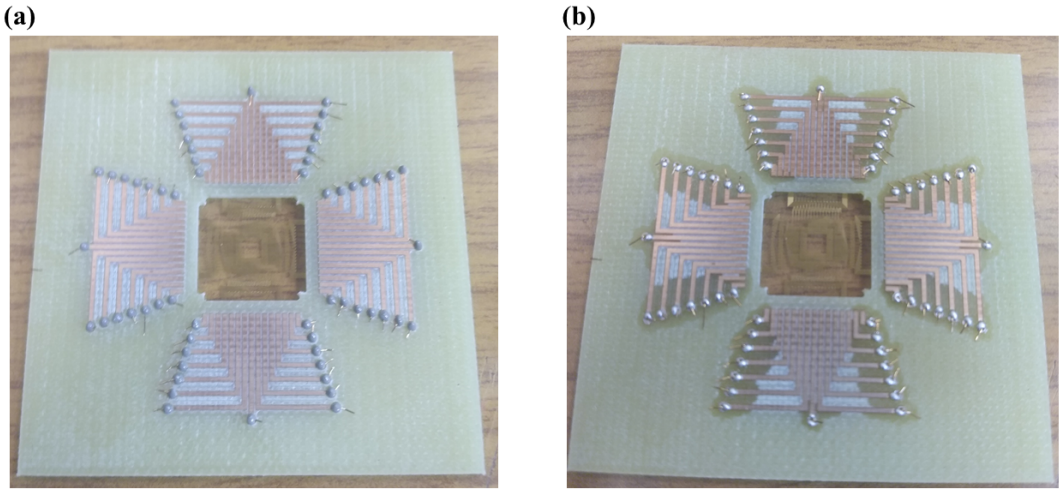


Figure 2.44: Soldering of pseudo-PCB. (a) Inserting copper wires into through holes and dispensing the solder material, (b) Reflowed solder materials.

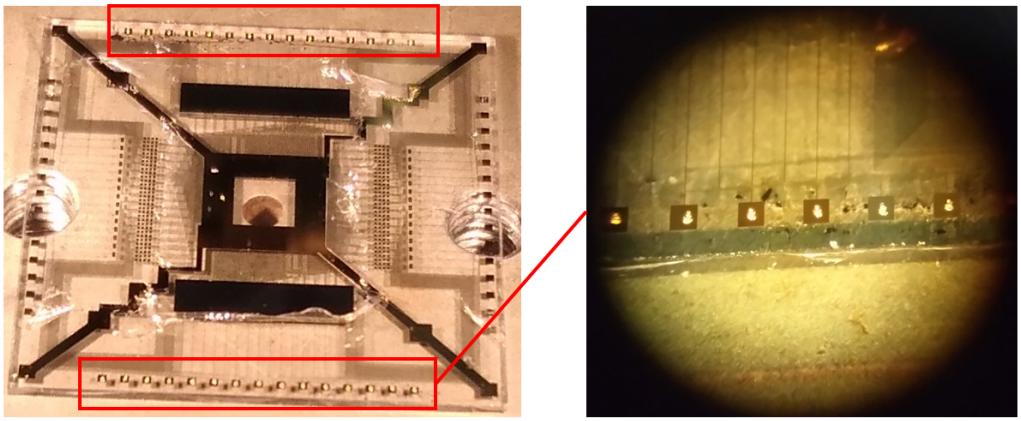


Figure 2.45: Stacked GSBs on the PCB pads of the real CMUT chip.

2.6.8 FCB integration of a real CMUT and a real PCB

A real CMUT chip with 2 real ASIC chips is selected for the CMUT – PCB FCB integration process. The CMUT chip is sealed with the Parylene C coating previously. Stacked GSBs were bonded to 30 PCB bonding pads of the CMUT chip using parameters are given in **Table 2.12** (**Fig. 2.45**). The stacked GSBs were coined by the force-controlled coining approach. 10 N normal force is applied during the coining process.

SMD (Surface-mount devices) components of the PCB were soldered before the FCB integration due to the necessity of high temperature during the soldering. There is a 7x2 IDC connector component of the PCB. The IDC connector is a through-hole component. The IDC connector has to be soldered after the FCB integration to have a flat PCB on the heated stage of the flip-chip bonder. The presence of the IDC connector creates a tilt, and the FCB process cannot be performed on a tilted PCB surface. Details of soldering the PCB components are given in Chapter 2.7. The real PCB prior to the FCB process is shown in **Fig. 2.46a**.

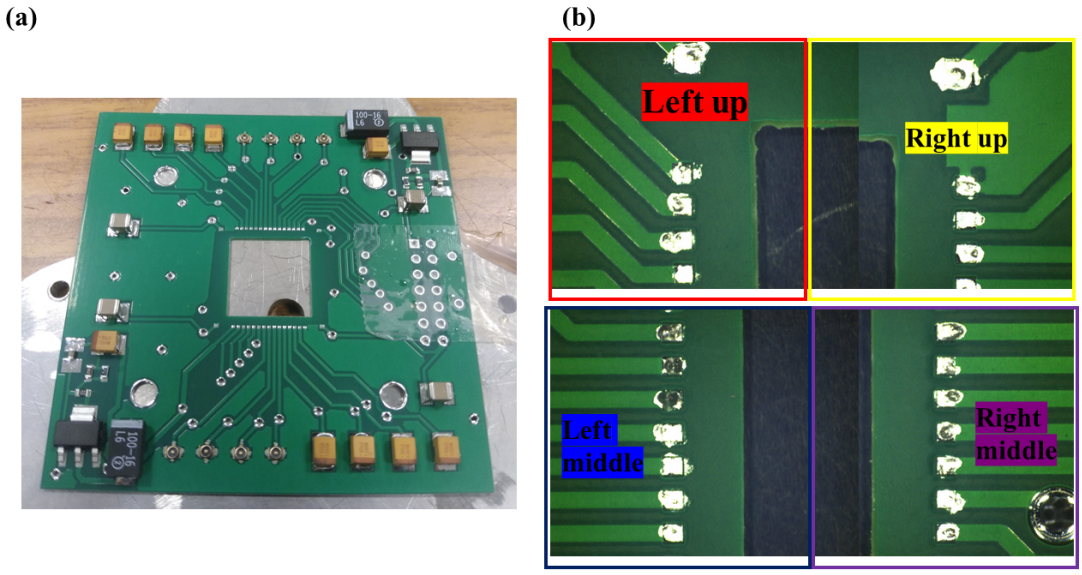


Figure 2.46: (a) The real PCB with soldered SMD components prior to FCB integration, (b) Conductive paste bumps were dispensed by a paintbrush on the PCB bonding pads.

A paintbrush was used to dispense the H20E onto the PCB bonding pads of the real PCB. Since the paintbrush was used to dispense the H20E, conductive paste bumps were placed on the PCB pads inside the used cleanroom. Therefore, the risk of contamination decreased. Various PCB pads of the real PCB with the H20E are shown in **Fig. 2.46b**.

The flip-chip bonder aligned the real CMUT chip and the real PCB. The real CMUT chip was put on the real PCB by the SDC tool. After the initial contact, the FCB process was completed by applying 1 N of normal force at 80 °C curing temperatures for 3 hours. There was no misalignment or electrical short connections due to the overflow of the H20E (**Fig. 2.47**). It was observed that the real CMUT chip was attached to the real PCB mechanically. 30 PCB pads and 4 device layer pads are integrated. The integrated structure of the real CMUT and real PCB is shown in **Fig. 2.48**.

After the CMUT – PCB integration process, the ASIC chips, the CMUT chip, and the PCB are mechanically and electronically connected. Finally, the 7x2

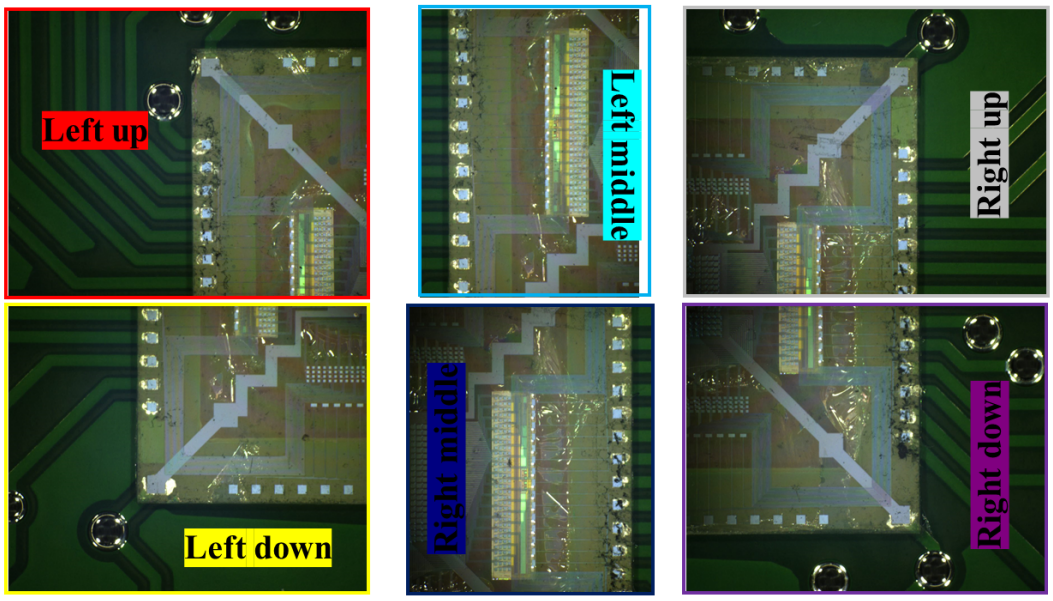


Figure 2.47: Alignment between the real CMUT chip and the real PCB after the FCB process.

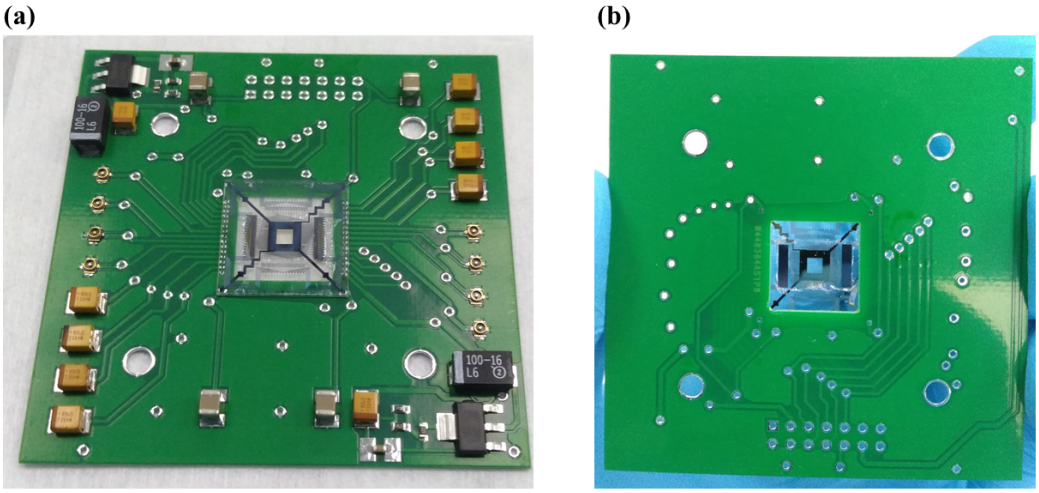


Figure 2.48: CMUT-PCB integrated structure. (a) Front side of the PCB, (b) Back side of the PCB.

IDC connector soldering and the wire bonding of the device layer steps need to be performed. Then, the whole structure will be ready to be assembled into the probe.

2.7 PCB Component Soldering and Wire Bonding of the Device Layer

2.7.1 The Prototype PCB for alignment control

In the probe design, the PCB is positioned on an aluminum surface. Four screws are used to attach the PCB to the aluminum part. To accommodate and protect the CMUT chip and the fiber, two aluminum parts are attached on top of the PCB right in the middle. PCB components had to be located in the perimeter of the two aluminum parts. Since the PCB stays on top of the aluminum part, all the components except a 7x2 IDC connector were chosen to be SMD (surface-mount devices). SMD PCB components ensure that connection will be only on the top layer of the PCB and avoid contact with the aluminum.

Prototypes of the PCB are fabricated at the Electrical and Electronics Department of Bilkent University. An LPKF S62 milling machine dedicated for PCB prototyping is used for the fabrication of the PCB prototypes. The alignment of the PCB components to the SMD positions and the alignment of the PCB to the aluminum probe parts was checked with the help of the prototype PCBs before the real fabrication of the PCB at PCBWay company (**Fig. 2.49**).

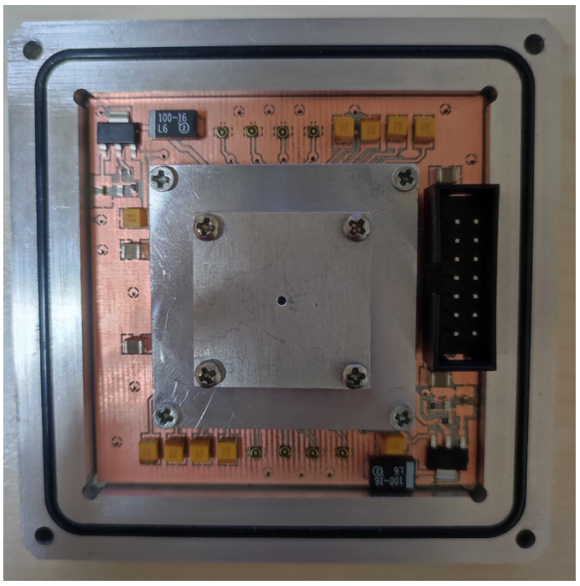


Figure 2.49: The prototype PCB is assembled into the probe, and the alignment of the PCB components is checked.

2.7.2 Time-pressure dispenser (TPD), the Solder material, and the Soldering Station

A time-pressure dispenser (TPD) is a machine that dispenses liquid or paste material by applying air pressure for a known amount of time. An air hose is connected to a polymer syringe. A needle is attached to the end of the syringe via a Luer lock fitting mechanism. The pressure, time and diameter of the needle are the adjustable parameters of the TPD [99].

A Fluidmatic 1000T time-pressure dispenser machine is used for dispensing underfill 353ND nonconductive epoxy material, H20E ICA material, and SAC 305 alloy (Indium Corporation) solder material. It has a syringe container. Needles can be put to the tip of the syringe. The syringe contains the fluid. The position of the syringe and the needle is adjusted manually by a human hand. Pressure, time, and diameter of the needle are the adjustable parameters. It is known in the literature that decreasing pressure or decreasing needle diameter, decreases dispensed fluid volume [100].

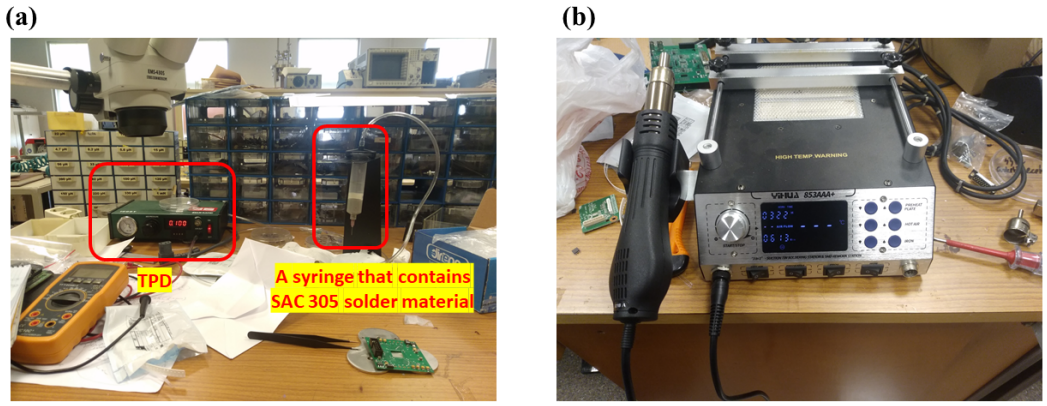


Figure 2.50: (a) The TPD and a syringe that contains SAC 305 solder material, (b) YIHUA 853AAA+ solder station.

A solder material of SAC 305 alloy from Indium Corporation is used to solder the PCB components. The TPD dispenses the solder material on the bonding pads. The TPD and a syringe that contains the solder material are shown in **Fig. 2.50a**.

A soldering station of the YIHUA 853AAA+ machine is used to reflow the solder material. The solder station is shown in **Fig. 2.50b**.

2.7.3 Soldering of the PCB components

SMD components of the PCB are soldered before CMUT – PCB FCB integration. First, the TPD tool dispenses the solder material to the HASL (hot air solder leveling) bonding pads. Second, the SMD components are placed on the surface. Third, hot air is applied by the solder station to reflow the solder material. 300 °C hot air was used during the reflow. The PCB components are given in **Table 2.14**.

No	Component name	Quantity
1	LM1117-ADJ SMD regulator	2
2	7x2 IDC Connector Receptacle	1
3	2.2 uF 100 V 1210 SMD capacitor	4
4	10uF 16V SMD polarized capacitor	10
5	100uF 16V SMD polarized capacitor	2
6	1 uF 16V SMD polarized capacitor	2
7	1.5K 603 SMD resistor	2
8	3.9K 603 SMD resistor	2
9	220 603 SMD resistor	2

Table 2.14: The PCB component list.

After soldering the SMD components, the PCB is ready for the CMUT – PCB FCB integration process (**Fig. 2.46a**). Soldering the components before the FCB integration is chosen to decrease the high-temperature exposure time of the CMUT – PCB bonding interface. After the CMUT – PCB FCB integration process, the 7x2 IDC through hole connector is soldered with the same approach. The soldering work of the real PCB is completed by soldering the 7x2 IDC connector. The PCB, shown in **Fig. 2.51**, is integrated with the ASIC chips - the CMUT chip structure and components are soldered.

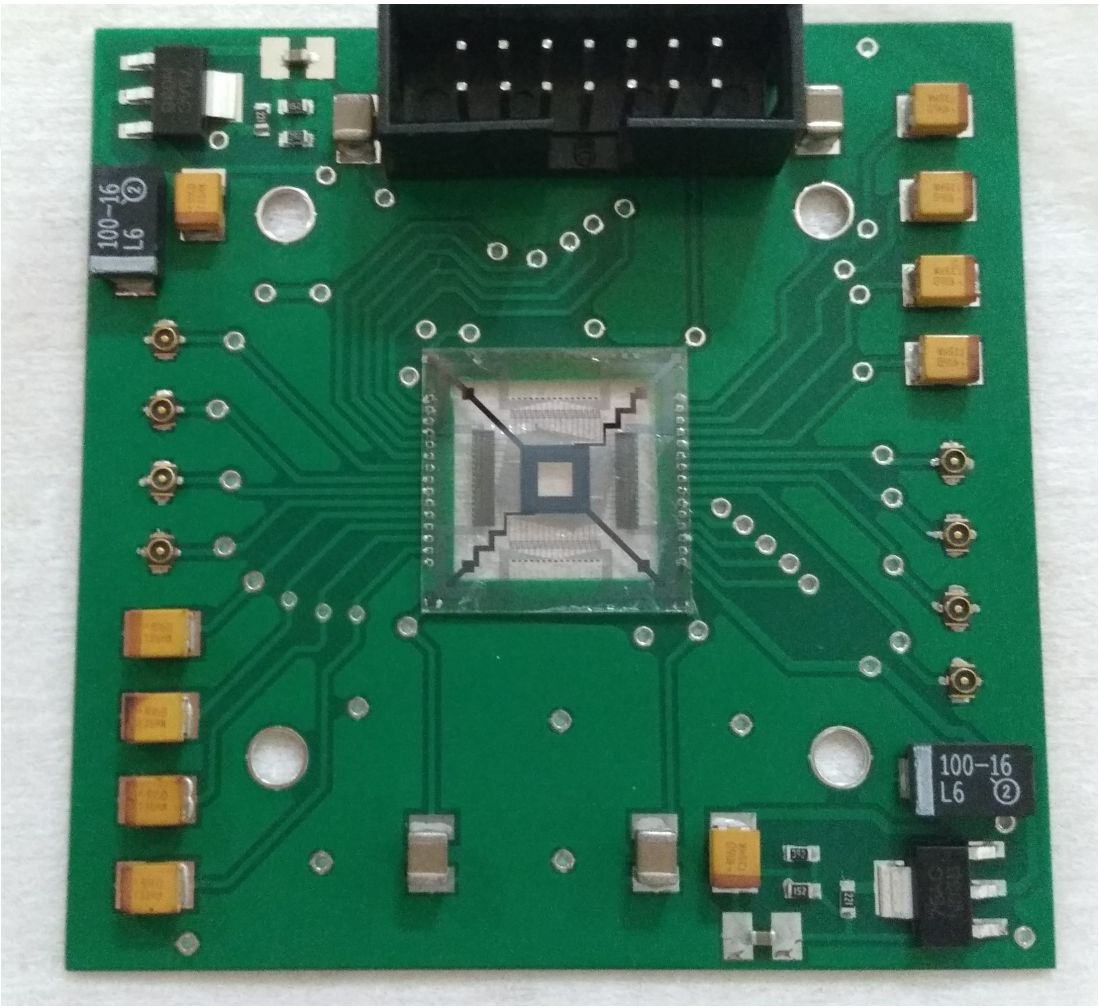


Figure 2.51: Photo of the real PCB after soldering work is completed. The PCB is integrated with the ASIC chips - the CMUT chip structure and components are soldered.

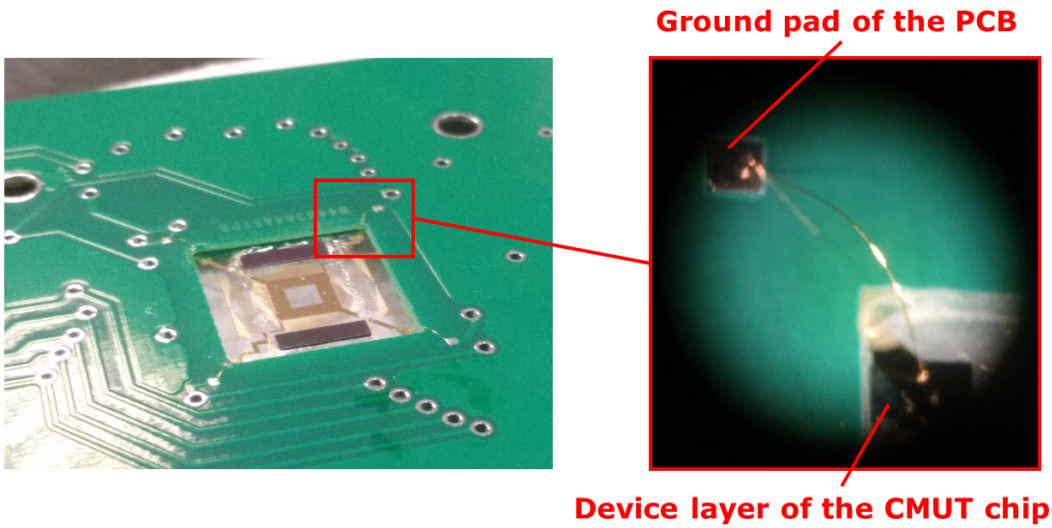


Figure 2.52: Wire bonding connection between the PCB ground pad and the device layer of the CMUT chip.

2.7.4 Wire Bonding of the device layer

The CMUT device layer is designed as the ground electrode. During the CMUT – PCB FCB integration, the H20E ICA material connects the CMUT device layer and the PCB for ground connection. Also, the same connection can be obtained using wire bonding as an alternative. A 25.4 µm diameter gold wire (Heraeus HA3) was used for the wire bonding process. Gold ball bonding was performed on the device layer of the CMUT chip, and the stitch bond was performed on the ground bonding pad of the PCB (**Fig. 2.52**). Wire bonding parameters are given in **Table 2.15**.

	Bond1	Bond2
Ultrasonic Power (mW)	200	225
Ultrasonic Time (ms)	200	200
Force (mN)	250	250
Temperature (°C)	120	120
EFO (%)	80	N/A
UPCO (µm)	N/A	600
Loop up (µm)	2000	N/A
Loop y-axis (µm)	0	N/A

Table 2.15: Wire bonding parameters of the PCB ground pad and the device layer of the CMUT chip.

2.8 Probe Assembly

2.8.1 Design and Fabrication of the Probe

3D mechanical structure and mechanical integrity of a handheld probe is designed for PAI imaging by project principal investigator Dr. Mehmet Yilmaz, and mechanical engineering undergraduate student and TÜBİTAK STAR intern Halil İbrahim Şener. Undergraduate student and TÜBİTAK STAR intern Hazal Vural has also worked on design modifications. The designed probe consists of outer and inner parts that protect the ASIC-CMUT-PCB integrated structure. The probe integrates fiber and the ASIC-CMUT-PCB integrated structure for PAI imaging. PAI imaging is performed in gel-containing or liquid-containing environments. Water tightness is especially critical to protect the electronic systems of the probe.

The designed probe is shown in **Fig. 2.53a**. Top holder part is suitable for a human hand (**Fig. 2.53b**). Top holder part is 3D printed from PLA material. It is 200 mm long, and it has 2 holes. The bigger hole is an aperture (Diameter: 56 mm) for wire bundles coming from the PCB. The smaller hole is an aperture (Diameter: 16.5 mm) for fiber connection for light transmission during PAI. The smaller hole lets fiber reach the back side of the CMUT chip. There is an outer body part shown in **Fig. 2.53c**. It protects the internal structure. It is made

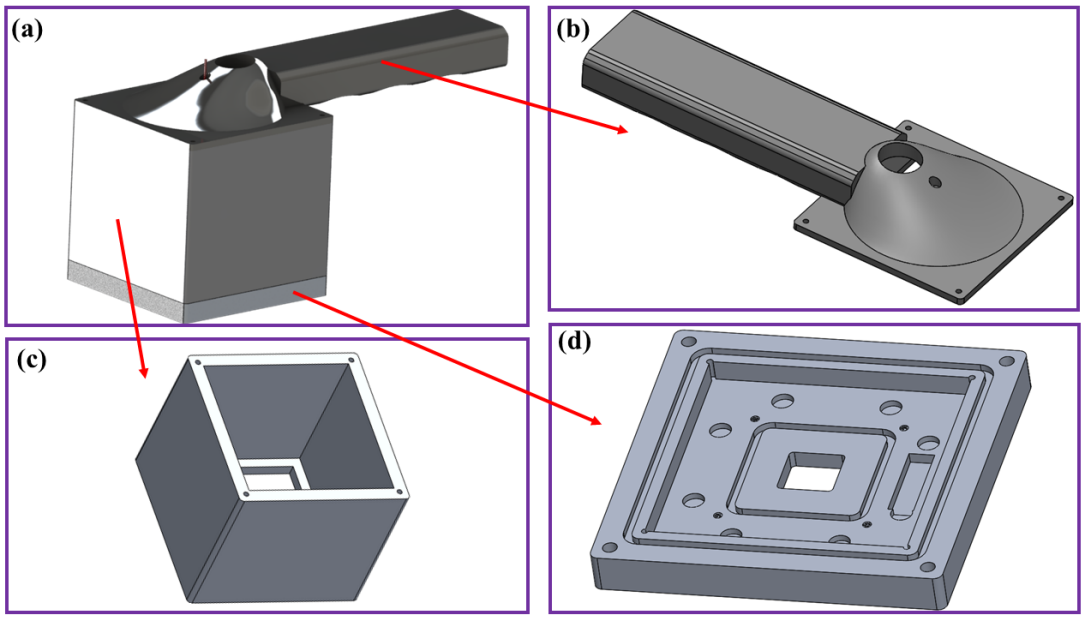


Figure 2.53: The design of the Probe. (a) The assembled probe, (b) The 3D printed holder part, (c) The outer aluminum part, (d) The bottom aluminum part.

of an aluminum 6061 alloy. Dimensions of the outer body part are 82 x 82 x 70 (height) mm. Moreover, the bottom part is an aluminum 6061 alloy (**Fig. 2.53d**). It has an aperture that lets CMUT cells reach the outer environment. The dimensions of the bottom part are 82 x 82 x 9 (height) mm. The dimension of the aperture is 12.6 x 12.6 mm.

The bottom aluminum part is designed as a nest for the PCB (**Fig. 2.54a**). The PCB is attached to the bottom aluminum part via 4 M2 screws. The 7x2 IDC connector of the PCB is a through-hole component. To accommodate the through-hole legs, a nest (6 x 20 x 1.5 (height) mm) is designed (shown in **Fig. 2.54b**) that is deeper than the height of the legs to avoid contact with the aluminum surface. Thus, the PCB can be appropriately attached to the bottom part without tilt or contact risk. Two O-ring nests (Diameter: 2 mm) are located at the bottom aluminum part. O-ring 1 is designed to avoid water leakage from the side walls. The bottom part is attached to the top part via 4 M4 screws. The O-ring 1 is compressed between the bottom and the top aluminum part. Therefore, the O-ring 1 must be compressed to a point where the water leakage is avoided.

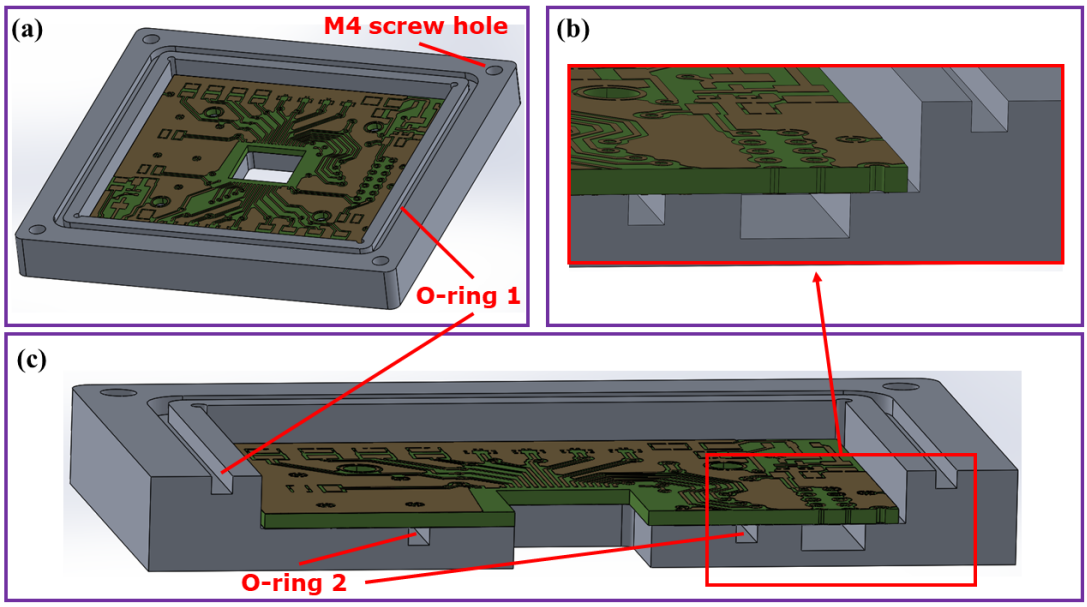


Figure 2.54: The bottom aluminum part. (a) the bottom aluminum part with PCB, (b) the nest for the 7x2 IDC connector through-hole legs, (c) the Cross section of the bottom aluminum part. O-ring 1 and O-ring 2 locations are shown with red arrows.

The torque value used to tighten the M4 screws is critical to compress the O-ring 1. Halil İbrahim Şener has performed experiments to optimize the torque values, and he concluded that a 35 cN.m torque value should be used to tighten the M4 screws. Furthermore, the O-ring 2 is located under the PCB and is designed to avoid water leakage from the CMUT cell aperture. The O-ring 2 is compressed between the bottom aluminum part and the PCB (**Fig. 2.54c**).

The cross-section of the probe is shown in **Fig. 2.55a**. There are 2 aluminum parts on top of the PCB. Inner aluminum part 1 (39 x 39 x 5 (height) mm) (shown in **Fig. 2.55b**) is designed to cover the CMUT chip. There is a 33 x 33 mm nest reserved for the CMUT chip. The nest has a 2 mm peripheral channel for O-ring 3. The O-ring 3 is compressed between the PCB and the inner aluminum part 1. The primary functions of the O-ring 3 are to protect the CMUT chip from external forces coming from the inner aluminum part 1 and to prevent water leakage. There is another 2 mm peripheral channel for O-ring 4. The primary function of the O-ring 4 is to support the CMUT chip. Finally, another circular

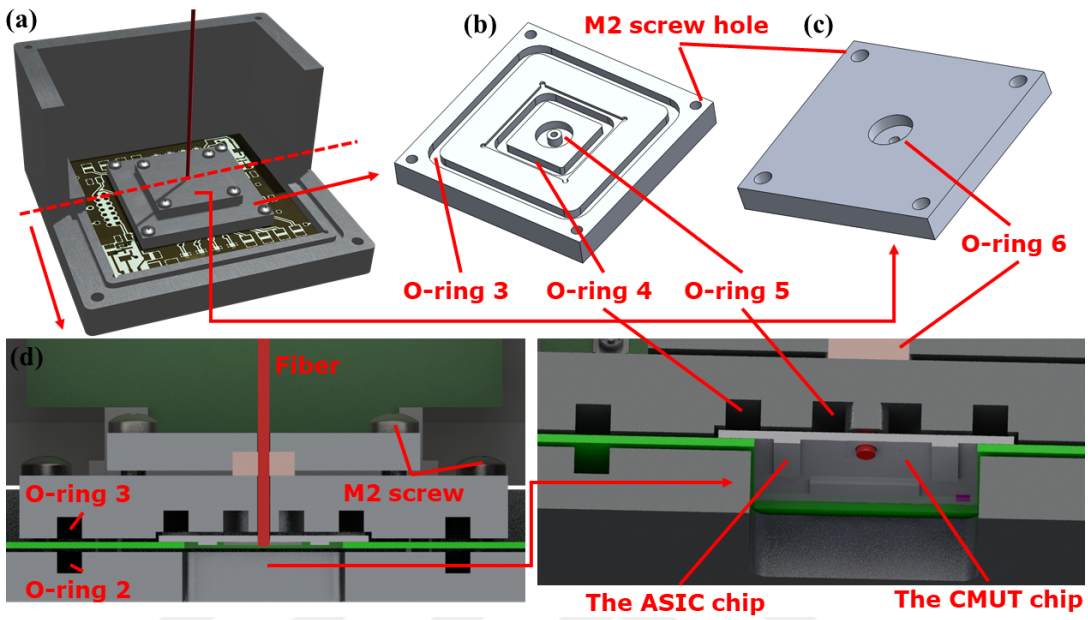


Figure 2.55: (a) The cross-section view of the probe, (b) The inner aluminum part 1, (c) The inner aluminum part 2, (d) The cross-sectional view of the internal aluminum parts, the CMUT chip, the PCB, and the fiber assembled.

O-ring 5 is in the middle of the inner aluminum part 1. The primary function of the O-ring 5 is to stabilize the position of the fiber.

There is the second aluminum part called inner aluminum part 2 (25 x 25 x 3 (height) mm) (shown in **Fig. 2.55c**). The inner aluminum part 2 is designed to stabilize the position of the fiber. A circular O-ring 6 and a 1.2 mm hole are in the middle. The inner aluminum part 2 is attached to the top of the inner aluminum part 1 by 4 M2 screws. The cross-section of the complete assembly is shown in **Fig. 2.55d**. The CMUT chip is flip-chip bonded to the PCB and is located at the top of the PCB. The inner aluminum part 1 covers the CMUT chip and supports it. The inner aluminum part 2 is attached to the top and supports the fiber. The O-rings are there to support and prevent water leakage. The torque value used to tighten the M2 screws is critical to compress the O-rings. Halil İbrahim Şener has performed experiments to optimize the torque values. He concluded that a 15 cN.m torque value should be used to tighten the M2 screws during the assembly of the Probe.

A CNC milling machine fabricated the aluminum parts of the probe. Aluminum 6061 alloy is selected to avoid bending of the probe during the assembly. The O-rings can easily be compressed between aluminum parts and provide water tightness. The probe is first assembled using a test PCB and a pseudo-ASIC - pseudo-CMUT flip-chip bonded structure. Test assembly is aimed to confirm water tightness. It was also desired to test the effects of the compression forces on the ASIC-CMUT flip-chip bonding interface.

2.8.2 Assembling a Test Probe to Validate Water Tightness and to Observe the Effects of the Compression Forces

The test probe is assembled using pseudo chips for a bending experiment. A pseudo-ASIC flip-chip bonded to a pseudo-CMUT structure with a known resistance value and a test PCB with the exact dimensions of the real PCB are chosen for the bending experiment.

The test PCB is placed on the bottom aluminum part. The pseudo-ASIC flip-chip bonded to the pseudo-CMUT structure is placed on the PCB (**Fig. 2.56a**). There was no bonding between the CMUT and the PCB. 2 aluminum inner parts are assembled, as shown in **Fig. 2.56b**. The ASIC-CMUT structure was flip-chip bonded, and there was neither underfill nor Parylene C coating for protecting the flip-chip bonding interface. The bottom part of the Probe is shown in **Fig. 2.56c**. The flip-chip bonded ASIC-CMUT interface is directly looking at the outer environment. The bottom part is assembled using a 35 cN.m torque value. The inner aluminum parts are assembled using a 15 cN.m torque value. Thus, the flip-chip bonded interface is subjected to a compression force during the assembly.

The test probe is disassembled later. The alignment between the ASIC-CMUT structure and the test PCB was preserved (shown in **Fig. 2.57a**). 2-probe

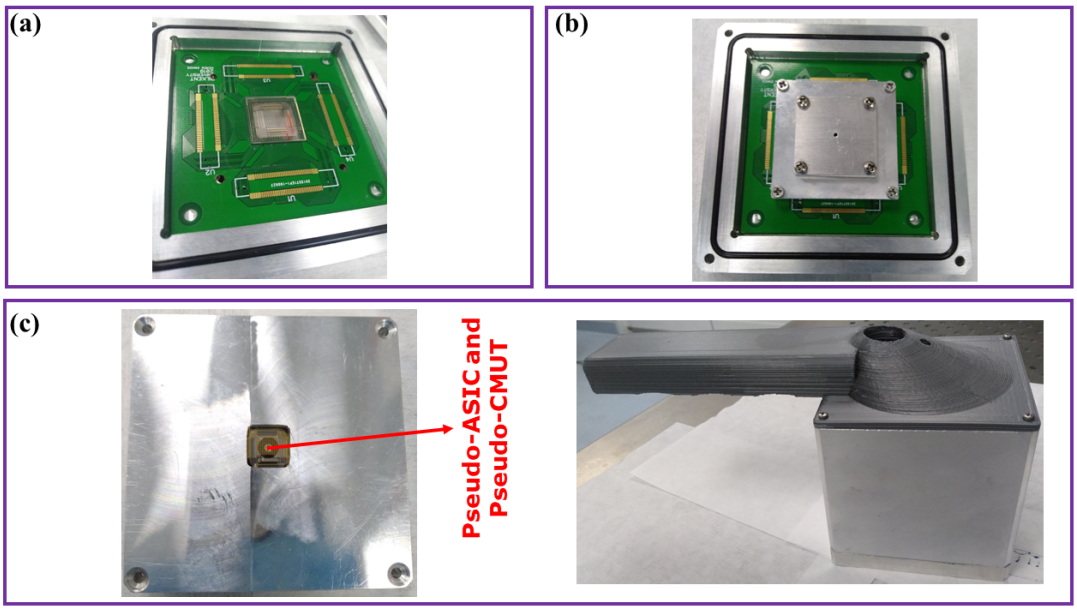


Figure 2.56: Test probe assembly. (a) The test PCB is placed on the bottom part, and the ASIC-CMUT flip-chip bonded structure is placed on top of the test PCB, (b) 2 inner aluminum parts are placed on the PBC, (c) The bottom part of the test probe, (c) Assembled test probe.

resistance measurement is performed by the SCS tool to pseudo-ASIC – pseudo-CMUT flip-chip bonding interface. The average resistance value of the ASIC-CMUT structure before the test assembly was 44 $\pm$ 12 Ω. The average resistance value was measured as 54.16 $\pm$ 17 Ω after the experiment (shown in **Fig. 2.57b**). All of the 143 GSB connections were found to be conductive.

After the test assembly experiment, the same ASIC-CMUT structure and test PCB have been assembled again into the probe with the same steps and torque values. The test probe was put inside a container that contained water. The test probe was inside the water for 10 minutes and moved up, down, left, right, and rotated for 10 minutes (Shown in **Fig. 2.58a**). Since there was neither underfill nor Parylene C coating for protecting the flip-chip bonding interface, the FCB interface was in contact with water. The test Probe was disassembled after. It was observed that one corner of the ASIC-CMUT structure was broken. The ASIC-CMUT structure was not bonded to the test PCB. Thus, the alignment was lost during the assembly, and the ASIC-CMUT structure moved and contacted

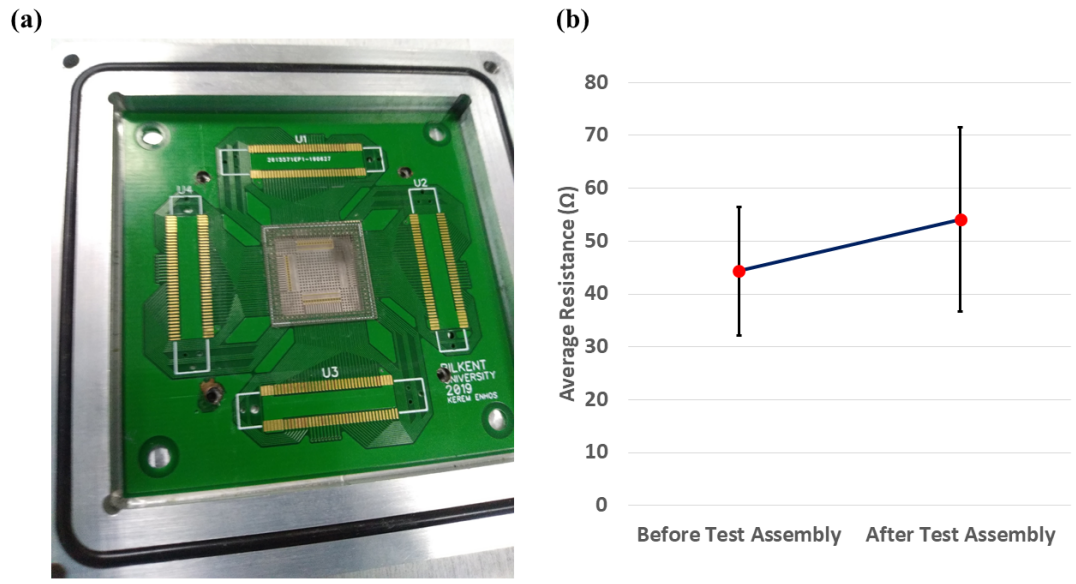


Figure 2.57: (a) The ASIC-CMUT structure on the test PCB after the experiment, (b) Average resistance value before and after the test assembly.

the inner aluminum part 1. The compression force was too strong, and one corner was broken (**Fig. 2.58b**). There was no water penetration into the probe. This suggests that O-rings attached by the calculated torque values provide water tightness (**Fig. 2.58b**). Before the 2-probe resistance measurement, the ASIC-CMUT structure was dried to remove residual water at the TSFCB interface. Again, the resistance was measured by the SCS tool. Before the experiment, the average resistance value was 54.16 $\pm$ 17 Ω. After the experiment, the average resistance value was 45.4 $\pm$ 13 Ω (**Fig. 2.58c**). All of the 143 GSB connections were found to be conductive.

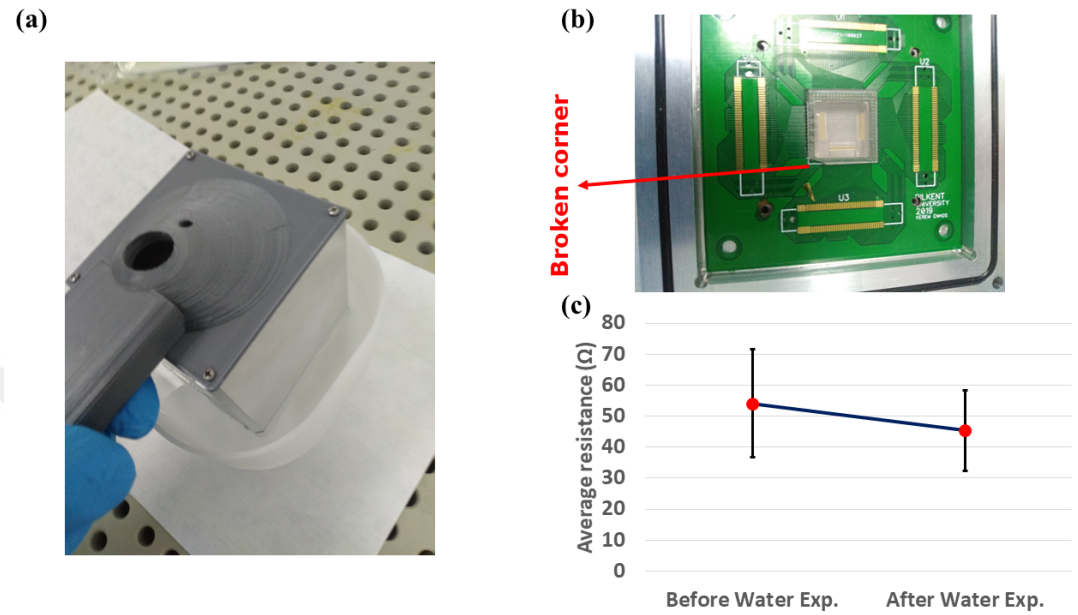


Figure 2.58: (a) The test probe inside the water, (b) The ASIC-CMUT structure on the test PCB after the experiment. The broken corner is shown. No water penetrated into the probe, (c) The average resistance values before and after the experiment.

2.8.3 Assembling the real Probe

Experiments with the test probe have shown no risk of water leakage and no risk of damaging the electronic systems of the probe while assembling. The experiments have also demonstrated the durability of the TSFCB interface. Although no protection layer like underfill or Parylene C coating existed, the TSFCB interface did not damage due to compressive forces or water contact. Therefore, the probe is safe for electronic systems. It was decided to assemble the probe with real electronic systems.

The ASIC-CMUT-PCB structure from **Fig. 2.51** is chosen for the assembly. The flip-chip bonded structure is placed on the bottom aluminum part (**Fig. 2.59a**). The inner aluminum parts are placed atop the PCB with a 15 cN.m torque value (**Fig. 2.59b**). The bottom aluminum part is assembled to the outer aluminum part with a 35 cN.m torque value (**Fig. 2.59c**). Finally, the 3D-printed holder part is assembled. The probe is believed to be ready for the

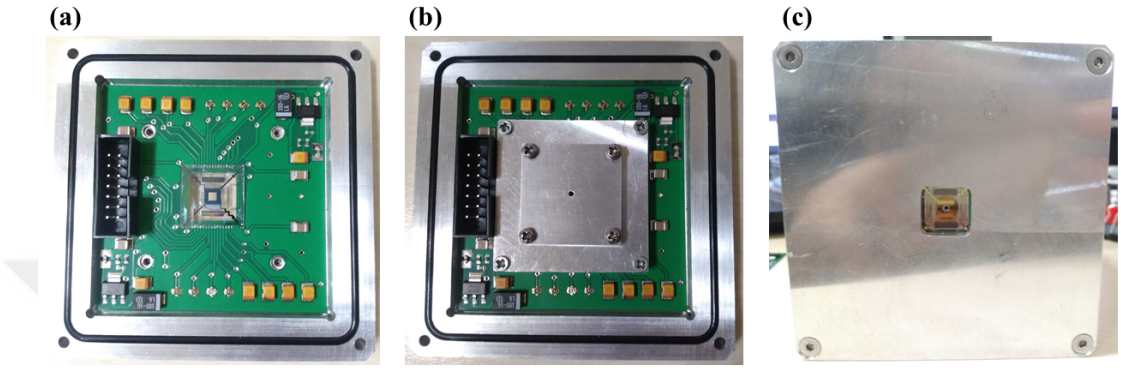


Figure 2.59: Real Probe assembly. (a) The PCB is placed on the bottom aluminum part, (b) The inner aluminum parts are placed atop the PCB with a 15 cN.m torque value, (c) The bottom part of the probe after the assembly, where ASIC-CMUT structure is visible.

PAI imaging after the fiber and cables are attached.

Chapter 3

Conclusion

This thesis is about the packaging of CMUT chips for a PAI imaging probe. Using FCB techniques, two ASIC chips had to be integrated with a single CMUT chip for signal processing. A suitable FCB process was searched and found for ASIC and CMUT integration. With the resources available at the cleanroom facilities of Bilkent University UNAM, TSFCB was found to be the most suitable FCB process for ASIC and CMUT integration. To develop a TSFCB process, pseudo-ASIC chips, and pseudo-CMUT chips were designed and fabricated. Pseudo-ASIC and pseudo-CMUT chips are geometrical replicas of real chips, and they were used for TSFCB process development. This way, the psychological stress and the process development costs of the TSFCB was decreased. Furthermore, specific connections were designed for pseudo-ASIC and pseudo-CMUT that made possible to measure the resistance of the FCB structures after the TSFCB process trials via the 2-probe resistivity method.

To perform the TSFCB process of ASIC-CMUT, GSB fabrication was required. GSB fabrications with 25.4 µm and 17.5 µm diameter gold wires are developed and optimized. Suitable capillary tools were found and used for the fabrication. The optimized process parameters were presented. To flatten the sharp tails of the GSBs and eliminate the height variations, a coining process was necessary before the TSFCB.

Coining processes in the literature are performed by pressing the GSBs against a flat surface. Around 1 N/bump force is suggested. The approach stated in the literature controls the force during the coining process. Suggested 1 N/bump force value was not applicable to our scenario. The ASIC chip has 143 bonding pads and is required 143 GSBs. Therefore, around 143 N total force was needed to perform the coining process stated in the literature. The flip-chip bonder used in this thesis is capable of applying only 20 N force. To perform the coining of the 143 GSBs, we had to find another solution.

In this thesis study, a displacement-controlled coining (DCC) process for gold stud bumps (GSBs) is developed, which does not exist in the available technical literature so far, to the best of our knowledge. Displacement-controlled approach controls displacement of the coined flat surface successfully so that height of the stud bumps can be controlled by selecting desired mold cavity depth value. With the bump geometries and wire diameter we used in this stud, the method produces $\pm$ 1.09 µm bump height variation and helps to achieve successful thermo-sonic flip-chip bonding (FCB) results. The method is also suitable to coin large arrays and small arrays both for R&D and for mass manufacturing, because there is no need to use advanced level FCB equipment for coining process. However, it is important to emphasize that, as the stud bump sizes become smaller and smaller, the bump height tolerances also become tighter and tighter. This means, higher precision CNC machining of the molds would be needed for higher precision DCC. Furthermore, height and surface area of the stud bumps can be adjusted by defining desired mold cavity depth value. All GBSs of the pseudo-ASIC chips and real ASIC chips were coined using the developed DCC process.

Optimization of the selected TSFCB process for ASIC-CMUT integration was performed. A heat energy transfer based analytical model that is capable of calculating the bonding interface temperature (T_{int}) for the TSFCB process is developed. The developed analytical model is experimentally studied by using pseudo Silicon ASIC chips and pseudo Pyrex ASIC chips that have GSBs and gold bonding pads. Both Silicon and Pyrex trials show that, between 46 %-70 % T_m value is required to obtain successful bonding at the Au-Au bonding interface.

The results of the study of the developed analytical model are listed below.

I. For both Silicon chips and Pyrex chips, between T_{int} value from 46 % to 70 % T_m value is required to obtain successful TSFCB bonding at the Au-Au bonding interface. Less than the specified T_{int} value range leads to incomplete bonding by insufficient deformation of GSBs and more than the specified T_{int} value range leads to unsuccessful bonding by severe deformation of GSBs and creating slippage/misalignment. Also, studied substrate materials (Silicon and Payrex) have a negligible effect on the interface temperature (T_{int}).

II. The analytical model is capable of estimating and tailoring process parameters. T_{int} can be tuned by ultrasonic power, ultrasonic time, normal force (hence, pressure), mass and specific heat capacity of the GSBs. The TSFCB process was performed at process temperatures ($T_{process}$) of 24 °C, 25 °C, 40 °C, 150 °C, and 375 °C by tailoring other process parameters (i.e. ultrasonic power, ultrasonic time, mass and specific heat capacity of the GSBs) to obtain the same T_{int} at the desired $T_{process}$. Low-temperature processing enables working with temperature-sensitive materials and platforms, enabling faster TSFCB processes which may increase throughput by decreasing total process time. Decreasing total process time may also decrease the total cost.

III. GSBs fabricated by 25.4 µm gold wire and 17.5 µm gold wire are used in the TSFCB process trials. Smaller GSBs can be fabricated by using smaller diameter gold wires and the mass of the GSBs can be decreased. Smaller GSB mass requires less ultrasonic power to reach the same amount of T_{int} during the TSFCB process. Using less ultrasonic power may be helpful for bonding delicate substrates. Also, the coining process prior to the TSFCB process is critical to obtain flat surfaces with known surface areas on top of the GSBs and leveling the heights of the GSBs. Leveling the heights at higher or lower height values affect the surface area on top of the GSBs. The surface area affects the pressure per bump (pressure/bump) value that is used during FCB. The developed DCC process is useful to manipulate the surface area and the height of GSBs.

IV. Low force/bump or low pressure/bump value can lead to unsuccessful

bonding due to lack of contact between GSBs and the corresponding bonding pads during FCB process. Below 80 MPa pressure/bump values were found insufficient for bonding.

V. The developed analytical model was integrated into a mechanical deformation model (**Equation 2.10-2.14**) [48] to estimate the mechanical deformation of the bumps during the TSFCB process. Bump deformation can be estimated with less than 2 µm accuracy. Estimating/controlling bump deformation allows controlling of stand-off distance which is critical during the underfilling process.

VI. Using the developed TSFCB process, multi-chip packaging on the same planar substrate, and high-density packaging are possible.

Although the developed analytical model works by making some assumptions, the developed model enables estimating and tailoring the process parameters of the TSFCB process. The model enables faster decision-making and foreseeing results of the TSFCB process prior to doing initial process trials. Implementing the model may be helpful during R&D studies and mass production. Tailoring the process parameters can be helpful to foresee the total time, total cost, and total energy consumption of a TSFCB process. Using the developed analytical model, less amount of experimental studies may be sufficient to optimize the TSFCB process for various applications such as MEMS packaging and die bonding.

After the development of the analytical model for the TSFCB, 2 real ASIC chips were integrated with the CMUT chip using the TSFCB process. SEM imaging shows that all 143 GSBs were in contact with bonding pads. Thus, 256 CMUT cells were connected to ASIC chips which may lead to the use of the CMUT chip at full capacity.

To strengthen and increase the reliability of the FCB structure, an underfill process is developed. A suitable underfill material (353 ND) was found and TPD dispensing of the underfill material was optimized. 353 ND material is applied to a pseudo-ASIC pseudo-CMUT FCB structure via TPD dispensing. Results of the optical imaging and SEM imaging showed that 353 ND filled the gap of

the FCB structure via capillary flow. Furthermore, to strengthen and increase the reliability of the FCB structure and to seal the CMUT cells simultaneously, Parylene C coating was applied. To protect the PCB bonding pads of the CMUT during the Parylene C coating process, a dicing tape was attached to the PCB bonding pads. After the Parylene C coating, the dicing tape was removed by applying UV exposure. Only the real ASIC – real CMUT FCB structure and the CMUT cells were coated by the Parylene C material.

As the second part of the packaging, the ASIC-CMUT structure had to be integrated with a PCB for PAI imaging. A suitable FCB process was searched for and found for CMUT-PCB integration.A combination of stacked GSB and ICA was the most suitable FCB process. It enables low temperature and low force processing which is critical to perform FCB integration of CMUT-PCB while protecting the previous ASIC-CMUT FCB structure and the CMUT cells. A suitable ICA was found. H20E was selected due to its superior properties. TPD dispensing of H20E was optimized. To avoid the overflow of the H20E due to applied FCB force, stacked GSBs are fabricated on the bonding pads to increase the total height and serve as mechanical stops. Coining of the stacked GSBs was performed via force-controlled coining (FCC).

A previously TSFCB-bonded FCB structure (pseudo-ASIC pseudo-CMUT) was subjected to 80 °C (curing temperature of H20E) for 3 hours to observe the effects of temperature on the FCB structure. No significant effect was found.

To decrease the FCB development cost of the CMUT-PCB, a pseudo-PCB was designed and fabricated, a geometrical replica of the real PCB. Pseudo-CMUT and pseudo-PCB were integrated via stacked GSB and ICA combination. 2-probe resistivity results showed that the structure was 100 % conductive. Then, the integration of CMUT-PCB was completed by using stacked GSBs and ICA.

SMD components of the PCB were soldered prior to CMUT-PCB integration. After the CMUT integration, the 7x2 through-hole IDC connector was soldered, as well. Device layer ground connections of CMUT were connected to ground connections of the PCB via wire bonding.

Components of the designed and fabricated probe were presented. A test probe was first assembled via a test PCB and a pseudo-FCB structure to observe the effects of the compression forces on the pseudo-FCB structure. Pseudo-FCB structure was 100 % conductive before and after the experiment. Also, the test probe was put inside the water to validate water tightness. No water was found inside the probe. The pseudo-FCB was again 100 % conductive before and after the experiment.

Finally, the integrated real electronic system of the probe (two ASIC chips are TSFCB attached to the CMUT chip. The CMUT chip is attached to the PCB via stacked GSBs and ICA combined FCB process. Components of the PCB were soldered) was assembled into the real probe.

As future work, the remaining steps of PAI imaging experiments will be completed.

Bibliography

[1] T. M. Khan, A. S. Taşdelen, M. Yilmaz, A. Atalar, and H. Köymen, "High-intensity airborne cmut transmitter array with beam steering," *Journal of Microelectromechanical Systems*, vol. 29, no. 6, pp. 1537–1546, 2020.

[2] C. Seok, F. Y. Yamaner, M. Sahin, and Oralkan, "A wearable ultrasonic neurostimulator - part i: A 1d cmut phased array system for chronic implantation in small animals," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 4, pp. 692–704, 2021.

[3] M.-C. Chen, A. Peña Perez, S.-R. Kothapalli, P. Cathelin, A. Cathelin, S. S. Gambhir, and B. Murmann, "A pixel pitch-matched ultrasound receiver for 3-d photoacoustic imaging with integrated delta-sigma beamformer in 28-nm utbb fd-soi," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2843–2856, 2017.

[4] J. M. Rothberg, T. S. Ralston, A. G. Rothberg, J. Martin, J. S. Zahorian, S. A. Alie, N. J. Sanchez, K. Chen, C. Chen, K. Thiele, *et al.*, "Ultrasound-on-chip platform for medical imaging, analysis, and collective intelligence," *Proceedings of the National Academy of Sciences*, vol. 118, no. 27, p. e2019339118, 2021.

[5] K. Enhoş, "Electrically unbiased and half frequency driven waterborne 16× 16-element 2-d phased array cmut," Master's thesis, Bilkent Universitesi (Turkey), 2019.

[6] T. M. Khan, *Design, Fabrication and Operation of a Very High Intensity CMUT Transmit Array for Beam Steering Applications*. PhD thesis, Bilkent Universitesi (Turkey), 2020.

[7] Y. A. Abhoo, "Designing, fabrication and post-fabrication characterization of half-frequency driven 16 x 16 waterborne transmit cmut array," Master's thesis, Bilkent Universitesi (Turkey), 2021.

[8] D. K. B. Özyiğit, "Batch-compatible micromanufacturing of a cmut array for optoacoustic imaging of tissue-like phantoms," Master's thesis, Bilkent Universitesi (Turkey), 2021.

[9] A. Outlook, "Integrated circuit engineering corporation," *Scottsdale, Arizona*, 1991.

[10] L.-T. Hwang and T.-s. J. Horng, *3D IC and RF SiPs: Advanced Stacking and Planar Solutions for 5G Mobility*. John Wiley & Sons, 2018.

[11] K.-N. Tu and K. Zeng, "Tin–lead (snpb) solder reaction in flip chip technology," *Materials science and engineering: R: reports*, vol. 34, no. 1, pp. 1–58, 2001.

[12] T. Wirebonder, "Hb 06/08/10/12/14/16 wire bonder operation manual version s30." https://www.tpt.de/, Accessed: November, 2021.

[13] C. Luk, Y. Chan, and K. Hung, "Development of gold to gold interconnection flip chip bonding for chip on suspension assemblies," *Microelectronics Reliability*, vol. 42, no. 3, pp. 381–389, 2002.

[14] S.-S. Ha and S.-B. Jung, "Thermal and mechanical properties of flip chip package with au stud bump," *Materials Transactions*, vol. 54, no. 6, pp. 905–910, 2013.

[15] B. C. Roberto de Almeida, "Gold stud bumps for flip chip technology." https://www.gov.br/cti/pt-br/publicacoes/producao-cientifica/seminario-pci/ix$_s$*eminario*$_p$*ci* − 2019/*pdf*/*seminario* − 2019$_p$*aper*$_7$*.pdf*, *Accessed* : *September*, 2021.

[16] J. Jordan, "Gold stud bump in flip-chip applications," in *27th Annual IEEE/SEMI International Electronics Manufacturing Technology Symposium*, pp. 110–114, IEEE, 2002.

[17] M. Lim, Z. Sauli, H. Aris, V. Retnasamy, C. Lo, K. Muniandy, N. Khan, and C. Foong, "Thermosonic vs thermocompression flip chip bonding for low cost system in package," in *AIP Conference Proceedings*, vol. 2045, p. 020093, AIP Publishing LLC, 2018.

[18] T. McLaren, S. Y. Kang, W. Zhang, D. Hellman, T.-H. Ju, and Y. Lee, "Thermosonic flip-chip bonding for an 8/spl times/8 vcsel array," in *1995 Proceedings. 45th Electronic Components and Technology Conference*, pp. 393–400, IEEE, 1995.

[19] S. Suppiah, N. R. Ong, Z. Sauli, K. Sarukunaselan, J. B. Alcain, M. M. Shahimin, and V. Retnasamy, "A short review on thermosonic flip chip bonding," in *AIP conference proceedings*, vol. 1885, p. 020266, AIP Publishing LLC, 2017.

[20] S. Tripathi, B. Holbrook, M. Irving, R. Lander, M. Woods, J. Brau, R. Frey, D. Strom, M. Breidenbach, D. Freytag, *et al.*, "Gold-stud bump bonding for hep applications," *Journal of Instrumentation*, vol. 5, no. 08, p. C08005, 2010.

[21] A. Roshanghias, A. D. Rodrigues, and D. Holzmann, "Thermosonic fine-pitch flipchip bonding of silicon chips on screen printed paper and pet substrates," *Microelectronic Engineering*, vol. 228, p. 111330, 2020.

[22] G. Dou and A. S. Holmes, "Thermosonic-adhesive flip-chip assembly," in *2012 4th Electronic System-Integration Technology Conference*, pp. 1–5, IEEE, 2012.

[23] L. Levine, "Ball bumping and coining operations for tab and flip chip," in *1997 Proceedings 47th Electronic Components and Technology Conference*, pp. 265–267, IEEE, 1997.

[24] M. Tani, H. Watanabe, A. Nishimura, S. Kachi, N. Katada, and S. Sugiura, "Development of ultrasonic flip chip bonding technology," *Fujitsu Ten Tech. J.*, vol. 34, pp. 19–25, 2010.

[25] G. Zhang, X. Ang, Z. Chen, C. C. Wong, and J. Wei, "Critical temperatures in thermocompression gold stud bonding," *Journal of Applied Physics*, vol. 102, no. 6, p. 063519, 2007.

[26] L. E. Rohwer and D. Chu, "Thin gold to gold bonding for flip chip applications," in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, pp. 907–910, IEEE, 2011.

[27] H. Maruo, Y. Seki, Y. Unami, and T. Ominato, "Ultrasonic flip chip bonding on fpc," *Fujikura Technical Review*, pp. 36–39, 2004.

[28] K. Tanida, M. Umemoto, Y. Tomita, M. Tago, R. Kajiwara, Y. Akiyama, and K. Takahashi, "Au bump interconnection with ultrasonic flip-chip bonding in 20 μm pitch," *Japanese Journal of Applied Physics*, vol. 42, no. 4S, p. 2198, 2003.

[29] M. Lim, Z. Sauli, H. Aris, V. Retnasamy, C. Lo, K. Muniandy, N. Khan, and C. Foong, "The optimization of ultrasonic power and bonding time for thermosonic flip chip bonding," in *AIP conference proceedings*, vol. 2045, p. 020094, AIP Publishing LLC, 2018.

[30] T. Tomioka and I. Shohji, "Bondability investigations of thermosonic flip chip bonding using ultrasonic vibration perpendicular to the interface," *Transactions of The Japan Institute of Electronics Packaging*, vol. 12, pp. E18–013, 2019.

[31] J. Lee, J. H. Kim, and C. D. Yoo, "Thermosonic bonding of lead-free solder with metal bump for flip-chip bonding," *Journal of electronic materials*, vol. 34, pp. 96–102, 2005.

[32] C.-W. Ha, K.-R. Kim, K.-S. Kim, and S. Kim, "Sliding mechanism of lateral thermosonic process with anisotropic conductive film for high productivity and high reliability," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 2, pp. 205–212, 2013.

[33] A. Coucoulas, "Hot work ultrasonic bonding-a method of facilitating metal flow by restoration processes," in *Proc. 20 IEEE Electronic Components Conf.*, pp. 549–556, 1970.

[34] D. Staiculescu, J. Laskar, and E. M. Tentzeris, "Design rule development for microwave flip-chip applications," *IEEE transactions on microwave theory and techniques*, vol. 48, no. 9, pp. 1476–1481, 2000.

[35] M. H. M. Hizukuri, N. W. N. Watanabe, and T. A. T. Asano, "Dynamic strain and chip damage during ultrasonic flip chip bonding," *Japanese Journal of Applied Physics*, vol. 40, no. 4S, p. 3044, 2001.

[36] F. Wang, J. Li, L. Han, and J. Zhong, "Effect of bonding parameters on thermosonic flip chip bonding under pressure constraint pattern," in *Conference on High Density Microsystem Design and Packaging and Component Failure Analysis, 2006. HDP'06.*, pp. 87–89, IEEE, 2006.

[37] T. T. Luu, H.-V. Nguyen, A. Larsson, N. D. Høivik, and K. E. Aasmundtveit, "Gold to gold thermosonic bonding characterization of bonding parameters," in *IMAPS Nordic Annual Conference 2010: Proceedings of a meeting held 6-8 June 2010, Gothenburg, Sweden*, 2010.

[38] F. Wang and Y. Chen, "Modeling study of thermosonic flip chip bonding process," *Microelectronics Reliability*, vol. 52, no. 11, pp. 2749–2755, 2012.

[39] J. Li, L. Han, J. Duan, and J. Zhong, "Interface mechanism of ultrasonic flip chip bonding," *Applied Physics Letters*, vol. 90, no. 24, p. 242902, 2007.

[40] S. Kang, P. Williams, T. McLaren, and Y. Lee, "Studies of thermosonic bonding for flip-chip assembly," *Materials Chemistry and Physics*, vol. 42, no. 1, pp. 31–37, 1995.

[41] C. Huang, W. Tang, and L. Zhang, "The bonding forming simulation and reliability research of the flip-chip stacked gold stud bump," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, no. 1, pp. 153–161, 2016.

[42] T. S. McLaren, S. Y. Kang, W. Zhang, T.-H. Ju, and Y.-C. Lee, "Thermosonic bonding of an optical transceiver based on an 8/spl times/8 vertical cavity surface emitting laser array," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 20, no. 2, pp. 152–160, 1997.

[43] P. Lawyer, D. Choudhury, M. Wetzel, and D. Rensch, "Thermosonic bonding of high-power semiconductor devices for integration with planar microstrip circuitry," in *Twenty Third IEEE/CPMT International Electronics Manufacturing Technology Symposium (Cat. No. 98CH36205)*, pp. 390–393, IEEE, 1998.

[44] C.-L. Chuang, Q.-A. Liao, C.-C. Hsu, J.-N. Aoh, S.-J. Liao, and G.-S. Huang, "Thermosonic flip-chip bonding for stud bumps onto copper electrodes with titanium and silver layers," in *2007 International Microsystems, Packaging, Assembly and Circuits Technology*, pp. 266–269, IEEE, 2007.

[45] F. Wang and L. Han, "Ultrasonic effects in the thermosonic flip chip bonding process," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 2, pp. 336–341, 2012.

[46] J.-h. Li, L. Han, and J. Zhong, "Ultrasonic power features of wire bonding and thermosonic flip chip bonding in microelectronics packaging," *Journal of Central South University of Technology*, vol. 15, no. 5, pp. 684–688, 2008.

[47] Y. N. Zhou, *Microjoining and nanojoining*. Elsevier, 2008.

[48] D. Liu, Y. Chao, and C. Wang, "Study of wire bonding looping formation in the electronic packaging process using the three-dimensional finite element method," *Finite Elements in Analysis and Design*, vol. 40, no. 3, pp. 263–286, 2004.

[49] T. Tomioka, T. Iguchi, and I. Mori, "Thermosonic flip-chip bonding for saw filter," *Microelectronics reliability*, vol. 44, no. 1, pp. 149–154, 2004.

[50] S. Y. Kang, T. McLaren, W. Zhang, and Y. Lee, "Thermosonic bonding for flip-chip assembly," in *Proceedings of 1995 IEEE Multi-Chip Module Conference (MCMC-95)*, pp. 75–80, IEEE, 1995.

[51] J. lau, "Chapter 12: Flip chip mounting using stud bumps and adhesive for encapsulation," in *FLIP CHIP TECHNOLOGIES*, pp. 357–366, McGraw-Hill, 1995.

[52] G. Riley, "Flipchips: Tutorial 99 pressure control in flip chip assembly." https://www.sensorprod.com/news/articles/2010-01$_c sr/pr_c sr$ $-$ $2010 - 01.pdf, Accessed : November, 2020$.

[53] C. Neher, R. Lander, A. Moskaleva, J. Pasner, M. Tripathi, and M. Woods, "Further developments in gold-stud bump bonding," *Journal of Instrumentation*, vol. 7, no. 02, p. C02005, 2012.

[54] R. Ren, X. Qiu, J. C. Lo, and S. R. Lee, "Experimental parametric study on the bumping and coining of gold studs for flip chip bonding," in *2016 China Semiconductor Technology International Conference (CSTIC)*, pp. 1–4, IEEE, 2016.

[55] Z. Zhong, "Stud bump bond packaging with reduced process steps," *Soldering & surface mount technology*, 2001.

[56] L. Condra, J. Svitak, and A. Pense, "The high temperature deformation properties of gold and thermocompression bonding," *IEEE Transactions on Parts, Hybrids, and Packaging*, vol. 11, no. 4, pp. 290–296, 1975.

[57] M. J. Yim and K. W. Paik, "Review of electrically conductive adhesive technologies for electronic packaging," *Electron Mater Lett*, vol. 2, no. 3, pp. 183–194, 2006.

[58] R. Aschenbrenner, R. Miessner, and H. Reichl, "Adhesive flip chip bonding on flexible substrates," in *Proceedings. The First IEEE International Symposium on Polymeric Electronics Packaging, PEP '97 (Cat. No.97TH8268)*, pp. 86–94, 1997.

[59] J. Haberland, C. Kallmayer, R. Aschenbrenner, and H. Reichl, "Fundamental studies of isotropic conductive adhesives focused on the current loadability of ica for flip chip applications," in *First International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics.*

Incorporating POLY, PEP & Adhesives in Electronics. Proceedings (Cat. No. 01TH8592), pp. 185–195, IEEE, 2001.

[60] W. Reinert and T. Harder, "Performance of the stud bump bonding (sbb) process in comparison to solder flip chip technology," in *4th International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing. Proceedings. Presented at Adhesives in Electronics 2000 (Cat. No. 00EX431)*, pp. 136–140, IEEE, 2000.

[61] Y. Singh, "Electrical resistivity measurements: a review," in *International journal of modern physics: Conference series*, vol. 22, pp. 745–756, World Scientific, 2013.

[62] Chemeurope.com, "Contact resistance." https://www.chemeurope.coml, Accessed: March, 2023.

[63] M. Leung, H. Lai-Wah, and P. Chou-Kee, "Comparison of bonding defects for longitudinal and transverse thermosonic flip-chip," in *Proceedings of the 5th Electronics Packaging Technology Conference (EPTC 2003)*, pp. 350–355, IEEE, 2003.

[64] Q. Tan, B. Schaible, L. J. Bond, and Y.-C. Lee, "Thermosonic flip-chip bonding system with a self-planarization feature using polymer," *IEEE transactions on advanced packaging*, vol. 22, no. 3, pp. 468–475, 1999.

[65] S.-Y. Kang, P. M. Williams, and Y.-C. Lee, "Modeling and experimental studies on thermosonic flip-chip bonding," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 18, no. 4, pp. 728–733, 1995.

[66] S.-Y. Kang, T.-H. Ju, and Y. Lee, "Thermosonic bonding: An alternative to area-array solder connections," in *Proceedings of IEEE 43rd Electronic Components and Technology Conference (ECTC'93)*, pp. 877–882, IEEE, 1993.

[67] J. H. Li, L. Han, J. A. Duan, and J. Zhong, "Features of machine variables in thermosonic flip chip," in *Key Engineering Materials*, vol. 339, pp. 257–262, Trans Tech Publ, 2007.

[68] M. Mayer and A. Zwart, "Ultrasonic friction power in microelectronic wire bonding," in *Materials science forum*, vol. 539, pp. 3920–3925, Trans Tech Publ, 2007.

[69] T. Bergman, A. S. Lavine, F. P. Incropera, and D. DeWitt, "Fundamentals of heat and mass transfer. wiley," *Hoboken, NJ*, 2011.

[70] massachusetts institute of technology, "Material property database." http://www.mit.edu/ 6.777/matprops/pyrex.htm, Accessed: May, 2023.

[71] E. C. Editors, "The thermal conductivity of silicon." https://www.electronics-cooling.com/1998/05/the-thermal-conductivity-of-silicon/, Accessed: May, 2023.

[72] S. Selberherr, *Analysis and simulation of semiconductor devices*. Springer Science & Business Media, 1984.

[73] J. Wan, W. Zhang, and D. Bergstrom, "Numerical modeling for the underfill flow in flip-chip packaging," *IEEE Transactions on Components and Packaging Technologies*, vol. 32, no. 2, pp. 227–234, 2009.

[74] Y. B. Kim and J. Sung, "Capillary-driven micro flows for the underfill process in microelectronics packaging," *Journal of mechanical science and technology*, vol. 26, pp. 3751–3759, 2012.

[75] X. Cheng, Q. Wang, L. Tan, G. Li, Y. Chen, and J. Cai, "Numerical analysis on muf process for flip chip packaging," in *2014 15th International Conference on Electronic Packaging Technology*, pp. 703–710, IEEE, 2014.

[76] A. Abas, Z. Gan, M. Ishak, M. Abdullah, and S. F. Khor, "Lattice boltzmann method of different bga orientations on i-type dispensing method," *PloS one*, vol. 11, no. 7, p. e0159357, 2016.

[77] J. J. Licari and D. W. Swanson, *Adhesives technology for electronic applications: materials, processing, reliability*. William Andrew, 2011.

[78] A. Babiarz and H. Quinones, "Advances in fast underfill of flip chips," in *Pan Pacific International Conference, Kawai*, 2001.

[79] A. J. Babiarz, "Paradigm shift in applying underfill," *Asymtek, Carlsbad, CA*.

[80] EPO-TEK, "Epo-tek 353nd technical data sheet for reference only." https://www.epotek.com/docs/en/Datasheet/353ND.pdf/, Accessed: July, 2021.

[81] M. Golda-Cepa, K. Engvall, M. Hakkarainen, and A. Kotarba, "Recent progress on parylene c polymer for biomedical applications: A review," *Progress in Organic Coatings*, vol. 140, p. 105493, 2020.

[82] S. Coating, "Parylene coatings for elastomeric components." https://scscoatings.com/wp-content/uploads/2020/05/35-Parylene-Coatings-for-Elastomeric-Components-1218.pdf, Accessed: March, 2023.

[83] R. Zhang, J. C. Agar, and C. Wong, "Recent advances on electrically conductive adhesives," in *2010 12th Electronics Packaging Technology Conference*, pp. 696–704, IEEE, 2010.

[84] R. Kay, M. Desmulliez, S. Stoyanov, C. Bailey, R. Durairaj, N. Ekere, M. Hendriksen, F. Frimpong, B. Smith, D. Price, *et al.*, "Low temperature flip-chip packaging based on stencil printing technology," *MicroTech 2003*, pp. 50–57, 2003.

[85] R. Durairaj, N. Ekere, and B. Salam, "Thixotropy flow behaviour of solder and conductive adhesive pastes," *Journal of materials science: materials in electronics*, vol. 15, pp. 677–683, 2004.

[86] X. Chen and H. Ke, "Effects of fluid properties on dispensing processes for electronics packaging," *IEEE transactions on electronics packaging manufacturing*, vol. 29, no. 2, pp. 75–82, 2006.

[87] M. Panalytical, "A basic introduction to rheology," 2016.

[88] H.-X. Li, J. Liu, C. Chen, and H. Deng, "A simple model-based approach for fluid dispensing analysis and control," *IEEE/ASME Transactions on mechatronics*, vol. 12, no. 4, pp. 491–503, 2007.

[89] X. Chen, "Modeling and control of fluid dispensing processes: a state-of-the-art review," *The International Journal of Advanced Manufacturing Technology*, vol. 43, pp. 276–286, 2009.

[90] C.-P. Chen, H.-X. Li, and H. Ding, "Modeling and control of time-pressure dispensing for semiconductor manufacturing," *International Journal of Automation and Computing*, vol. 4, no. 4, pp. 422–427, 2007.

[91] D. D. Lu and C. Wong, "Conductive adhesives for flip-chip applications," *Advanced Flip Chip Packaging*, pp. 201–261, 2013.

[92] R. Aradhana, S. Mohanty, and S. K. Nayak, "A review on epoxy-based electrically conductive adhesives," *International Journal of Adhesion and Adhesives*, vol. 99, p. 102596, 2020.

[93] R. L. Zenner, G. Connell, and J. A. Gerber, "Adhesive and conductive adhesive flip chip bonding," in *Proceedings 3rd International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces*, pp. 117–119, IEEE, 1997.

[94] B. Majeed, I. Paul, K. M. Razeeb, J. Barton, and S. C. O'Mathuna, "Effect of gold stud bump topology on reliability of flip chip on flex interconnects," *IEEE transactions on advanced packaging*, vol. 30, no. 4, pp. 605–615, 2007.

[95] B. Rosner, J. Liu, and Z. Lai, "Flip chip bonding using isotropically conductive adhesives," in *1996 Proceedings 46th Electronic Components and Technology Conference*, pp. 578–581, IEEE, 1996.

[96] J. E. Clayton, "Very high pin count flip chip assembly using conductive polymer adhesives," in *PROCEEDINGS-SPIE THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING*, pp. 275–281, International Society for Optical Engineering; 1999, 2003.

[97] A. Brewin, L. Zou, and C. Hunt, "A guide to best practice for electronic materials dispensing (npl report matc (a) 82)," *New Delhi: National Physics Laboratory*, 2001.

[98] EPO-TEK, "Epo-tek h20e technical data sheet for reference only." https://www.epotek.com/docs/en/Datasheet/H20E.pdf, Accessed: July, 2021.

[99] Intertronics, "An introduction to time/pressure dispensing." https://www.intertronics.co.uk, Accessed: December, 2021.

[100] A. D. Ltd, "Time pressure dispensing tutorial." https://www.adhesivedispensing.net/kb$_r$$esults.asp?ID$ = 146., $Accessed$: $January$, 2022.

Appendix A

Supplementary

Trial	Resistance (Ω)	SD (Ω)	No of unbonded
FCB Trial 1	58.4	27.0	0
FCB Trial 2	59.8	20.4	0
FCB Trial 3	44.4	14.5	0
FCB Trial 4	67.9	19.1	0
FCB Trial 5	72.4	28.6	0
FCB Trial 6	76.3	41.2	0
FCB Trial 7	54.2	17.3	0

Table A.1: Resistance results of the TSFCB trials at Fig. 2.11.

Trial	ASIC Chip	Depth of MC (µm)	CF/bump (N)	Mean h (µm)	SD h (µm)	Total SA (mm^2)	Total pressure (MPa) (Total CF/Total SA)	No of uncoined bump
1	Pseudo ASIC 32'	545	0.25	55.46	0.84	0.057	592.2	13
2	Pseudo ASIC 32"	545	0.5	52.1	0.85	0.091	787.2	4
3	Pseudo ASIC 32"'	545	0.75	45.7	0.87	0.149	715.3	0

Table A.2: Measured values table of Pseudo ASIC 32 after 0.25 N/bump, 0.5 N/bump, 0.75 N/bump coining processes. MC: Mold cavity, h: Height, SD: Standard deviation, SA: Surface area, CF: Compressive force.

Trial	ASIC Chip	Depth of MC (µm)	CF/bump (N)	Mean h (µm)	SD h (µm)	Total SA (mm^2)	Total pressure (MPa) (Total CF/Total SA)	No of uncoined bump
1	Pseudo ASIC 31'	545	1	45.6	0.61	0.149	715.7	0
2	Pseudo ASIC 31"	545	2	43.4	0.66	0.178	1601.5	0

Table A.3: Values of the GSBs after 1 N/bump and 2 N/bump DCC processes. MC: Mold cavity, h: Height, SD: Standard deviation, SA: Surface area, CF: Compressive force.

Trial	Force/bump (N/bump)	Displacement-controlled coining					Force-controlled coining				
		Mean h (µm)	SD h (µm)	Total SA (mm^2)	Avg SA/bump ($µm^2$/bump)	SD SA/bump ($µm^2$/bump)	Mean h (µm)	SD h (µm)	Total SA (mm^2)	Avg SA/bump ($µm^2$/bump)	SD SA/bump ($µm^2$/bump)
1	0.25	55.5	0.84	0.057	448.706	55.432	52.7	0.57	0.112	898.789	119.256
2	0.5	52.1	0.85	0.091	667.817	36.8	45.3	0.55	0.181	1260.577	417.674
3	0.75	45.7	0.87	0.149	1070.986	36.1	36.5	0.50	0.274	1884.579	334.831
4	1	45.6	0.61	0.149	1047.938	45.4	32.8	0.56	0.386	2651.369	469.876
5	2	43.4	0.66	0.178	1248.848	42.5	22.8	0.36	0.874	6114.682	705.33

Table A.4: Values of GSBs after the FCC and the DCC processes. h: Height, SD: Standard deviation, SA: Surface area, Avg: Average.

Appendix B

Supplementary

FCB Tool (Finetech Fineplacer Matrix Ma) User Manual A Technical Document of xfrontiers Research Group

This is a technical document about performing flip-chip bonding (FCB) with flip-chip bonder (FCB) tool at UNAM (Finetech Fineplacer Matrix Ma).

This document contains enough information to perform the thermosonic FCB process and CMUT-PCB integration process. Do not change anything without being sure. Anything you change can affect the process in a variety of ways. Avoid changing anything until you feel comfortable with the FCB tool!

I. Introduction

The brand of the flip-chip bonder (FCB tool) is Finetech Fineplacer Matrix Ma. The website link is given below.

https://www.finetech.de/

We collaborated with Finetech Company for the preparation of the FCB tool. You can read the story in the link given below.

https://www.finetech.de/knowledge/customer-stories/ultrasonic-flip-chip-bonding-for-bilkent-university-unam/

II. Thermo-sonic flip-chip bonding process (TSFCB) process parameters calculation before the process

TSFCB process uses gold stud bumps (GSB) to integrate ASICs to CMUTs. Force, temperature, ultrasonic power, and ultrasonic time are used. The top surface of the GSBs must be flattened by the coining process prior to the TSFCB process.

Then, you should measure the height, diameter, and surface area of the GSBs. Take SEM images and measure the height with ImageJ. Also, take optical microscope images and measure the diameter and surface area with ImageJ. Later, find the average height, average diameter, and total surface area of the GSBs.

Important: Total surface area is used to measure the pressure value that is used during the TSFCB process. For example, if you use 19 N and assume that the total surface area is 0.2 mm^2, the pressure will be 95 MPa. Make sure that the pressure is more than 80 MPa to have sufficient contact between the GSB and the bonding pad.

Fig .1 depicts the calculation of the TSFCB process parameters. **Fig .1a** shows the anatomy of the GSB. **Fig .1b** shows the ultrasonic power-ultrasonic time plot. You can only have this data after the process. Therefore, before the TSFCB process, you need to select your ultrasonic power and ultrasonic time approximately and from experience. **Fig .1c** shows the calculation of the interface temperature (T_{int}).

At this point, you know the average height and average diameter values of GSBs. Let's have an example of the calculation of the T_{int}.

Example: Assume you have 143 GSBs on the ASIC surface.

Average height: 45.24 µm

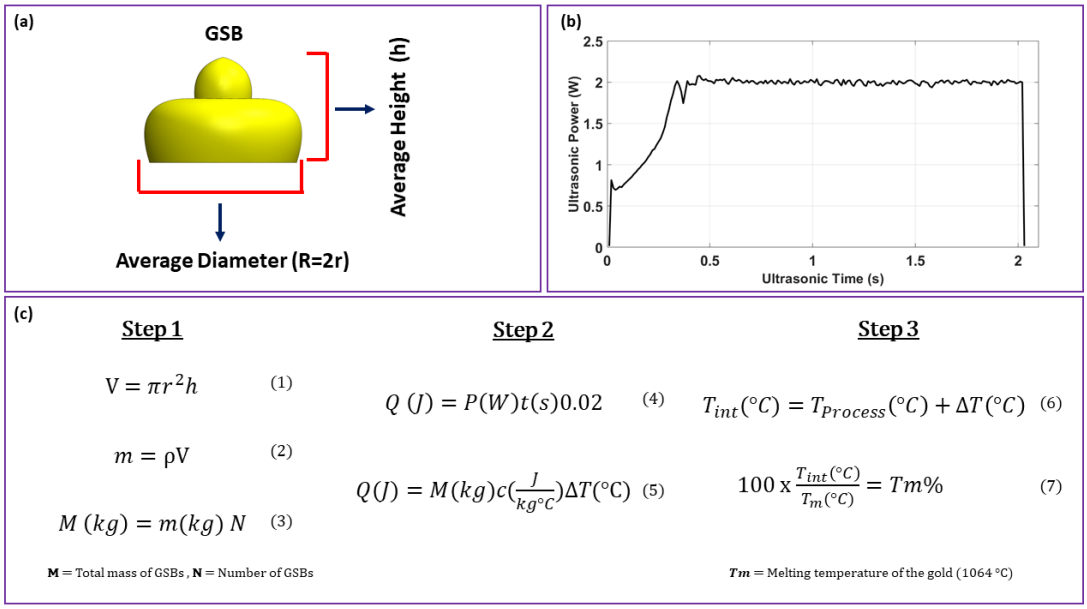


Figure .1: (a) Anatomy of a GSB, (b) An example ultrasonic power-ultrasonic time plot, (c) T_{int} calculation for a TSFCB process.

Average diameter: 81.42 µm

Temperature that you want to apply: 150 °C

What should be the ultrasonic power and ultrasonic time?

Step-1: At **Fig .1c**,

Calculate the volume by using average height and average diameter (**equation 1**).

Calculate the average mass (**equation 2**).

Calculate the total mass (**equation 3**). If you have 143 GSBs, multiply the average mass by 143 to obtain the total mass.

Step-2: At **Fig .1c**,

Equation 4 shows the calculation of the ultrasonic energy. According to the

literature, only 2% of the ultrasonic energy is used for the integration. Thus, we should take 2% of the ultrasonic energy.

Equation 5 shows the relation between temperature and ultrasonic energy. Assume you give 2 Watts of ultrasonic power and 1.2 seconds of ultrasonic power. You can find the ΔT from **equation 5**.

Step-2: At **Fig .1c**,

Equation 6 shows the relation between the process temperature ($T_{process}$=150 °C) and the T_{int}. Calculate T_{int}.

T_{int} can be shown as the percentage of the melting temperature of the gold by **equation 7**.

If you do the calculation for the values of this example, you will have 67.9% T_m before the TSFCB.

THIS VALUE IS THE ESTIMATED VALUE. AFTER THE TSFCB PROCESS, YOU WILL CALCULATE THE REAL VALUE!

Important: Please aim for 80-90% T_m because **Fig .1b** plot will not be perfectly flat and some of the ultrasonic energy will be lost. During the TSFCB, you will get 50-70% T_m.

Important: You can prepare an Excel file to calculate the T_{int} value prior to the TSFCB process.

After calculating the process parameters, you are ready to perform the TSFCB process.

This document will continue by describing operating the FCB tool.

III. Using the FCB tool for the TSFCB process

The computer of the FCB tool is always ON.

• Turn on the monitor.

• You will see the UNAM-IS page.

• First, you should start open the software. Please open IPM hybrid software.

• Once the software is opened, the file that we use is going to be opened automatically (20201126_19N_19W_375C_myv001). Please use this file, before you become sufficiently experienced with the operation of the tool.

• Now, you should press the power button to open the hardware. The beam-splitter will go to the zero position and the placer arm will go to the zero position. Then, you will see a message on the screen. It will say ready to initialization. **Important**: If this step is not successful, please control the emergency stop button (red button in front of the machine). If it is pressed, release the emergency button. If initialization is successful, the machine is now ready.

• THIS DOCUMENT ASSUMES THE US DIE COLLET IS NOT ATTACHED YET. If the die collet is already attached and the height of the die collet is calibrated, please ignore this step.

How to attach the US die collet and how to adjust the height of the die collet:

• Please see **Fig. .2** below that shows the attached US die collet.

• If there is no die collet on the placer arm, untighten the screw.

• Place the US die collet and move it to the back. The tip of the die collet should be very close to the placer arm to avoid a collision.

• Tighten the screw with the torque-adjustable wrench of the FCB tool. **Tighten it with 40 cN.m torque and do not change this torque value!**

• Place a CMUT chip on the heated stage. Focus on the surface of the CMUT chip with a z-direction micrometer screw.

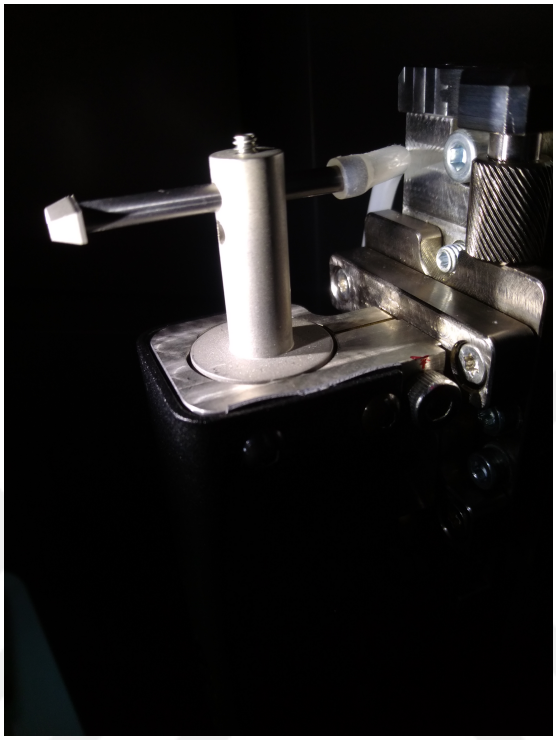


Figure .2: The US die collet attached to the placer arm.

• Align the die collet and CMUT chip. The die collet should touch the CMUT chip when the placer arm swivels down.

• Go to the swivel module. Adjust touchless = 0 mm. Swivel down.

• There will be a small gap between the die collet and the surface of the CMUT chip. Please untighten the screw and allow the die collet to touch the surface of the CMUT chip. At this point, tighten the screw with the torque-adjustable wrench (40 cN.m).

• Swivel up again. Attach the vacuum hose to the back side of the US die collet.

• **IMPORTANT**: After completing the height adjustment of the US die collet, please go to the ultrasonic module. Press start calibration, do not touch the machine! Make sure that the US die collet is not holding anything!

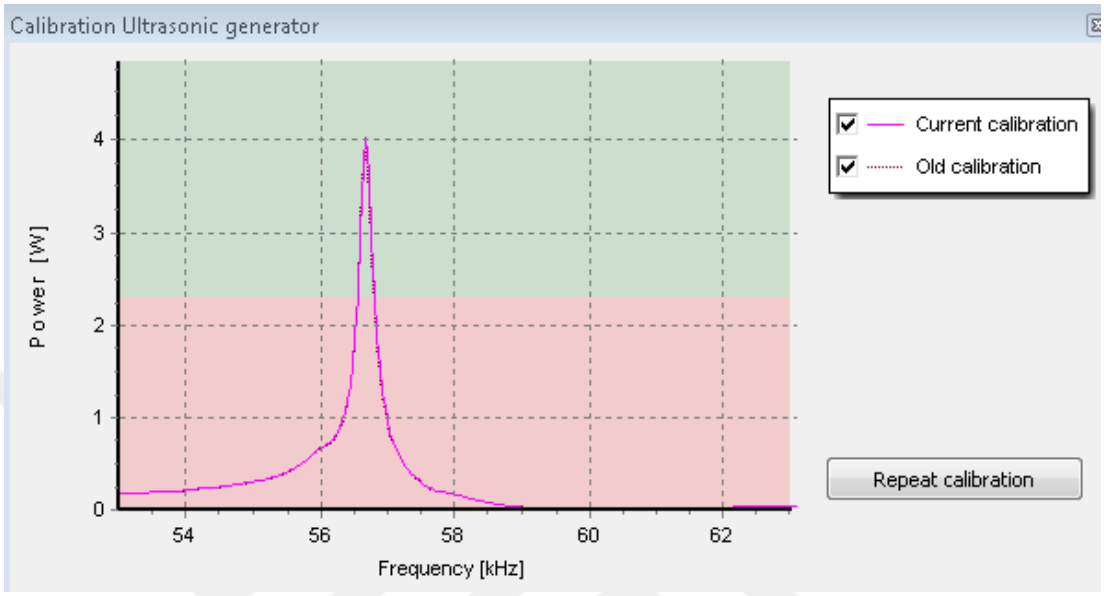


Figure .3: Ultrasonic calibration plot after the calibration.

After the US calibration, you will obtain a plot (**Fig. .3**). There must be one peak and the peak must be in the green zone. Otherwise, please control the height of the US die collet.

IMPORTANT: The ultrasonic calibration plot is highly critical to obtain ideal ultrasonic vibration performance. Make sure that calibration of the US die collet is satisfied.

- To read more, please visit the ultrasonic module manual of the tool.

IV. How to Assemble Spring Mechanism of the FCB Tool

• The spring mechanism is used for stabilizing the position of the substrate chip during the TSFCB process. Please see the **Fig. 2.17a**. There is a notch on the top side and there is a spring on the bottom side.

• Notch supports the substrate from the top and from the left. The spring is used to mechanically clamp the substrate from the bottom. The position of the spring can be manipulated via a cantilever on the right side.

• First, take 2 screws, 2 nuts, and 2 mechanical stopper nuts from the plastic bag.

• Second, put 2 mechanical stopper nuts on relevant holes of the steel plate of the heated stage.

IMPORTANT: There are only 2 mechanical stoppers. Do not lose them!

• Third, please put the spring mechanism on the steel plate of the heated stage. Make sure that the screws on the top side of the spring mechanism are properly placed in the holes. Do not tighten the top screws of the spring mechanism. Make sure that the holes on the bottom side are on top of the 2 mechanical stopper nuts.

• Fourth, place 2 screws with nuts on them in the bottom holes. Start tightening the screws. Tighten them 2 turns and tighten the other 2 turns. Proceed in this order until the screws are properly tightened.

• Fifth, move the spring and make sure that the spring is free and is not in contact with anywhere.

• Later, place a substrate on the heated stage. Slide the substrate from the right side to the left until the substrate is in contact with the notch. Make sure that the left side and top of the substrate are in contact with the notch. Then, start clamping the substrate with the spring by moving the cantilever slowly.

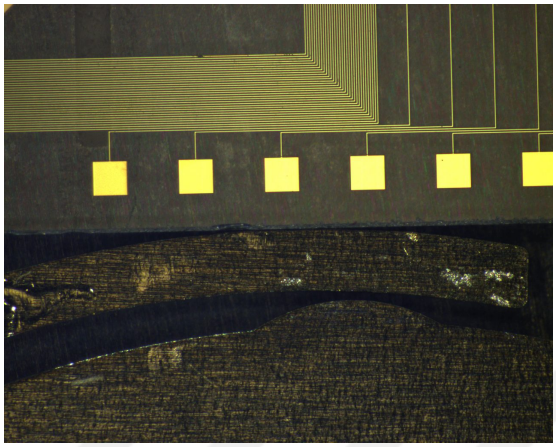


Figure .4: Ideal clamping of the substrate with the spring.

IMPORTANT: When you clamp the substrate, there must be a gap between the spring and the body of the spring mechanism as shown in **Fig. .4**.

• When the clamping is completed, check the position of the substrate near the notch. Make sure that the notch and the substrate are in contact with the left side and the top side.

• If the position is correct, please open the vacuum of the heated stage. To open the vacuum of the heated stage, you can press the F8 button or go to the functions submenu and press "switch vacuum at the heated stage". Please make sure that you see the green light on the software that suggests that the vacuum is holding the substrate.

V. How to Place Top Chip and Hold the Top Chip with the US Die Collet

• Place the top chip (The ASIC chip in this study) on the Gel-Pak of the FCB tool. Make sure that the back side of the top chip looks up. GSBs of the top chip must be in contact with the Gel-Pak surface.

• Focus on the surface of the top chip via the z-direction micrometer screw under maximum zoom.

• Please align the US die collet to the top chip. Use the air table to perform the coarse alignment. Then, via micrometer screws, perform the fine alignment. Make sure that alignment is good as shown in **Fig. 2.17b**.

• Please go to the swivel module. Select "touch the target" option for the touch down mode. Select touch down force as 2 N.

• Press the swivel down button. The beamsplitter will go to the safety position. The arm will swivel down motion. The swivel down motion stops until the force sensor records the 2 N value. When the touch down force is 2 N, swivel down stops.

• Please start vacuum of the US die collet. Press the F4 button or go to the functions submenu and select "switch vacuum at placer arm". The vacuum will start and hold the top chip. Make sure that the vacuum is more than 50%. If not, there may be a problem with the US die collet-top chip alignment, or the dicing saw process quality of the top chip can be bad.

• If the vacuum is more than 50%, please press the swivel up button. The placer arm will swivel up and the beamsplitter will go to the optical position.

• At this step, you will be able to see the front side of the top chip and GSBs. Please focus on the surface of the top chip by using the placer arm backward or the placer arm forward button. You have to focus on the bonding pads of the top chip.

IMPORTANT: The alignment between the substrate and the top chip must be performed by aligning the bonding pads. This important suggestion assumes that there are no other alignment marks for alignment of the chips, as was the case in our studies.

VI. Alignment Between the Top Chip and the Substrate Chip

• Please focus on the bonding pads of the substrate stage under maximum zoom and maximum light conditions.

• Use the air table to perform the coarse alignment. Press the vacuum pedal of the FCB tool to deactivate the vacuum that holds the heated stage. Gently move the heated stage by sliding it on the air table.

• After the coarse alignment, use the micrometer screws that move the heated stage to perform the fine alignment. First, adjust the x-direction and y-direction alignments. If there is theta misalignment, use the theta micrometer screw of the FCB tool to adjust the theta alignment.

• After the alignment, increase the magnification and move the beamsplitter to the right edge of the top chip. To move the beamsplitter, press and hold CTRL+SHFT and the arrow key (→). Check the alignment of the right side (**Fig. .5a**). Later, move the beamsplitter to the left edge of the top chip. To move the beamsplitter, press and hold CTRL+SHFT and the arrow key (←). Check the alignment of the left side (**Fig. .5b**). Make sure that the alignment is good. If there is misalignment, try to align again by using the x-direction, y-direction, and theta micrometer screws. A good alignment is shown in **Fig. .5c**.

IMPORTANT: The alignment is one of the the most critical parts of the TSFCB process. Make sure that the alignment is good before the TSFCB process.

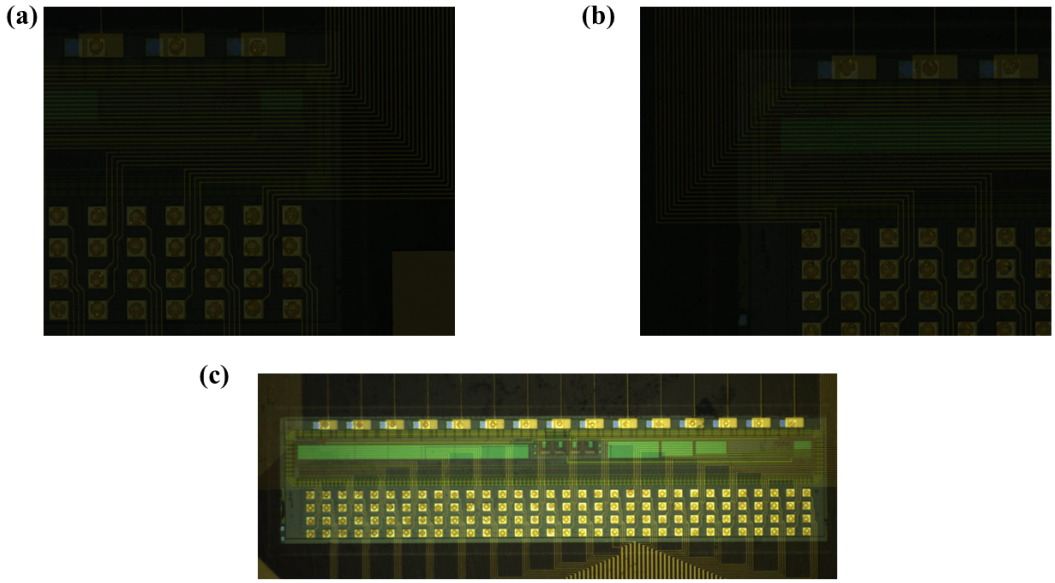


Figure .5: Alignment of the top chip and the substrate chip. (a) Alignment of the right side, (b) Alignment of the left side, (c) A good alignment.

VII. How to Adjust Process Parameters

After the alignment, now it is time to adjust the process parameters.

Adjusting Temperature

• First, go to the heating plate process module of the IPM software.

• Select use the heating plate process.

• There are sections for controlling the temperature. Select "current section-1".

• Adjust the ramp first (for example 5 K/s). Adjust temperature (for example, 150 °C). Adjust duration plateau (for example, 45 seconds).

IMPORTANT: Section-1 controls the heating to the target temperature and duration at the target temperature.

• Select “current section-2”.

• Adjust the ramp first (for example, 5 K/s). Adjust temperature (for example, 50 °C). Adjust duration plateau (for example, 10 seconds).

IMPORTANT: Section-2 controls the cooling to the standby temperature.

IMPORTANT: The temperature of section-2 must be equal to the standby temperature of the heated stage.

IMPORTANT: Heating and cooling take more time than other process parameters. Therefore, the total process time of the TSFCB process is controlled by the temperature. Thus, first, adjust the temperature and adjust the other parameters with respect to the temperature.

Adjusting Ultrasonic Time Ultrasonic Power

• Go to Ultrasonic module.

• Select, “use ultrasonic module”.

• Start mode: Process time.

• Start time should be close to the end of the plateau of the target temperature. For example, if the target temperature is 150 °C and the duration of the plateau is 45 seconds, end of the plateau will be at 64^{th} seconds. Thus, the start time can be selected as 60^{th} or 61^{st} seconds.

• Adjust the ultrasonic power.

• Adjust the working time (ultrasonic time).

Adjusting Force

• Go to Swivel module.

• Touch down mode: Touch the target.

• Touch down force: 2 N.

• In the force sections part, select new.

• Select to force (for example, 19 N).

• Select working time. The working time must be as long as the temperature profile. If the target temperature is 150 °C, total heating/cooling will take 87 seconds. Thus, the working time must be 87 seconds.

• In the "lift off" part, you can control the swivel up motion of the placer arm after the process.

Start mode: Working time. It automatically adjusts working time as the working time that you adjust in the force sections part.

• In the miscellaneous part, you can control the mode of the vacuum of the US die collet.

Mode of vacuum switching: Before "lift off". This means the vacuum of the US die collet will be switched off before swivel up motion.

VIII. Performing the TSFCB Process

• After the alignment and adjustment of process parameters, now we can start the process.

• Press the start button.

• The machine will ask for a serial number. Write "1", and press enter.

• At this point, please control the process parameters again and make sure that you are happy with the process parameters.

• Press the continue button.

• The process will start. First, the beamsplitter goes to the safety position.

Then, the placer arm will swivel down.

• GSBs of the top chip are going to touch the bonding pads of the substrate material. When the force is equal to the touch down force (for example, 2 N), the TSFCB process starts. Temperature starts to increase to the target temperature and the force starts to increase to the target force value. When time is equal to the working time of the ultrasonic module, ultrasonic vibration is applied with respect to ultrasonic power and ultrasonic time. Later, the temperature starts to decrease to the standby temperature. When the total process time is reached, the temperature is at standby temperature. Also, when the total process time is reached, the vacuum of the US die collet is closed and the placer arm swivels up.

• The beamsplitter goes to the optical position and the process is completed.

• Please release the spring and switch off the vacuum of the substrate.

• Slide the substrate to the right side of the heated stage. Then, take the substrate with a tweezer.

• In IPM Hybrid software, go to file. In the pop-up menu, go to protocol. Select "show protocol from the last working step".

• Please export the data as a pdf file.

• Please save the data.

IMPORTANT: The raw data is important to calculate the ultrasonic energy applied during the TSFCB process.

IX. Calculating the Interface Temperature (T_{int}) After the TSFCB Process

• Open the raw data in an Excel document.

• Please find ultrasonic power and ultrasonic time.

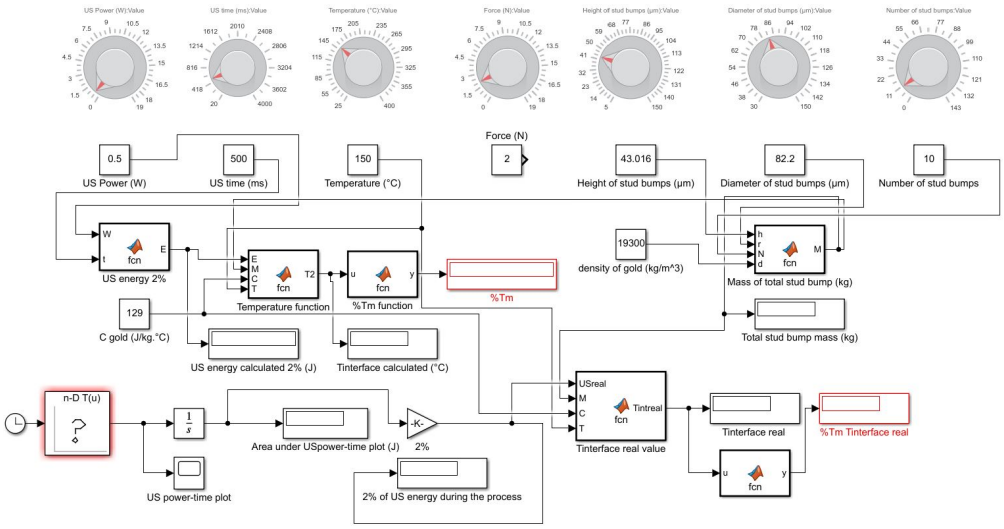


Figure .6: FCB Process model (Simulink).

• Mind the temperature during the ultrasonic time. If the target temperature was 150 °C, make sure that the thermocouple data is also the same.

• You may generate a MATLAB Simulink with an interface shown in **Fig..6**. Open this file in MATLAB Simulink. Import ultrasonic power (as watts) and ultrasonic time (as seconds) values to the Simulink file.

• Adjust the simulation time. If the ultrasonic time is 1.4 seconds, make sure that the simulation starts at zeroth second and ends at 1.4^{th} seconds. If there is a time difference between the ultrasonic time and simulation time, integration gives different results which leads to miscalculation.

• The process model takes ultrasonic power raw data and ultrasonic time raw data and creates ultrasonic power-ultrasonic time plot automatically. It calculates the area under the curve to find the ultrasonic energy.

• Adjust Ultrasonic power (US power), ultrasonic time (US time), temperature, the height of stud bumps, the diameter of stud bumps, and the number of stud bumps. Please see **Fig. .6**.

• After adjusting the parameters, start the calculation. You will obtain %Tm

real value. This value is the calculated real interface temperature (T_{int}). If T_{int} is between 46%-69%, the process will most likely be successful if there are no other issues in the process or pre-process arrangements.

IMPORTANT: T_{int} should be 46%-69% of the melting temperature of gold to achieve good TSFCB bonding under sufficient pressure value. The observed sufficient pressure value is more than 80 MPa during these studies.

IMPORTANT: Compare estimated T_{int} and calculated real T_{int} value. You can estimate process parameters prior to the TSFCB.

X. Performing CMUT-PCB Integration with the FCB Tool

• The FCB tool can be used to perform CMUT-PCB integration.

• Prior to the FCB process, perform stacked GSB fabrication on the bonding pads of the CMUT chip. Also, perform placing conductive paste on the bonding pads of the PCB.

• Opening procedure of the FCB tool is the same as the TSFCB process. To understand opening the FCB tool, please see section III in this Appendix.

• The FCB tool has a standard die collet (SDC). The SDC tool is used for CMUT-PCB integration.

• CMUT-PCB integration is completed using force and temperature, only. Ultrasonic vibration is not applied. Thus, ultrasonic module will not be used. Go to ultrasonic module, and unselect "use ultrasonic module".

• Since the ultrasonic module is not used, ultrasonic calibration is not unnecessary.

How to attach the SDC tool and how to adjust the height of the SDC tool

• Please untighten the screw on the placer arm with the torque adjustable

wrench of the FCB tool.

• Please insert the SDC tool into the hole of the placer arm. The tip of the SDC tool should be very close to the placer arm to avoid a collision.

• Tighten the screw.

• Focus on the surface of the heated stage via z-direction micrometer screw under maximum magnification and under maximum light conditions.

• Go to the swivel module.

• Adjust touchless = 0 mm. Swivel down.

• There will be a gap between the SDC tool and the surface of the heated stage. Please untighten the screw and allow the SDC tool to touch the surface of the heated stage. At this point, tighten the screw with the torque-adjustable wrench (40 cN.m).

• Swivel up again. Attach the vacuum hose to the back side of the SDC tool.

IMPORTANT: Adjusting the height of the SDC tool is highly critical to avoid collusion of CMUT to the PCB.

Performing CMUT-PCB Integration

• Place the CMUT chip on the heated stage of the FCB tool. The backside of the ASIC chips must look up.

IMPORTANT: The ASIC chips bonded by the TSFCB process prior to CMUT-PCB integration will be in contact with the heated stage of the FCB tool.

• Align the SDC tool to the CMUT chip. The SDC tool must hold the CMUT chip from the middle of the CMUT chip as shown in **Fig. .7**.

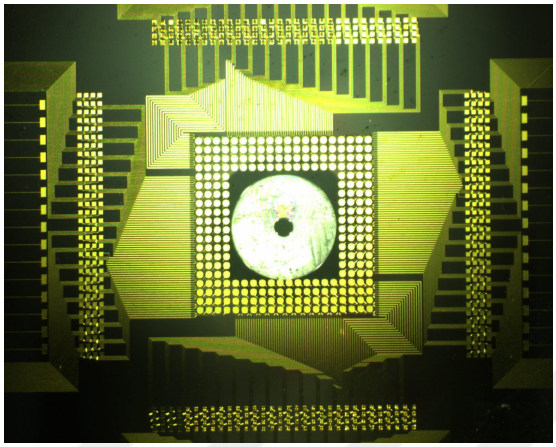


Figure .7: The SDC die collet touches the CMUT chip from the middle of the CMUT chip.

- After the alignment, go to the swivel module.

- Touch down mode: "Touch the target".

- Touch down force: 1 N.

- Swivel down. When the SDC tool touches the CMUT chip, open the vacuum of the placer arm by pressing the F4 button (to open the vacuum, go to the functions menu and select "switch vacuum at the placer arm").

- Swivel up.

IMPORTANT: There are 2 ASIC chips bonded by the TSFCB process on the CMUT chip. The ASIC chips must be on the right and on the left side of the CMUT chip because the beamsplitter can only move in the x- direction.

- Move the beamsplitter to the right side (press and hold CTRL+SHFT and press arrow key →).

- Focus on the bonding pad of the CMUT chip under maximum magnification and under maximum light conditions. Use the placer arm backward or forward motion button to focus.

• Place the PCB on the heated stage of the FCB tool. The bonding pads with conductive paste must be on the right and on the left side.

• Focus on the bonding pad of the PCB via z-direction micrometer under maximum magnification and maximum light conditions.

• Now it is time to do the alignment between the CMUT chip and the PCB.

• Since the CMUT chip is bigger than the field of the screen. We cannot see bonding pads on the right and bonding pads on the left at the same time. Therefore, we must move the beamsplitter to see the left and right sides.

• First, by using the air table, move the heated stage to perform a coarse alignment.

• Go to the right side with the beamsplitter (press and hold CTRL+SHFT and press the arrow key →). Check the alignment. Perform a fine alignment by using x-direction, y-direction, and theta micrometer screws.

• Go to the left side with the beamsplitter (press and hold CTRL+SHFT and press the arrow key ←). Check the alignment. Perform a fine alignment by using x-direction, y-direction, and theta micrometer screws.

• Then, check the alignment on the right side. If the alignment is good on both sides. The alignment is completed. If not, realign again. A good alignment is shown in **Fig. .8**.

• After the successful alignment, now it is time to adjust the process parameters.

• First, start by adjusting the temperature.

IMPORTANT: Conductive paste used in this study cures at 80 °C for 3 hours. However, the FCB tool cannot apply a temperature value for 3 hours. Thus, instead of adjusting the temperature section, we will adjust the standby temperature as the target temperature.

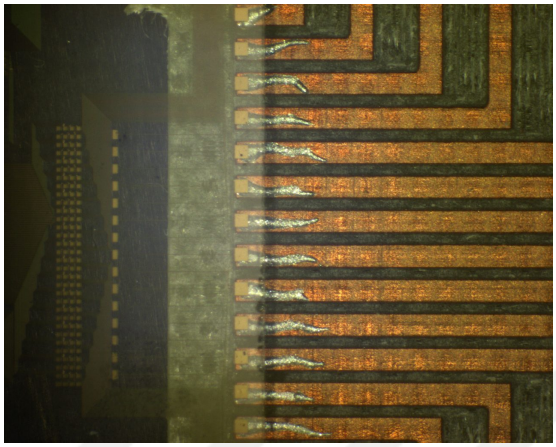


Figure .8: A good alignment between the CMUT and the PCB.

- Go to the heating plate process module.
- Adjust the standby temperature to the target temperature (80 °C).
- Second, we need to adjust the force value.
- Go to the swivel module.
- Touch down mode: "Touch the target".
- Touch down force: 1 N.
- Touch down height untaught: 6 mm.

IMPORTANT: Untaught touch down height ensures that the placer arm will slowly swivel down when the distance between the heated stage is 6 mm. It reduces the risk of damaging the CMUT or PCB by collusion.

- Go to force sections. A force can only be applied for 3900 seconds at each section. However, we need to apply the force for 3 hours.

3 hours $\rightarrow$ 10800 seconds

Section-1: Force value is 1 N for 3900 seconds.

Section-2: Force value is 1 N for 3900 seconds.

Section-3: Force value is 1 N for 3000 seconds.

In total, we will apply 1 N for 10800 seconds (3 hours).

• In miscellaneous part, mode vacuum switching → before lift off.

• When process parameters are adjusted, start the process.

• Press the start button.

• The machine will ask for a serial number. Write "1" and press enter.

• At this point, please control the process parameters again and make sure that you are happy with the process parameters.

• Press the continue button.

• The process will start. First, the beamsplitter goes to the safety position. Then, the placer arm will swivel down.

• The stacked GSBs will be in contact with the bonding pads of the PCB. The stacked GSBs will be embedded into the conductive paste material.

• After 3 hours, the vacuum of the placer arm switches off and the placer arm swivels up.

• The beamsplitter goes to the optical position.

• The process is completed.

XI. Closing the FCB Tool

• Closing the FCB tool is the same for both the TSFCB and CMUT-PCB processes.

- Move the beamsplitter to the safety position.
- Move the heated stage to the right side of the air table.
- Always close the software first.
- Go to file and select “Finish”.
- It will ask to save the PCB. Select “yes” after the TSFCB process, but select ”no” after the CMUT-PCB integration process.
- The IPM Hybrid software is now closed.
- Close the FCB tool by pressing the power button.
- Close the screen of the FCB tool but do not close the computer of the FCB tool.