TIME OF FLIGHT BASED LIDAR

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Master's Thesis

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Programme in Nanotechnology

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ABSTRACT

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In this study, how a time of flight (TOF) based light detection and ranging (LiDAR) works and how LiDAR systems can be done is investigated. The focussed part of the LiDAR is the receiver circuit. Photodiodes produce a very low current in response to light. This low photodetector current should be amplified in a fast and noiseless way. For this reason, a trans-impedance amplifier (TIA) circuit is designed and simulation results are shown. A comparator circuit should compare the output voltage of the trans-impedance amplifier and produce a stop signal for field programmable gate array time to digital converter FPGA TDC. Therefore, a fast comparator circuit with low overdrive dispersion is designed and simulation results are shown. To measure the distance by calculating the time of flight of the light, an FPGA TDC is designed and test experiments are done. A simple and cheap analog timer circuit is designed, and simulation results are shown in addition to FPGA TDC. LiDAR systems must measure time in a very accurate way. The calculation of signal processing times of electronic components in LiDAR systems is vital. It is found and shown in the simulation results that TIA signal processing time changes according to photodetector current magnitude and comparator signal processing time changes with the output voltage of TIA. Two objects with different reflectances at the same distance can be perceived as different positions by LiDAR systems and it is shown by simulation results. In summary, how to perform a precise time measurement for LiDAR systems is researched and supported by simulation results.

Keywords: Light detection and ranging (LiDAR), Field programmable gate array time to digital converter (FPGA TDC), Trans-impedance amplifier (TIA), Time of flight (TOF).

ÖZET

IŞIĞIN UÇUŞ ZAMANI TEMELLİ LİDAR

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Danışman: Prof. Dr. Uğur SERİNCAN

Bu çalışmada, temel olarak ışık uçuş zamanı ölçümlerine (TOF) dayanan bir LiDAR sisteminin nasıl çalıştığı ve nasıl yapılabileceği araştırılmıştır. Daha çok LiDAR sisteminin alıcı devreleri üzerinde durulmuştur. Fotodiyotlar ışığa tepki olarak çok düşük bir akım oluştururlar. Bu düşük fotodiyot akımı hızlı ve gürültüsü az bir şekilde yükseltilmelidir. Bunun için bir trans-empedans yükseltici devresi tasarlandı ve simulasyon sonuçları gösterildi. Trans-empedans yükselticinin (TIA) çıkış gerilimi bir eşik gerilimi ile karşılaştırıp alanda programlanabilir kapı dizleri (FPGA) zamandan dijitale dönüştürücü (TDC)'ın zaman ölçümünü bitirebilmesi için bir bitiş sinyali verilmelidir. Bunun için hızlı ve işlem zamanı sapması düşük bir karşılaştırıcı devresi tasarlandı ve simulasyon sonuçları gösterildi. Işığın uçuş zamanının hesaplanıp hedef nesnenin mesafesinin ölçümü için bir FPGA TDC zamanlayıcı tasarlandı. FPGA TDC zamanlayıcısının test deneyleri yapıldı. Bunun yanında basit ve ucuz bir analog zaman ölçüm devresi önerilmiş ve simulasyonları yapılmıştır. LiDAR sistemleri çok hassas bir zaman ölçümü gerektirir. Elektronik devrelerin işlemlerinden kaynaklanan zaman gecikmelerinin hesaplanması önemlidir. Dedektör akımına bağlı olarak trans-empedans yükseliticilerin işlem süreleri, trans-empedans yükselticilerin çıkış gerilimlerine bağlı olarak da komparatör devrelerinin işlem süreleri değiştiği simulasyon sonuçları ile gösterilmiştir. Aynı mesafedeki yansıtıcılıkları farklı olan iki hedefin LiDAR sistemleri tarafından farklı mesafelerde olarak algılanabileceği simulasyon sonuçları ile gösterilmiştir. Özet olarak LiDAR sistemleri için hassas bir zaman ölçümünün nasıl gerçekleştirelebileceği araştırılmış ve simulasyon sonuçları ile desteklenmiştir.

Anahtar Sözcükler: LiDAR, Trans-empedans yükseltici (TIA), FPGA zamandan dijitale dönüştürücü (FPGA TDC), Işık uçuş zamanı (TOF)

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Azad Ozan KORKAN

08/10/2020

STATEMENT OF COMPLIANCE WITH ETHICAL PRINCIPLES AND RULES

I hereby truthfully declare that this thesis is an original work prepared by me; that I have behaved in accordance with the scientific ethical principles and rules throughout the stages of preparation, data collection, analysis and presentation of my work; that I have cited the sources of all the data and information that could be obtained within the scope of this study, and included these sources in the references section; and that this study has been scanned for plagiarism with "scientific plagiarism detection program" used by Eskişehir Technical University, and that "it does not have any plagiarism" whatsoever. I also declare that, if a case contrary to my declaration is detected in my work at any time, I hereby express my consent to all the ethical and legal consequences that are involved.

Azad Ozan KORKAN

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GLOSSARY OF SYMBOLS AND ABBREVIATIONS

ADC	:	Analog to digital converter
AR	:	Anti-reflection
ASIRT	:	Association for safe international road travel
eV	:	Electron volt
fF	:	Femtofarad
FPGA	:	Field programmable gate array
FWHM	:	Full-Width half maximum
GaAs	:	Gallium arsenide
IDE	:	Integrated development environment
JFET	:	Junction field-effect transistor
Khz	:	Kilohertz
Laser	:	Light amplification by stimulated emission of radiation
LiDAR	:	Light detection and ranging
LVCMOS33	:	3.3 V low voltage CMOS output voltage
LVDS	:	Low voltage differential signaling
Mhz	:	Megahertz
MMCM	:	Mixed-mode clock manager
mV	:	Millivolt
NEP	:	Noise equivalent power
nm	:	Nanometer
ns	:	Nanosecond
OPAMP	:	Operational amplifier
PCB	:	Printed circuit board
pF	:	Picofarad
PLL	:	Phase locked loop
ps	:	Picosecond
RADAR	:	Radio detection and ranging
RAM	:	Random access memory
Si	:	Silicon
SiO2	:	Silicon dioxide

SNR	:	Signal to noise ratio
TDC	:	Time to digital converter
TIA	:	Trans-impedance amplifier
TOF	:	Time of flight
UART	:	Universal asynchronous receiver transmitter
μm	:	Micrometer

1. INTRODUCTION

Transportation has a very important place in human life and society. The invention of motor vehicles made possible to travel long distances easily. Cars are now very common, and their numbers are much higher than before. This allows more people to travel freely and go to workplaces, holiday centers, family visits. But despite the advantages, increase in vehicle number increases the possibility to encounter accidents mostly because of driver failure. According to the association for safe international road travel (ASIRT), 1.35 million people die, and 20-50 million people are injured or disabled because of car accidents in every year. This is obviously very sad and great loss. It is shown in a review paper that the primary reason behind %60 of the crashes is driver based while the %95 of the crashes includes driver behaviors in addition to other reasons [1]. Automated driving systems (ADS), commonly referred to as self-driving cars appear as a very good solution to reduce car accidents. Many people believe that self-driving cars will save millions of people's lives by preventing crashes related to driver failure. Besides the reduction of car crashes, self-driving cars will help disabled peoples drive cars individually. Therefore, they can live freely then before. In addition, it is believed that self-driving cars will reduce fuel use and carbon emission. Therefore, they will help fight against global warming.

One of the key technologies behind the self-driving car is light detection and ranging (LiDAR). LiDAR is like the eyes of a human for automated driving systems. Ordinary cameras give information about the environment to the automated driving systems, but LiDAR technology gives the depth information as well. Depth information of the objects around the self-driving cars is very important. Because autonomous vehicles must know the locations of pedestrians, traffic lights, sidewalks, trees, in short, every object around it so that it can travel without hitting them and causing any crash [2]. LiDAR technology always monitors around self-driving cars and help maintain the braking distance with pedestrians and vehicles in front of it. LiDAR technology supplies high-resolution three-dimensional images [3]. Therefore, LiDAR systems in autonomous cars can also measure the speed and orientation of pedestrians to act by taking pedestrians as a reference [4].

LiDAR technology is also used for geomorphology, urban planning, forestry which is called topographic LiDAR [5]. It is used to make depth observations in critical areas to

prevent landslides. A type of LiDAR called Bathymetric LiDAR is used to get water depth and elevation information [6]. Some drones use LiDAR technology to take off and land easily, which prevents them from hitting objects around the drones [7].

In recent years, LiDAR technology has become very popular. However, there is a lack of studies in Turkey related to electronics and software of LiDAR. Designing a LiDAR system is not so common. There is a road map for Turkey to produce a national electric car. For this purpose, engineers and scientists in Turkey should increase their knowledge about this important technology. Hence, in this thesis, circuit simulations and software research on LiDAR technology were performed. A time to digital converter was designed in a field programmable gate arrays (FPGA) device to measure the time of flight of the light to calculate the distance. Experiments were done to prove the method followed to make FPGA time to digital converter is true. According to the results, a few hundred ps resolution would be possible.

In Chapter 2, the basic structure and schematic of a time of flight-based LiDAR are mentioned. An example transmitter circuit and infrared detector design stages and parameters are mentioned. A cheap and simple analog timer circuit is designed and simulated. In Chapter 3, the designed trans-impedance amplifier of the LiDAR is demonstrated. In Chapter 4, the designed comparator circuit of the LiDAR is demonstrated. In addition, important time errors caused by electronic components are shown via simulations. In Chapter 5, the third part of the LiDAR receiver circuit which is the designed FPGA time to digital converter for the time of flight calculation is demonstrated. Finally, in Chapter 6, the conclusion of the thesis is presented.

2. BASIC STRUCTURE OF A TIME OF FLIGHT BASED LIDAR

LiDAR is a distance measurement method. It is similar to radio detection and ranging (RADAR) in the manner of the target range detection. While RADAR transmits radio waves to determine the range, angle, and velocity, LiDAR transmits invisible or visible light to detect the target object distance. Some LiDAR systems can also measure the speed and direction of the objects by using the Doppler effect like RADAR systems [8]. A basic structure of a pulsed time of flight LiDAR which consists of transmitter, receiver, time measurement circuit and optic is shown in Figure 2.1. It includes laser diode, laser diode driver, an avalanche photodiode, two plano-convex lenses, an amplifier circuit behind the photodiode to trigger the time measurement circuit, one FPGA TDC, and one computer for calculating the time of flight of the light to measure the distance of the object. In this thesis, the focussed part is the time measurement, transimpedance amplifier and comparator circuit design rather than designing lenses, photodiode, laser diode and laser modulator circuit.

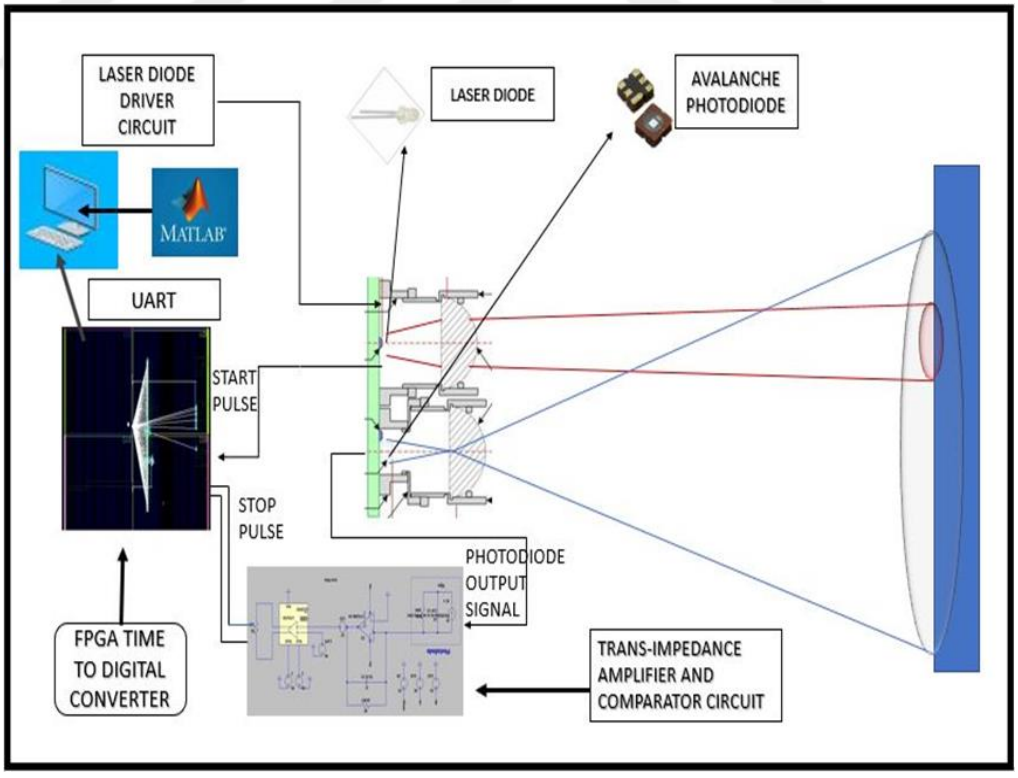

Figure 2.1. *A basic structure of the pulsed time of flight LiDAR*

2.1. Laser Diode

Laser diodes are the main illumination sources of the LiDARs. Since illumination is included in LiDAR systems, they can operate in the night as well. Actually, LiDAR systems work better in the environment in which there is no sunlight. Because sunlight causes a noise for the photodetectors of the LiDAR. The acronym laser stands for light amplification by stimulated emission of radiation. The photons coming from the laser have well defined wavelength unlike the sunlight. Therefore, laser light is coherent which means it contains waves with same frequency and phase. Laser light has high intensity and narrow beam in addition to its coherent feature. The laser purchased for this thesis is OSRAM SPL PL90_3. A 905 nm laser diode with 90 W peak output power is chosen for the planned LiDAR for this thesis. Its relative spectral distribution is shown in Figure 2.2.

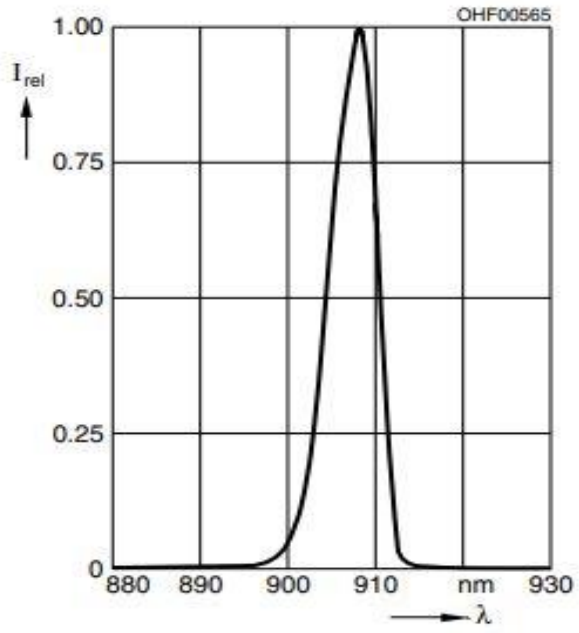

Figure 2.2. *The relative spectral distribution of OSRAM SPL PL90_3 laser diode* [9].

The selected laser diode's maximum peak output power is 90 W. It is suited for short laser pulses from 1ns to 100 ns. 90 W continuous laser output power can be destructive for the human eye and other body parts. But, short pulses from 1ns to 100 ns decrease its average power such that it is not harmful to human eyes anymore. The IEC 60825 standard for the safety of laser products is very important. Before designing a

LiDAR system this standard must be checked. OSRAM SPL PL90_3 laser diode is found suitable for the targeted LiDAR system and IEC 60825 standart.

The rise time and fall time of the selected laser diode is 1 ns. Fast rise and fall time are important for LiDAR design. Because it decreases deviation in time calculation. It can decrease the walk error which will be shown in the Section 4.2. The maximum forward current of the laser diode is 40 A. The Repetition rate of the laser diode is 1 kHz. To be able to operate the laser diode an external circuit is required. Laser modulator circuits for LiDAR are commercially available. They can be found and purchased on the internet easily.

The first part of the LiDAR is to transmit the laser light. When a proper bias voltage is applied to the laser diode from the laser driver circuit in a short pulse, the laser diode starts to emit stimulated light. To start the timer which is shown in the basic structure in Figure 2.1, a parallel wire can be connected to the timer to monitor the time of the peak output power of the laser diode. As a timer, an FPGA time to digital converter (TDC) is designed to measure the time of flight of the light which is emitted from the laser diode. Two methods that can be a candidate for time measurement are shown in Section 2.4. Another method to start the timer is to use a beam splitter and two photodiodes instead of one photodiode. Some of the laser light hits the beam splitter and change direction after emitting from the laser diode. The light in which its direction is changed by beam splitter hits the first photodiode. A circuit behind the first photodiode amplifies the photodiode current to a sufficient voltage level to start the timer. The emitted laser light in which its direction is not changed by the beam splitter propagates through the air until it hits an object. After hitting an object, it reflects back to the photodiode. When the reflected light hits the receiver, it produces a current depending on the number of the photons in the light if photodiode is reversed biased. The calculation of the photocurrent is explained in Section 3.1. The produced current in the photodiode is amplified to a sufficient voltage level to trigger the timer to stop the time of flight calculation. After subtracting the time delays in the electronic components from the measured time by the timer, time of flight can be found.

An appropriate optical part should be designed for the laser light and photodiode to focus on the objects and return back at a maximum intensity after hitting and reflecting from objects. Designing optic parts for the LiDAR is out of the scope of this thesis.

2.2. Optic

Since the lenses are important to increase the range of the LiDAR a few examples should be shown. In LiDAR systems, photodiodes and lasers are generally placed in the same printed circuit board (PCB). The laser diode and photodiode optics should be placed as close as possible. Because the field of view of the photodetector should cover the collimated laser beam in the short-range. In other words, being placed of laser and detectors as close as possible determines the minimum measurable distance of the LiDAR [10]. Plano-convex lens is a lens that has a shape of one flat surface and one spherical surface. Two plano-convex lenses can be seen in Figure 2.3. A plano-convex lens is used to collimate the laser light. Another plano-convex lens is used to focus parallel rays of the collimated laser light to the photodetector in Figure 2.3.

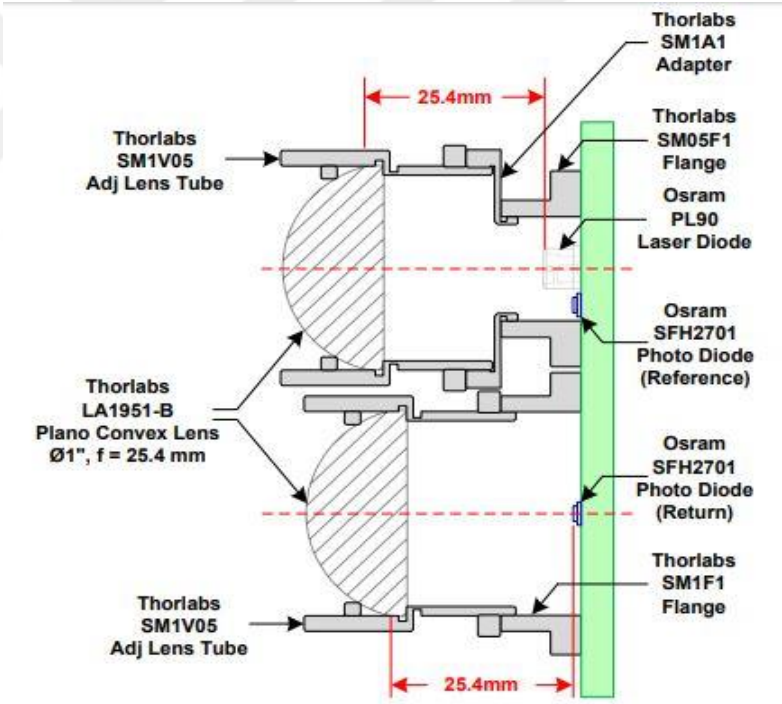

Figure 2.3. *An example of a laser diode and photodiode optics for LiDAR applications* [10].

To be able to calculate the LiDAR distance measurement range determined by the optics, as a first step optical aperture and beam divergence angles of the selected OSRAM SPL PL90_3 should be learned from its datasheet. The optical aperture of the laser is 200 µm x 10 µm.

The full-width half maximum (FWHM) beam divergence parallel to the p-n junction of the laser diodes is 9º. The FWHM beam divergence vertical to the p-n junction of the laser diodes is 25º. To calculate the collimated beam width and collimated beam divergence, Equation 2.1 and Equation 2.2 can be used, respectively [10]. Ø is the produced beam after the laser beam is collimated. The focal length of the plano-convex lens of the laser diode is denoted by *f*, Q is the laser beam divergence angle before collimation, laser diode optical aperture is shown by y and the divergence angle of the collimated laser beam is shown by α. The focal length of the plano-convex lens is 25.4 mm, the optical aperture is 200 µm and the laser beam divergence is 25º. Therefore, the calculated collimated laser beam is 11.5 mm according to Equation 2.1. The collimated laser beam width is not constant as can be seen in Figure 2.4. There is a divergence angle which is calculated as 0.226º according to Equation 2.2. Thus, laser beam width increases with the increased distance to the aperture of the laser diode. For 3D LiDARs, it decreases the resolution of the depth image. Let assume that there are two objects which are very close to each other. The wide laser beam hits both. Therefore, source objects of reflected laser beam cannot be understood.

$$Ø\ Laser = 2\ \times\ f\ \times \tan\left(\frac{Q}{2}\right) + y \tag{2.1}$$

$$\alpha\ Laser = 2\ \times \arctan\left(\frac{y}{2\times f}\right) \tag{2.2}$$

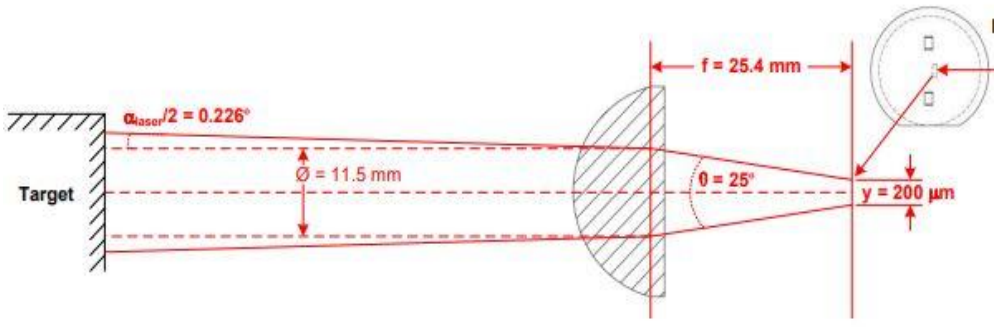

Figure 2.4. *Collimated laser beam width and divergence calculated by Equation 2.1* [10].

After the calculation of the collimated beam width and its divergence angle, the field of view of the photodiode should be calculated to determine the minimum

measurable distance. The divergence angle of the collimated laser beam in one direction is the 0.226º. The total divergence angle is twice of it which is 0.452º. The field of view of the photodetector should be larger than the total divergence angle to cover all collimated laser beam and measure the distance better. One important optical design criterion is that increasing the lens diameter gives the advantage to collect a larger reflected laser beam. However, as the laser and detector move away from each other, field of view of the photodetector cannot cover all reflected laser beam. Thus, minimum sensing range increases. The Equation 2.3 can be used to determine the field of view of the photodetector.

$$\alpha = 2 \times \arctan\left(\frac{d}{2xf}\right) \tag{2.3}$$

The diameter of the area in which collimated laser light is focused is shown by d in the equation and Figure 2.5. The field of view of the photodiode is shown by α and the focal length of the plano-convex length is shown by f. The selected avalanche photodiode for this thesis is MTAPD-07-015 which has a circular active area with a diameter of 500 µm. In Figure 2.4, a calculation result for an active area with 850 µm is illustrated.

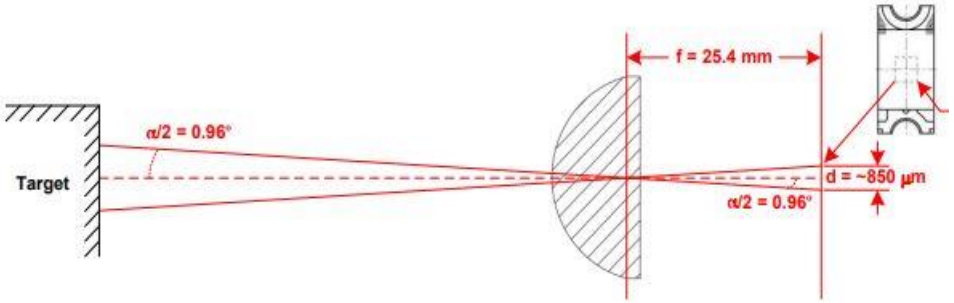

Figure 2.5. *A result of Equation 1.3 for 850 µm focus area* [10].

The field of view calculated for 850 µm focus area is 1.92º. The divergence angle of the collimated laser beam was 0.452º. The field of view angle is much larger, so it is proper for collecting all reflected light of the laser beam. It is suitable also for the selected avalanche photodiode sensing area because it covers the sensing area of the photodiode easily. The Equation 2.4 can be used to determine the minimum detectable range. The measurable distance is shown by d. Distance between the lens of the photodetector and

lens of the laser is shown by x. Tan(a) is the tangent of half of the field of view angle. Tan(b) is a tangent of half of the divergence angle of the collimated laser beam. Let assume x is 3 cm, then the minimum measurable range is calculated as 145 cm. It means the reflected laser beam is not focused on the photodetector before 145 cm.

$$d > x/(\tan(a) + \tan(b)) \tag{2.4}$$

2.3. Photodiode

The first stage in the receiver circuit is the photodiode and it is in the main structure of the LiDAR which can be seen in Figure 2.1. Photodiodes are sensors which convert the light into electrical current. The basic photodiode structure consists of a p-n junction.

2.3.1. The working principles of photodiodes

A p-n photodiode and its working principle can be seen in Figure 2.6. P-type material is the source of the holes while n-type material is the source of electrons. In other words, in p-type region number of the holes are much larger than the electrons and it is vice versa for the n-type region. P-type and n-type materials are formed by doping the intrinsic semiconductor materials. Si is a Group 4A element. When Si atoms are doped with Group 3A elements such as boron, aluminium, gallium, indium, a p-type material is formed and when Si atoms are doped with Group 5A elements such as phosphorus, arsenic, and antimony an n-type material is formed [11]. Doping atoms that form the n-type region are called donor atoms because they give their electron which does not have a bond to the lattice. Doping atoms that used to form the p-type region are called acceptor atoms because they produce holes that accept electrons.

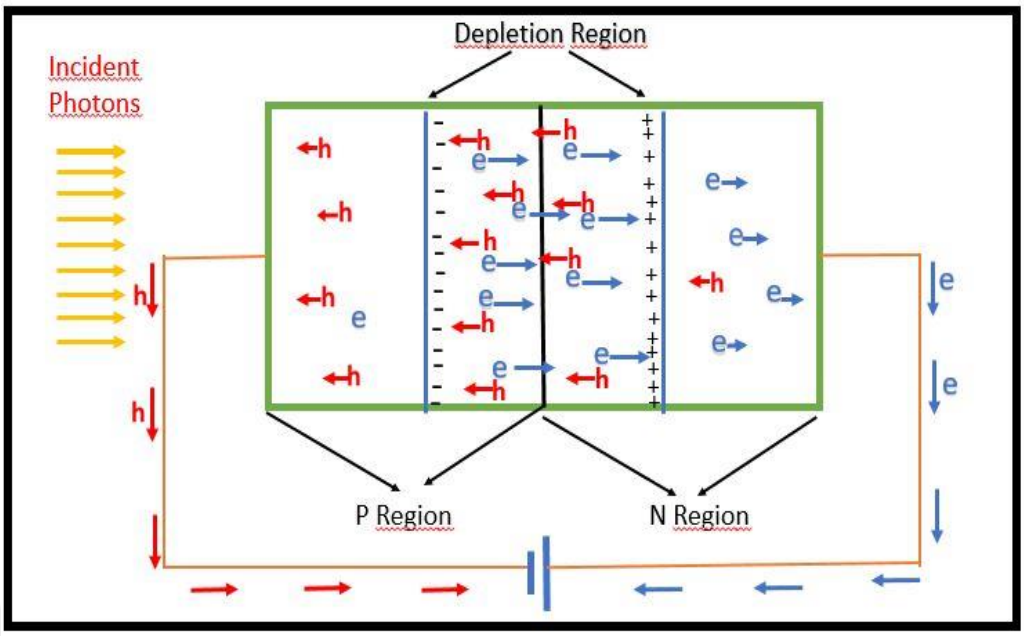

Figure 2.6. *Working principle of a p-n photodiode.*

In Figure 2.6, a mechanism in p-n photodiode to produce a voltage or current when incident photons strike the lattice of the photodiode is shown. When a p-n junction is formed, electrons in the n region starts to flow towards the p region and holes in the p region starts to flow toward the n region because of diffusion. Diffusion takes place from an area of high concentration to an area with less concentration region [12]. Electrons recombine in the p-type region and holes recombine in the n-type region. Therefore, a region is formed called the depletion region [13]. There are no mobile carriers in the depletion region. After the movement of the electrons toward the p-type region, positively charged ions are created in the place where electrons leave. In the same manner, holes leave negatively charged ions in their departure regions. Thus, an electric field is formed from the n-type region towards the p-type region [14]. No more carrier's movement occurs after the depletion region is formed. Electrons cannot move towards the p-type region and holes cannot move towards the n-type region. The active region which senses the light in the photodiodes is the depletion region. When photons with enough energy hit the bonds between atoms in the lattice, they break some bonds and form electron-hole pairs [15]. Electron and holes sense a force on them, and they start to drift by the electric field [16]. Electrons are forced to move towards the n-type region and holes are forced to move towards the p-type region in the effect of the electric field. When the electrons and

holes reach the contacts of the photodiode, a current and voltage signal is produced.

According to Pauli exclusion principle, when atoms come together and make bonds to form molecules, electrons connot have same quantum number [17]. To obey this rule, the orbitals split to M different numbers where M represents the number of atoms in crystal lattice. Therefore, M different energy levels are produced. Since this energy levels are very close to each other, it looks like a continous band [18]. The energy gap between valance and conduction energy level is called bend gap. Energy of the coming photons must be greater than the bandgap of the semiconductor material of the photodiode to be able to jump the electrons from the valance band to conduction band and produce a current [19]. As the wavelength of a photon increases the energy of the photon decreases. The equation of the energy of a photon according to its wavelength is shown with Equation 2.5 [20]. The speed of the light is shown by c and the Planck constant is shown by h. Therefore, hc value in the equation is constant. The energy of the photon is shown by E and the wavelength of the photon is shown by λ. If E is expressed with eV unit and λ is expressed with nm unit hc is approximately equal to 1240 eVnm.

$$\lambda = hc/E \tag{2.5}$$

The cheap commercially available laser diodes with high output power to use in LiDAR has 905 nm wavelength. Therefore, the semiconductor material of the photodiode should be chosen so that the energy of photons of the laser light is higher than the chosen semiconductor's bandwidth. 905 nm wavelength corresponds to 1.37 eV energy according to Equation 2.5. Therefore, the semiconductor materials with bandgap below the 1.37 eV can be used as a photodetector. In Table 2.1 band gaps of various semiconductors are shown at 0 and 300 K temperatures. For example, the bandgap of the Si is 1.17 eV, so it can be used with the selected laser. But the bandgap of the GaAs is 1.52 eV so the laser light can not produce a voltage or current on a GaAs photodiode. Because photons of laser light have not sufficient energy to jump an electron from GaAs valance band to GaAs conduction band. Most of the commercially available photodiodes are made by Si [21].

Table 2.1. *Band gaps of various semiconductor materials at 0,300 K .*

Semiconductor	Si	Ge	InSb	InAs	InP	GaP	GaAs	GaSb
Band Gap (eV) 0K	1.17	0.74	0.23	0.43	1.42	2.32	1.52	0.81
Band Gap (eV) 300K	1.11	0.66	0.17	0.36	1.27	2.25	1.43	0.68

2.3.2. The rise and fall time calculations of photodiodes

To be able to choose a photodiode to use in LiDAR. The photodiode characteristics should be understood well. The photodiode should be fast, and it should detect the low light power. Besides, the photodiode should have low noise. The first photodiode characteristic to be considered is the rise and fall times of the photodiode. The rise and fall time of the photodiode should be fast to capture the short laser diode light pulses and to decrease the time of flight calculation error. The rise time of a photodiode is defined as the required time for the signal to rise from 10% to 90% of the final value while the fall time is defined as the required time for the signal to fall from 90% to 10% of the final value [22]. Rise time can be calculated by using frequency response information of the photodiode as a first way. The rise time of a photodiode can be calculated by the Equation 2.6 [23].

If a modulated laser signal is projected on the photodiode and the frequency is increased by observing the output of the photodiode, the frequency in which the photodiode output signal decreases by 3 dB can be calculated. If 0.35 is divided by the found frequency, the result gives the rise time of the photodiode. The rise time of the selected avalanche photodiode is 0.6 ns for 905 nm, 100 Mhz and 50Ω load resistance parameters. The response time of a photodetector is the time required that carriers reach the contacts to produce a signal after photons hit the photodetector.

$$t_r \cong \frac{0.35}{f_{3dB}} \qquad (2.6)$$

One of the parameters affecting the response time is the carrier drift time in the depletion region of the photodiode [24]. Photons create the most carriers in the depletion region and the first road of the carriers is in the depletion region [25]. Velocities of the carriers are not the same in every region of the photodiode since different effects exist on the carriers to move them towards the contacts of the photodiode. The speed of the carriers in depletion regions is called transit speed in some resources [26]. Transit speed depends

on the mobility of the carriers and electric field which is applied on the carriers. Mobility is a feature that shows how fast carriers in semiconductors travel when they are affected by an external electric field. The units of mobility of the carriers and electric field are $m^2/(V \cdot s)$ and V/m in the MKS system, respectively [27]. When these units are multiplied, the result is in the unit of m/s which is the unit of the speed. Therefore, drift velocity or transit speed can be found by multiplying the mobility by the electric field applied. Transit time is the time required for carriers to reach the end of the depletion region. Transit time can be calculated with the Equation 2.7 [28]. The depletion layer width, transit speed, mobility of the carriers and applied reverse bias are shown by d, V_d, μ and V_R, respectively. The depletion region width changes according to applied reverse bias. Hence, transit time equation should be extended to observe which parameters affect the transit time and how those parameters affect the transit time so the rise time of the photodiode. To expand the Equation 2.7, first the equation of the depletion region width should be found. Depletion region width or depth can be calculated with the Equation 2.8 [29].

$$t = \frac{d}{V_d} = \frac{d^2}{\mu V_R} \tag{2.7}$$

$$W_d = \sqrt{2\epsilon_{Si}\epsilon_0\mu\rho(V_R + V_{bi})} \tag{2.8}$$

$$t = 2\epsilon_{Si}\epsilon_0\rho(V_R + V_{bi})/V_R \tag{2.9}$$

The last transit time calculation can be attained by putting the depletion width equation to the place of the depletion width in the Equation 2.7. The last transit time after this operation is shown in Equation 2.9. $\epsilon_{Si}, \epsilon_0$ are permittivity of the free space and silicon dielectric constant which have values 8.854×10^{-14} and 11.9, respectively. ρ is the resistivity of the silicon and as resistivity increases, the transit time increases. The case here is that resistivity increases the depletion width in direct proportion with its square root. Therefore, in the pin diode which will be mentioned later in the Section 2.3.5, there is an intrinsic region between the p and n regions. Since this region is intrinsic which is undoped, resistivity is greater than the doped regions. Thus, it increases the depletion layer width. pin diodes are commonly used in LiDAR because they have a fast response time. μ is the mobility which is 1400 cm^2/Vs for electron and 450 cm^2/Vs for the hole for the Si. V_R is the reverse bias that is applied externally. V_{bi} is the built-in voltage inside the photodiode. In diodes, a built-in voltage occurs due to the electric field of the depletion

region. The applied forward voltage must be greater than this built-in voltage to make a diode conduct the electricity. Since the built-in voltage, dielectric constant and resistivity are related to material and manufacturer, they are not in our control to change. The only reverse bias voltage can be controlled to change the transit time of the carriers. Equation 2.9 can be rewritten to show the effect of the V_R clearly.

$$t = 2\epsilon_{Si}\epsilon_0\rho(1 + \frac{V_{bi}}{V_R}) \tag{2.10}$$

The only adjustable parameter to change the transit time of the carriers is the reversed bias voltage. According to Equation 2.10, if the reverse bias voltage is increased then transit time decreases. Therefore, the time for the carriers to reach contacts of the photodiode decreases and the rise time of the photodiode decreases, so the photodiode acts faster. The reverse bias also increases the width of the depletion region according to Equation 2.8. Thus, decrease the junction capacitance and increase the rise time. The maximum reverse voltage is limited by a voltage value. That voltage value is called the breakdown voltage. If the voltage value is increased above that breakdown voltage, the photodiode can be damaged. The fast rise time by applying the low reverse voltage is an advantage. Because it does not require an external voltage supply circuit. For instance, the suitable pin photodiode for this thesis is OSRAM SFH2701. It requires only 5V to achieve rise and fall time of 1.8 ns and it it is very cheap.

One of the parameters that affect the rise time of the photodiode is the diffusion time of the carriers which is generated in the region outside of the depletion region [30]. Diffusion time is longer than the drift time and limits the rise time [31]. Therefore, if current generated by a photodiode is dominated by the diffusion of carriers that are generated outside the depletion region, rise time will be slower than the current which is generated by the drifted carriers. To understand the generated carriers in a different region of a photodiode, a Si photodiode structure and penetration depth according to wavelength are shown in Figures 1.7 and 1.8, respectively. The example photodiode in Figure 2.7 is planar diffused Si photodiode. The substrate is n-type and the upper part of the photodiode is doped with acceptors such as boron to make the region p-type to form a p-n junction. AR coating is the anti-reflection coating and it is grown on the photodiode to let most photons transmit in. Optical bandpass filters are also important for LiDAR applications [32]. The selected avalanche photodiode which its brand is mentioned before has a 905 nm filter to prevent the environment light sources affect the LiDAR system. SiO_2 is used

for passivation to prevent surface leakage currents. Surface leakage current is a type of noise current [33]. This type of current decreases signal to noise ratio (SNR) and noise equivalent power (NEP) which will be mentioned in Section 2.3.3. Therefore, surface leakage current decreases the maximum measurable range of LiDAR systems by decreasing the SNR.

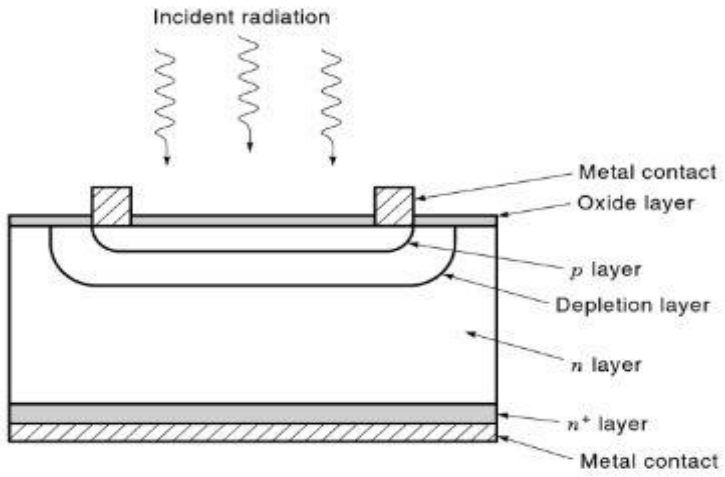

Figure 2.7. *The structure of a Si photodiode* [34].

Figure 2.8 shows the penetration depth of the visible and near-infrared region's wavelengths. As wavelength of light increases the penetration depth increases. Higher wavelengths can be absorbed in the surface of the photodiode without coming to the depletion region [36]. Thus, the source of current is the diffusion of generated carriers not drifted carriers in depletion region. It decreases the rise time of the photodiode. Therefore, laser wavelength can be a factor that decreases response time. In the pin photodiodes, most carriers are generated in the depletion region rather than other regions [37]. Hence, rise time of the pin photodiode is greater than pn photodiodes. That is why pin photodiodes are chosen with avalanche photodiodes for LiDAR applications.

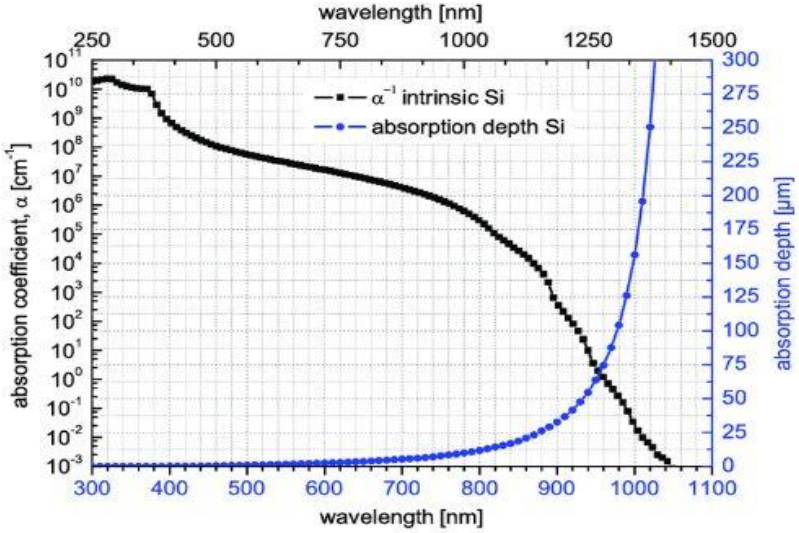

Figure 2.8. *The penetration depth in Si according to wavelengths of the photons* [35].

One of the important parameters which affect the rise time is the RC time constant of the photodiode and its circuit [38]. To understand the RC time constant, electrical characteristics of photodiodes should be known. A photodiode is a current source when it is illuminated. The current produced by the photodiode is shown by Iph in Figure 2.9 which shows the electrical characteristics of a photodiode. The Id is the current of the diode. Photodiodes are a type of diodes as explained before. Rsh is shunt resistance. Shunt resistance determines the slope of the I-V curve when the photodiode is forward biased. It can be found by applying a small forward bias voltage such as 10 mV to a photodiode. The value of the shunt resistance is desired to be highest as possible for the best photodiode performance. It is an important factor to understand the noise level of the photodiode in photovoltaic mode which is the mode of no bias applied. Rsh is the series resistance. In an ideal photodiode series resistance is zero. The produced current under illumination goes on Rs and RL in the electrical equivalent circuit in Figure 2.9. Therefore, a voltage drops on the series resistance Rs and the voltage on RL decreases. RL gives the voltage signal which is used to measure or amplified. Series resistance also increases the RC time constant and rise time. Since it affects the rise time it is important for LiDAR. Series resistance can be analyzed with Equation 2.11. Contacts of photodiodes play an important role in the series resistance. Contact resistance is shown by Rc in the equation. Thus, contacts should be made with the metals of best conductivity to decrease the series resistance and increase the rise time when designing a photodiode.

Ws is the thickness of the substrate of photodiodes and Wd is the depletion region width which is shown by Equation 2.8. When this equation is interpreted, it is seen that the region outside of the depletion region contributes to the series resistance. This region in the p-n diode is larger than the pin diode. Thus, a parameter that contributes pin diode fast rise time is low series resistance because of larger depletion width. A is the sectional area or diffused area of photodiodes. It is nearly proportional to the active illumination area of photodiodes. Although the diffused area decreases the series resistance, it increases the junction capacitance in photodiodes. Therefore, it decreases response time in photodiodes. ρ is the resistivity of the substrate. As resistivity increases series resistance increases.

$$R_s = \frac{(W_s - W_d)\rho}{A} + R_c \tag{2.11}$$

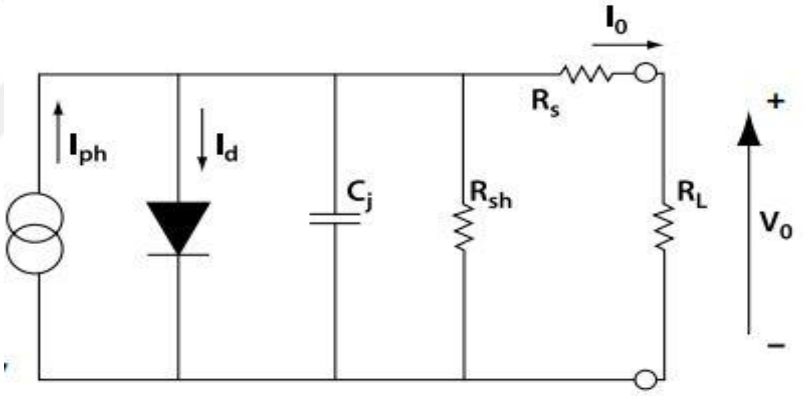

Figure 2.9. *Electrical characteristics of a photodiode* [29].

Junction capacitance is shown by Cj in the electrical characteristics in Figure 2.9. The depletion region can be considered as a parallel plate capacitor [39]. The diffused areas of the depletion region can be considered as parallel plates of a capacitor. Junction capacitance is proportional to the diffused area of photodiodes and it depends on depletion region width by inverse proportionally. The junction capacitance is shown in Equation 2.12 where A is diffused area and other parameters are as in the Equations in Section 2.3.2 [29]. Diffused are is an important parameter for junction capacitance of photodiodes and response time. Photodiodes with small active illumination areas have lower capacitance and faster response times [40]. After purchasing a photodiode only thing that

can be done to change junction capacitance is to change reverse bias voltage. An example of a junction capacitance graph according to applied reverse bias is shown in Figure 2.10 and rise and fall time according to applied reverse bias can be seen in Figure 2.11. This graph belongs to the datasheet of OSRAM SFH 2701 photodiode which is selected as the pin diode of this thesis addition to the selected avalanche photodiode.

$$C_J = \frac{\epsilon\epsilon_0 A}{\sqrt{2\epsilon\epsilon_0\mu\rho(V_A+V_{bi})}} \tag{2.12}$$

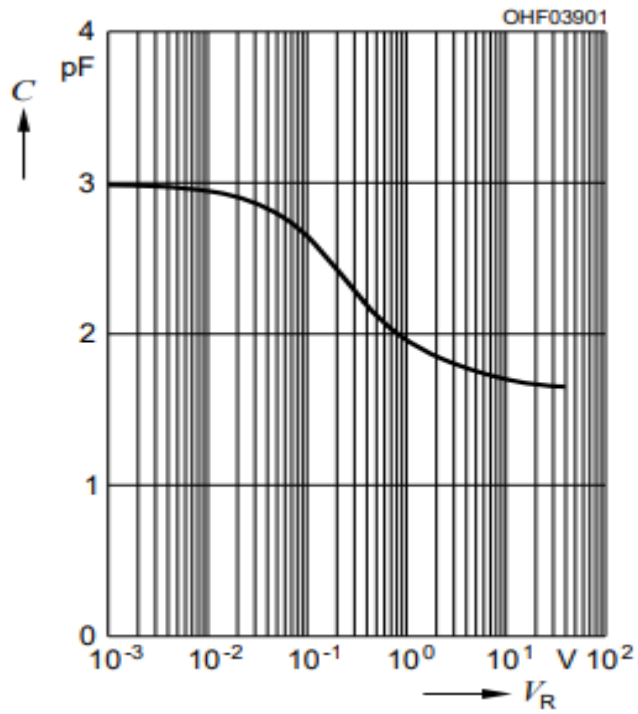

Figure 2.10. *Capacitance vs applied reverse bias of OSRAM SFH2701 pin photodiode* [41].

The RC time constant is important to get faster response time. The RC time constant is determined by 2.2 RC. R can be found by adding series resistance with load resistance which are shown in Figure 2.9. They are explained on the last page. C can be found by summing PCB capacitance or stray capacitance and junction capacitance of the photodiode. Therefore, PCB design and short leads are important to minimize stray capacitance to attain a faster response time [42]. Since junction capacitance depends on the diffused area and applied reverse bias. Small photodiodes with large reverse bias can achieve rise time below a few ns.

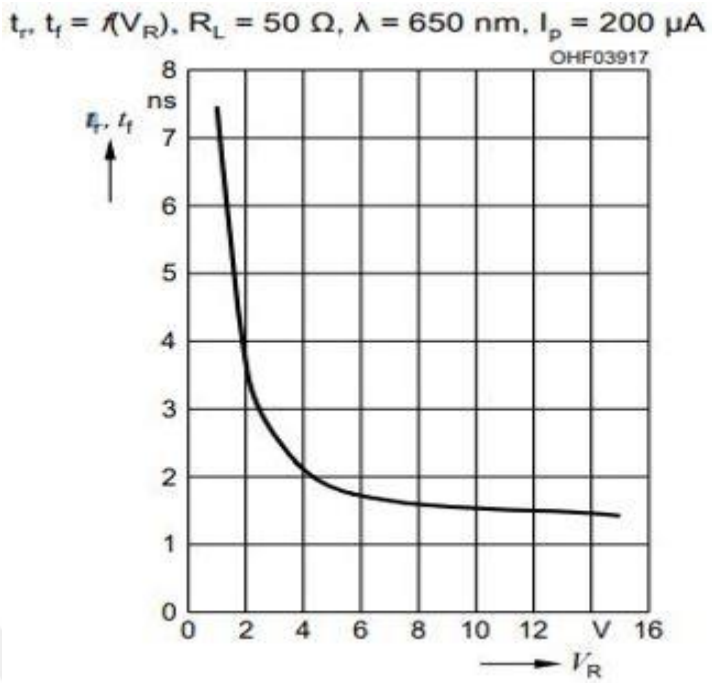

Figure 2.11. *Rise time vs applied reverse bias of OSRAM SFH2701 pin photodiode* [41].

The overall representation of the rise time of photodiodes depends on the drift, diffusion and RC times is shown in Equation 2.13 [30]. Rise time depends on three different times in Equation 2.13. One of them can be dominant to shape rise time and response waveforms. In Figure 2.12, an example of response waveforms of a photodiode is shown. The shape of the coming signal to photodiode is a perfect rectangle assuming rise time is zero. But the produced voltage is not in the shape of a rectangle. It shows that the photodiode loses some time to extract carriers which are generated by the incoming signal. The Drift time is less than diffusion time because of the effect of the electric field of the depletion region of photodiodes. The t1 and t3 times are drift and RC times, respectively. The t2 time of diffusion time. The first output waveform shape which is closer to the rectangle is under the domination of drift and RC times. Because the output waveform can respond to the input waveform quickly. But the other output waveform is dominated by diffusion time. Diffusion is a slow process. Therefore, output waveform does not capture input waveform. In pin and avalanche photodiodes depletion region is wide so they can collect the generated carriers quickly and their rise time is dominated by drift time and RC times if their junction capacitance is small and PCB capacitance is low.

$$t_R = \sqrt{t_{DRIFT}^2 + t_{DIFFUSED}^2 + t_{RC}^2} \tag{2.13}$$

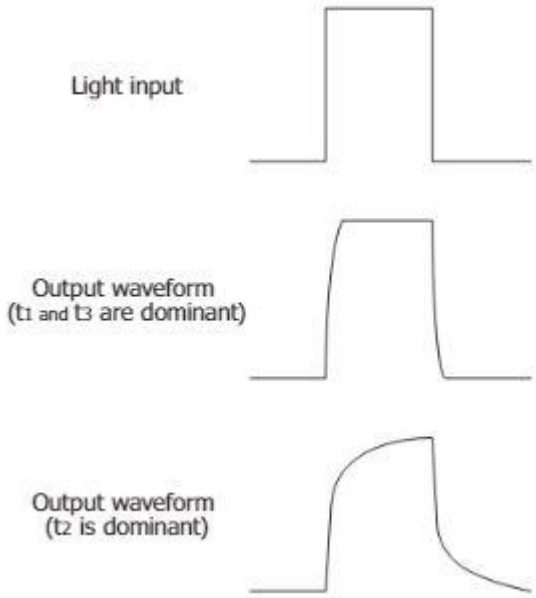

Figure 2.12. *An example of the effect of time parameters on rise time* [43].

2.3.3. Noise types in photodiodes

Response time is an important factor to select or design a photodiode. Another important factor is noise. One of the important things for photodiode performance is the noise level of the photodiode. There are three main noises in photodiodes. They are Shot noise, Johnson noise and 1/f noise. Since 1/f noise or flicker noise is only dominant in low frequencies, it will not be mentioned. Shot noise is related to dark current and photodiode current. There are always fluctuations in these current types statistically. The dark current is unwanted currents that exist even there is no light. The shot noise amplitude is represented in Equation 2.14 [29].

$$I_{sn} = \sqrt{2q(I_P + I_D)\Delta f} \tag{2.14}$$

Isn in the Equation 2.14 is magnitude of Shot noise. Ip is generated photocurrent. The id is dark current. Δf is the bandwidth of the measurement system. Electron charge which is 1.6x10-19C is expressed by q. As it is seen Shot noise is proportional to dark current and photocurrent. So, the most effective type of noise in photoconductive mode is Shot noise [29]. Photodiodes are more linear in the photoconductive mode than the photovoltaic mode of operation and they produce much current in photoconductive mode [44]. Therefore, photodiodes in LiDAR are used in photoconductive mode. In photoconductive mode, photodiodes are reversed biased. As can be seen in the equation,

shot noise does not depend on input light frequency but measurement system bandwith.

Johnson noise is related to resistance. In photodiode, the source of Johnson noise is shunt resistance [45]. Carriers can be generated by thermal energy in photodiodes in a low amount compared to generated by light. Thermally generated carriers in shunt resistance of photodiodes are the source of Johnson noise [29]. They are also important in feedback resistance of opamps used in LiDAR. Shunt resistance can be seen in the electrical characteristic of photodiodes in Figure 2.9. The magnitude of Jhonson noise is represented by Equation 2.15. k_B is the Boltzmann Constant which has a constant value of 1.38 x 10-23 J/K. T is the temperature in unit of Kelvin. T in equation shows the Jhonson noise depends on temperature. R_{SH} is shunt resistance of photodiodes which has high values such as greater than 1 GΩ. Δf is the bandwidth of noise measurement. The total noise is represented by Equation 2.16 and noise types distribution in the frequency domain is shown in Figure 2.13. Since flicker noise is not powerful in the frequencies above 100 Hz, the flicker noise is not added to Equation 2.16 [46]. In Equation 2.16, Itn is total noise. Isn is Shot noise and Ijn is Jhonson noise. In Figure 2.13, the x-axis is frequency while the y-axis is the magnitude of the noises. It is difficult to determine, and it needs good measurement devices after purchasing a photodiode. Therefore, a general term called noise equivalent power (NEP) will be mentioned.

$$I_{jn} = \sqrt{\frac{4k_B T \Delta f}{R_{SH}}} \tag{2.15}$$

$$I_{tn} = \sqrt{I_{sn}^2 + I_{jn}^2} \tag{2.16}$$

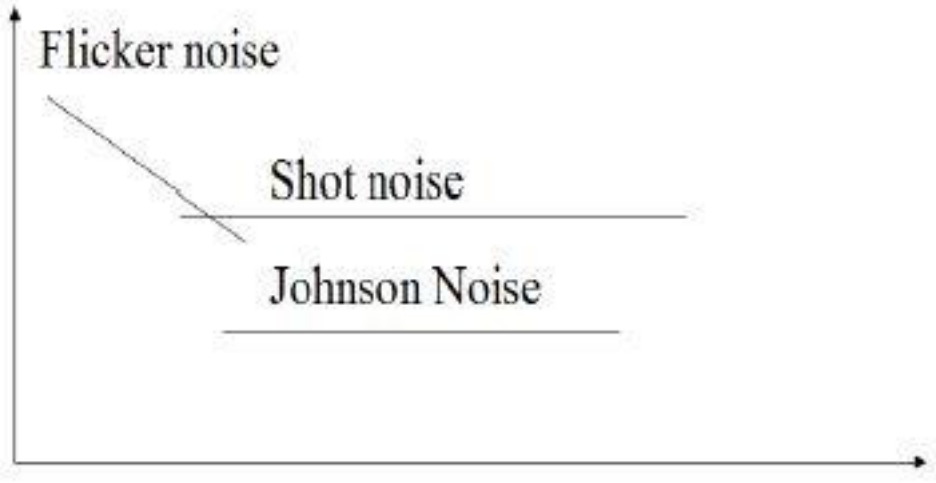

Figure 2.13. *Distribution of photodiode noise in the frequency domain* [46].

The noise equivalent power is the amount of power of incoming light that hits the photodiode to produce a current equals to noise current [30]. It determines minimum detectable incident light power via photodiodes. Some manufacturers give NEP information. For instance, NEP is given as 0.009 pW/Hz½ in the datasheet of the selected pin diode OSRAM SFH2701 at 5 V reverse bias and 650 nm wavelength [41]. The NEP is represented by the Equation 2.17 where NEP is noise equivalent power, Itn is total noise current of the photodiode which is shown by Equation 2.16 and R_λ is the responsivity of the photodiode [30]. To be able to interpret Equation 2.17 responsivity will be mentioned on the next page. NEP values can be between 10-11 W/√Hz and 10-15 W /√Hz . Since large area photodiodes produce much noise current their NEP is low compared to small area photodiodes. The area is the diffused area which can be seen in Figure 2.7.

$$NEP = \frac{I_{tn}}{R_\lambda} \tag{2.17}$$

2.3.4. Responsivity and quantum efficiency of photodiodes

The responsivity of photodiodes is important. It is an optical characteristic. Responsivity determines how much current will be produced according to the power of incident light [47]. Therefore, it is the capability of a photodiode which shows how well the photodiode converts light energy into electrical energy. The responsivity is

represented by Equation 2.18 where R_λ is the responsivity of the photodiode, Ip is the produced current, and P is the power of light which hits the photodiode. Although reverse bias and temperature are not involved in this equation, they can be change the responsivity. Because reverse bias changes responsivity a little by changing the generated carrier collecting capability in the depletion region. Temperature changes the bandgap of semiconductor slightly. Since bandgap changes, cut-off wavelength changes and new photons with energy greater than bandgap can generate carriers. An example responsivity graph of different InGaAs photodiodes from an article can be seen in Figure 2.14 [48].

$$R_\lambda = \frac{I_P}{P} \tag{2.18}$$

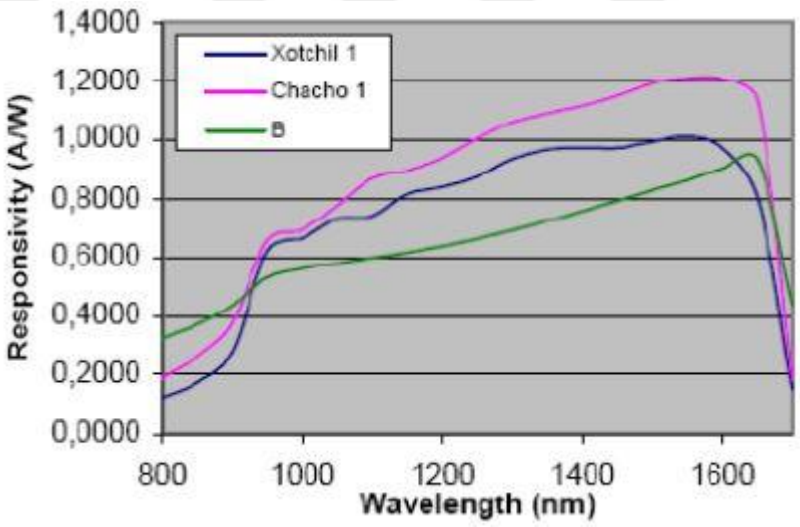

Figure 2.14. *Responsivity of different photodiodes* [48].

Quantum efficiency is another important optical characteristic of photodiodes. It is the fraction of the number of photons in the incident light to the number of photons that contribute to the photocurrent. It is a measurement again that shows how effective a photodiode uses the incident photons to convert them into electricity. The Quantum efficiency equation is related to responsivity and it is represented by Equation 2.19. λ is wavelength while R_λ is responsivity.

$$\text{QE}=1240\frac{R_\lambda}{\lambda} \tag{2.19}$$

Before a photodiode is chosen for LiDAR, responsivity, and quantum efficiency graphics of photodiodes in their datasheets must be analyzed. To be able to take the maximum signal from the incident laser light, a photodiode should be chosen such that the wavelength which corresponds to peak responsivity should be very close to the laser wavelength. For instance, the peak responsivity wavelength of the selected Marktech MTAPD-07-015 avalanche photodiode for LiDAR is 905 nm which is the same with selected OSRAM SPL PL90_3 laser diode as can be seen in Figure 2.15. Since the wavelengths are matched, the maximum measurable range is greater.

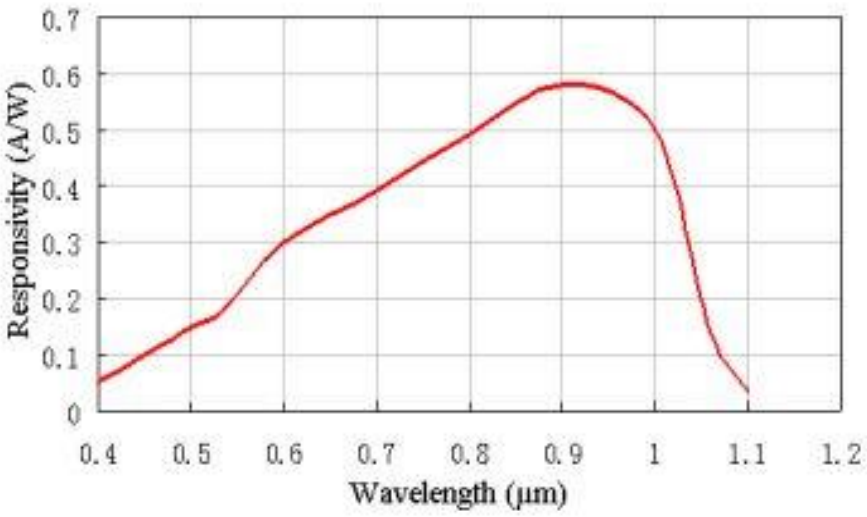

Figure 2.15. *Responsivity graph of selected avalanche photodiode* [49].

2.3.5. Pin and avalanche photodiodes

Two types of photodiodes are used in LiDAR applications widely. One of them is pin photodiode and the other one is avalanche photodiode. The main structure of a pin photodiode and electric field distribution can be seen in Figure 2.16. The difference of the main structure of pin photodiode from p-n photodiode is that there is a wide intrinsic region between p and n regions [50]. The resistivity of the intrinsic region is more than p and n regions since the number of free charge carriers is less. Therefore, most of the applied reverse bias is on the intrinsic region. The structures of pin photodiodes are designed so that most of the carriers are generated by incident photons in the depletion

region, junction capacitance be very low and carrier transit time of carriers in the depletion region is short. Thus, generated carriers by incident photons are drifted easily and fast. Hence, pin photodiodes are very fast and used in high-speed fiber-optic communication systems and time-critical applications such as LiDAR applications. There is no internal gain in pin photodiodes. One photon generates one electron-hole pair and generated carriers are swept towards contacts. But in avalanche photodiodes, there is an internal gain [51]. The responsivity of avalanche photodiodes is much greater than pin photodiodes. The selected avalanche photodiode's responsivity is 50 A/W with 1μW incident light power and multiplication factor of 100. The main structure of an avalanche photodiode is shown in Figure 2.17.

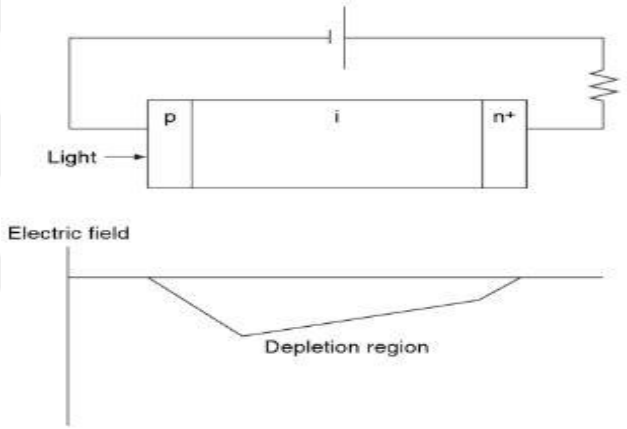

Figure 2.16. *The main structıre of pin photodiode* [52].

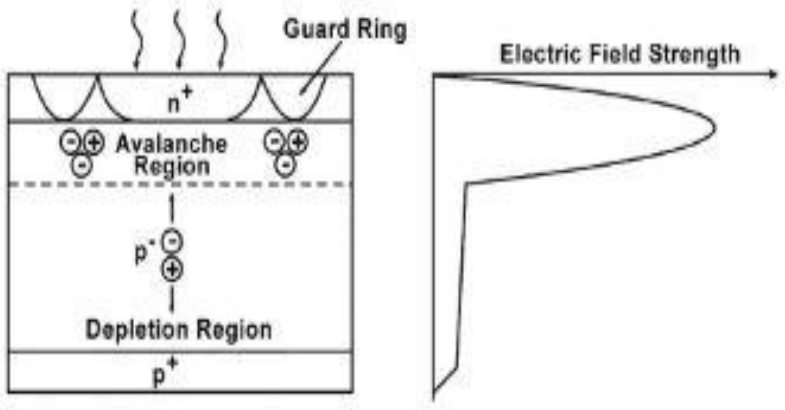

Figure 2.17. *The main structıre of an avalanche photodiode* [53].

The photocurrent generation mechanism of avalanche photodiodes is similar to conventional p-n photodiodes. There is a wide intrinsic region in which most carriers are generated in this region. The upper region is highly doped n region. The region below that region is a p-type region. Most of the applied reverse bias is seen on these layers. Therefore, electric field strength is larger in these areas as seen in Figure 2.17. The generated electron-hole pairs in the intrinsic region which is shown by negative p in Figure 2.17 are swept towards contacts. The electrons are drifted towards n+ while holes are drifted toward p+ region. When the strength of the electric field is increased, the drift speed increases. If carrier drift speed reaches a value, carriers begin to crate electron-hole pairs when they collide the atoms in the crystal lattice. If electric field strength is increased more, new carriers generated from collisions create new electron-hole pairs by colliding the lattice again. Collisions occuring in the avalanche region shown in Figure 2.17. This multiplication process of carriers is called impact ionization. So a small signal is amplified internally by avalanche photodiode. Therefore, using avalanche photodiode increases the maximum measurable range. But optical filters should be designed for avalanche photodiodes to prevent avalanche photodiodes increase unwanted signals and make false alarms. Si avalanche photodiodes require reverse bias from 100-200 V. Thus, they require external dc-dc boost converter circuit for reverse bias. Noises can be much compared to pin photodiodes. One photon can create 100 electrons totally with multiplication in selected avalanche photodiodes.

2.4. Analog Timer Design

Timers are used in LiDAR to measure the time of flight of the light. An FPGA time to digital converter is designed in Chapter 5 for the time of flight measurement. Capacitors can be used to measure time. Time to voltage converters use capacitors to express the time of flight in terms of voltage. Let consider a water source. It flows 10 liters of water per minute. We do not know how many minutes the water supply remains open. We opened the tap and when we arrived, we saw that 110 liters of water was filled. We can say that the water supply remains open for 11 minutes because we know that it flows 10 liters open per minute. We can think of capacitors as a water tank that stores the water of water supply and constant current sources as a water source. The voltage of the capacitors rises equally with the constant current source per unit time. It can be shown by Equation

2.20 where I is the amplitude of direct current and C is the capacitance value of the capacitor. A circuit for time measurement with a capacitor is designed and simulated by the LTspice simulation program. It is a very cheap circuit such that it costs approximately 2-3 $. The designed circuit is shown in Figure 2.18.

$$Volts/Seconds = I/C \tag{2.20}$$

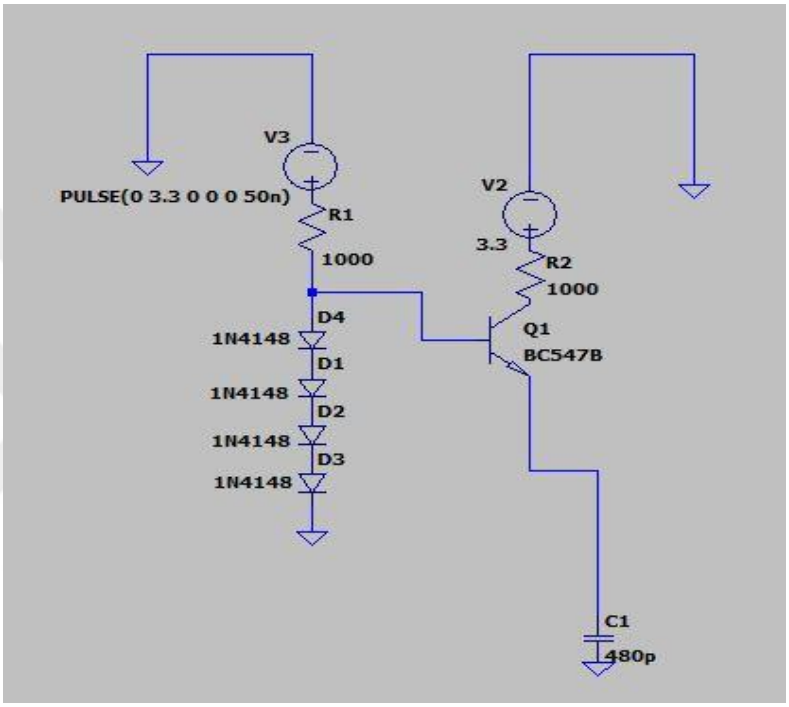

Figure 2.18. *A timer circuit with a capacitor for the time of flight measurement*

The voltage source V3 in Figure 2.18 gives a pulsed voltage. The pulse width represents the time of flight time. In this case, it is given as 50 ns. The circuit behind which creates pulse is generally trans-impedance amplifiers and comparator circuits. Therefore, they are not mentioned here. An npn transistor is used to switch the capacitor charging current. Diodes are used to make a constant voltage between the gate and emitter legs of the BC547B npn transistor. The simulation result of the designed circuit in Figure 2.18 is shown in Figure 2.19.

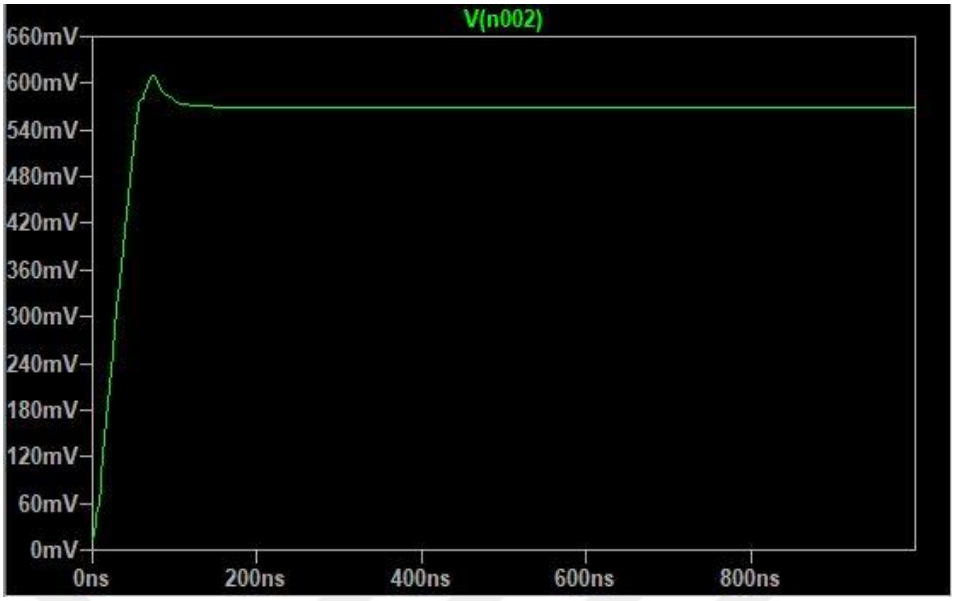

Figure 2.19. *The simulation results of the designed circuit in Figure 2.18.*

To be able to test the designed circuit pulse width of the V3 voltage source is increased from 30 ns to 60 ns by 2 ns steps. The test simulation result is shown in Figure 2.20 and Figure 2.21. The experiment is a linearity test of the time measurement circuit indeed. The capacitor voltage increases approximately 19 mV for every 2ns time interval increment as can be seen in Figure 2.20. In Figure 2.21 a line chart is shown. The X-axis of the line chart is pulse width which corresponds to the time of flight in ns and y-axis of the line chart corresponds to the capacitor voltage in mV.

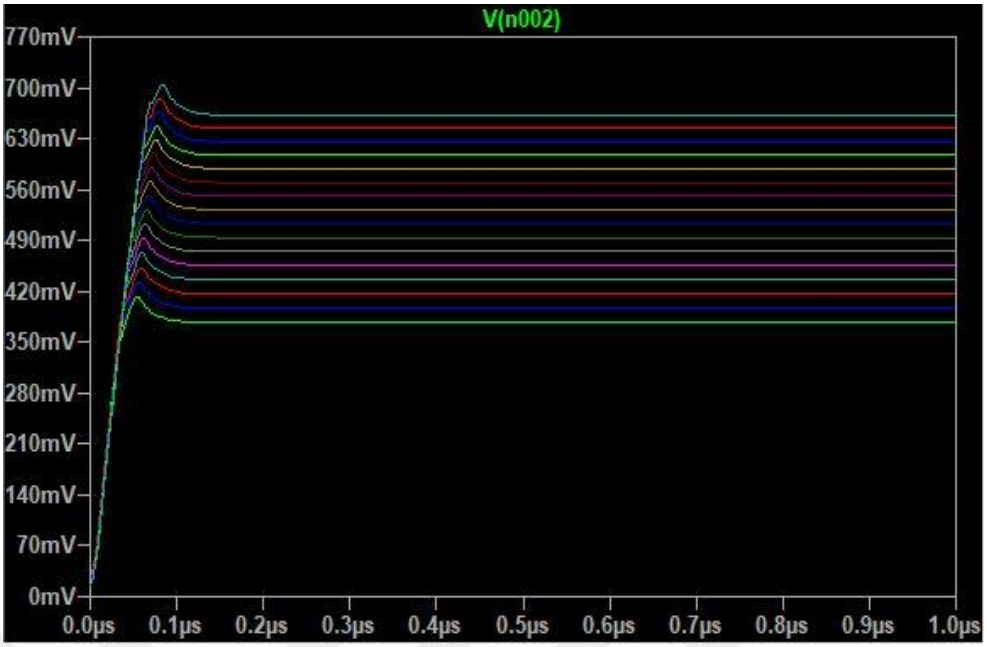

Figure 2.20. *A linearity test by increasing pulse width from 30 ns to 60 ns by 2ns intervals*

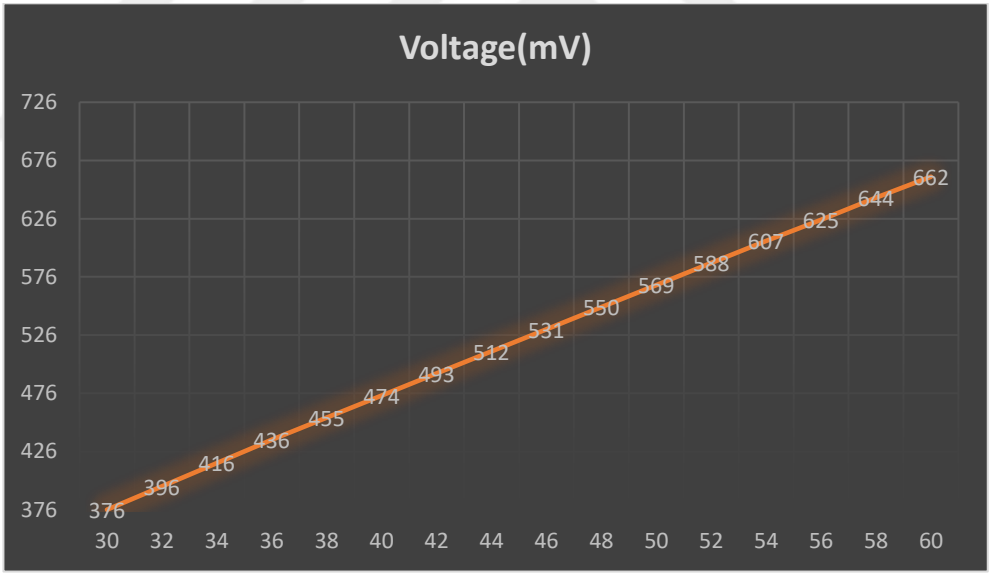

Figure 2.21. *A line chart which shows the linearity of time measurement in Figure 2.20*

The results of the experiment with 2 ns increment of time of flight show that the designed simple and cheap capacitor time measurement circuit behaves linearly as can be seen in Figure 2.21. But the detailed simulation test should be done to determine the time measurement resolution of the design circuit. Therefore, pulse width of the V3 voltage source in the designed circuit in Figure 2.18 is increased with 100 ps from 50 ns to 52 ns

to test whether the circuit can achieve 100 ps resolution or not. The simulation result of this test is shown in Figure 2.22. The detailed view of the graph in Figure 2.22 can be seen in Figure 2.23.

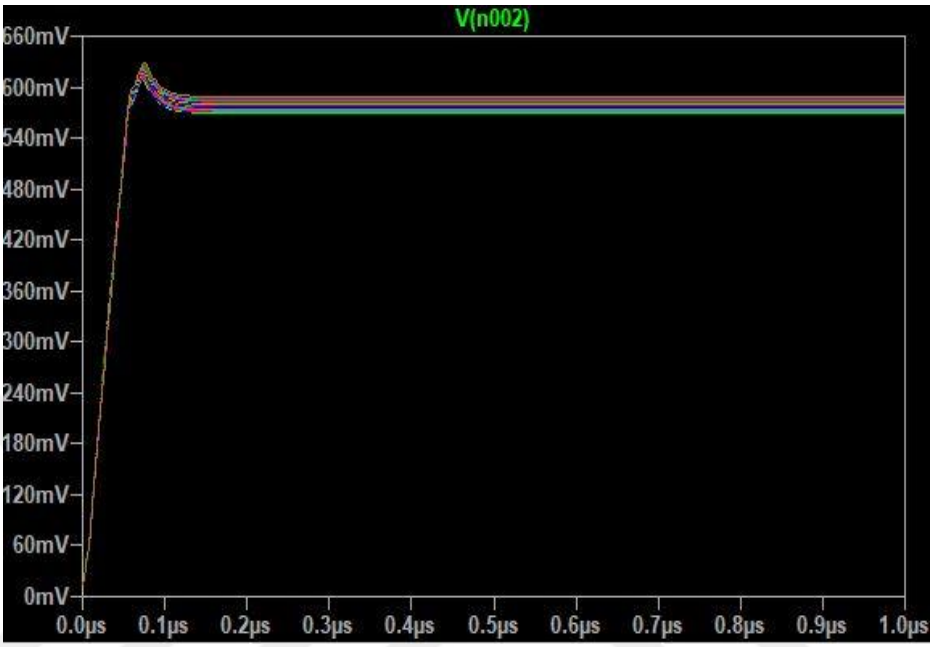

Figure 2.22. *The test experiment from 50 ns to 52 ns with 100 ps increment of time*

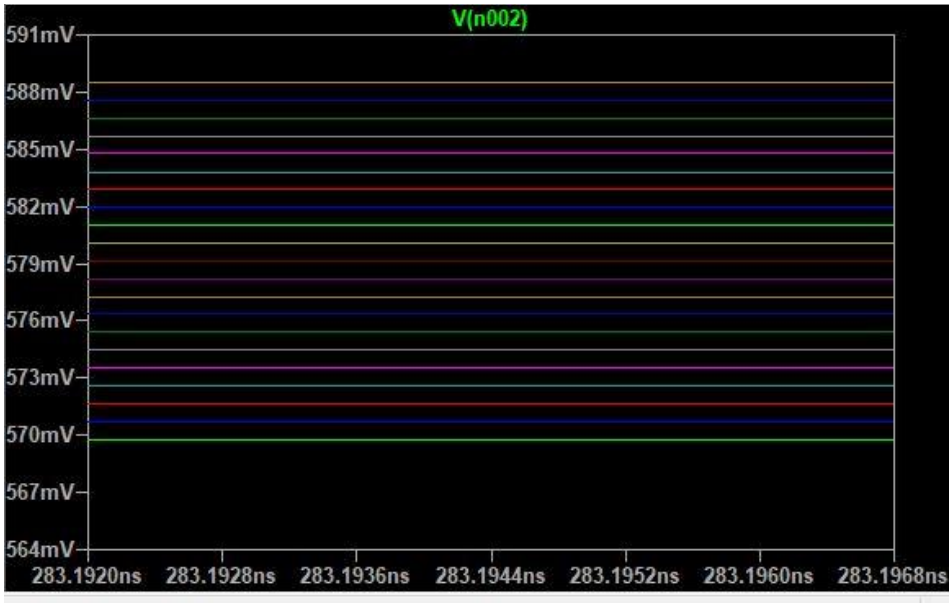

Figure 2.23. *The zoomed version of capacitor voltages in Figure 2.22*

Increments of time with 100 ps results in approximately 0.9 mV in capacitor voltage. It is an excellent value because 0,9 mV is a voltage that can be easily measured by conventional cheap analog to digital converters (ADCs). The line chart in Figure 2.24 shows that the designed time of flight measurement circuit based on the charging capacitor has 100 ps time resolution. It corresponds to 1,5 cm distance measurement resolution which is very good to implement a LiDAR system. This circuit with trans-impedance amplifier and comparators can be used in LiDAR applications if it is tested with real experiments and its linearity is proved by this experiment.

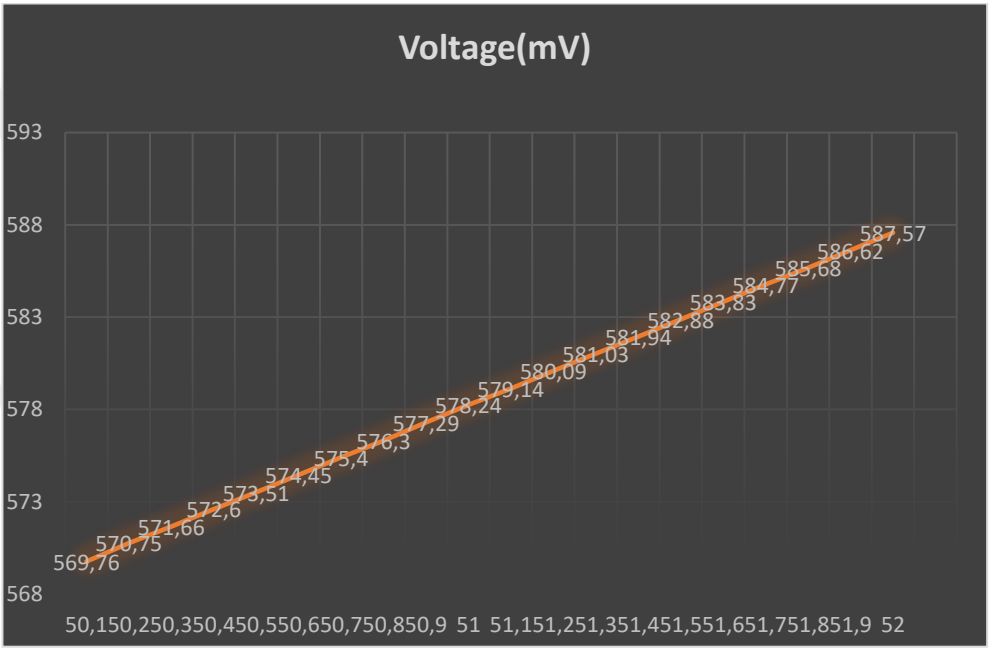

Figure 2.24. *A line chart which shows the linearity of time measurement in Figure 2.22*

One method of time measurement can be done by using the low-speed XOR logic gate. For instance, an 1155 Khz 5V square signal is generated by a signal generator and it is connected to successive XOR gates to achieve a time delay in Image 2.1. The achieved time delay is 333 ns. XOR logic gates are used to measure the differences in two logic signals. They can be used to measure phases of the transmitted and received signals to determine the distance if they are fast enough. XOR gates give the output a logic signal if they are fast enough. But XOR gate in the experiment does not capture the 333 ns phase delay as can be seen in Image 2.2 since it does not give a 5 V logic signal.

The peak output voltage of the XOR gate seen in Image 2.2 is 4.53 V. In Image 2.3, a XOR gate output is shown as a result of 170 ns phase difference of input signals. Since the XOR gate does not catch the 170 ns phase difference, the peak output voltage of the XOR gate is 1.68 V. If these output voltages of XOR gates according to different phase difference times are detected by a fast peak detector circuit and established an equation which shows the time delay according to the output voltage of XOR gates, then this method can be used to measure the time of flight of LiDAR. The idea of realizing the lidar for this thesis was based on the phase-shift method, not the time of flight measurement at the first stage. In the phase-shift method for this thesis, a square signal is applied to power led. The power led is focused via lenses on a photoresistor. A 5 V is applied to the photoresistor and a 1k resistor. When light falls on a photoresistor, the photoresistor does not produce a voltage or current. But its resistivity decreases. Since the applied voltage is constant, current on the 1k resistor increases. Therefore, the voltage on the 1k resistor increases. A low noise voltage amplifier system is used to amplify the voltage on that resistor. Since the photoresistor does not capture fast signals, a 75 Khz signal was used. But the frequency should be high to detect the phase shift. The phase-shift method to measure distance can be seen in Equation 2.21 where c is the speed of light, d is the distance of the object, $\Delta\phi$ is the phase difference of transmitted signal and received signal, f_0 is the frequency of the transmitted signal and n is the ambient refraction index. A phase shift occurs between the transmitted and received signals. Because it takes time for the transmitted signal to come back to the main circuit. These experiments were carried out since it was not known that the XOR gate, which was owned in the first experiments, was running slowly. Afterward, the necessity of making time to digital converter circuit emerged with the experiences gained from these experiments.

$$d = \frac{c}{n}\frac{\Delta\phi}{4\pi f_0} \tag{2.21}$$

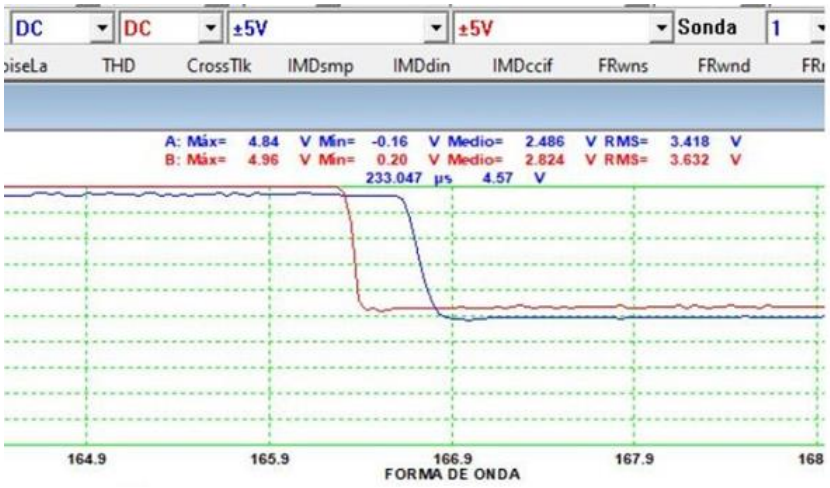

Image 2.1. *Two input signals of the XOR gate with a time delay of 333 ns*

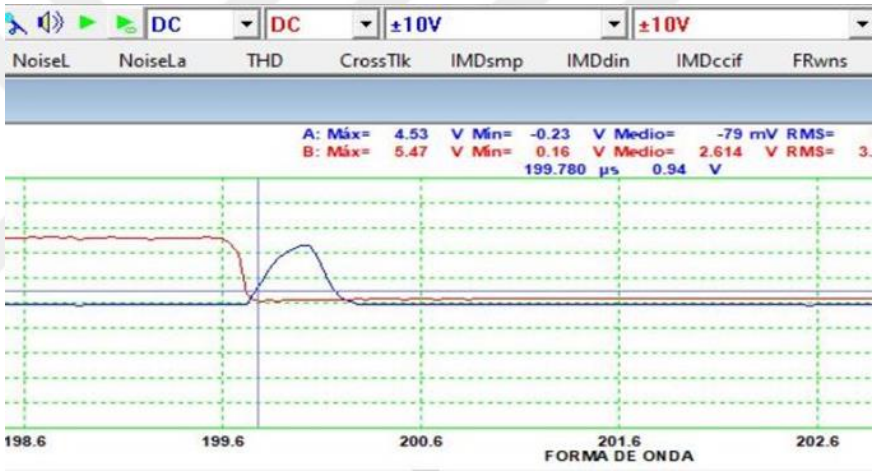

Image 2.2. *The output of the XOR gate for inputs with a time delay of 333 ns*

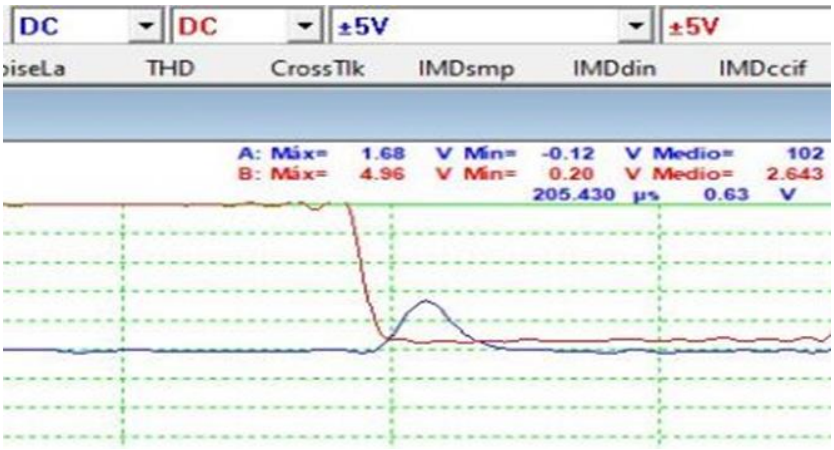

Image 2.3. *The output of the XOR gate for inputs with a time delay of 170 ns*

3. TRANS-IMPEDANCE AMPLIFIER

3.1. Calculation of Photocurrent

To be able to determine the produced current which goes to trans-impedance amplifiers, the amount of energy which infrared detector receives should be known. The well-known RADAR equation which is Equation 3.1 can be applied to LiDAR [54].

$$Pr = Gt \times Gr \times Pt \times \frac{\pi r^2}{\pi d^2} \tag{3.1}$$

In Equation 3.1 Pr is the received power by an infrared photodetector. Gt is the efficiency of the transmitter element. Gr is the efficiency of the receiver element. πr^2 is the area of the lens which is in front of the photodetector. Distance from the target is shownby d. Equation 3.1 is true if it is assumed that the all transmitted power is reflected by the target without any loss. In addition to transmitter power, the effect of solar power must be accounted for to make the LiDAR work in outdoor addition to indoor. Because the sunlight is a noise for the photodiodes. Signal power caught from reflected laser signal must be greater than the sunlight power. For indoor conditions, light emitted from factory lights and other light resources causes a noise for infrared photodetectors of LiDAR systems. Because of this unwanted sunlight and indoor light sources, unwanted dc offset occurs after the trans-impedance amplifier and before the comparator. Comparator circuits in pulsed time of flight LiDAR systems compare the coming voltage from trans-impedance amplifiers to a determined voltage level to understand whether the transmitted signal is received or not. In Figure 3.1, TLV3201 opamp is used as a comparator and the voltage to compare is 43 mV. The dc offset changes according to light noise level such as in indoor and outdoor conditions. Thus, comparator voltage value changes according to that dc offset. For instance, the minimum voltage that comes to the comparator can be 50 millivolts in some environmental conditions. Therefore, the output of the comparator will always be high voltage. A bypass capacitor which is shown by the red arrow on the example circuit of Figure 3.1 is used to prevent dc offset signals to pass. To filter the unwanted signals from the environment, optical filters are used in front of the infrared detectors as a good solution. A 905 nm filtered MTAPD-07-015/016-905F avalanche photodiode is found suitable for this thesis. According to the Figure 3.2 from ASTMG173, the power density of the sunlight is 0.76337 W/m^2 at 905 nm [55]. If a 3.5 cm lens is used in front of

the photodiode, 134 µW solar energy will be focused on the photodiode [56]. But it does not reflect real-life conditions because the lidar optic is not directed to the sun.

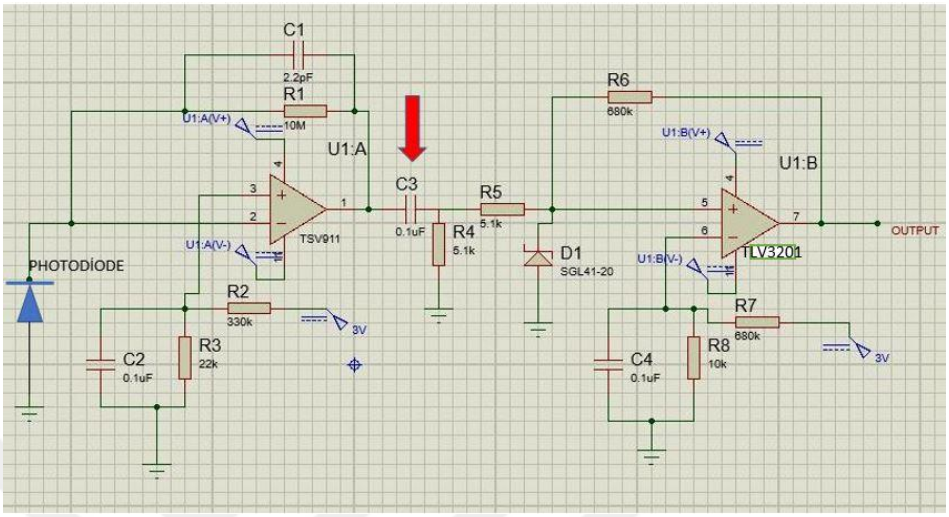

Figure 3.1. *Example circuit of a bypass capacitor before the comparator circuit.*

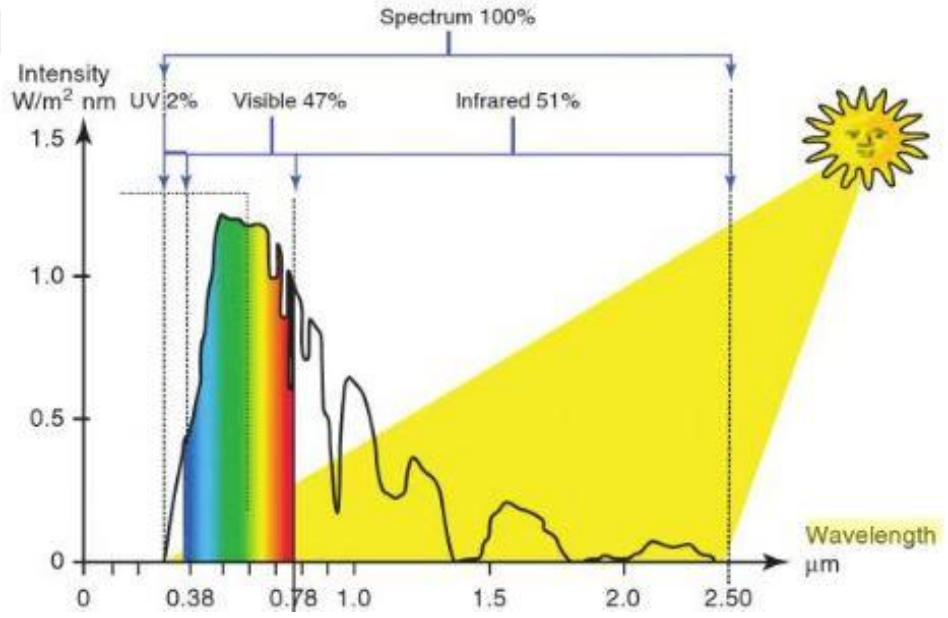

Figure 3.2. *Sunlight energy density according to wavelength* [55]

The first assumption to calculate the current of the photodetector based on Equation 3.1 is that the laser wavelength is completely matched to the photodiode wavelength and the efficiency of the laser is 1. If it is assumed that the laser optic is ideal and collimate

the laser beam perfectly, then all the photons reach the photodetector after reflected by the target. 2π solid angle is inside the field of view of the detector like in Figure 3.3. A short distance is before dashed line 1 is a blind area for the LiDAR. Because the red circle is not inside the blue circle. Thus, the reflected laser beam is outside the field of view of the photodiode.

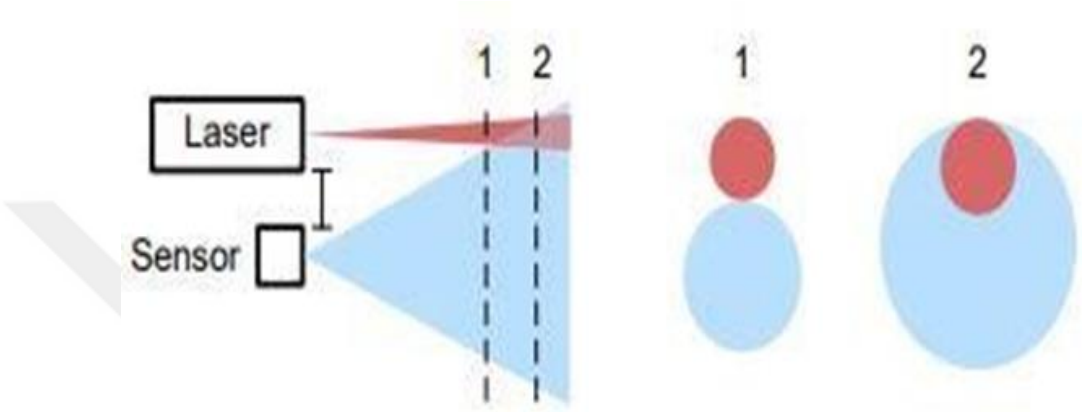

Figure 3.3. *Field of View of Photodiode to Sense All Laser Beam Efficiently* [56].

Assuming the responsivity of the detector is 0.5 A/W. It means if the detector sees the light which has the energy of 1 watt, it will generate 0.5 A current. Assuming also the transmitter laser energy is 70 W and the radius of the receiver lens is 3.5 cm. Power received by the pin photodiode and produced current will be like in Table 3.1. For 100 meters distance, the produced current is 0.4 μA. Assuming the dark current level will be 10 nA. 0.4 μA is a good signal to process. A trans-impedance amplifier with 100k gain will produce 25 mV. It is possible to get a 250 mV signal using a 1 MΩ feedback resistor or 2.5 V with a 10 MΩ feedback resistor. But the bigger gain means lower bandwidth. 25 mV signal is enough voltage level for a comparator to turn that into 3.3 V LVCMOS33 signal for the FPGA of the LiDAR. That 3.3 Volt signal will be the stop signal for the time to digital converter of the FPGA.

Table 3.1. *Received Power and Produced Current According To Distance* [56].

Distance(m)	Power Received	Current Produced
10	80 µW	40 µA
30	9 µW	4.5 µA
100	0.8 µW	0.4 µA

3.2. Trans-impedance Amplifier

Transimpedance amplifiers are used to get a useable voltage signal from a very small current. Ideal photodiodes produce current proportional to the light intensity which strikes it when they are reverse biased. It can be seen in Figure 3.4.

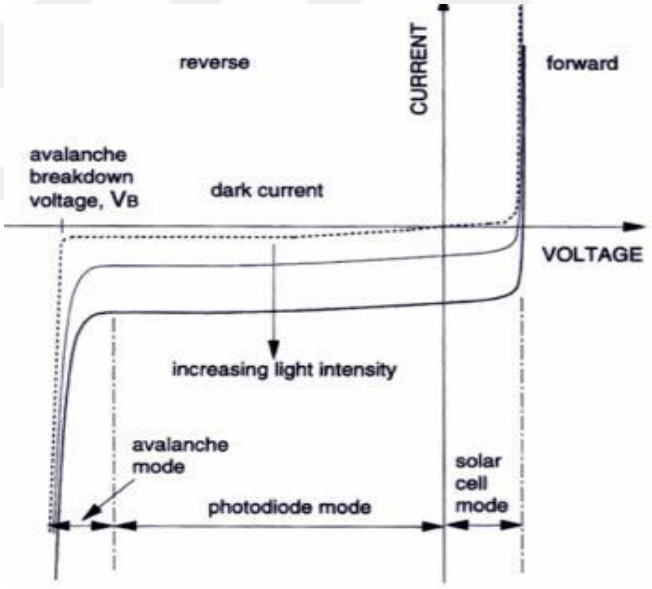

Figure 3.4. *An example of a photodiode reverse current according to light intensity* [57]

An example schematic of the trans-impedance amplifier is shown in Figure 3.5. The resistor of 20 kΩ is used as a feedback resistor. The feedback resistor of the trans-impedance amplifier is used for the multiplication of the current to get a useful voltage value. The photodiode is reversed biased. If it is assumed that 1 µA current comes from the photodetector, the output voltage will be 20 mV. Because the current will be multiplied by 20000.

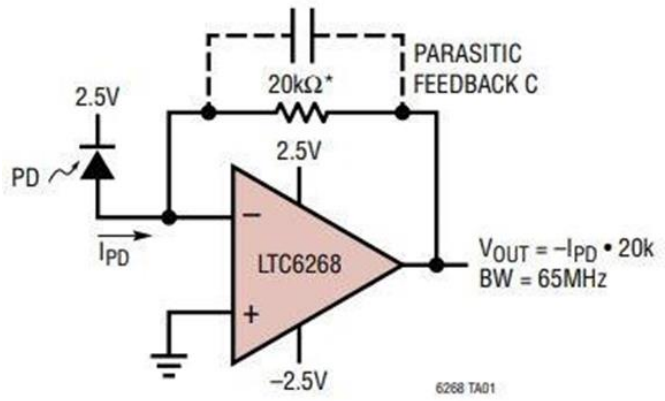

Figure 3.5. *An example schematic of the trans-impedance amplifier: LTC6268* [58].

The capacitor of the example trans-impedance amplifier seen in Figure 3.5 is used to make the opamp stable. That capacitor is called feedback capacitor. The feedback capacitor is very important and used to adjust the bandwidth of the trans-impedance amplifiers. TIAs bandwidth depends on the feedback resistance as well. The frequency response of the circuit of Figure 3.5 can be seen in Figure 3.6.

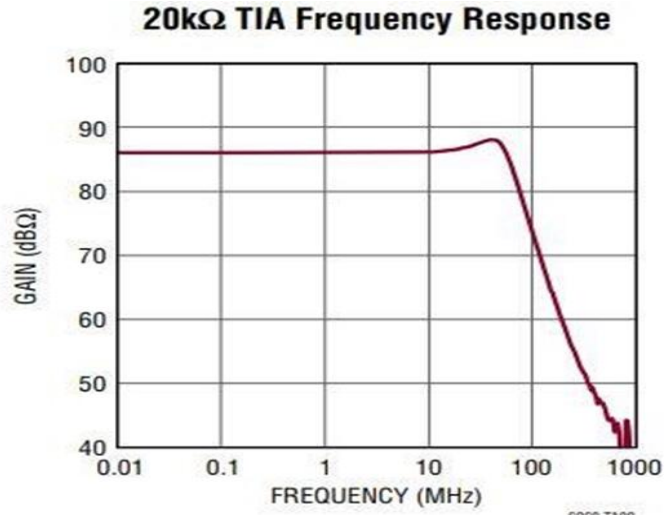

Figure 3.6. *The frequency response of the circuit in Figure 3.5* [58].

Every infrared detector has a dark current. Dark current is the unwanted current produced by thermal energy. Dark current exists even there is no light. Dark current

information can be learned from the datasheets of the photodetectors. For instance, the dark current of avalanche photodiode chosen for the LiDAR of this thesis is the maximum of 1 nA at the multiplication factor of 100 as can be seen in Table 3.2 [49].

Table 3.2. *Electrical and Optical Characteristics of the MTAPD-07-015-905F avalanche photodiode* [49].

Electrical And Optical Characteristics (Ta 23º)						
ITEMS	SYMBOL	CONDITIONS	MIN.	TYP	MAX.	UNIT
Spectral Response				400-1100		nm
Active Area	λ			Diameter 500		µm
Responsivity	Re	λ= 905nm φe=1µW M=100	50	55		A/W
Rise Time	t_R	f =1Mhz RL=50Ω λ = 905nm		0.6		ns
Dark Current	I_D	M=100	0.1	0.4	1	nA
Capacitance	C_j	M=100 f =1Mhz		12		pF
Optimal Gain	M			100		V
Breakdown Voltage	Vbr	IR=2µa	80	-	200	
Temperature Coefficent		Tc= -40ºC - 85ºC		0.9		V/ºC

Transimpedance amplifiers amplify the dark current too. The signal which comes from photodetector must be greater than the 1 nA to differentiate the signal from the noise. Dark current is important in the calculation of feedback resistor. If it is too high, TIAs can amplify to it millivolts. The design steps of the trans-impedance amplifier can be divided into 3 steps. Design goals should be defined first. An example design goal can be seen in Table 3.3.

Table 3.3. *An example design goal of a TIA.*

Input Minimum Current (Imin)	Input Maximum Current (Imax)	Output Minimum Voltage (Vmin)	Output Maximum Voltage (Vmax)	Bandwidth (BW)
0μA	30μA	0 V	3 V	10 khz

The first step to design a TIA is the selection of the feedback resistor which gives the gain of the trans-impedance amplifier. To calculate the feedback resistor, maximum and minimum desired output voltages should be determined. After that, maximum and minimum input currents should be determined. For instance, according to Table 3.3 the maximum input current is 30 μA while the minimum input current is 0 μA and the minimum desired voltage is 0 V while the maximum voltage is 3 V. The feedback resistor Rf can be calculated by the Equation 3.2.

$$Rf = \frac{Vmax - Vmin}{Imax - Imin} \tag{3.2}$$

According to Equation 3.2 feedback resistance for desired output voltages must be 100kΩ. Another important criterion is the circuit bandwidth. The frequency of the input signal must be in the bandwidth of the circuit. Feedback capacitors are used to make the TIAs stable and they are used to adjust the bandwidth of the TIAs. Proper calculation of the feedback capacitor Cf can be made by the Equation 3.3. According to the equation, Cf must be smaller than 159 pF. It could be chosen at 150 pF. Because 150 pF is a more commonly used capacitor.

$$Cf \leq \frac{1}{2 \times \pi \times Rf \times BW} \tag{3.3}$$

The feedback capacitor also forms a pole (Fp) in the graph of the frequency response of the TIA. After that pole, the gain of the TIA decreases. The position of that pole can be calculated by Equation 3.4 in terms of frequency.

$$Fp = \frac{1}{2 \times \pi \times Rf \times Cf} \tag{3.4}$$

The chosen TIA for LiDAR of this thesis is LTC6268-10. Gain bandwidth product of this junction field effect transistor (JFET) TIA is 4 GHz which is a verygood for for

LiDAR applications. It is proper for high-speed optical communication systems because of its wide bandwidth as well. The LTC6268-10 has a great slew rate of 1500 V/µs. Slew rate is defined as the change of output voltage value in a unit time. 1500 V/µs means that LTC6268-10 can supply a 1.5 V in a 1 ns short duration if both voltage value and the time is divided by 1000. It can be stated that it requires only 1 ns to give 1.5 V output voltage in addition to the propagation delay of the LTC6268-10. LTC6268-10 has extremely low input bias current which is ±3 fA at room temperature. It has very low common mode capacitance such that 0.45 pF and differential mode input capacitance such that 0.1 pF [58]. These capacitance values are important for high-speed photodiode amplification. The lower the input capacitance of the opamp, the higher the bandwidth if the feedback and parasitic capacitance values are constant.

Photodiode equivalent circuit information is vital for designing a proper TIA circuit. A circuit is designed to understand the transient, noise, and ac analysis. That circuit is shown in Figure 3.7.

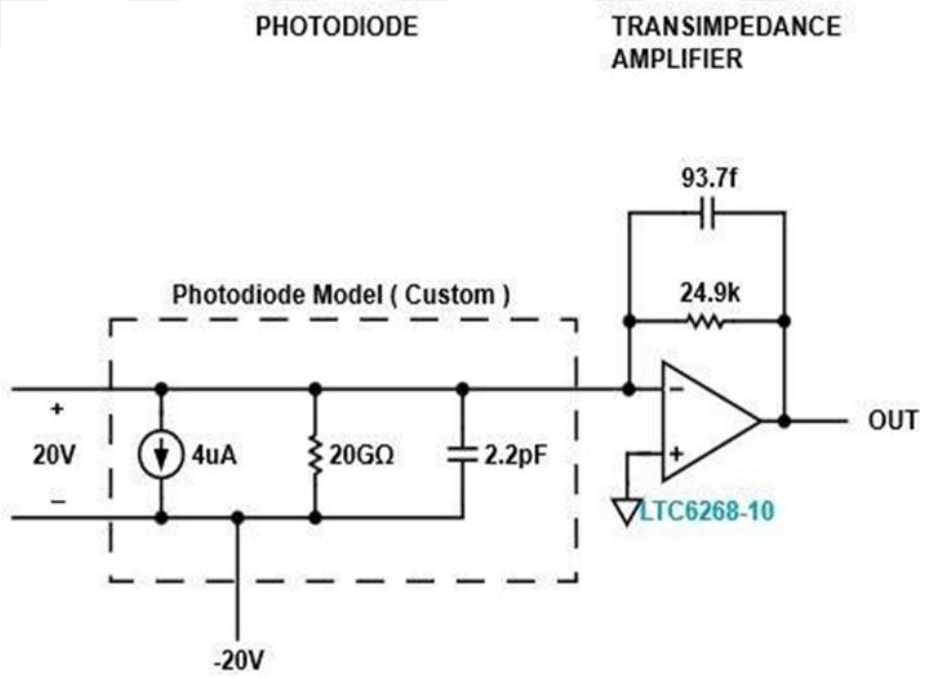

Figure 3.7. *The main schematic of targeted TIA for LiDAR*

The photodiode model is OSRAM SFH2400FA-Z pin photodiode. Rise and fall time of this photodiode is 5ns at 20 V reverse bias. The dark current is a 5 nA at 20 V reverse bias. The responsivity of this photodiode is 620 mA/W. According to the datasheet, the capacitance of the photodiode is 2.2 pF at 20 V reverse bias. If it is assumed that the maximum current produced by the photodiode is 4 μA, the photodiode model will be as shown in Figure 3.9. Changing photodiode capacitance produces high-frequency noises. 93.7 femtofarad feedback capacitor is used to balance the flickering capacitance of photodiode and make the TIA circuit stable. It is a very low capacitance value. Therefore, the board capacitance plays an important role. The actual feedback capacitance value should be determined empirically with different PCBs. The capacitance value of the feedback resistor which is called parasitic capacitance may be enough to supply the feedback capacitance value. It is hard to find a capacitor below 50 fF. When PCB parasitic capacitance is considered, feedback capacitance can be desired below 50fF. There is an example in Figure 3.8 in the datasheet of the LTC6268-10 which shows the importance of the PCB design technique for feedback capacitance [58].

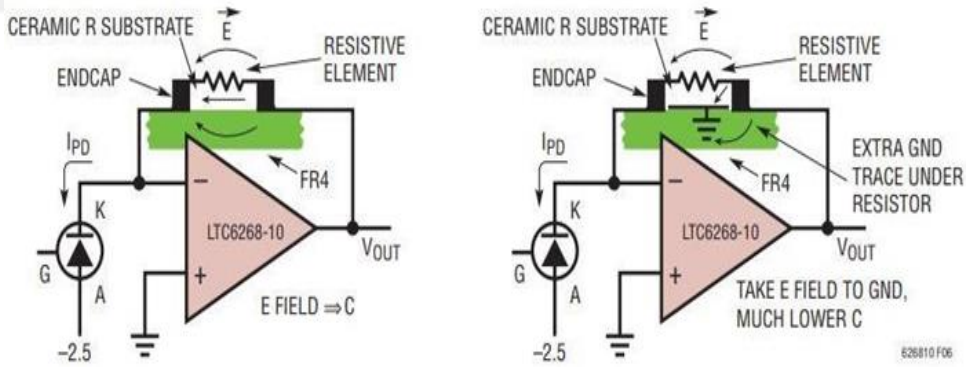

Figure 3.8. *A PCB design method to get the better parasitic capacitance* [58]

There is a normal layout of the feedback resistor at the left and field shunting layout of the feedback resistor at right in Figure 3.8. According to the datasheet of LTC6268-10 making a ground trace under the feedback resistor reduces feedback capacitance from 100 fF to 11.6 fF.

3.3. Simulation Results

3.3.1. Transient analysis

The circuit which is designed in the LTspice simulation program to simulate the result of the TIA is shown in Figure 3.9. The simulation results of the transient response of the designed TIA circuit of Figure 3.9 can be seen in Figure 3.10. LTspice circuit simulation program is used to get the simulation results. The signal with blue color shows the current pulse generated by the photodiode. The laser emits infrared light. The infrared laser light propagates through the air and hits an object. Then the laser light comes back to the photodiode and produces a current pulse. An example calculation of the produced current depending on the distance, lens diameter, laser optical power, and responsivity of the photodetector was shown in Section 3.1. The current pulse begins from 1 ns and reaches its maximum of 4 μA within 1 ns. It is used in the simulation to determine the rise time of the TIA. The rise time of TIA is a delay that must be calculated to achieve a correct TOF calculation. The time between the start signal and stop signal of time to digital converter of FPGA covers LiDAR circuit delay and photodiode rise time as well as the TOF. The LiDAR circuit delay consists of the propagation delay of the TIA circuit, the comparator circuit, delay of PCB traces, and cable delays. The red signal in Figure 3.10 shows the output voltage of the LTC6268-10 TIA. If 500 kΩ is used as the feedback resistor, a 1.95 V output will be attained. But the rise time of TIA will be much larger as shown in Figure 3.11.

The reason behind the selection of the 24.9k feedback resistor and attaining 100 mV output voltage is to decrease the propagation delay of the TIA and the low overdrive dispersion of the LTC6754 comparator which will be used in Chapter 4. According to the datasheet of LTC6754 overdrive dispersion is only 1 ns between 10 mV and 125 mV. The overdrive dispersion must be calculated to measure the time of flight accurately. A high-speed analog to digital converter can be used to measure the output voltage of the TIA. An equation should be established which shows overdrive dispersion according to the output voltage of the TIA. An accurate time delay of the comparator can be calculated from the equation established.

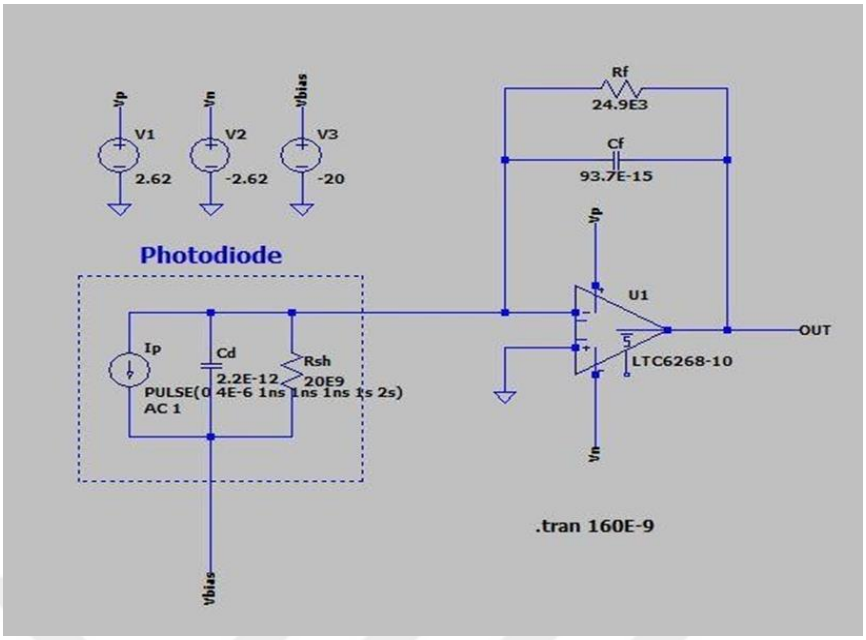

Figure 3.9. *The designed circuit in LTspice for the circuit in Figure 3.7*

The red line which shows the output of the TIA in Figure 3.10 starts increasing before the photodiode current settles its final value. It reaches 100 mV at approximately 6 ns time interval. The rise time of the output voltage is approximately 2.6 ns. The green line shows the current of the capacitor in the equivalent circuit of the photodiode used in the circuit of TIA. It begins to rise with the current signal of the photodiode.

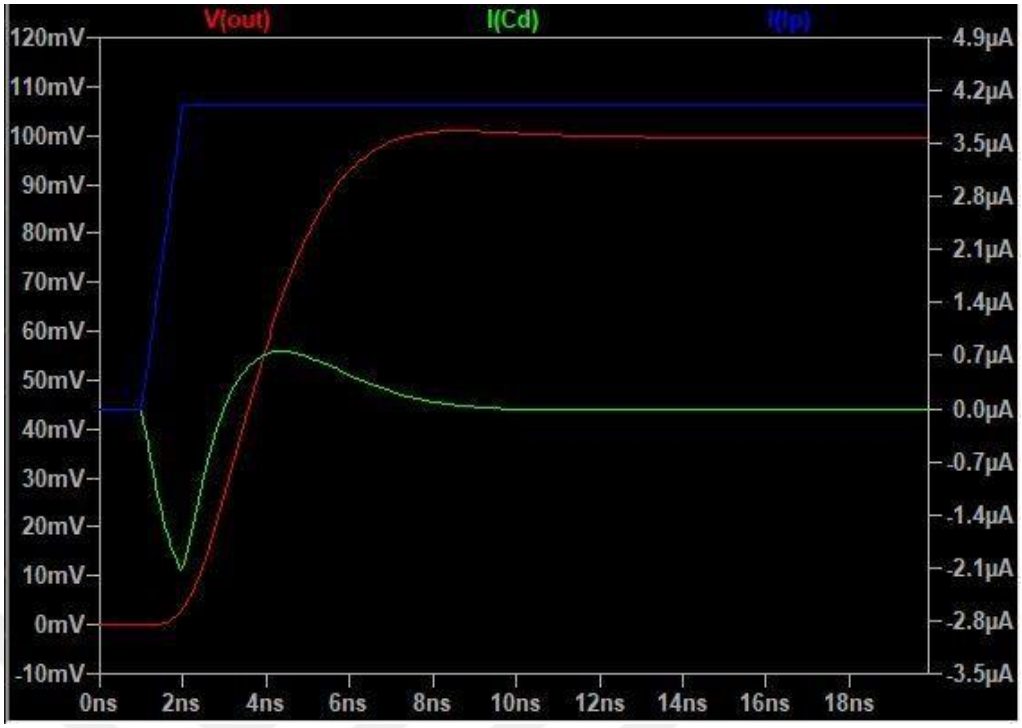

Figure 3.10. *Transient response simulation results of the designed circuit in Figure 3.7*

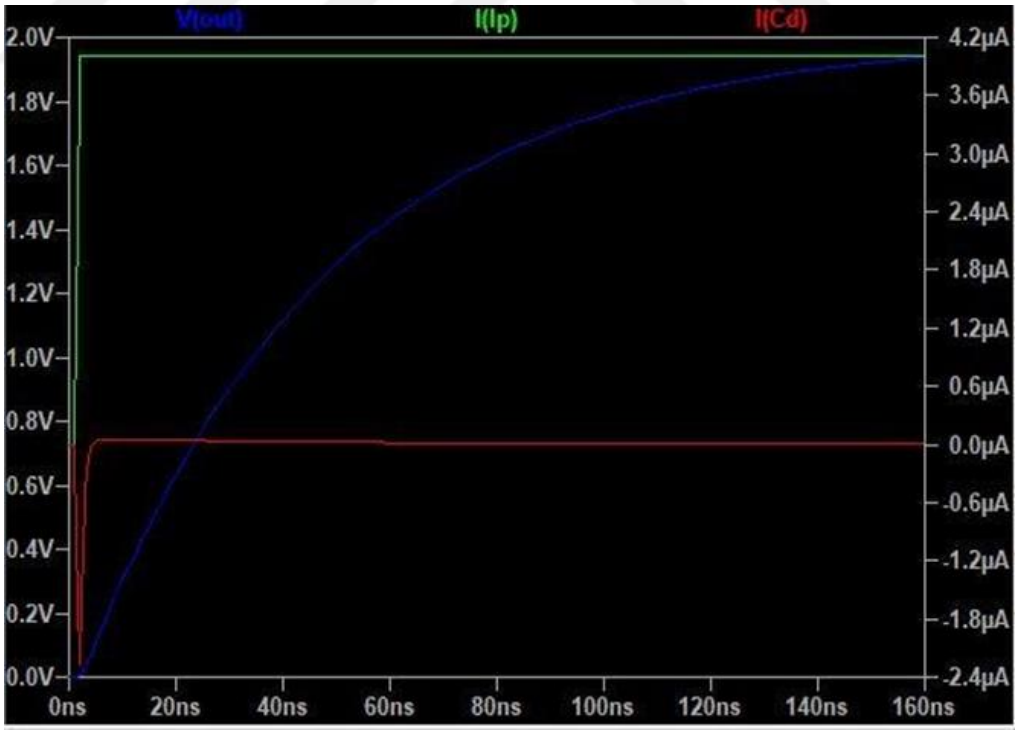

Figure 3.11. *Transient response simulation results of the circuit designed with 500k feedback resistor*

3.3.2. Spectral response

The spectral response of the designed TIA can be seen in Figure 3.12. Analog devices company provides a useful program to get simulation results of the frequency response of TIAs [59]. The designed TIA has a wide bandwidth. 24.9 k gain is constant until the 95.6 Mhz. After 95.6 Mhz the gain begins to decrease. A specific gain with respect to the frequency can be observed in Figure 3.12.

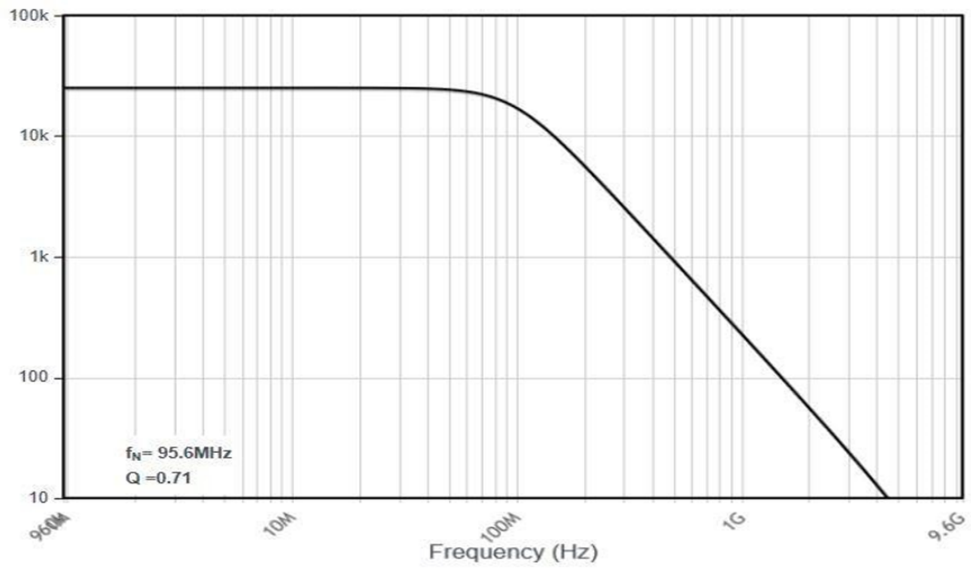

Figure 3.12. *Frequency response of the simulated TIA*

3.3.3. Spectral noise and signal to noise ratio

Noise spectral analysis is important. Because it helps determine the sources of noise in detail. The spectral noise graphic can be seen in Figure 3.13. The black dashed line shows the total noise of the system. The green line of noise belongs to the feedback resistor of TIA. The red line shows the noise contribution of LTC6268-10 opamp to current signals. The lilac color shows the noise coming from the input resistor of the opamp. Depending on the frequency main noise contributor changes. For instance, the main voltage noise contributor after 10 Mhz frequency is LTC6268-10 opamp itself. But the main voltage noise contributor before 10 Mhz frequency is the feedback resistor of TIA.

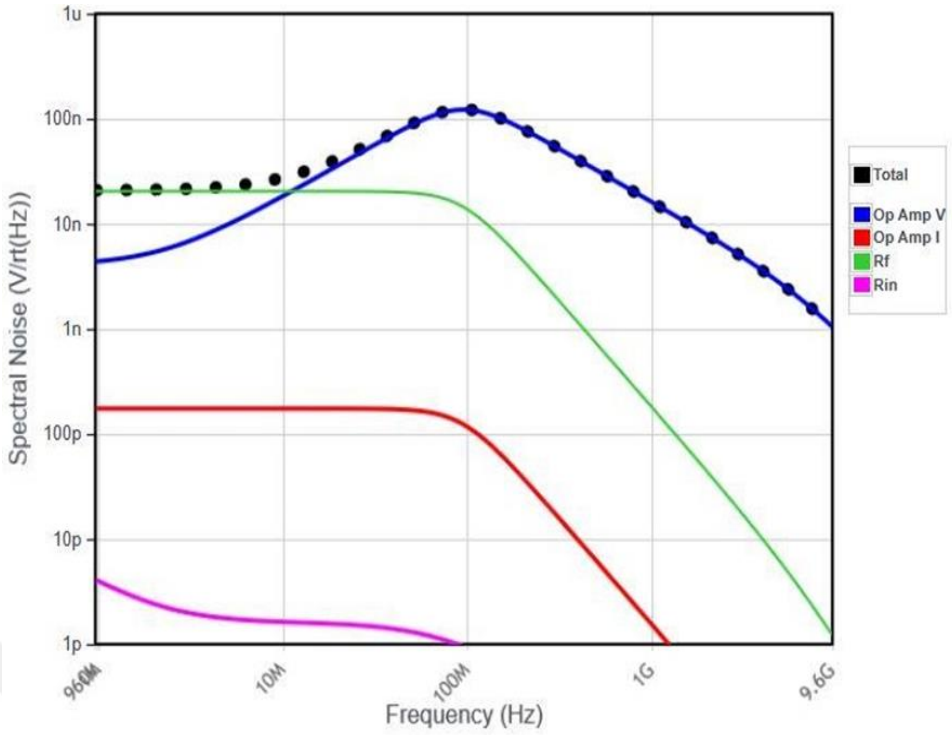

Figure 3.13. *Spectral noise of the simulated TIA*

The total noise information can be achieved by using the online simulation program [59]. Signal to noise ratio (SNR) can be seen by using that simulation program. Signal to noise ratio gives the information that how clear the signal can be read and what is the minimum meaningful voltage value to read. SNR compares the expected signal level to the total unwanted signal level which is called noise. SNR is generally in terms of decibel unit. Equation 3.5 is for SNR which is calculated using electrical signal and noise power and Equation 3.6 is for SNR that is calculated using signal and noise voltage.

$$SNR(db) = 10xlog\left(\frac{Signal\ Power}{Noise\ Power}\right) \tag{3.5}$$

$$SNR(db) = 20xlog(\frac{Signal\ Voltage}{Noise\ Voltage}) \tag{3.6}$$

Total noise value, SNR, and noise contributors can be seen in Figure 3.14. The noise floor is 1.75 mV RMS according to simulation results in Figure 3.14. The noise floor of 1.75 mV corresponds to 2.474 mV peak voltage by multiplying it with its square root of 2. If it is multiplied by 2 to find the peak to peak voltage, the result will be 4.948 mV. According to Equation 3.6, SNR can be found as 26.1 dB as in Figure 3.14.

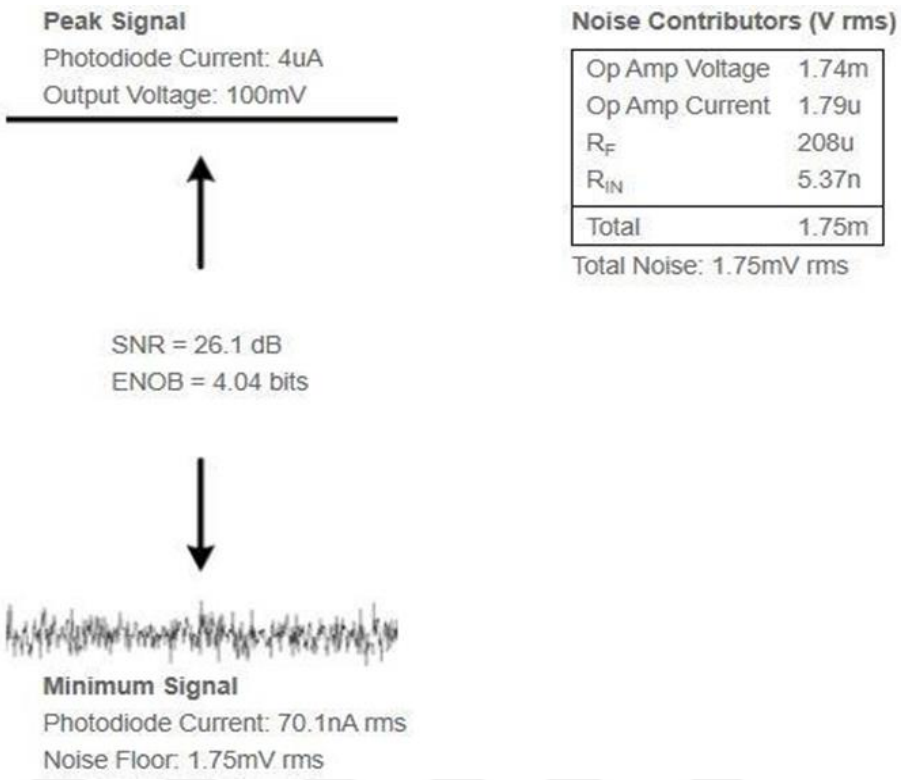

Figure 3.14. *SNR, Noise floor and Noise Contributors of the Simulated TIA*

In this chapter, A trans-impedance amplifier is designed and simulated as the first stage of the LiDAR receiver circuit. Simulation results showed that the chosen LTC6268-10 TIA opamp can be used in the LiDAR system. Because the simulation of the transient response of the opamp showed that it has a fast slew rate, low propagation delay, low rise time as much as 2.6 ns as mention in the datasheet indeed. The simulation of frequency response showed that it has a wide bandwidth. Fast opamps generally suffer from low SNR. But according to simulation results, the total noise level and SNR is acceptable for wideband applications. The next chapter will be the second stage of the LiDAR receiver circuit. A proper comparator opamp will be found and a circuit will be designed and simulated by the LTspice simulation program.

4. COMPARATOR CIRCUIT

Comparators are similar to operational amplifiers (op-amp). But comparators are used to compare two input voltages. One of them is inverting input and the other one is noninverting input. One of the input voltages is used as a threshold. If the other input voltage goes beyond the threshold voltage, the comparator output will be high voltage stage. If the input voltage which will be compared to threshold voltage is less than the threshold voltage, the output of the comparator circuit will be in low voltage stage. The offset voltage is important as well. The offset voltage is the voltage that the input voltage must pass addition to the threshold voltage to make the output of the comparator logic one. The comparators are basic elements of analog to digital converter (ADC). Example usage of comparators in an ADC can be seen in Figure 4.1. In the figure, there is a 3-bit ADC. Reference voltage Vref is divided into 8 voltages. Each comparator of the ADC compares the reference voltage of itself. If the input voltage is greater than the reference voltage of the comparators, the output of the comparators will be one otherwise zero. There are exclusive or gates (XOR) as the second stage of the ADC in the priority encoder end latch part. The binary output of ADC is determined by XORs, latches, and the output of the comparators.

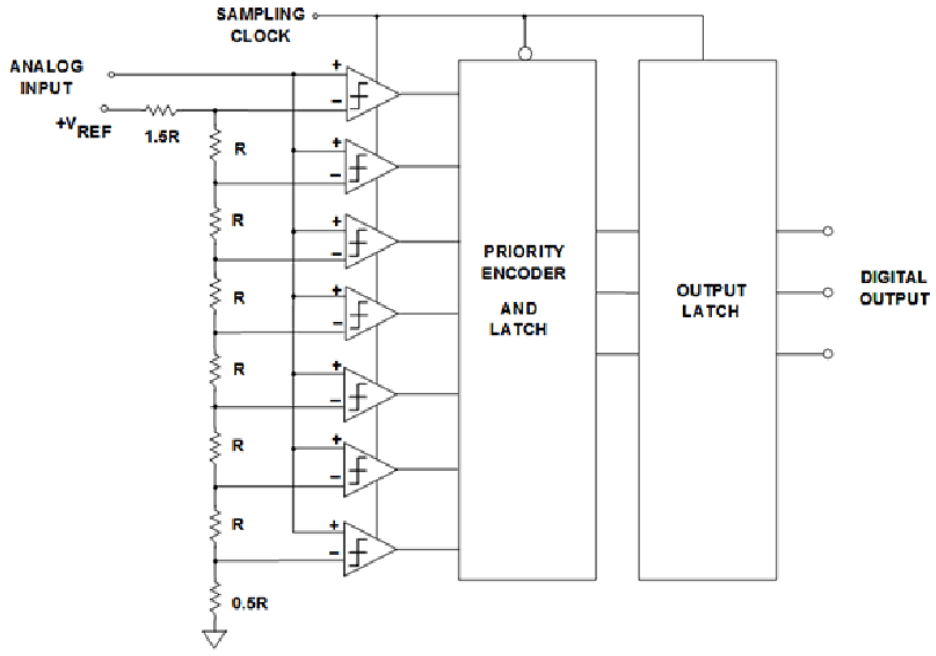

Figure 4.1. *Example usage of comparators in a 3-bit ADC* [60]

4.1. Comparator Circuit Design

Comparator opamp circuit is used after the trans-impedance amplifier circuit in LiDAR. TIA circuit amplifies the current of the photodetector as mentioned in Chapter 3 to supply a voltage which comparator can handle. Low feedback resistance which is 24.9k is used to get a fast response time in the TIA circuit. Thus, the gain of 24900 is attained. It is estimated that there will be a maximum of 200mV at the output of the TIA circuit. That voltage level is not enough to trigger the FPGA TDC to make the input logic one. Therefore, the FPGA does not understand whether it has received the stop signal or not. The comparator circuit of the LiDAR determines whether the laser signal is received or not to stop the time measurement of the FPGA TDC. The noninverting input of the comparator opamp is connected to the output of the TIA. A threshold voltage should be determined experimentally. A target with minimum reflectivity should be located at the maximum desired range. After the laser emits light, echo signals which come from the determined target should be observed by an oscilloscope. The oscilloscope should be connected to the output of the TIA circuit. The minimum observed signal minus offset voltage of the comparator opamp will be the threshold voltage of the comparator circuit. The comparator circuit output will logic one if a voltage which is greater than the threshold voltage comes.

The selected comparator opamp for LiDAR is LTC6754 from Linear Technology company. LTC6754 will be simulated to see whether it is suitable or not for LiDAR. LTC6754 is a high-speed rail to rail input. The output of LTC6754 is in the form of low voltage differential signaling (LVDS). Nexys A7 FPGA board will be used in this thesis. The LVDS output of the comparator is suitable for the FPGA. LVDS signals are proper for high-speed data transmission. An example of LVDS output from the datasheet of LTC6754 can be seen in Figure 4.2.

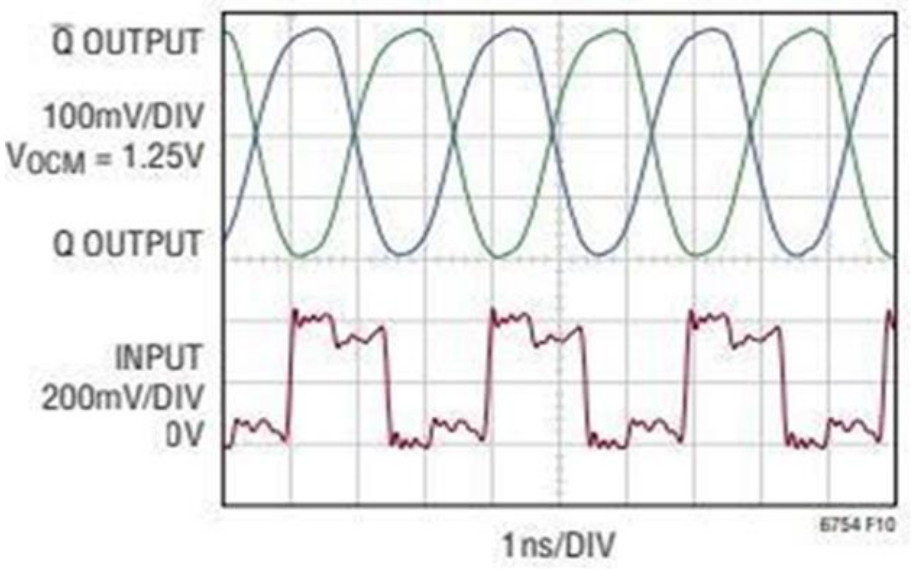

Figure 10. LVDS Output at 340MHz

Figure 4.2. *Example LVDS output of LTC6754* [61]

The selected comparator is suitable for timing-critical applications. Sensitive time calculation is vital for LiDAR. The propagation delay of the comparator circuit and overdrive dispersion must be subtracted to measure the actual time of flight of laser light. TLV3501 is an offered comparator for LiDAR application but input overdrive dispersion of TLV3501 is approximately 5ns from 5 mV to 100 mv as shown in Figure 4.4. Thus, it requires high-speed ADC to get the input overdrive voltage and calculate the overdrive dispersion. It increases the cost of LiDAR a lot. Because high-speed ADC chips are not cheap. 5 ns wrong time calculation brings about 75 cm of distance measurement deviation. The selected LTC6754 comparator's overdrive dispersion from 20 mV to 125 mV is only 1 ns. It is an important advantage for accurate time calculation for LiDAR. LTC6754 has a 1.8 ns propagation delay. The more propagation delay in the electronic circuit can cause more time deviation by a change in temperature or other environmental parameters. Input and output supply voltages should be separated. It makes isolation between input and output circuitry. The comparator has a high toggle rate which is 890 Mbps. Hysteresis voltage of comparators is important for noise immunity. Input voltages of comparators are not smooth like in the simulations. LTC6754 has a 4.5 mV internal hysteresis voltage. Additional hysteresis voltage can be adjusted by connecting a resistor between LE/HYST and VEE pins as shown in Figure 4.3. The changes in hysteresis voltage according to the

connected control resistor can be shown in Figure 4.3 as well. As control resistance increases hysteresis voltage decreases. Adjustable hysteresis gives the flexibility to operate the LiDAR in noisy environments.

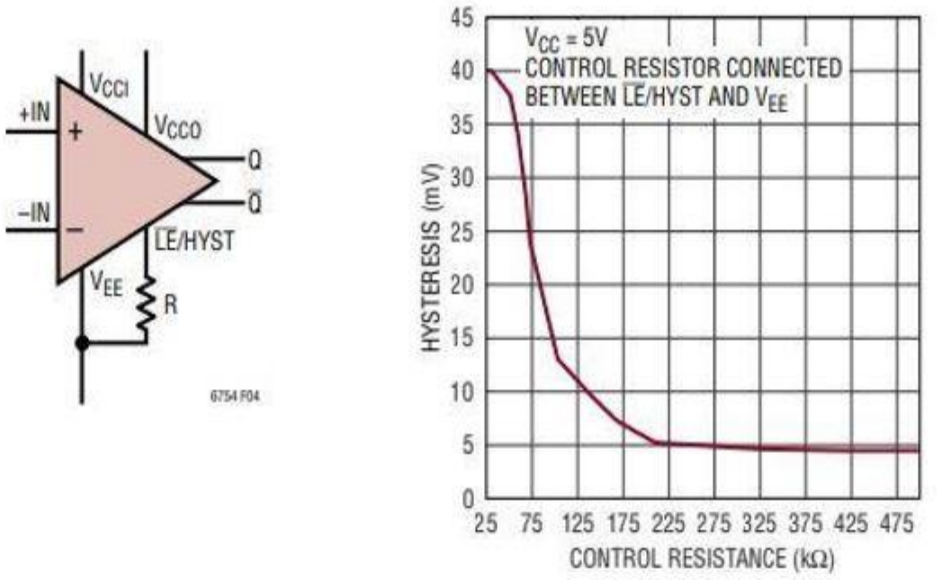

Figure 4.3. *External hysteresis addition by a control resistor* [61]

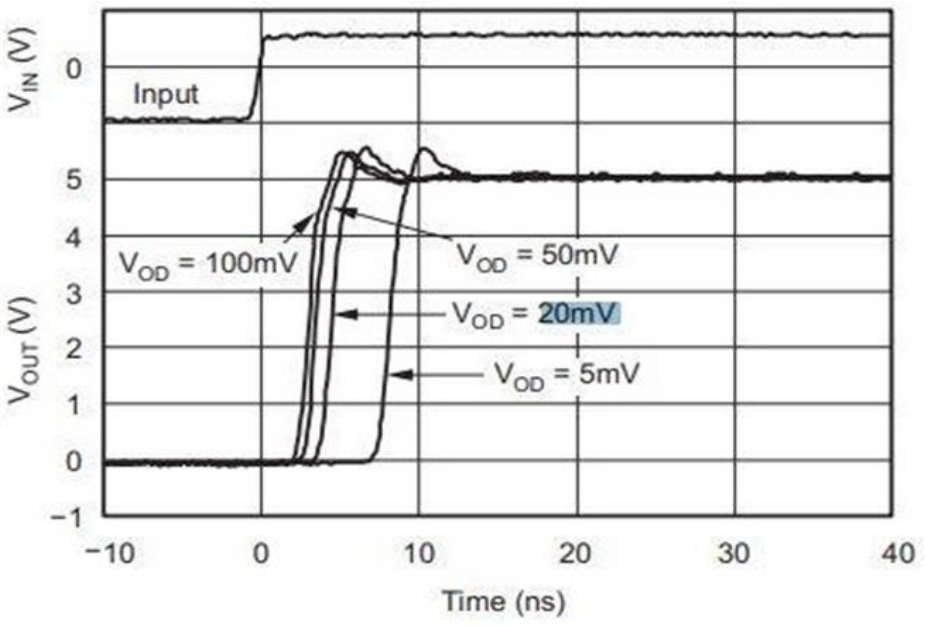

Figure 4.4. *Overdrive Dispersion of Comparator TLV3501* [62]

4.2. The Walk Error

There is an accuracy error for LIDARs called walk error. If it is assumed that there are two targets with different reflectivities at the same distance. Since their reflectivities are different the received energy and the produced current of the photodiode will be different although they are located at the same distance. Thus, time to amplify that current above the threshold of the comparator circuit will be changed. Therefore, the threshold voltage will be reached at different times. It can be observed in Figure 4.5. All three signals come from the targets which are positioned at the same distances. But the reflectivity constants are different. Therefore, echo signals have different energy and produce different currents. The threshold voltage value of the comparator must be constant. The signal with the highest energy arrives at the threshold voltage first. The signal with the lowest energy arrives at the threshold voltage last.

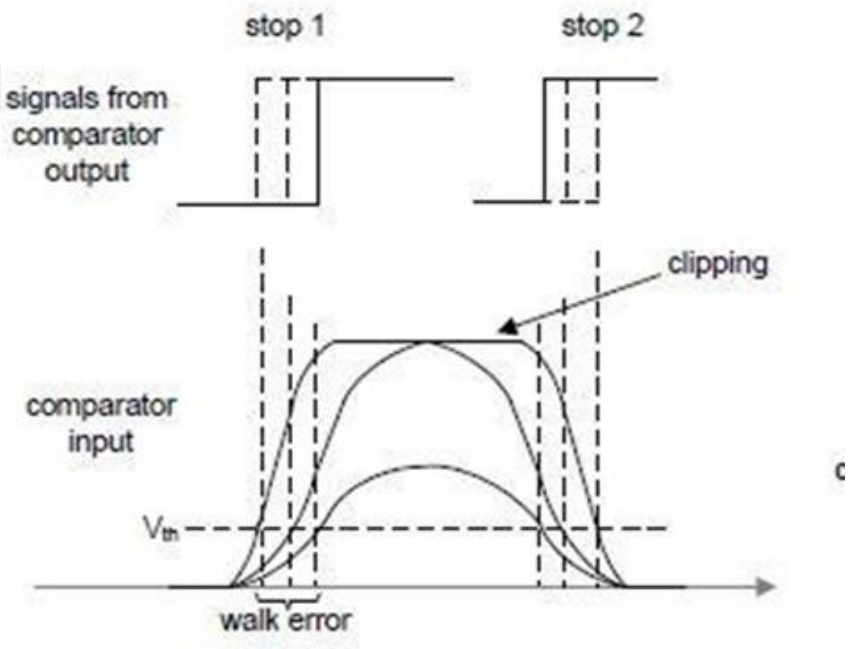

Figure 4.5. *The walk error* [56]

Although the distance of three signals is the same, the signal with the highest energy seems like it comes from the closest distance. Because it crosses the threshold signal first and produces a stop signal to the time to digital converter of the FPGA before others. Hence, a time measurement error occurs due to the differences in reflectivity.

The walk error is simulated in Figure 4.6. The threshold voltage can be selected as 3 times or 6 times the noise floor depending on the conditions [56]. The noise floor for the designed TIA was 1.75 mV RMS. 5 times greater threshold voltage is selected. It corresponds to approximately 25 mV. LTspice circuit simulation program is used to simulate the walk error. In Figure 4.6, 3 different echo signals are simulated. The transmitted laser signal pulse width is assumed as 10ns. The simulated signals seen in Figure 4.6 is the output of the TIA of the LiDAR circuit. The output of the photodetector goes into the TIA directly. The input currents of the TIA are 2 µA, 5 µA, and 8 µA. The gain is 24900 as a result of a 24.9 k feedback resistor. The signal with the highest energy passes the threshold first as in Figure 4.5. The signal with the lowest energy crosses the threshold voltage last. Although their time of flight is equal, time to digital converter guesses that time of flight of the red signal which has the highest energy is less than others while the time of flight of the green signal is longer than others.

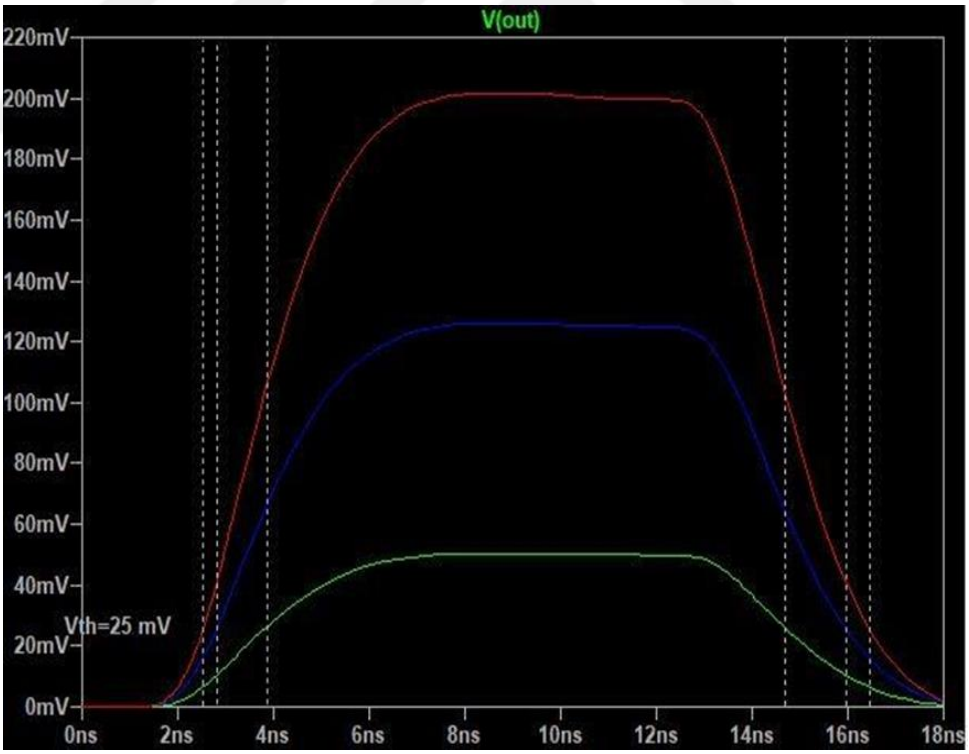

Figure 4.6. *The walk error simulation simulated by LTspice*

4.3. A Correlation Method to Increase Noise Immunity of Comparator

LiDAR technology is very popular in recent years. Self-driving cars are becoming widespread. The lasers of LiDAR systems of cars can deceive each other. To be able to prevent other lidar's effects, a time stamp method can be used. The time difference between stop 1 and stop 2 signals in Figure 4.5 can be used to measure pulse width. Tolerance should be determined when measuring the pulse width. Tolerance can be calculated by subtracting the maximum measured pulse width with the minimum measured pulse width. For instance, tolerance for simulation in Figure 4.6 can be found by subtracting the pulse width of the red signal with the pulse width of the green signal. Tolerance corresponds to approximately 3.1 ns.

The transmitter circuit can change the pulse width and inform the receiver circuit to improve the noise immunity of the LiDAR. Informed receiver circuit with time to digital converter expects the transmit signal patterns. Time to digital converter calculates the pulse widths and save it to buffer of the FPGA or send those time calculations to the computer. The computer eliminates the wrong time calculations caused by noise. An example of a LiDAR transmitter and comparator circuit output waveforms can be seen in Figure 4.7. The transmitter signal is only one signal. But the receiver output has two distinct signals. The first signal of comparator output which has a shorter pulse width comes from the rising edge of the transmitter signal. The second signal of comparator output which has a longer pulse width comes from the falling edge of the transmitter signal. The first signal corresponds to stop 1 and the second signal corresponds to stop 2 in Figure 4.5. Figure 4.7 shows the signals in the absence of noise. Figure 4.8 shows the transmitter signal and comparator output signals in the presence of the noise. Time difference between first stop signal and second stop signal gives the signature of the sent laser signal. This signature can be changed in time to get a better signal to noise ratio and prevent other laser sources effects.

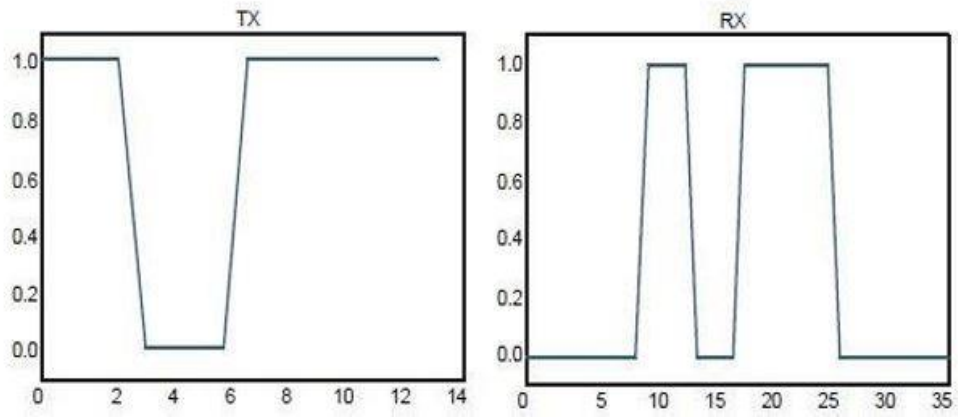

Figure 4.7. *An example LiDAR transmitter and comparator output in the absence of noise* [56]

When noise is considered, the output of the comparator can be in Figure 4.8. It can be seen that false comparator outputs appear. For instance, the signal at 5 ns does not result from the transmitted signal but noise. Comparator circuit output signals are the stop signals of time to digital converter. That noise signal causes the calculation process of the FPGA time to digital converter to finish prematurely. The actual stop signal is at the 10th ns, but the comparator output caused by noise is at 5th ns. Thus, time to digital converter thinks that stop signal comes 5 ns early. 5 ns mean 75 cm wrong distance measurement. Therefore, it is important to measure the pulse width of the received signal and compare the transmitted signal in a noisy outdoor environment. All the time measurements should be sent to a computer or recorded to block RAMs (Random Access Memory) in FPGA to compare the transmitted and received signals. If received and transmitted signals are the same, then the time measurement result can be print on a screen. In an FPGA or computer, signal processing methods can be applied. The cross-correlation function can be applied to see how much the transmitted and the received signals are similar. An example of a cross-correlation application for the transmitted signal and received signal in noisy and noise-free environments can be seen in Figure 4.9.

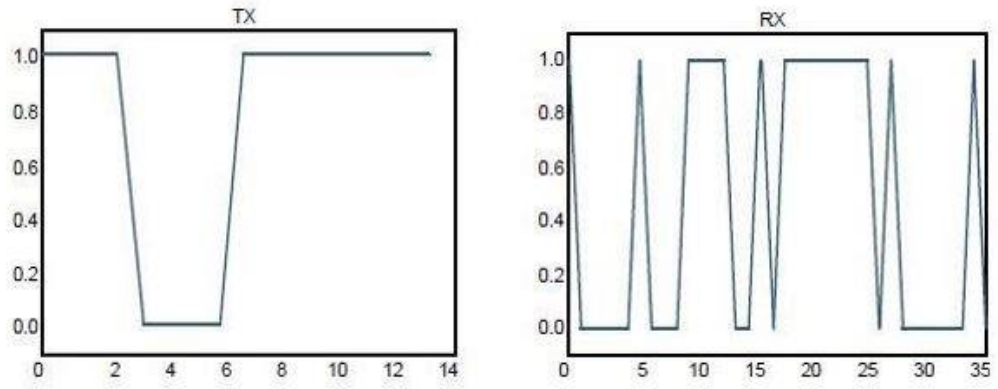

Figure 4.8. *An example LiDAR transmitter and comparator output in the presence of noise* [56]

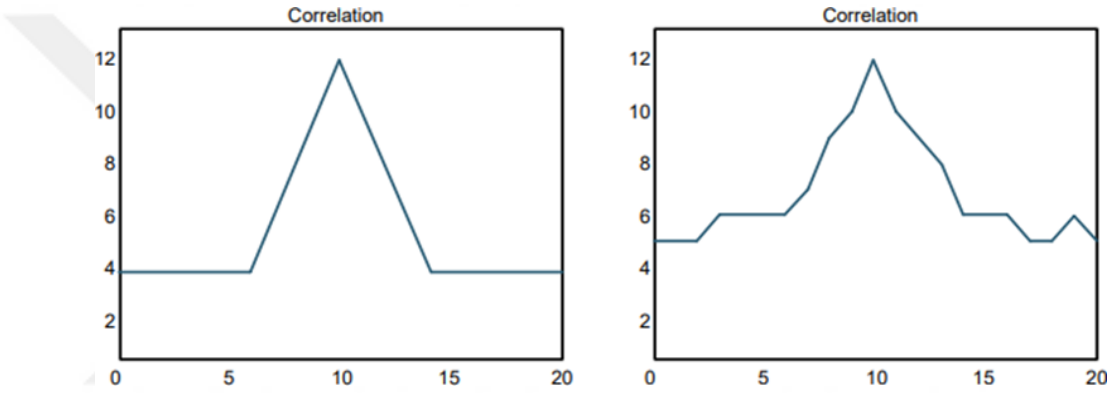

Figure 4.9. *Correlation of received and transmitted signals in noisy and noise-free environments* [56]

4.4. Simulation Results and Detecting Important Time Errors

The LTC6754 comparator chip is added to the LTC6268-10 trans-impedance amplifier circuit in Figure 4.10. The circuit is designed in the LTspice circuit simulation program. The TIA circuit was designed in Chapter 3. In addition to that circuit, only a comparator is added. The threshold voltage is determined as 25 mV as in Figure 4.6. 25 mV is 5 times the RMS noise floor of the designed TIA as can be seen in Figure 3.14. When TIA output and the comparator output is simulated in the same graph using a 25 mV threshold, signals of the TIA can not be seen clearly. Therefore, 1.25 V is added to both TIA output and the comparator threshold voltage to be able to see both comparator and TIA outputs together. The threshold voltage is connected to inverting input. Thus, the comparator output voltage increases when the input voltage increases. The output of the LTC6754 comparator is in the form of low voltage differential signaling (LVDS). Thus, there are two outputs of the comparator. These outputs are the opposite of each other.

When noninverting output rises inverting output falls. 100-ohm termination resistance is required to connect the output of the circuit to FPGA. The SHDN pin of the comparator left unconnected. Thus, no shutdown will occur, and power is continuous. HYST pin is unused because internal 4.5 mV hysteresis is used. No additional hysteresis is added. If more hysteresis voltage is required, it should be adjusted as shown in Figure 4.3. Latch enable can be activated if there is a need. A bypass capacitor can be connected between LTC6268-10 and LTC6754. Because bypass capacitor blocks dc offset voltage and lets ac signals pass. Dc offset can occur If the photodiode is not filtered well and dc offset differs from environment to environment.

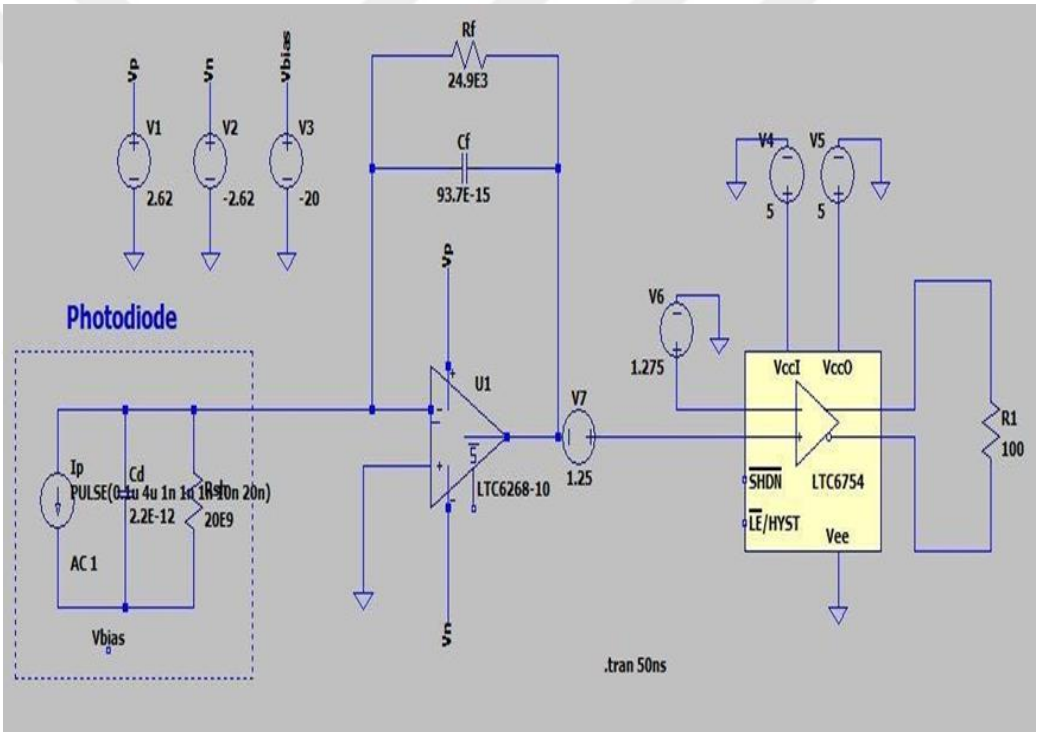

Figure 4.10. *The designed circuit before FPGA TDC*

The simulation result of the designed circuit of Figure 4.10 is in Figure 4.11. The simulation is done with the LTspice circuit simulation program. The green voltage signal is the output of the TIA. The maximum value of the output of the TIA is 100 mV. But 1.25 V dc offset is applied to be able to see all signals together. The blue signal is the threshold voltage. The red signal is the non-inverting output of the comparator. The light blue signal is the inverting output of the comparator. The TIA output signal crosses the

threshold voltage. 1.46 ns later, the non-inverting output of the comparator begins to rise, and the inverting output of the comparator begins to fall. The output common-mode voltage of the LVDS output of the comparator is approximately 1.25 V. Inverting and noninverting outputs of the comparator move between 1.08 V and 1.44 V. The LVDS output values of the comparator is nearly same with datasheet figure shown in Figure 4.2. An important detail is that the time required for the comparator to reach its %50 value after the output of TIA passes the threshold voltage is only 2.21 ns. It is a very low propagation delay and important for timing-critical applications such as LiDAR.

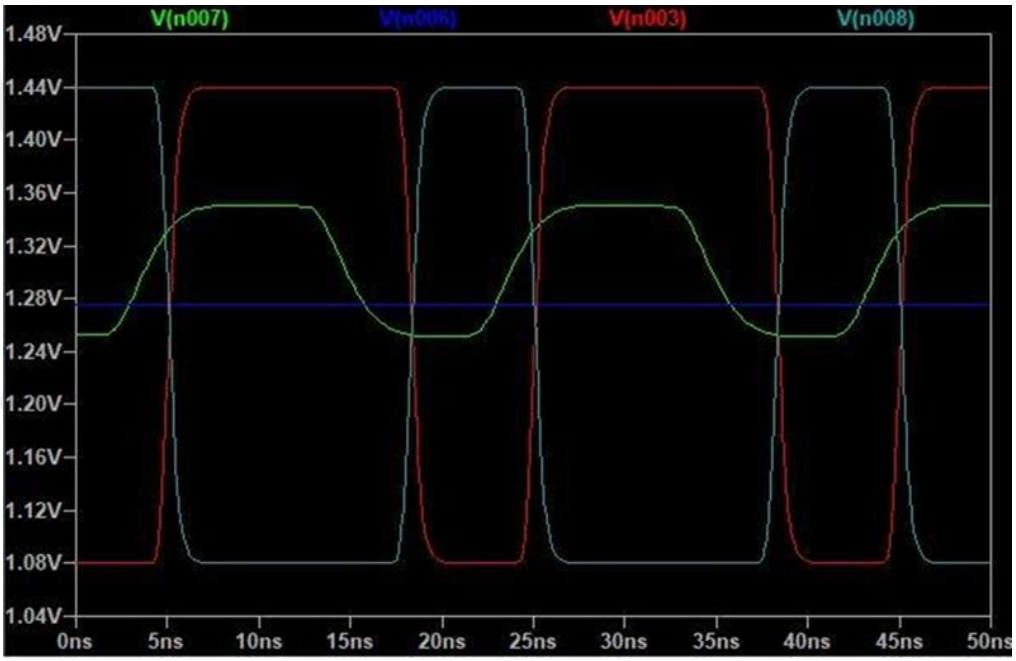

Figure 4.11. *LTC6754 comparator and TIA circuit simulation results*

The input overdrive dispersion is important. LTC6754 has low overdrive dispersion such that 1ns from 10 mV to 125 mV overdrive according to the datasheet. It is an important advantage for an accurate time of flight measurement. Overdrive dispersion causes a time calculation error. Thus, it is important to know input overdrive and establish an equation to calculate the error in time measurement. Input overdrive can be defined as the voltage difference between the threshold voltage and peak voltage value of TIA output. As input overdrive increases overdrive dispersion decreases in comparators. The difference between the blue signal and the peak value of the green signal in Figure 4.11

is input overdrive voltage. So, input overdrive in Figure 4.11 is 75 mV. The designed circuit in Figure 4.10 is simulated by changing the maximum photodiode current to 1.4 μA. 10 mV overdrive is attained by adjusting the photodiode current to 1.4 μA as can be seen in Figure 4.12. The time point the output voltage of the TIA circuit crosses the threshold is 4.47 ns. The time point the output voltage of the comparator reaches its %50 value is 7.49 ns. So, the elapsed time is 3.02 ns. This time was 2.21 ns for 75 mV overdrive dispersion. Overdrive dispersion is increased by 0.81 ns. It must be noticed that simulation begins after 1 ns delay, and the rise time and fall time of the photodiode current is 1ns. The pulse width of the photodiode is 10ns. Therefore, it can be analyzed that the total time passed after laser light hits the photodiode to produce a stop signal for FPGA is 6.49 ns. Since the energy of the received signal is low the TIA loses some time to amplify it when it is compared with received signals with high energy and an overdrive dispersion time error occurs. The designed circuit simulation results for 125 mV and 352 mV input overdrive can be seen in figures 4.13 and 4.14, respectively.

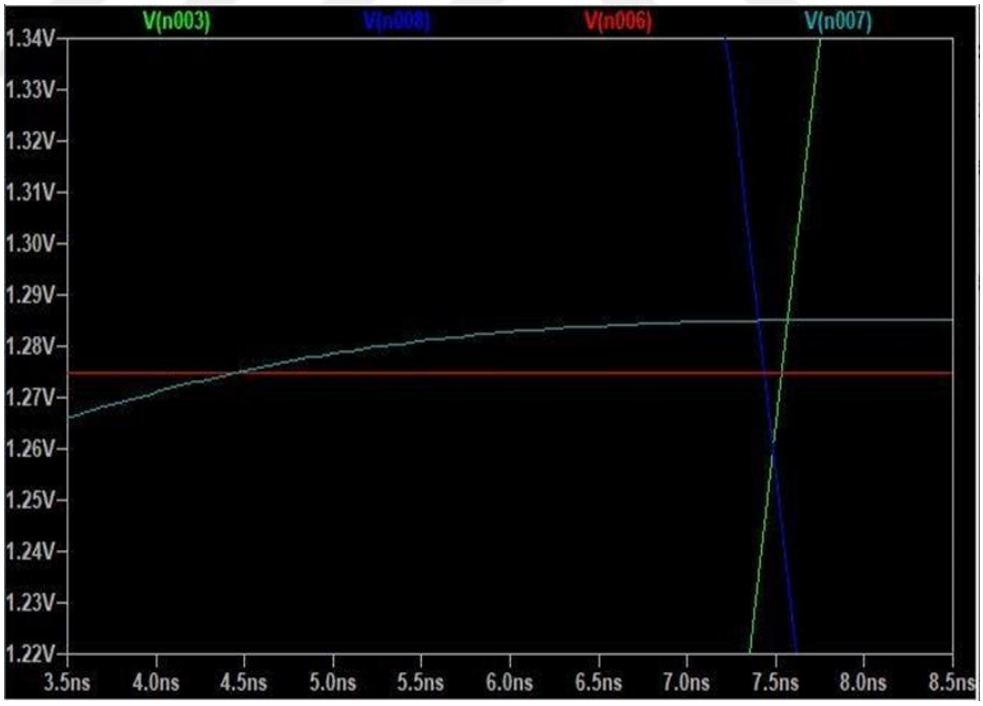

Figure 4.12. *Comparator output transient analysis with 10mV overdrive.*

It can be seen in Figure 4.13 that the blue signal which is the output of the TIA passes the 1.275 V threshold voltage at 2.6 ns. The green signal which is the noninverting output

of the comparator arrives at its %50 value at 4.7 ns. Thus, the time difference between these events is 2.1 ns. It was 3.2 ns in Figure 4.12 which has input overdrive of 10 mV. The overdrive dispersion difference between 10 mV and 125 mV is 1.1 ns. This is nearly the same with 1 ns as stated in the datasheet of the LTC6754. The simulation proves that selected opamp has a good time performance when it processes the low voltage signals. The critical voltage area is between 10 mV and 125 mV. 10 mV overdrive signal reaches the comparator output's %50 at 7.49 ns. But this time is 4.7 ns for 125 mV input overdrive. There is a 2.79 ns time calculation error for long-range time measurement. The echo signals lose much energy in long range. Therefore, the received energy of echo signals from the longe range target is low such that the TIA output voltage corresponds to a voltage between 10 mV and 125 mV. These voltages correspond to the biggest overdrive dispersion area.

In Figure 4.14, there is an overdrive dispersion of 352 mV. Big input overdrive causes low overdrive dispersion. It can be seen in Figure 4.14 that the green signal which is the output of the TIA passes the 1.275 V threshold voltage at 2.2 ns. The blue signal which is the noninverting output of the comparator arrives at its %50 value at 4.1 ns. Thus, the time difference between these events is 1.9 ns. It is 2.1 ns for 125 mV input overdrive. The difference of the input overdrive voltage is 227 mV, but the overdrive dispersion difference is approximately 200 ps. Although the LTC6268-10 TIA has 1500 V/μs, it loses time to amplify low currents. But the amplifying time of relatively high currents is less. Therefore, a constant current source with pA resolution can be added to the photodiode current to increase photodiode current. Amplifying time of TIA and input overdrive dispersion can be decreased in this way.

In this chapter, the LTC6754 comparator is selected by examining its datasheet features. A circuit is designed using the TIA of Chapter 3 and LTC6754 to test whether the selected comparator is proper for LiDAR or not. The decision is that it is suitable for LiDAR experiments. It is shown that it has a low overdrive dispersion. A receiver circuit for the stop signal of the FPGA TDC is tested with the LTspice simulation program. A very important time calculation error which is called walk error is shown with LTspice. The output of the TIA can be connected to a fast ADC or peak detector circuit to be able to calculate the overdrive dispersion of the comparator and amplification time of the TIA circuit as a future study.

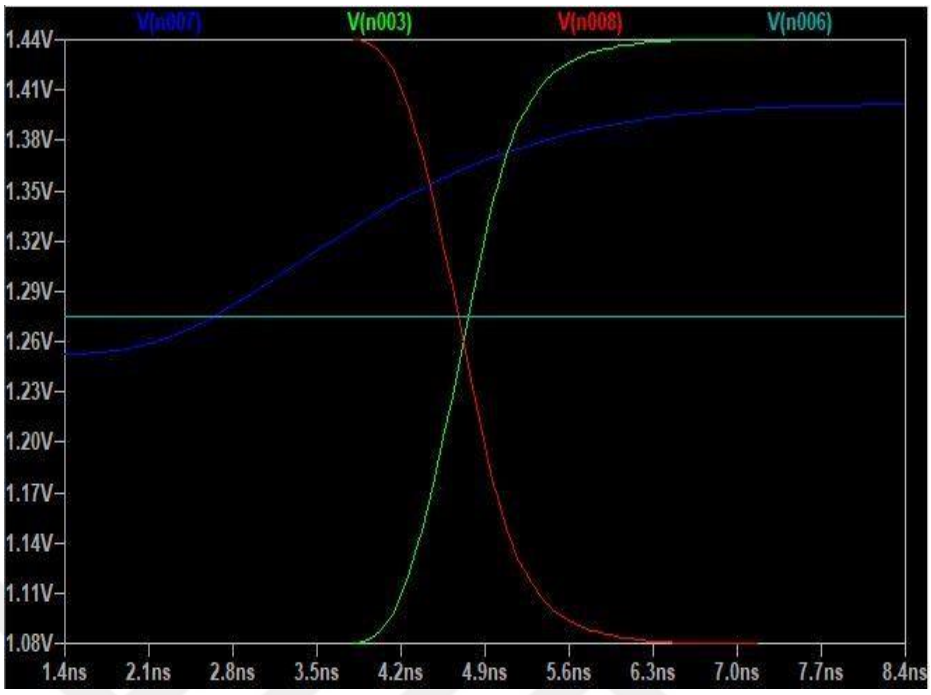

Figure 4.13. *Comparator output transient analysis with 125 mV overdrive.*

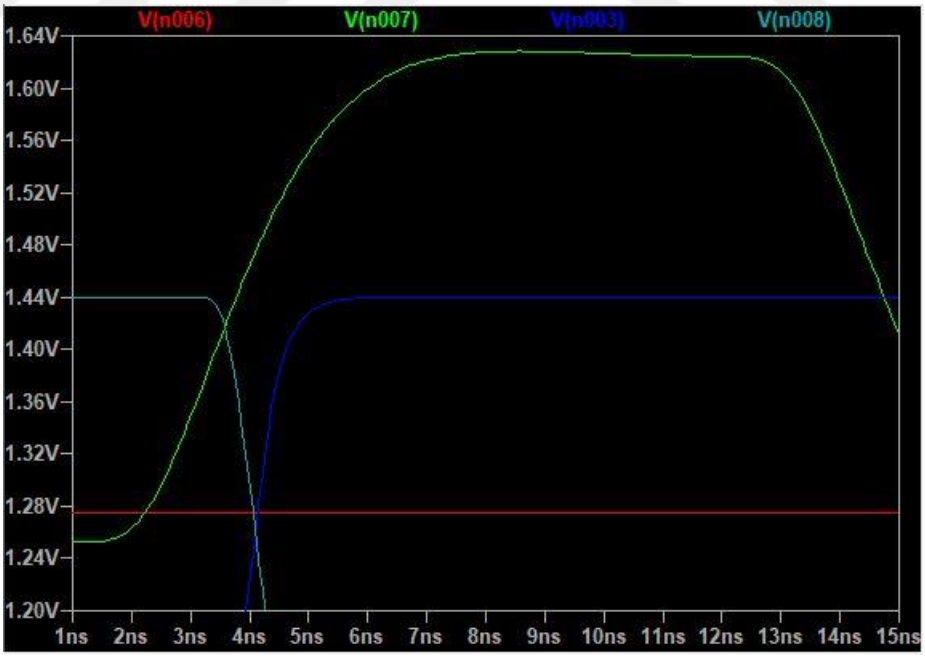

Figure 4.14. *Comparator output transient analysis with 352 mV overdrive.*

5. FPGA TIME TO DIGITAL CONVERTER

Time to digital converters (TDC) converts a time interval into digital data. For instance, the lifetime of electrons and holes in semiconductors could be from ns to ms. Measurement of the lifetime is possible with time to digital converters. Lifetime measurement is very important in solar cells and infrared detectors. The structure of the infrared detectors and the performance of the infrared detectors is related to the lifetime of electrons and holes. TDCs are used in the high-speed analog to digital converters (ADC) to make precise timing possible. TDCs are used in the area of particle physics such as in the CERN experiments [63]. TDCs are used in high-speed data transfer systems. Positron Emission Tomography requires sub-nanosecond time to digital converter for medical imaging [64]. An electromagnetic wave travels through a vacuum at a speed of 3.00×10^8 m/s. Distance from the objects can be determined by measuring the time of flight of light or other electromagnetic waves.. Time of flight measurement can be done by time to digital converters. A 3 ps resolution was achieved with an FPGA TDC for laser range finders in a paper [65]. In this thesis, a time to digital converter is designed to measure the time of flight to make distance calculations for LiDAR systems.

5.1. Vernier Delay Line Based FPGA TDCs

FPGA is a good candidate to design time to digital converters. Artix-7 XCA7100T FPGA is used in this thesis. There are a few methods to design time to digital converters in FPGA. One of them is Vernier delay lines. Vernier delay lines are widely used in FPGA time to digital converters. An example of a vernier delay line is shown in Figure 5.1.

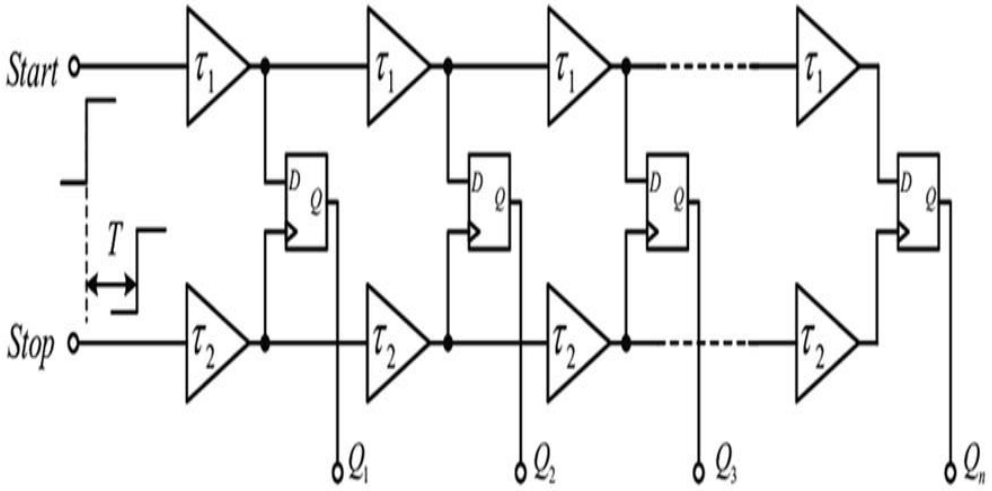

Figure 5.1. *A basic structure of FPGA TDC based on a Vernier delay line* [66]

There is a certain propagation delay difference in the delay elements of the path of the start and stop signal in Figure 5.1. Delay differences must be constant to achieve correct time measurement. Start signal propagates through the first delay line and the stop signal propagates through the second delay line. D flip flops are used to determine whether the coincidence of edges of start and stop signals occurred or not. For instance, let assume that the propagation delay of one element in the delay line of the start signal is 30 picosecond and the propagation delay of one element in the delay lines of the stop signal is 20 ps. Let assume that the time delay between the start and stop signal is 100 ps the number of the stages is 15. 100 picosecond corresponds to 1,5 cm for lidar distance measurement. If the output of the D flip flops is checked, it is observed that the output sequence of ones and zeros is like "111111111100000". There are 10 ones and 5 zeros. The stop signal is not able to catch the start signal until the 11th stage. The start signal makes the inputs of the 10 D flip flops one before the stop signal rising edge. After the 10th stage, the start signal propagates after the stop signal. Therefore, the rising edge of the stop signal occurs before the start signal makes the output of delay line one. The time interval between the start and stop signals can be calculated by Equations 5.1 and 5.2.

$$D = \tau_1 - \tau_2 \tag{5.1}$$

$$Time\ dif = D * (number\ of\ one) \tag{5.2}$$

5.2. Coarse Counter Based FPGA TDCs

Another time measurement method is the coarse counter method. The coarse counter method uses only clocks of the FPGA rather than two delay lines with two different propagation delays as in the Vernier delay line. Coarse counters with using only one clock of the many FPGAs cannot measure the time with sub-nanosecond resolution. For example, Artix-7 xc7a100tcsg324-1 FPGA is used to make the FPGA TDC. The maximum frequency which can be used to make coarse counter is 433 Mhz. 433 Mhz corresponds to approximately 2,3 nanosecond resolution. 1 nanosecond error for LiDAR is 15 cm. 2,3 nanosecond time error causes 34,5 cm deviation in the measured distance. Besides, 433Mhz does not meet the user timing constraints such as setup and hold times. It should be lower to meet timing constraints and decrease the Jitter noise.

Multiple clocks can be used to achieve sub-nanosecond time resolution. Four clocks with a 90º phase shift are used in a paper [67]. It is shown in Figure 5.2. If one clock is used to interpret the time, the time resolution will be one clock cycle period. If four clocks are used with a 90º phase shift, two times greater resolution can be attained. It is acceptable for long-range measurements such as 100 meters with a fast clock. For instance, the period of 400 Mhz clock is 2.5 ns. 1250 ps resolution can be achieved with a four 90º phased shifted clock interpolation method. 1250 picosecond corresponds to 18,6 cm distance resolution. For short-range measurement, better resolution is needed. A resolution below 5 cm is possible with a tapped delay time to digital converter which will be mentioned in the next section. Counting with clocks is done by the rising or falling edge of the clocks. The rising edge of the clock is usually selected by most FPGA programmers. The counting is done by the rising edge of the clock in Figure 5.2. If the start signal is one and the stop signal is zero, then every rising edge of the reference clock will increase the counter value one. Fine measurement can be done by interpolating the events of four clocks. If the start signal is one and the stop signal is zero, then the values of every clock cycle of the four clocks are recorded to logic vector signals. The results of the logic vector signals of timing events in Figure 5.2 are “0111110”, “0111100”, “0111100”, “1111100”, respectively. CLK4’s rising edge catches the start signal first. Therefore, the first bit of the four-bit logic vector signals is one and the first bit of other signals is zero. It shows the time between the start signal and the rising edge of the reference clock is greater than $\pi/2$ and less than π. The last bits of the logic vectors show

that the rising edge of the CLK1 signal sees the stop signal first. Thus, the time difference between the stop signal and the reference clock is less than π/2. The number of the rising edge of the reference clock will be counted by counting the number of the one in the first logic vector. The number of the rising edge will be multiplied by clock period time to find the coarse time. Fine time will be added to the coarse time to calculate the actual time interval between start and stop signals. The result value will be multiplied by the clock period to find the actual time. Since time measurement error is π/2 for start signal and π/2 for the stop signal. The total time measurement error is π. If the period of the reference clock is 3 ns, time measurement error will be 1.5 ns which corresponds to a time measurement with 1.5 ns resolution.

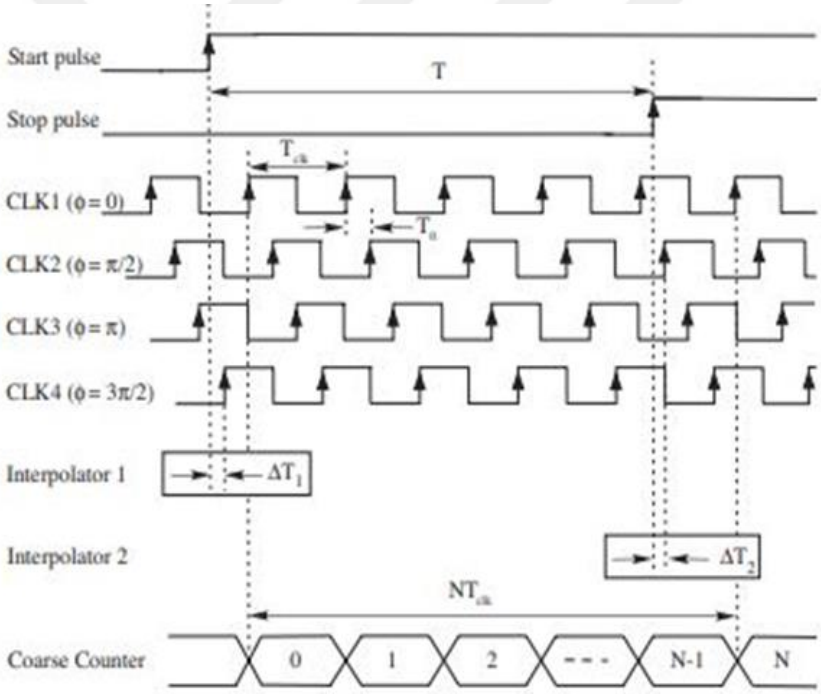

Figure 5.2. *Time measurement method by four clocks with a 90° phase shift* [67]

5.3. Tapped Delay Line Based FPGA TDCs

Another important method for time to digital converters (TDC) is a tapped delay line. A tapped delay line consists of taps of the same delay elements. These delay elements can be buffers, lookup tables, inverters, XOR elements, and precise RC delay lines. They are used in time to digital converters (TDC) to be able to measure the time with sub-

nanosecond resolution. When tapped delay lines are used with coarse counters, time measurement with a resolution up to a few ps is possible. For instance, a 7,4 picosecond time resolution was achieved via FPGA TDC [68]. 32 ps time resolution was presented in an FPGA TDC paper [69]. A time resolution of 42 ps was achieved in a paper [70].

5.3.1. Main delay element: carry4 primitive block

In this thesis, the tapped delay line is constructed with carry4 primitive blocks. Carry4 primitives are commonly used as a carry chain for precise FPGA TDCs [65-66], [63]. The structure of carry4 primitive block can be seen in Figure 5.3. The carry4 primitive block is connected to other carry4 primitive blocks to build a long delay chain. A start signal triggers the carry4 primitive delay chain and a stop signal latches the carry-out signals to measure the fine time between the start and stop signals. The start signal propagates through a carry4 primitive block in approximately 72 ps according to experiments done in Section 5.3.4.

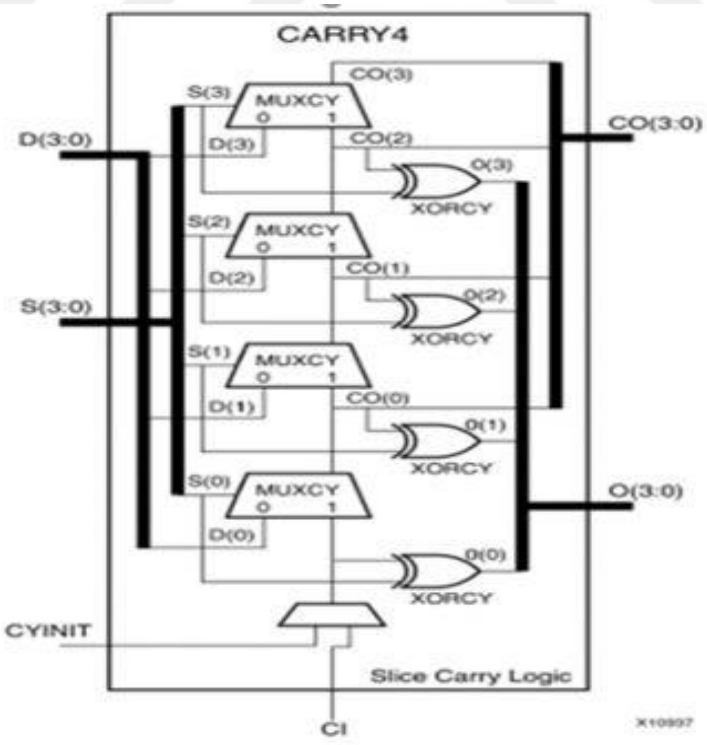

Figure 5.3. *Carry4 primitive in 7 series Xilinx FPGAs* [71].

In the structure of carry4 primitive block in Figure 5.3, there are 8 inputs and 6 outputs. S is a 4 bit std_logic_vector signal. 4 inputs presented by S control the multiplexers shown as MUXCY. The input of the MUXCY shown by “0” will be called as the first input. The input of the MUXCY shown by “1” will be called as the second input. For instance, if S(0) is zero then the first input of MUXCY will pass to the output of the MUXCY. All bits of the S get the value of one to let pass the second input signal of MUXCY to the output. The first inputs of MUXCYs are not considered as a part of the delay line structure. These inputs are used in other addition operations of VHDL codes. Since these inputs are not used in the delay line structure, their values will be 0. The connection points with other carry4 primitive blocks are the CI input and the third output of the CO logic vector signal.

The input CYINIT is used in only the first carry4 primitive block to trigger the delay line. Therefore, CYNINIT is used as a start signal of the FPGA TDC. It can be seen in Image 5.1 that the carry4 delay line is triggered by a signal which is connected to the CYNINIT input of first carry4 primitive block. Connections are shown by the white arrows. The second carry4 primitive block is connected to the first one via its CIN input while the first carry4 primitive block is connected to the second one via its CO3 output signal. Image 5.1 is taken from the designed delay line structure for FPGA TDC in the Vivado Design Suite integrated development environment (IDE). Vivado Design Suite IDE is used to program the Nexys A7-100T FPGA. The red squares which are connected to carry out signals are D flip flops. Delay lines are like domino stones lined up in a row. If the first falls, the others start to fall. Each stone has a fall time. The time elapsed can be estimated by looking at the groove of the last falling stone. If the start signal is one, the signal will propagate through the carry4 primitive blocks and activate the carryout signals. The difference of the delay line from the domino stones is that if the start signal is zero, then the next carry out signals become zero. Therefore, the start signal should be kept in high until the stop signal comes.

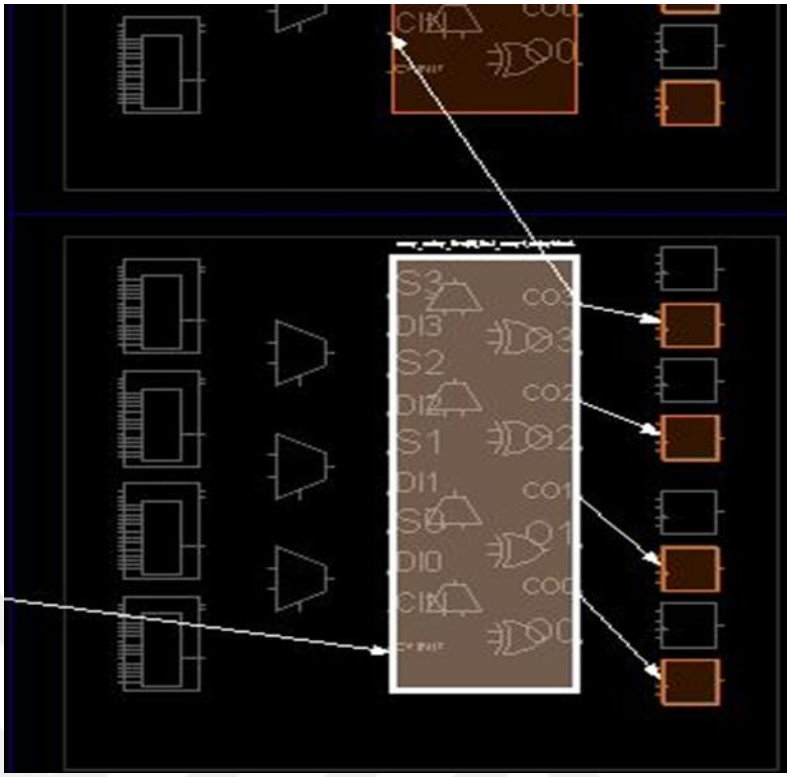

Image 5.1. *The first carry4 primitive block of the designed delay line*

5.3.2. Creating tapped delay line based FPGA TDC

The first carry4 primitive block can be created by the VHDL code in Image 5.2 by using the unisim library. The kaydedici std_logic_vector signal is used to record 4 carry out signals of the first carry4 primitive block. The value of the CI is 0. Because it is the first carry4 block and there is no third carry out signal which is connected to CI. The baslangic sinyali is an input port and defined in the entity part of the VHDL code. The baslangic sinyali is the start signal which triggers the carry delay line. DI corresponds to D in Figure 5.3. All the DI bits are set to zero to let the start signal propagate through carry delay chain. S consists of selection bits of MUXCY multiplexers as shown in Figure 5.3. All the S bits are set to one to be able to transfer carry out signals throughout the carry delay line.

```
delayline: CARRY4
                PORT MAP(
                        CO      => kaydedici (3 DOWNTO 0),
                        CI      => '0',
                        CYINIT  => baslangic_sinyali,
                        DI      => "0000",
                        S       => "1111");
```

Image 5.2. *The VHDL code to declare first carry4 block of the delay line*

The declaration of the rest of the carry primitive blocks can be done by the VHDL codes in Image 5.3. The variable “i” which is used in kaydedici std_logic_vector comes from the generate statement that is used in FPGA TDC codes to create successive carry4 primitive blocks. If the variable “i” is equal to 0, then VHDL codes in Image 5.2 should be written. If the variable “i” is greater than 0, then VHDL codes in Image 5.3 should be written. The equation for CO and CI in Image 5.3 is used to connect the third carry out signal of each carry4 primitive block to the CI of upper carry4 primitive block. The CI off first carry4 primitive block is kaydedici (3) which is the last carry out signal of the first carry4 primitive block.

```
delayblock: CARRY4
                PORT MAP(
                        CO      => kaydedici(4*(i+1)-1 DOWNTO 4*i),
                        CI      => kaydedici(4*i-1),
                        CYINIT  => '0',
                        DI      => "0000",
                        S       => "1111");
```

Image 5.3. *The VHDL code to declare the rest of the carry4 blocks of the delay line*

72 carry4 blocks are created to test the delay lines. The total carryout delay lines are 288. Thus, the start signal propagates through 288 delay elements to reach at the end of the delay line. A method must be applied to see the number of the delay line which passed by the start signal. D flip flops are used to latch the number of the delay lines passed before the stop signal comes. A basic D latch structure can be seen in Image 5.4. There are two inputs of the D latch structure as shown in Image 5.4. One of them is shown by the letter “D” and the other is shown by the letter “CK”. D is the value that will appear at the output of the D latch. CK input is normally used by the clock signal. When the rising edge of the clock occurs the value of the D input will be transferred to the output of the D latch which is shown by the letter “O”.

In the first carry delay line test experiment the carry out signals will be latched by the stop signal instead of the rising edge of the clock. The stop signal usage is not allowed by the Vivado Design Suite. Therefore, stop signal is used as a start signal of a delay line which consists of only one carry4 primitive block. The third output of that carry4 primitive block is used as the stop signal.

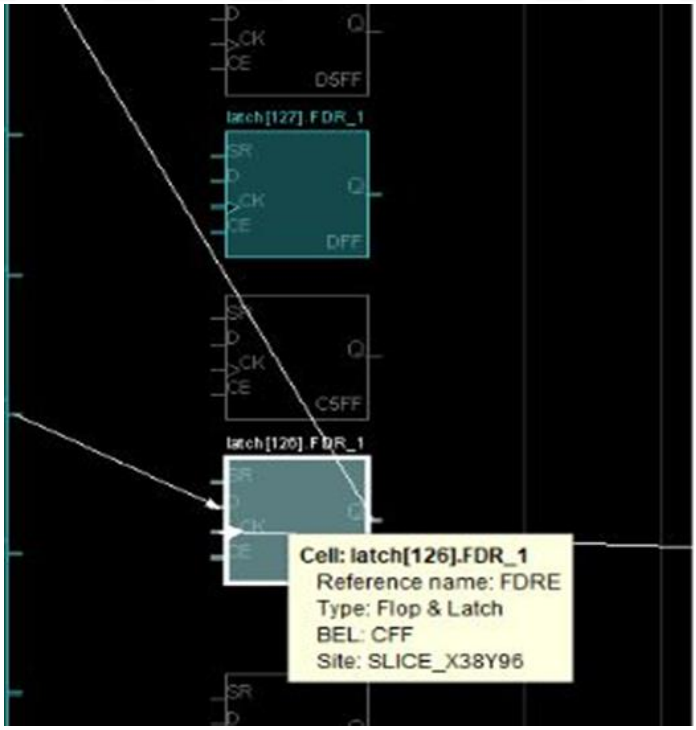

Image 5.4. *The D latch structure in the FPGA chip*

The main structure of the first test circuit is as in Figure 5.4. Trigger 1 is the start signal which triggers the carry delay line chain. Trigger 2 is the stop signal which is used to latch the outputs of the carry delay line chain. When trigger 2 signal goes to the high value the D latches will transfer the outputs of the carry delay line chain to the encoder. The encoder takes the D latches outputs and evaluates the number of the delay line passed by trigger 1 signal before trigger 2 signal comes. It counts the number of ones. The number of ones shows the number of activated delay lines. The number of the delay lines will be multiplied by a time delay of one element to find the total time elapsed between the trigger1 and trigger 2 signals. The encoder speed determines the FPGA TDC sampling rate. Because all the D latches parallel. The trigger signal arriving time to the D latches can change since the distance of the D latches is different according to the source of the trigger signal. Thus, the outputs of the D latches can occur at different times. But the time is not so big such that less than one ns.

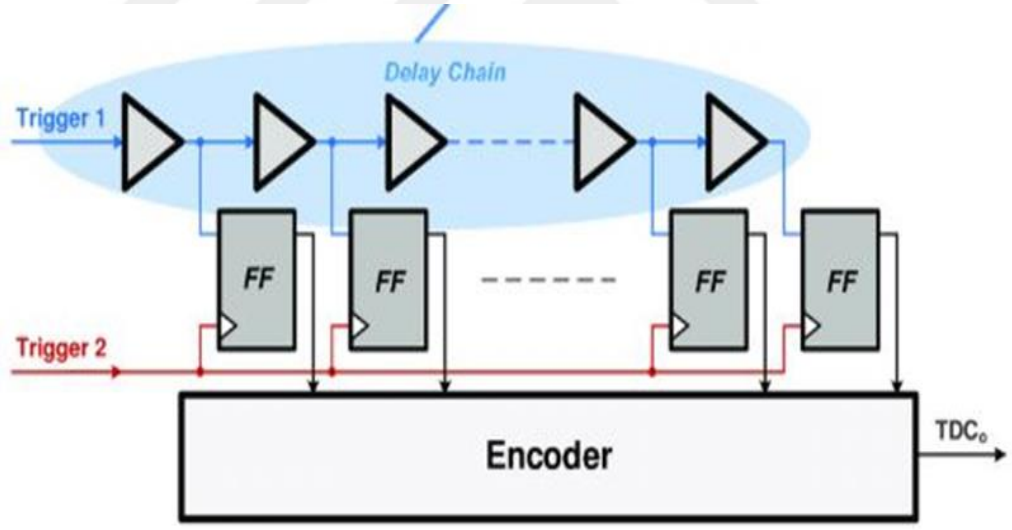

Figure 5.4. *The main structure of fine time measurement in FPGA TDC* [72**]**

The delay element and D latch structure in Figure 5.4 corresponds to the structure in the FPGA chip of Image 5.1. That structure repeats itself upward inside the FPGA chip as shown in Image 5.5.

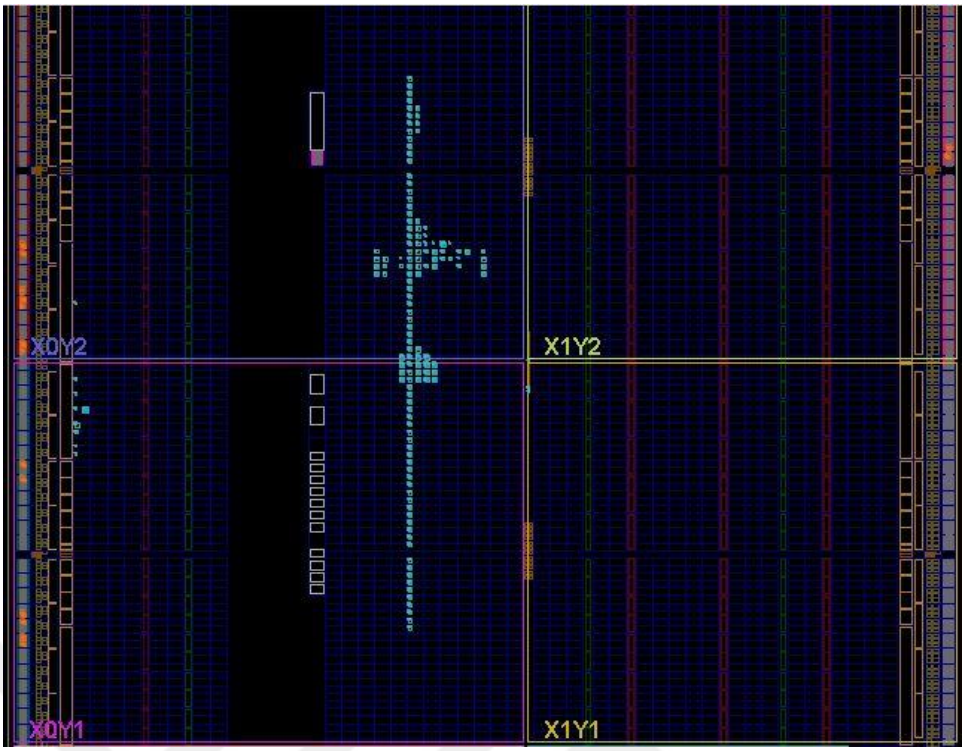

Image 5.5. *The created delay line chain in the FPGA Chip to test delay lines*

72 carry4 blocks are connected and create a long line towards upward in the X0Y1 clock region in Image 5.5. X0Y1, X0Y2, X1Y2, X1Y1 are the clock regions in the FPGA chip. The cluster in the region which is in the border of X0Y1 and X0Y2 is related to universal asynchronous receiver and transmitter (UART) in Image 5.6. UART protocol is used to communicate the FPGA with a computer. The information about the number of passed delay lines is sent to the computer using the UART protocol. Realterm computer program is used to make a communication bridge between the FPGA and the computer. The constructed delay line structure will be tested by changing the length of the jumper cables in Section 5.3.3. The number of delay lines passed will be printed to screen of the computer using the Realterm program.

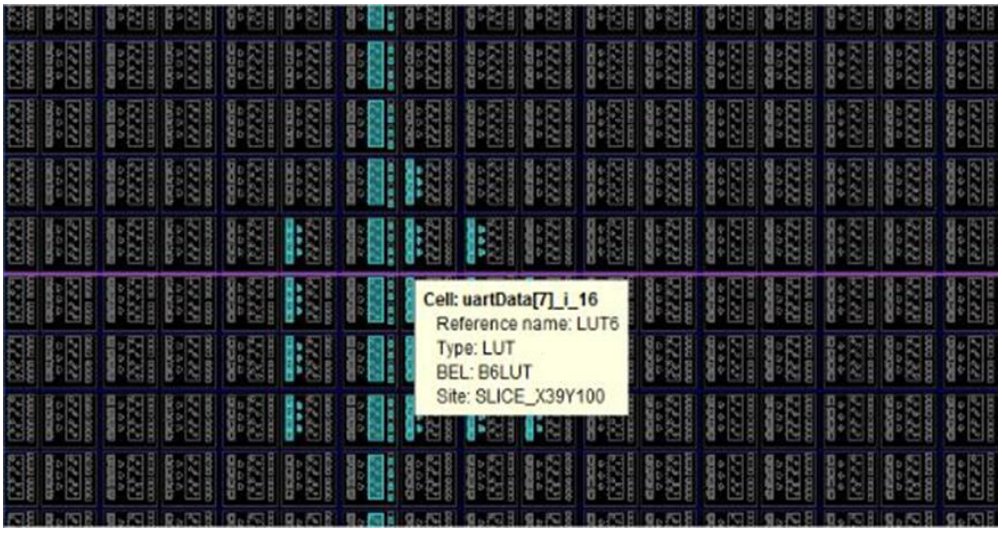

Image 5.6. *The region of the created delay line in FPGA chip related to the UART*

The start signal is written as baslangic_sinyali in VHDL codes. It triggers the carry delay line as explained before. The start signal can be seen in Image 5.7. Its starting point is from an FPGA input pad and directed toward the first carry4 primitive block to start the carry out the propagation chain.

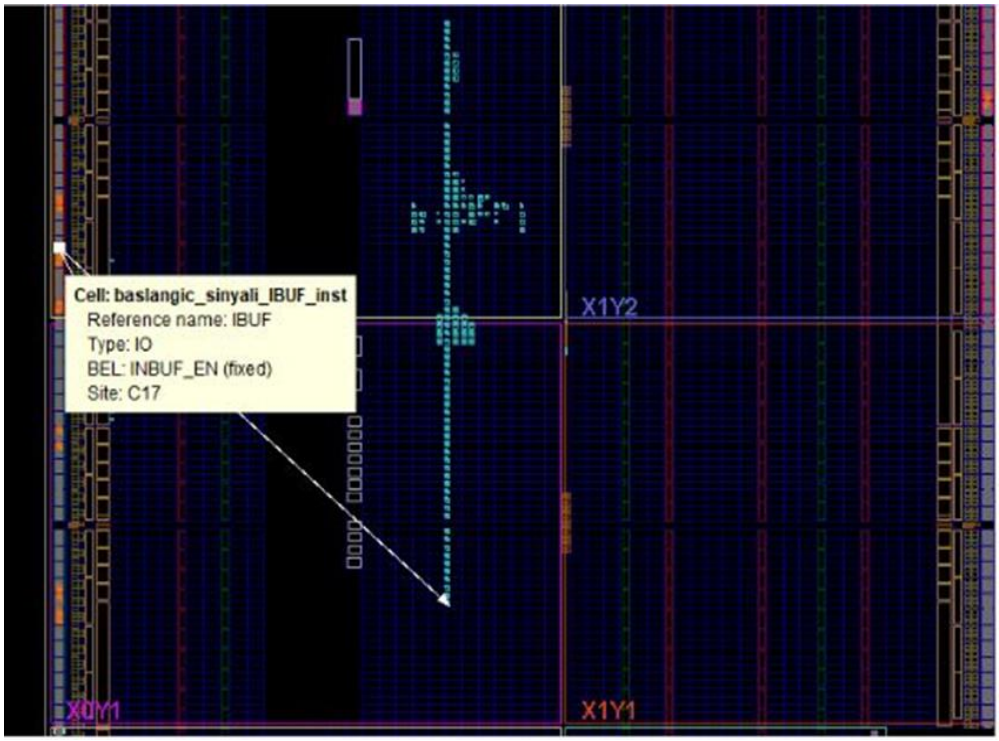

Image 5.7. *The start signal and its route to trigger carry delay line*

The stop signal is written as bitis_sinyali in VHDL codes. Vivado Design Suite does not allow to latch D flip flops directly. It gives a clock dedicated route error. Therefore, the baslangic_sinyali triggers a carry4 primitive block. The first carry out signal is used as the stop signal to latch the D latches to understand how much time passed by counting the ones in the output of the D latches. The stop signal input pad and that carry4 primitive block can be seen in Image 5.8. Routes of the stop signal in the FPGA chip are shown in Image 5.9. In Image 5.9, one white arrow pointing downward from the carry4 primitive block which is located near the input pads goes to coarse counter which to trigger the coarse counter. After the stop signal arrives at the coarse counter look-up table a counter starts to count the passed time considering the rising edge of the generated 200 Mhz clock. The main clock is the 100 Mhz clock. The white arrows which are drawn to the north-east go to the UART region. When a few clock cycles passed after the stop signal comes and the number of the ones of the output of the D latches counted, the results will be sent to the computer. The white arrow which is drawn to the south-east goes to the sources of the clock which has reference name BUFG and type clock.

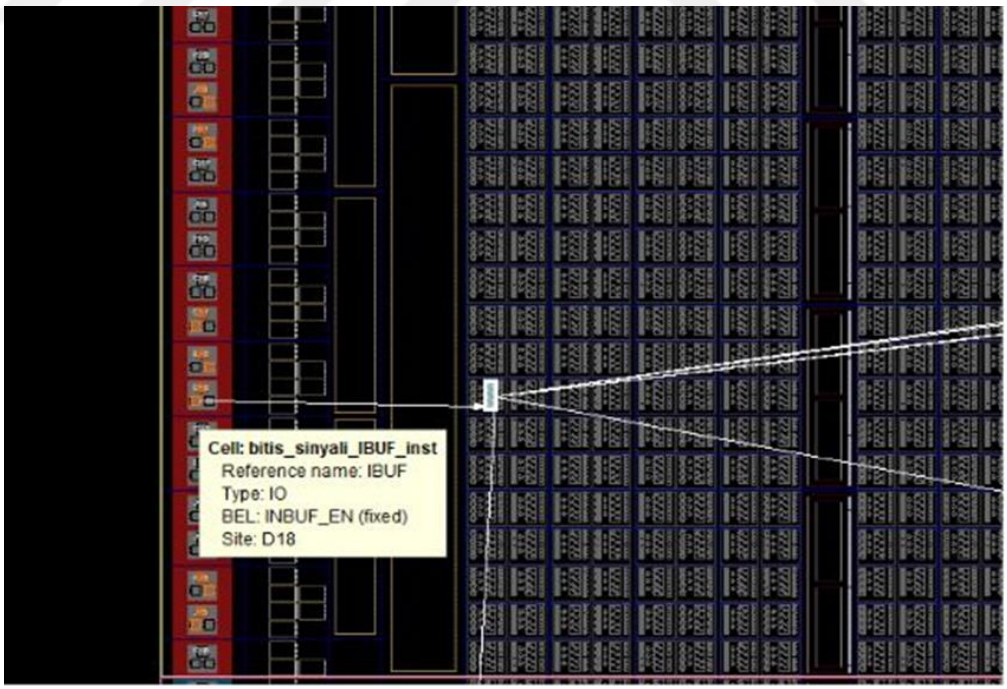

Image 5.8. *The stop signal input pad its carry4 primitive block*

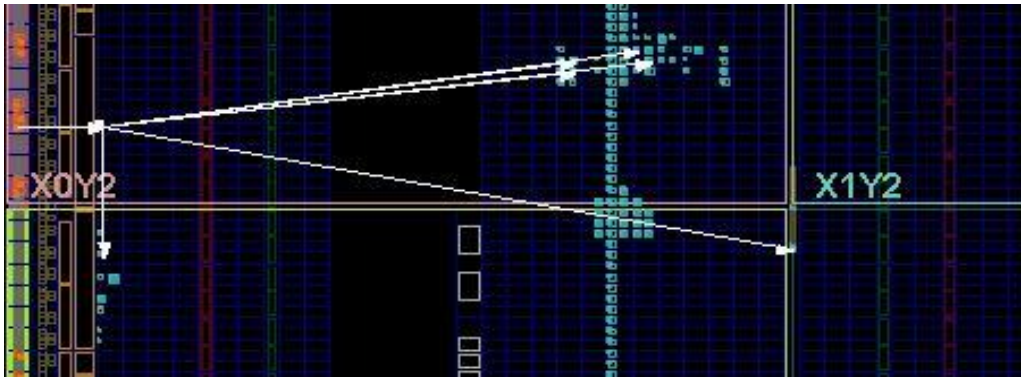

Image 5.9. *The stop signal route in the FPGA chip*

The stop signal is not connected to D latches directly but goest to the sources of the clocks first. Therefore, D latches CLK input signal comes from the source of the clock in the X0Y0 region as can be seen in Image 5.10. The white arrows coming from the birinci_BUFG which is the second station from the output of the birinci carry4 primitive block and third station from the stop signal input pad goes to D latches of the carry delay lines. There are 288 white arrows which correspond to 288 carry delay line and 72 carry4 blocks. Since distances of all D latches to signal source are not the same. Some latch time difference can occur in the orders of 10 ps.

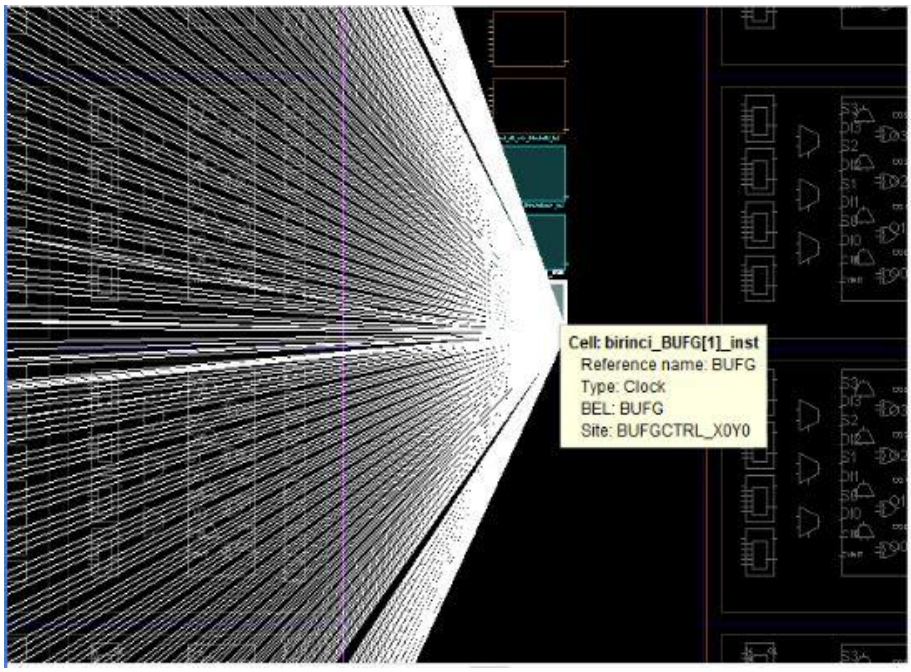

Image 5.10. *The source of CLK inputs of D latches*

The overall view of the delay line structure and its cell connections and nets can be seen in Image 5.11.

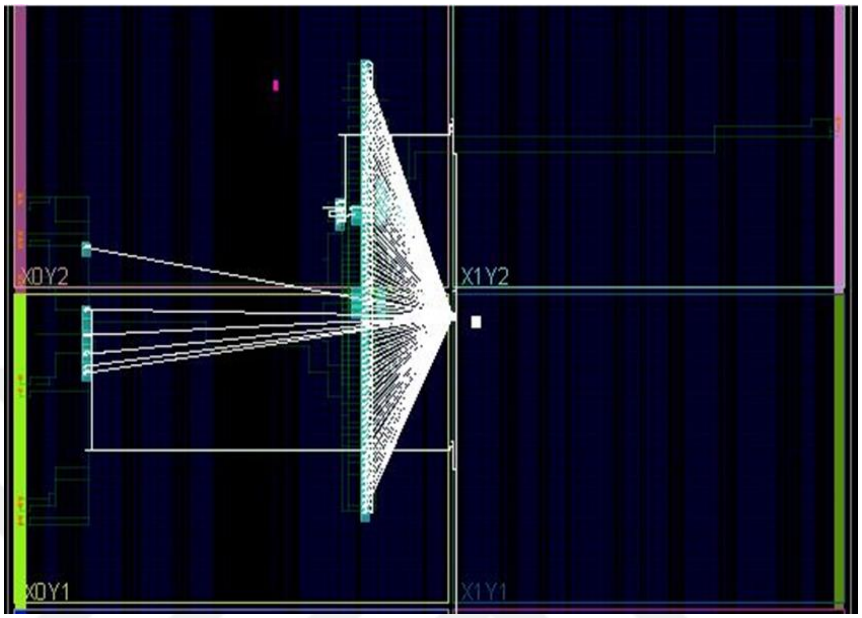

Image 5.11. *The cell connections and nets of the overall delay line structure*

5.3.3. First test experiments of created tapped delay line

To test the delay line sutructure which is seen in Image 5.11, a 3.3 V LVCMOS signal is applied from an output pin of the FPGA. A cable with constant length is used as the start signal. Another cable with varying lengths is used as a stop signal. The given voltage signal from FPGA goes to both cables for start and stop signals. The electrical signal traveling in the long cable arrives at the FPGA after some time delay. Changing the cable length will change the amount of time delay. When stop cable length increased it is expected that the number of the delay line passed will increase. Thus, the number of ones which are printed to the computer screen will increase. It is much better to give the start and stop signals with pulse pattern generators, waveform generators or arbitrary function generators. Due to the lack of these devices and the COVID-19 pandemic, the delay line structure test is done with jumper cables. But the test showed that the delay line works even though it does not show the exact resolution and accuracy and give an idea that carry4 primitive blocks can be used to build an FPGA TDC. The first experiment done by jumper cables to determine whether the delay lines work or not can be seen in

Image 5.12. The outputs of the experiment can be seen in Image 5.13. The brown cable on the left is used as a common voltage signal for both start and stop cables. The orange cable in the middle is used for the stop signal. The yellow cable on the right is used for the start signal. These cables are selected to be in equal length.

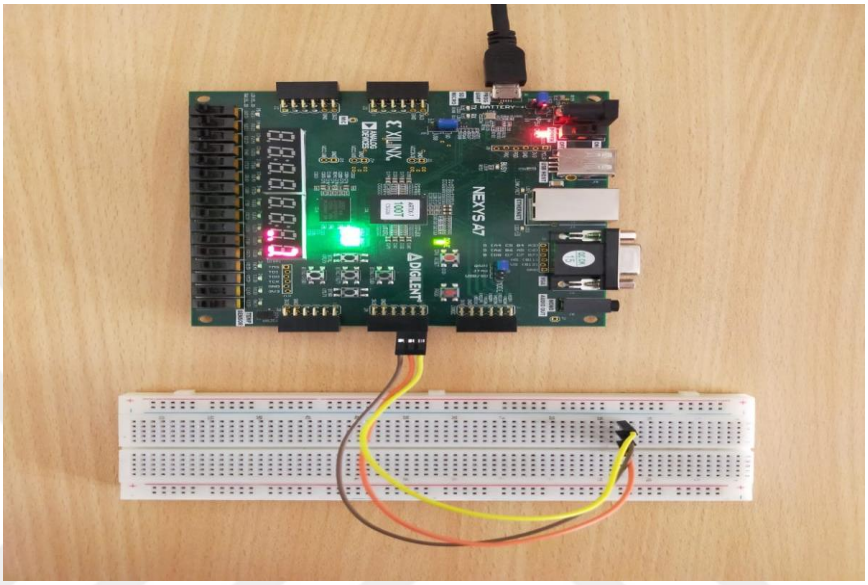

Image 5.12. *Delay line test with the same length start and stop signals*

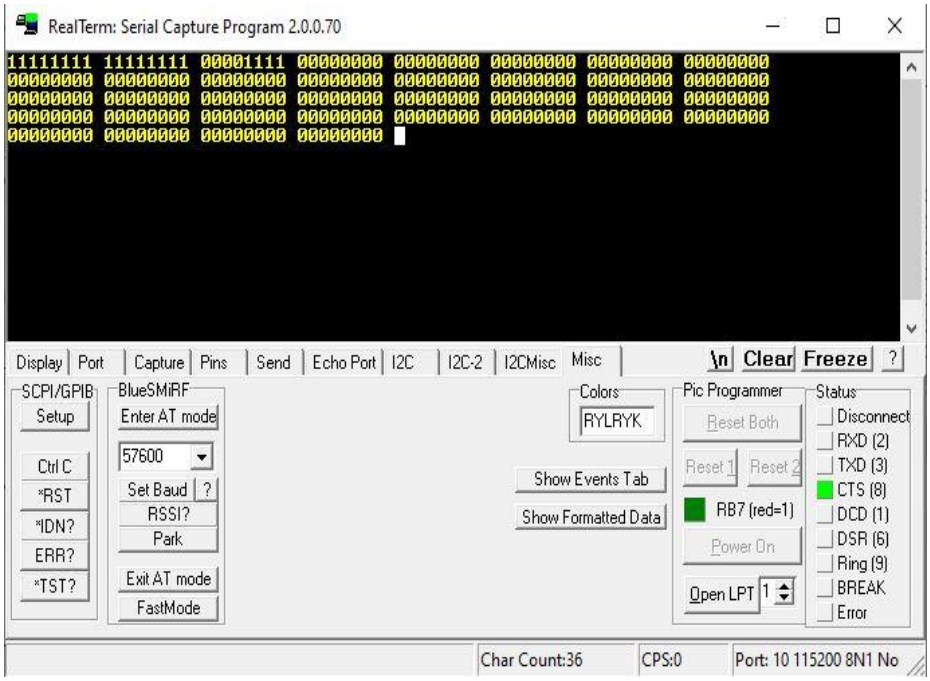

Image 5.13. *The output of the experiment in Image 5.12*

The stop signal can not directly latch the D flip flops to transfer the outputs of the carry delay lines. Therefore, a carry4 primitive block was triggered by the stop signal and the first carry out of that carry4 primitive block goes to the clock source region. After these steps stop signal can latch the D latches while the start signal goes only one the first carry4 primitive block of the delay line chain. Therefore, there is an offset delay time and it is calculated approximately 600 ps in Vivado Design Suite. 16 carry delay line is passed before the stop signal arrives because there are 14 ones in total 288 delay elements on the screen of the Realterm program as can be seen in Image 5.13.

Addition to time delay offset between the start and the stop signals. Cables are not calibrated but ordinary jumper cables to build some example circuits on the breadboard. They are not an HJ8-50B 3 inc Heliax coaxial cable which is a velocity factor of 93. Velocity factor for an electrical cable is an indicator that shows how fast an electrical signal travels in that cable. The velocity factor (VF) of the cables in Image 5.13 is not measured. Therefore, the time delay between the start and the stop signal may not be the same with different cables. Their velocity factor changes easily according to experiments done. The second experiment with a longer stop signal can be seen in Image 5.14.

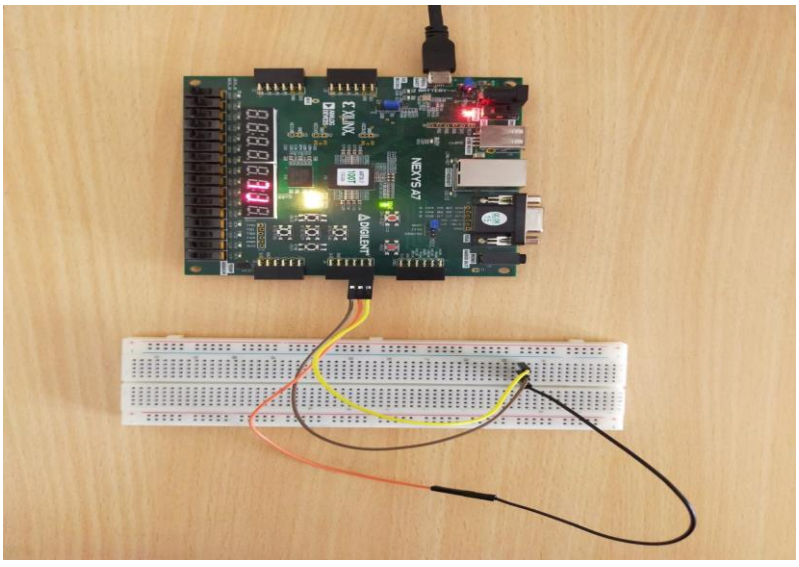

Image 5.14. *Delay line test with one cable longer stop signal*

The result of the experiment shown in Image 5.14 is shown in Image 5.15. In the last delay line test experiment start and stop signal's cable lengths were equal. In this

experiment, a jumper is added to the stop signal. The stop signal length is 21 cm longer than the first experiment. There are 54 ones on the screen of the Realterm program. It means that when the stop signal arrived at the FPGA and latched the D latches, the start signal was propagating through the 17th carry4 primitive block.

Longer cable results in a longer delay line propagated. Even loosely connecting cables to the breadboard change the number of the carry-out signals appear on the screen. But the number of carry-out signals change at most 5 when the program reloaded to the FPGA without changing any physical parameters. It shows that the delay lines in the FPGA work stable, but the measurement environment is not enough to test the resolution. The experiment with the stop signal which has 42 cm longer cable can be seen in Image 5.16. A jumper is added to the experiment in Image 5.14. It is expected that the number of ones will increase. And, it meets the expectations as shown in Image 5.17 because of the number of the ones which show the number of the delay line propagated through is increased.

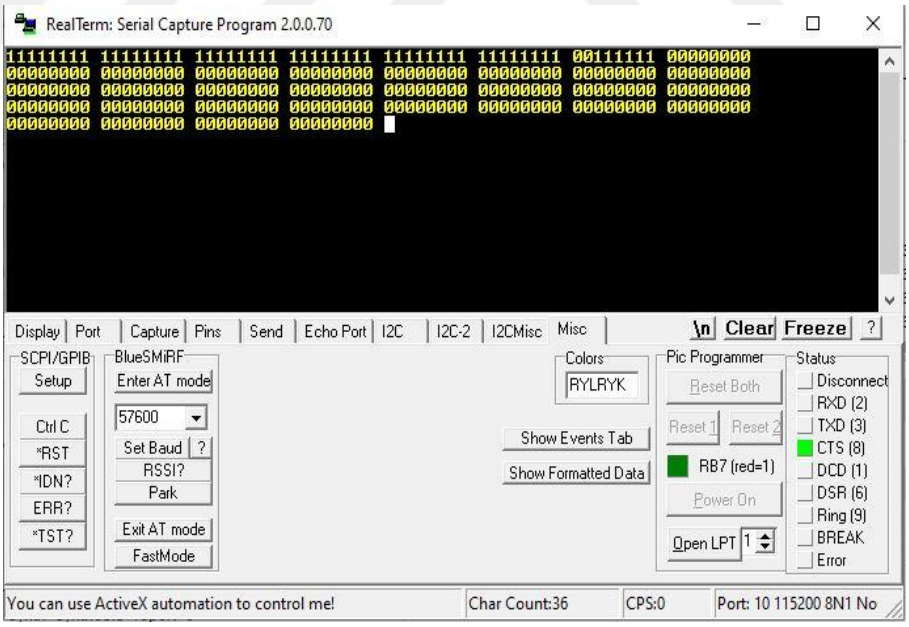

Image 5.15. *The output of the experiment in Image 5.14*

Due to their velocity factors of jumper cables are unknown, the electrical signal velocities are unknown. Therefore, only expectation from these experiments is that the number of the delay lines should increase when the length of the stop cable is increased.

The number of the delay line propagated through increases to 112 with 42 cm longer stop cable. Therefore, the created delay line works.

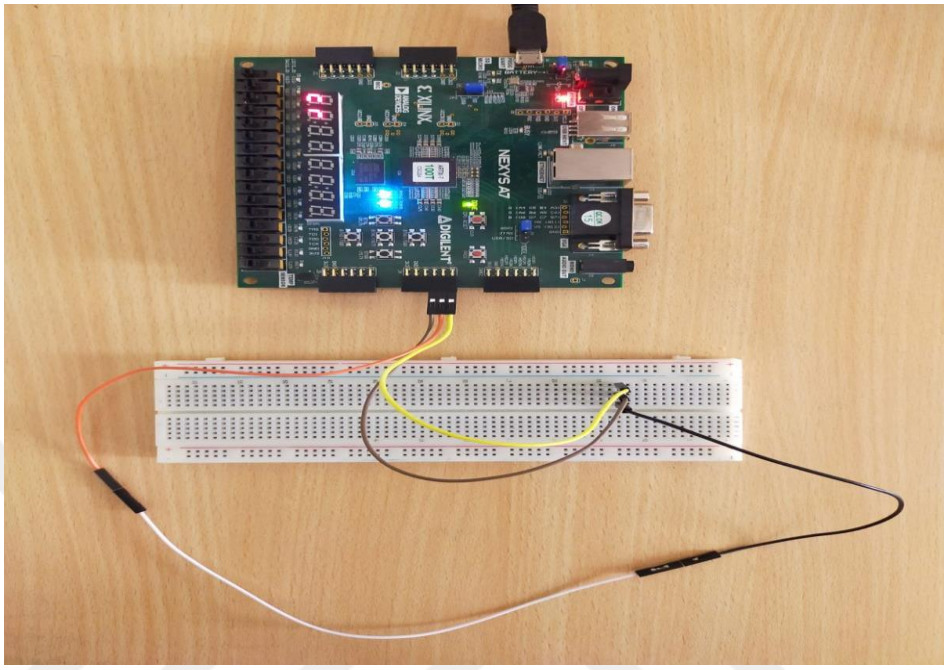

Image 5.16. *Delay line test with two cables longer stop signal*

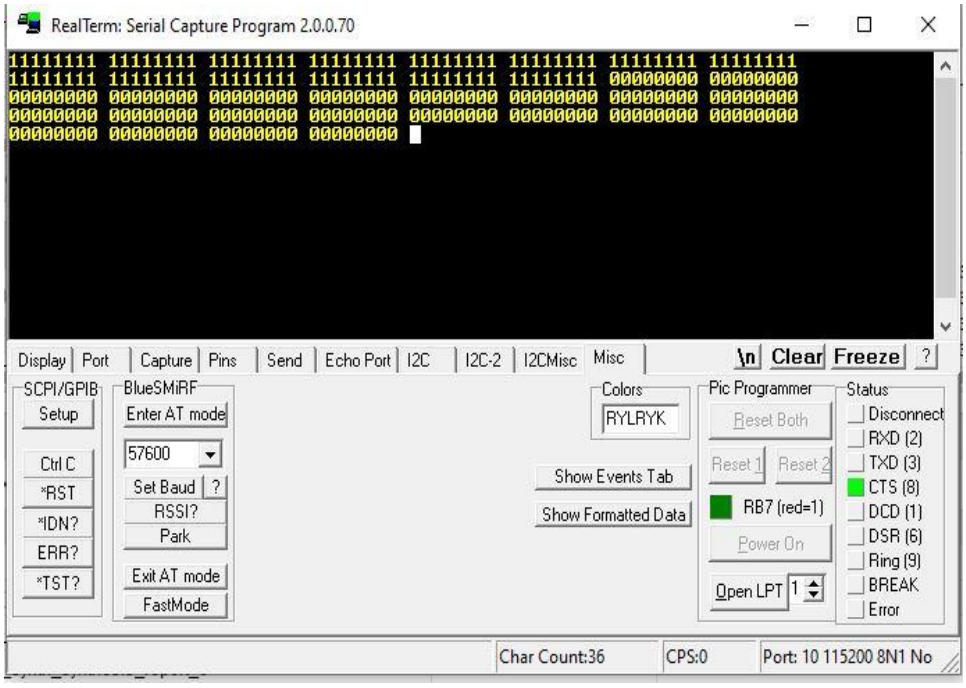

Image 5.17. *The output of the experiment in Image 5.16*

5.3.4. Detailed resolution experiments of created tapped delay line

To be able to make an FPGA TDC for LiDAR, the tapped delay line must work in a very precise way to measure the speed of light. The total time delay of the tapped delay line must be known. To obtain the total time delay, the delay of one smallest delay element which corresponds to carry4 primitive block's one carry must be known. The experiments in Image 5.12,5.14 and 5.16 showed that the carry delay line, in other words, tapped delay line works as explained. But it could not give a time measurement resolution since the velocity factors of the cables are different and that cables are not good to use in timing-critical applications such as LiDAR. Therefore, another method must be found to determine the propagation delay of the one carry delay cell which is the smallest unit of the carry4 primitive block. The developed method will be explained below.

Two phase lock loop (PLL) clocks will be used as a start and stop signals. Their frequencies are 100 Mhz. The phase of one clock will be shifted by 15º to get a time delay. Phase difference will be increased by 15º intervals to increase the time delay in an accurate way. The equation which gives the time delay according to phase is shown in Equation 5.1.

$$Time\ Delay = \frac{Period\ x\ Phase\ Shift}{360} \tag{5.1}$$

The period of the clocks is 10 ns since their frequencies are 100 Mhz. The phase shift interval is 15º. Therefore, time delay between two clocks is calculated as 416 ps. It means a 416 ps time delay interval will be produced to measure the time delay of one carry cell. The total delay of the tapped delay line must cover the period of the clock. The total number of the carry delay line required to cover the clock period can be calculated by dividing the period time of the clock by the propagation time of the one carry delay cell. The number of the carry delay cells in which the start signal propagates through in 416 ps time interval difference will be measured. If 416 ps time duration difference is divided by the number of the carry delay cells. Clock peak to peak jitter noise and phase error should be low to measure the propagation delay of the carry delay cells in an accurate way. The Clocking Wizard of the Vivado Design Suite IDE is used to generate two phase-shifted clocks. The user interface and generated clocks can be seen in Image 5.18. The clocking wizard uses a VCO to generate 900 Mhz frequency and divide it by 9 to get a 100 Mhz clock again. The summary of the generated clocks can be seen in Image

5.19. The phase requested is 15 in the first experiment. Then it will increase to 30,45,60,75,90,105. The results will be observed on the screen of the Realterm UART communication program. 115200 baud rate, 8 data bits, 1 stop bit, and no parity parameters are used for the UART protocol.

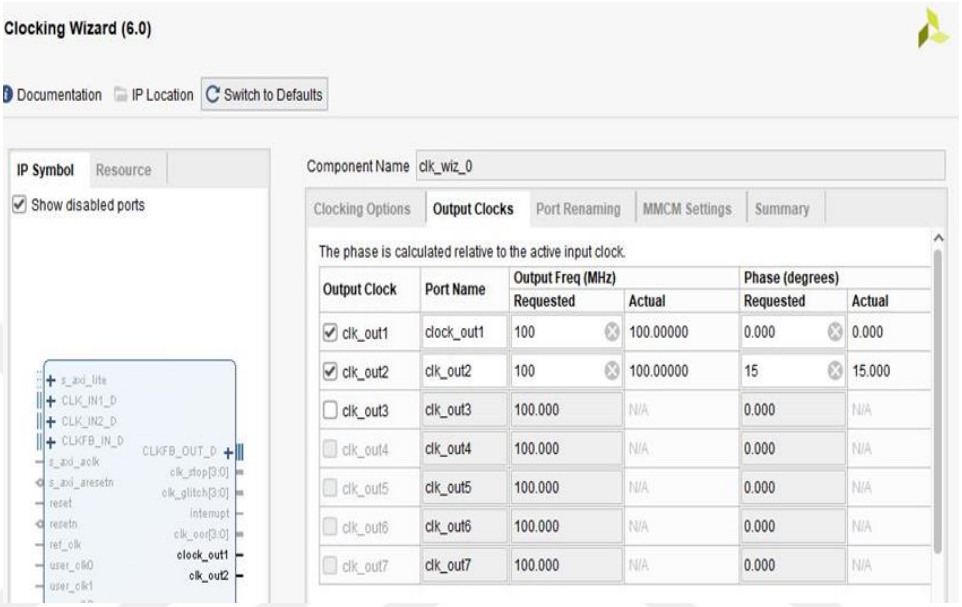

Image 5.18. *Clocking Wizard to generate two phase-shifted clocks*

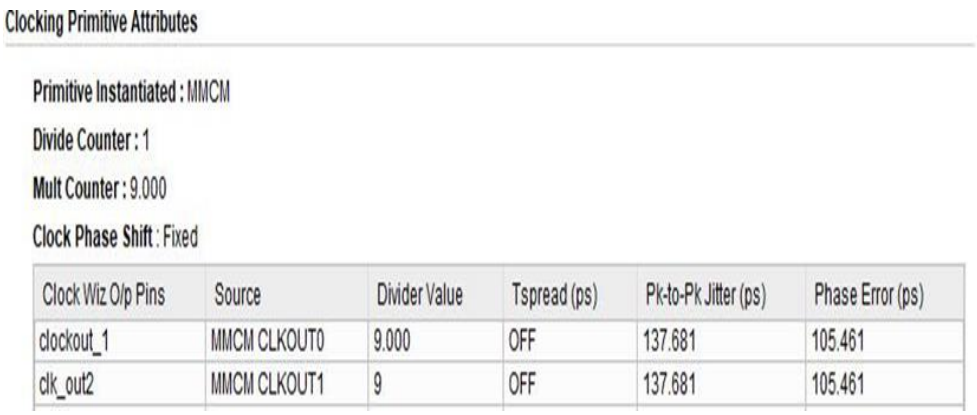

Image 5.19. *The summary of the generated clocks*

The result of the first experiment with phase-shifted clocks to measure the propagation delay of one carry delay cell is shown in Image 5.20. Two clocks start to count up to a fixed number in the VHDL codes. If clocks reach to that value reference

clock gives the start signal and 15º phase-shifted clock gives the stop signal. 15º corresponds to 416 ps time delay as explained before. This experiment is a reference experiment. Because the start signal is triggered when the 100 Mhz reference clock rising edge reaches the fixed number. The stop is triggered when the 100 Mhz 15º phase-shifted clock rising edge reaches the fixed number. There is an offset time delay between start and stop signals due to their signal routes and path lengths. Signals loose time even in a chip to arrive at their targets. The way of the stop signal is longer than the start signal. Therefore, the number of delay lines passed is greater than the normal. But it does not bring about a problem to measure the propagation delay of a single carry delay element. Since this first experiment is the reference experiment, the other results minus the reference experiment result will give the actual number of the delay line passed within the 416 ps time duration. For this experiment, 1024 delay lines generated to observe the linearity issues of the delay lines in the FPGA chip.

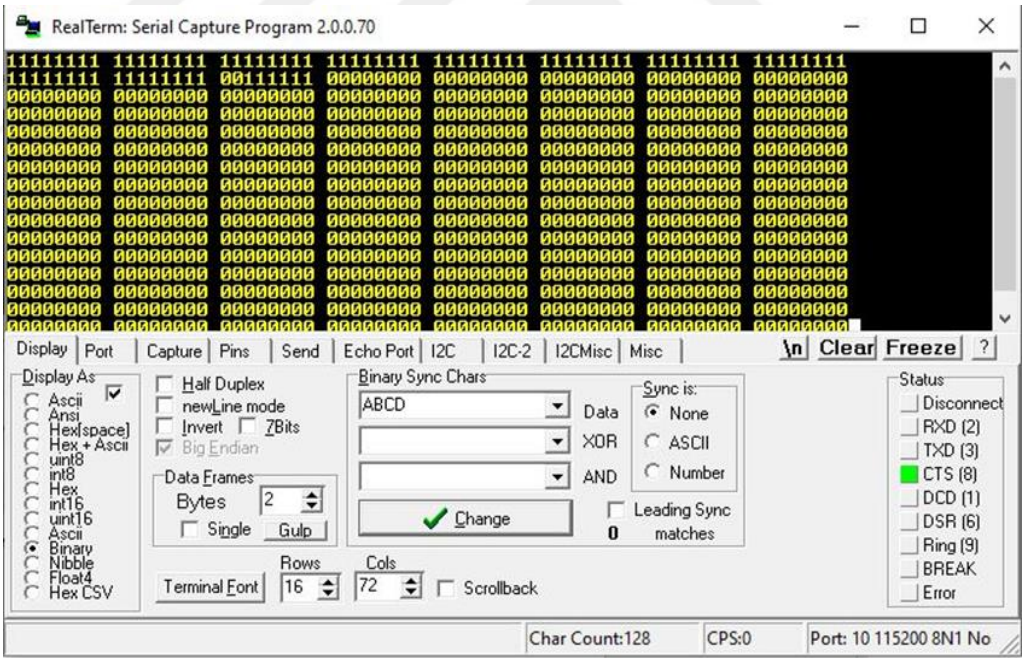

Image 5.20. *The result of the first experiment with 15º phase-shifted clocks*

The result of the first experiment is that there are 86 ones appearing on the screen of the Realterm serial capture program. The rest of the outputs are zeros. Thus, there is a 86 carry delay cell's propagation delay between start signal triggering and stop signal

latching events. Since net routes and lengths of the start and stop signals are different, there is a time offset that will be subtracted to get the true number of the carry delay line cell propagated through. For instance, the output of the second experiment is shown in Image 5.21. 108 ones appear on the output screen. Since the phase shift between the two clocks is 30º, the time duration between the start and stop signals is calculated as 833 ps according to Equation 5.1. The time difference from the first experiment is approximately 416 ps. The increased number of the carry delay cell which is propagated through is 22. As a result, the propagation delay of the 22 carry delay cells is the result of 416 ps time difference between the start and stop signal. Therefore, it is possible to calculate the propagation delay of one carry cell unit by these results. Dividing the 416 ps by 22 carry delay cells results in that one carry delay cell has an 18.9 ps propagation delay. The VHDL program for the experiment in Image 5.21 is run repeatedly to test whether the result changes or not. After waiting some time, the VHDL program gave the same results. So, the result is true and stable.

The results of the experiment in Image 5.21 and 5.20 shows that If a linearity study and calibration is done well enough, an 18.9 ps time resolution can be achieved by using tapped delay line FPGA TDC method which is the method of this thesis. But to be able to determine accurate propagation delay time of one carry delay cell more experiments are needed. The experiment with 45º phase-shifted clocks is shown in Image 5.22. There are 132 ones on the screen of the Realterm program. Therefore 132 carry delay line cell is propagated through by the start signal before the stop signal comes to latch D latches as explained before. The number was 108 for 30º phase-shifted clocks. So, 24 carry delay lines are responsible for the new 416 ps time difference. The number of carry-out signals was 22 in the last experiment. There are only two carry delay line differences. It is not so important. The reason behind that can be the jitter noise of the clocks. Also, the reason can be the homogeneity problem. The doping concentration of Si wafers changes from the middle to sides of the wafer, so it is not homogenous. The propagation delay of the carry delay line elements in a different region of the FPGA chip can be slightly different. Calculated one single carry element propagation delay for experiment in Image 5.22 and 5.21 is 17.3 ps if 416 ps is divided by 24 carry delay elements.

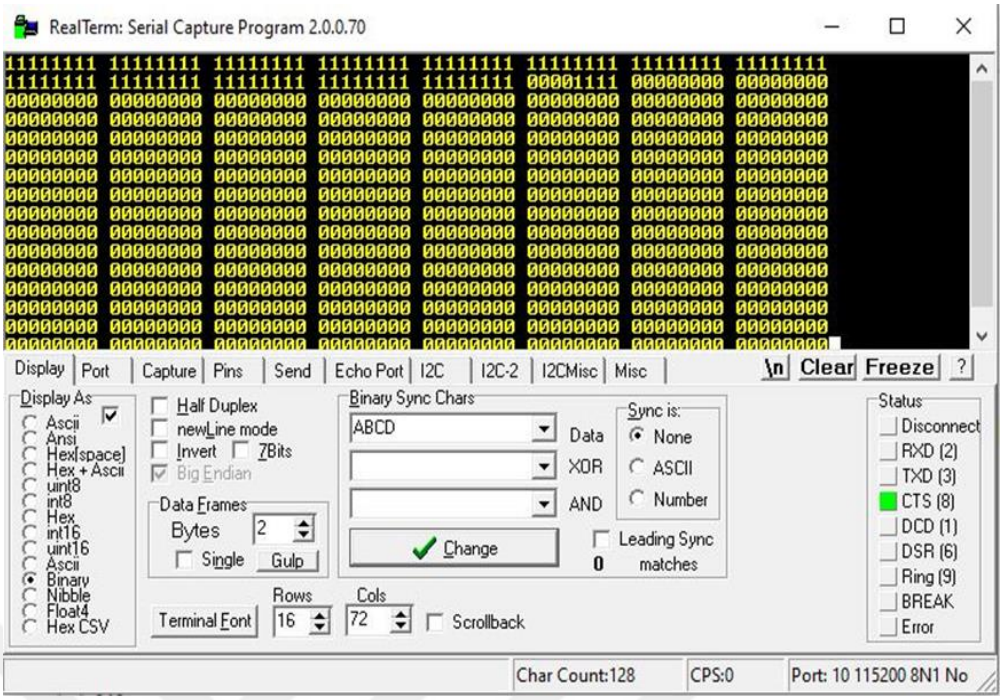

Image 5.21. *The result of the experiment with 30° phase-shifted clocks*

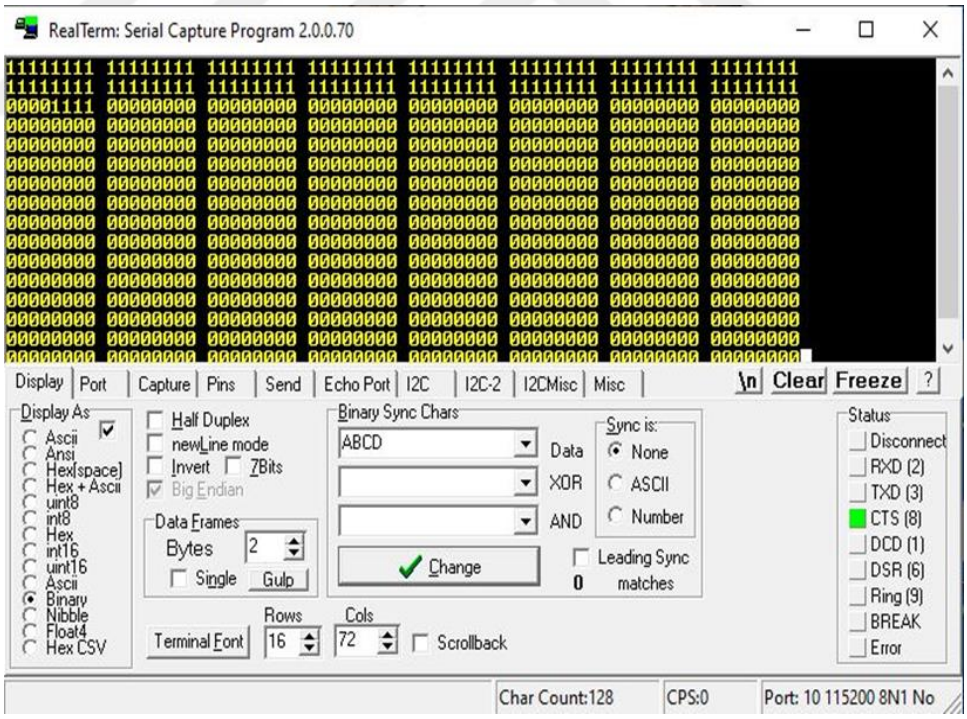

Image 5.22. *The result of the experiment with 45° phase-shifted clocks*

There are 158 ones in the experiment which is done by 60º phase-shifted clocks as can be seen in Image 5.23. It was 132 in the experiment with 45º phase-shifted clocks. Therefore 26 more carry delay element is passed by the start signal within the 416 ps more time delay between the start and stop signals. The propagation delay of one carry delay element corresponds to 16 ps. It is not different from the last experiment. But when it is compared to the experiment done with 30º phase-shifted clocks, there is a 2.9 ps difference in propagation delay of the carry delay elements. Thus, the reason behind this should be questioned. After the start signal triggers the carry delay line, 416 ps later stop signal starts traveling to latch the D latches. Since the distances of the D latches of every carry delay element to the source of the stop signal are different, the time durations passed between the stop signal starting and arrival to D latches are different. So, the reason behind the propagation delay time differences mentioned in the last paragraph can be this explanation. The net load delay time of the latch 102 can be seen in Image 5.24. It shows the traveling time of the stop signal from a buffer of clock region of X0Y0 to the latch 102. The traveling time is 1932 ps. Traveling time for the latches in the experiments done with 60º and 75º phase-shifted clocks will be investigating to determine whether the reason for the differences of the calculated propagation delays of the one carry delay element is valid or not.

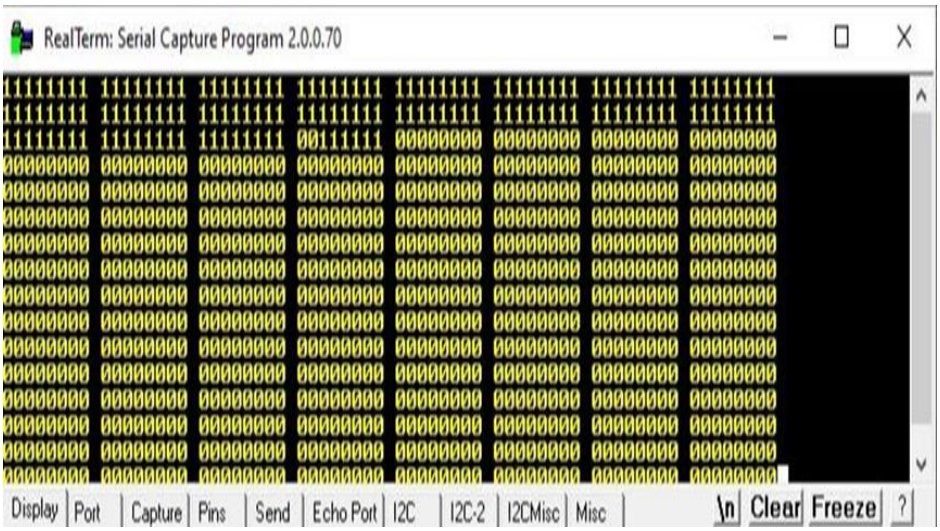

Image 5.23. *The result of the experiment with 60º phase-shifted clocks*

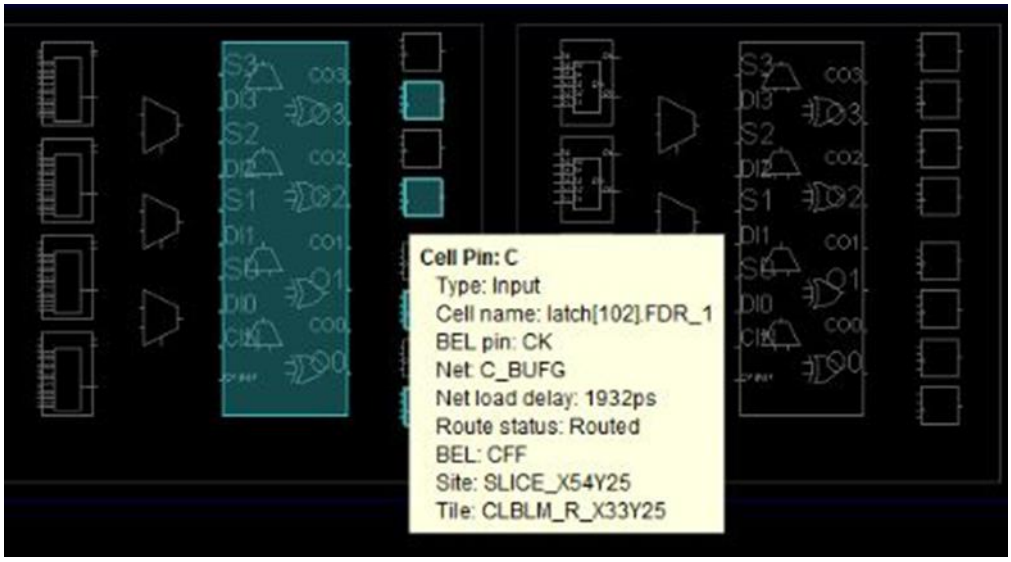

Image 5.24. *The net load delay of the latch 102*

The net load delays of the latch 158 and latch 175 can be seen in Image 5.25 and 5.26, respectively. The traveling time of the stop signal to the latch 158 is 1950 ps as seen in Image 5.25. And this traveling time for the latch 175 is 1952 ps which is nearly the same as the latch 158. Every experiment time interval difference was 416 ps and result in at most 26 carry delay elements. The net load delays of these elements are different with at most 5-6 ps. But the net load delay difference between latch 102 and 175 is 20 ps. This net load time difference is mainly responsible for the difference in the number of the delay lines propagated through by the start signal. Since the net load delay of the latch 175 is 20 ps more, a few more carry delay elements than the normal may be propagated through by the start signal. Therefore, after an experiment with 416 ps time duration difference is done, a closer time interval should be tested. Because the net load delay is nearly similar in the neighborhood latches. The experiments can be done for all delay elements to establish an equation to measure the time in a very accurate way. But four more experiments with 90º, 105º, 120º phase-shifted clocks will be done to determine one carry delay element propagation delay and test the tapped delay line which is aligned in the upward direction in the FPGA chip as shown in Image 5.5.

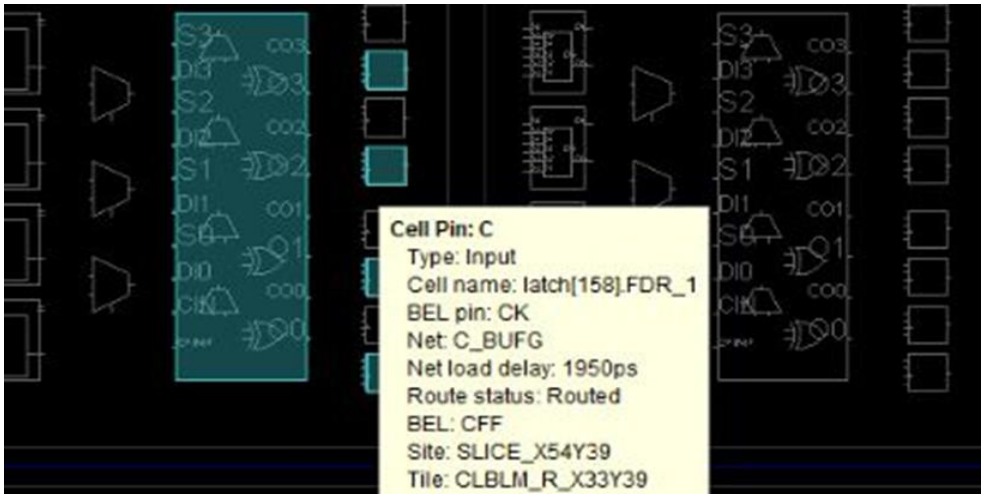

Image 5.25. *The net load delay of the latch 158*

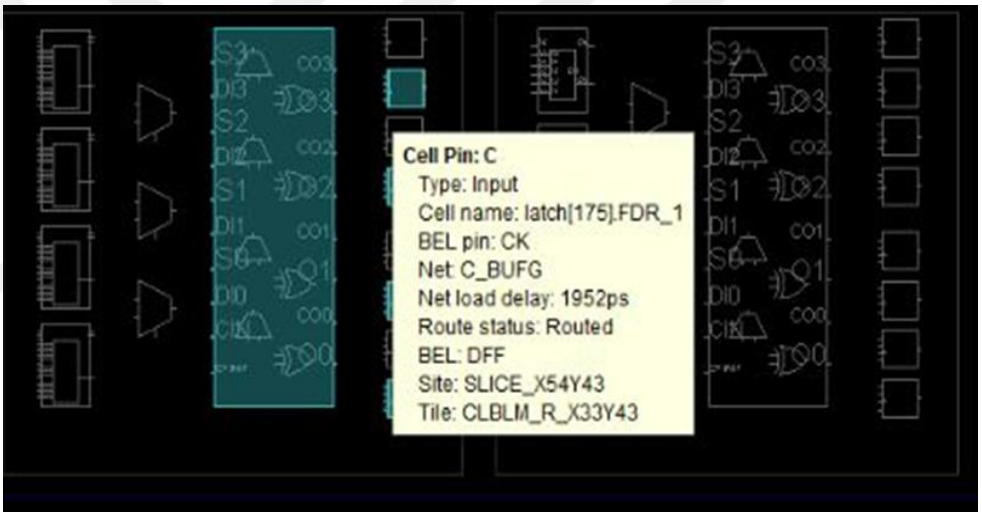

Image 5.26. *The net load delay of the latch 175*

The result of the experiment with 90º phase-shifted clocks is shown in Image 5.28. The number of ones on the screen of the Realterm program is 202. It is 184 in the experiment with 75º phase-shifted clocks as can be seen in Image 5.27. Therefore, there are 16 more carry delay elements. There is a 416 ps time difference between 75º and 90º phase-shifted clock experiments. 18 carry delay element corresponds to a 416 ps time delay. If 416 is divided by 18, one carry element propagation delay of 23.1 ps is attained. But there is a problem with this propagation delay. Because the calculated propagation delay of this experiment is deviated much. It will be investigated in this section.

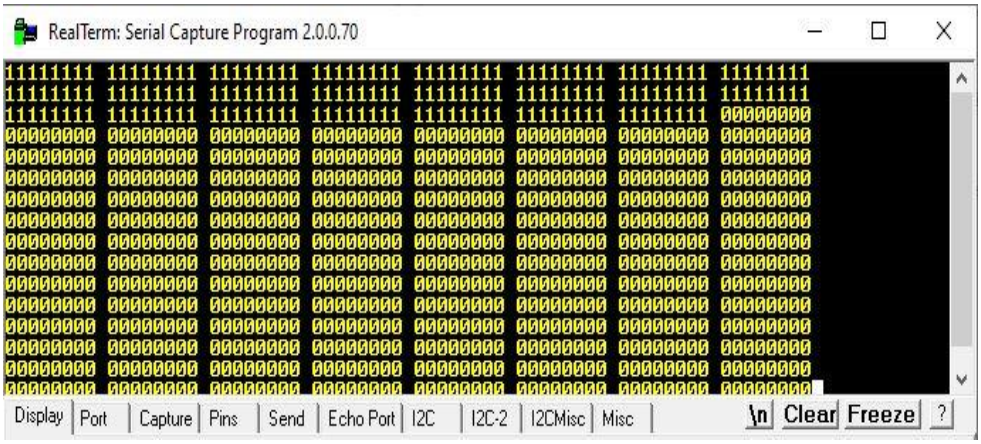

Image 5.27. *The result of the experiment with 75° phase-shifted clocks*

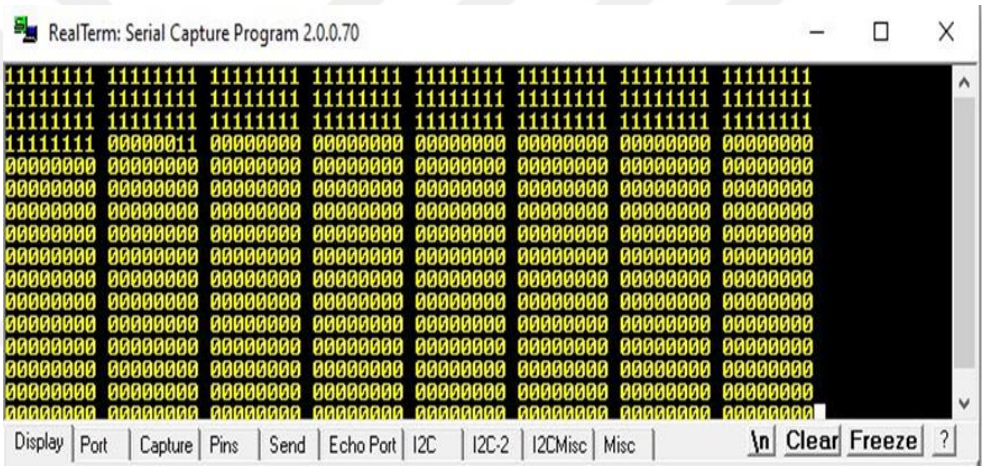

Image 5.28. *The result of the experiment with 90° phase-shifted clocks*

The 1-2 ps deviation of the propagation delay of one carry cell in the experiments with 60º and 75º phase-shifted clocks results from the net load delay of the CLK pin of the D latches as explained a few pages ago. 23.1 ps propagation delay can result from net load delay again. The 90 º phase shift increases the number of carry delay elements from 184 to 202. Therefore, the net load delays of D latches of this region should be investigating. The net load delay of the CLK pin of the latch 199 is 1953 ps as can be seen in Image 5.29. The ned load delay of the CLK pin of the latch 200 is 1780 ps as can be seen in Image 5.30. They are neighbors but there is 173 ps difference in net load delays. This difference in adjacent delay cells was 1-2 ps at most in the other experiments. The reason behind this huge net load delay difference is investigated. It is found that, the latch 199 is located on the X0Y0 clock region while the latch 200 is located on the X1Y1 clock

region. Therefore, the transition from a clock region to another can cause timing problems because of the net's routes in the FPGA chip. Thus, examining the tapped delay line with 416 ps time duration increment is a good idea to build a precise FPGA TDC. Experiments will be done with 105º and 120º phase-shifted clocks to test the hypothesis for the deviation of the propagation delay of one carry delay element is true or not. In addition to those experiments, an experiment with 125º phase-shifted clocks will be done to find a propagation delay of one carry delay element as close as possible.

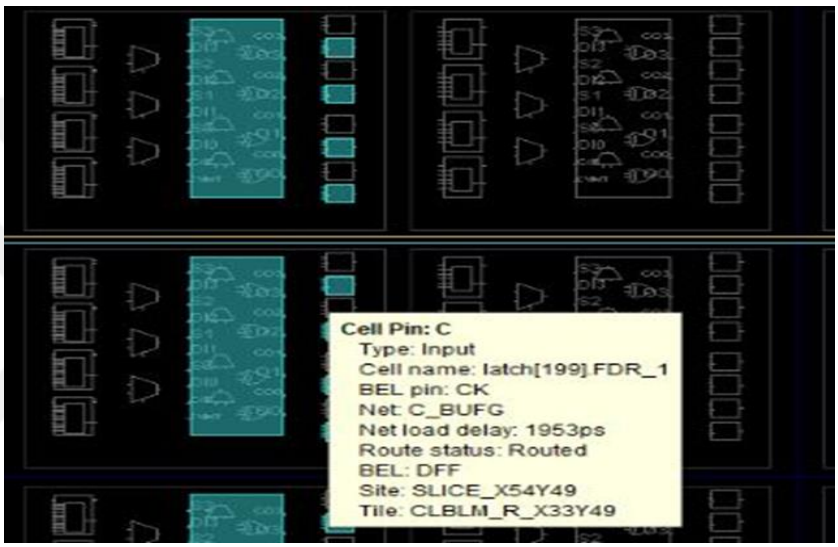

Image 5.29. *The net load delay of the latch 199*

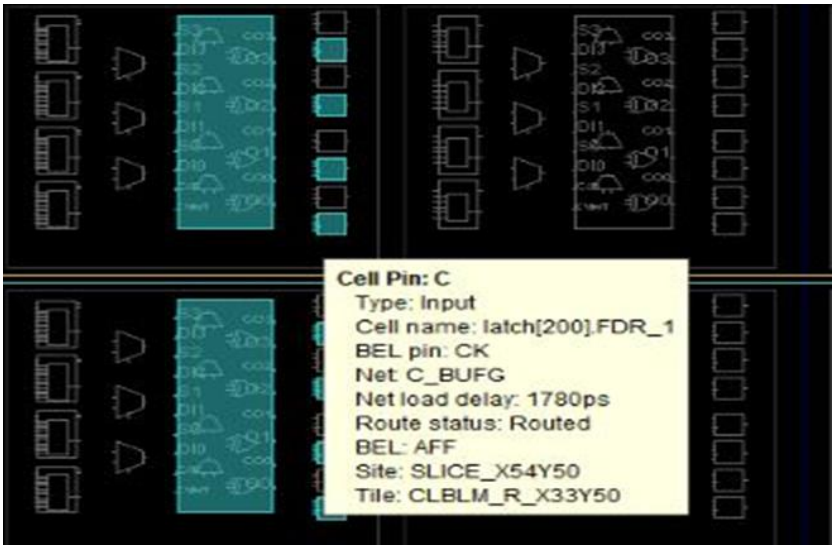

Image 5.30. *The net load delay of the latch 200*

The results of the experiments with 105º and 120º phase-shifted clocks can be seen in Image 5.31 and 5.32, respectively. The net load delays of D latches which are located on the border of the clock regions are affected greatly as shown before. So, the number of an excess carry delay element of the 90º phase-shifted experiment was 18. But that number was 26 for the experiment with 75º phase-shifted clock. If the deviation in the number of carry delay elements is caused by only the transition region of the clocks then the experiment with 105º and 120º phase-shifted clocks will give results like in previous experiments such as 22,24,26. There are 24 more carry delay elements in the experiment with the 105º phase-shifted clocks compared to 90º phase-shifted clocks. The result is not 18 more carry delay elements. Therefore, the reason behind the deviation in numbers is net load delay differences. There are 23 more carry delay elements in the experiment with the 120º phase-shifted clocks compared to the experiment before it. 23 carry delays correspond to 18 ps propagation delay of one carry delay element.

The result of the experiments showed that one carry delay element propagation delay is between 16 ps and 18.9 ps which changes according to the net load delays. But the resistance to the temperature changes should be investigated to make the FPGA TDC more stable. The only temperature resistance done for this thesis is to reprogram the FPGA after leaving the FPGA works a few hours. For instance, the experiment with 75º phase-shifted clocks is repeated one day later. There were two more carry delay elements. It corresponds to 36 ps time error. It is negligible because it corresponds to a 0.5 cm distance error. As explained before, it is not a simple calculation that the fine time measurement can be done by multiplying one carry delay element propagation delay by the total number of the carry delay elements. Because the propagation delay of the carry delay elements can change according to the location, temperature, power supply noises. Thus, an equation should be established to give time calculation of tapped delay line or a lookup table should be made which shows the corresponding time concerning the number of the carry delay elements. Since the components before FPGA TDC cause a time delay, the time interval to measure is not below ns. Tapped delay lines are used with the clocks of the FPGA in synchronization. In this way, FPGA TDCs can measure up to microseconds or milliseconds. A method is introduced in the next page showing how to synchronize the clocks and the tapped delay lines to make and FPGA TDC.

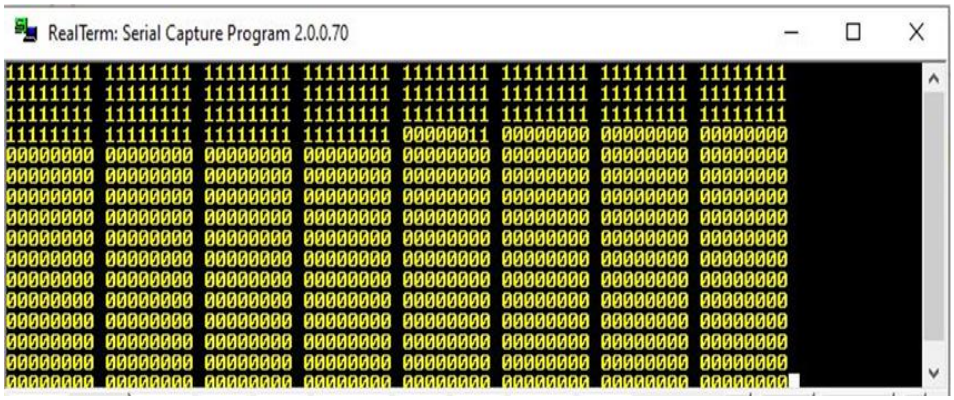

Image 5.31. *The result of the experiment with 105° phase-shifted clocks*

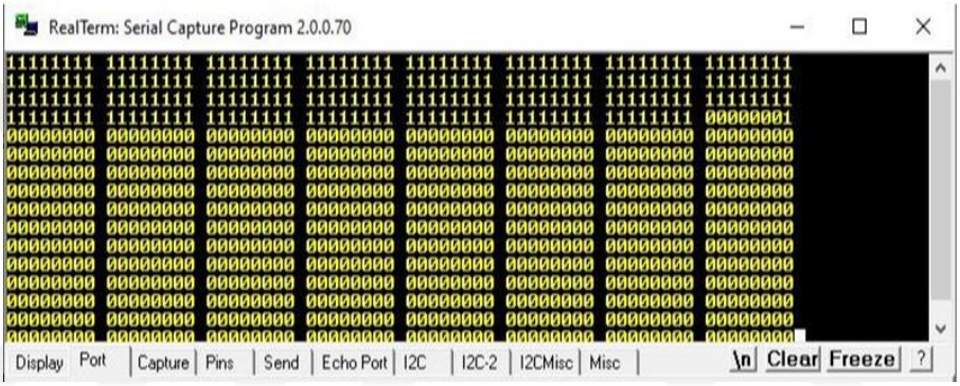

Image 5.32. *The result of the experiment with 120° phase-shifted clocks*

5.3.5. Nutt interpolation method

A method called the Nutt interpolation can be used to synchronize the clocks with tapped delay lines. The schematic of the Nutt interpolation method is shown in Figure 5.5.

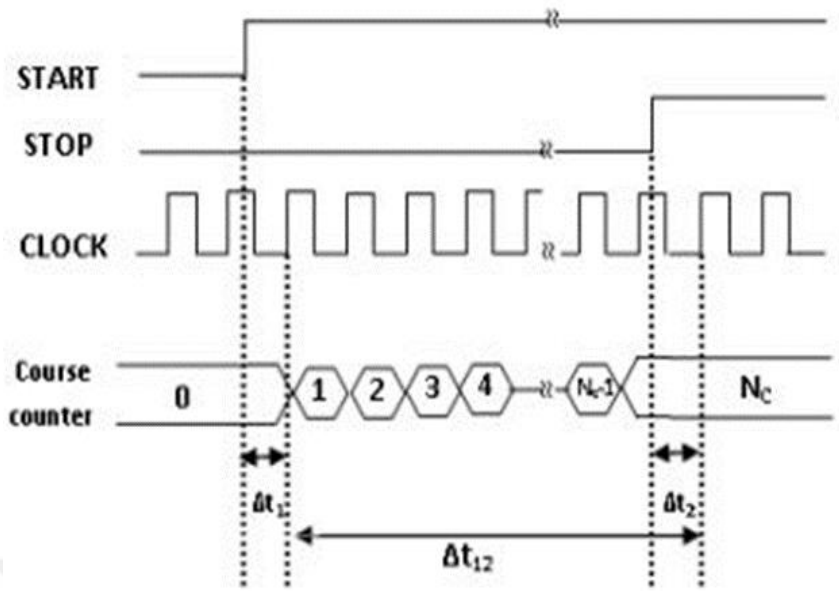

Figure 5.5. *The Nutt interpolation method for FPGA TDC* [73]

The start pulse triggers the FPGA TDC to start measuring the time until the stop signal comes. There will be two tapped delay lines used for this method. One tapped delay line is triggered by the start signal and stopped by the rising edge of the clock. Therefore, a fine time between the start signal and the first rising edge of the clock is measured. Then the clock starts counting until the stop signal comes. The time passed in this clock counter duration can be calculated by multiplying the clock period time by the counted number. After the stop signal arrives at the FPGA TDC, it triggers the second tapped delay line to measure the second fine time. The second triggered tapped delay line is stopped by following the rising edge of the clock. Therefore, all the time intervals can be measured by this method. The Equation to measure the time interval between the start and the stop signals with this method is shown in Equation 5.2. FT1 and FT2 are the first and second fine time measurements, respectively. N is the counted number by the clock and Tc is the clock period.

$$Time\ measured = FT1 + (N\ x\ Tc) - FT2 \tag{5.2}$$

The constructed first tapped delay lines in the FPGA chip for the first and second fine time measurements can be seen in Image 5.33. It is not so proper because tapped delay lines are in several clock regions. But an equation can be established to correct the

clock skews. The color of the tapped delay line on the right is red because the first carry4 block of the tapped delay line is fixed to a location that closes to the first delay lines.

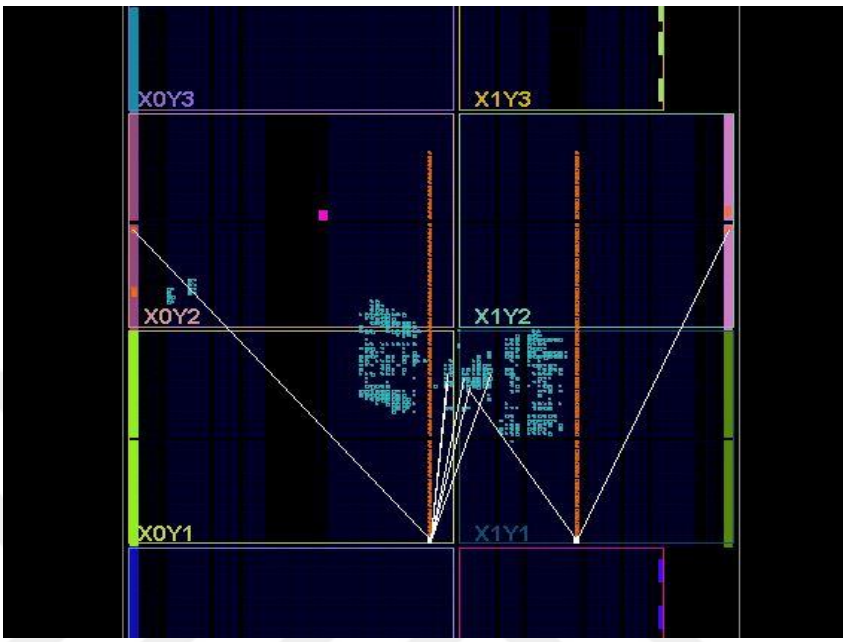

Image 5.33. *The constructed two tapped delay lines for Nutt interpolation method*

The used clock frequency is 200 Mhz and its period is 5 ns. According to experiments, 5ns corresponds to 288 carry delay elements. Therefore 288 carry delay elements are constructed. Two equations are established. One of them is for the first tapped delay line and the other is for second tapped delay lines. Equations determine fine times for start and stop signals according to the number of delay lines. A coarse counter with 200 Mhz clock is constructed with D latches. The counter counts in synchronization with fine times. The time resolution is below 500 ps. The only thing which should be improved is the rising edge of the clock and start, stop signal's coincidence. If the start and stop signal times correspond to the rising edge of the 200 Mhz clocks, the coarse counter may count one more. Therefore, a time measurement error may occur.

6. CONCLUSION

The main goal of this thesis was to investigate how to design a LiDAR system. As a result of the researches, a LiDAR structure as in Figure 6.1 has emerged. A fast laser diode, the laser diode driver circuit, avalanche photodiode seen in the LiDAR structure in Figure 6.1 can be purchased easily. But it has been understood that laser diode and photodiode selection is important for LiDAR systems. The selected laser diode must meet the IEC 60825 standard for the safety of laser products to ensure that the laser diode will not harm to the human eye. Laser pulses should be short and peak output power should be high to increase the range of LiDAR systems. Rise and fall times of laser diode and photodiode should be a few ns or below. Because time is very critical for LiDAR systems. The OSRAM SPL PL90_3 laser diode is found suitable for the targeted LiDAR system. Because the Laser diode has 90 W peak output power, 1 ns rise and fall time. And it is suitable for short laser pulses from 1 ns to 100 ns. The shorter the laser pulses, the lower the time measurement error known as the walk error described in Section 4.2. To increase the measurement distance, it has been found appropriate to use an avalanche photodiode in the targeted LiDAR system. Since avalanche photodiode amplifies noises too, an optical filter suitable for the wavelength of the laser should be in front of avalanche photodiode. The Marktech MTAPD-07-015 avalanche photodiode is found suitable for the targeted LiDAR system. Because it has an optical filter for 905 nm wavelength which is the wavelength of the selected laser. One reason for the preference of this avalanche photodiode is that it has typically 0.4 nA dark current even with 100 multiplication factors. It increases the signal to noise ratio (SNR) a lot. One another reason to select this avalanche photodiode, it has 1.2 ps capacitance and 0.6 ns rise time. It is found that peak responsivity wavelength of the photodiode and laser diode should be matched to attain maximum current from the photodiode and increase the maximum measurable range. Plano-convex lenses are found suitable to use. Because they collimate diverged laser diode output light and focuses the returned signal to the photodiode in an efficient way.

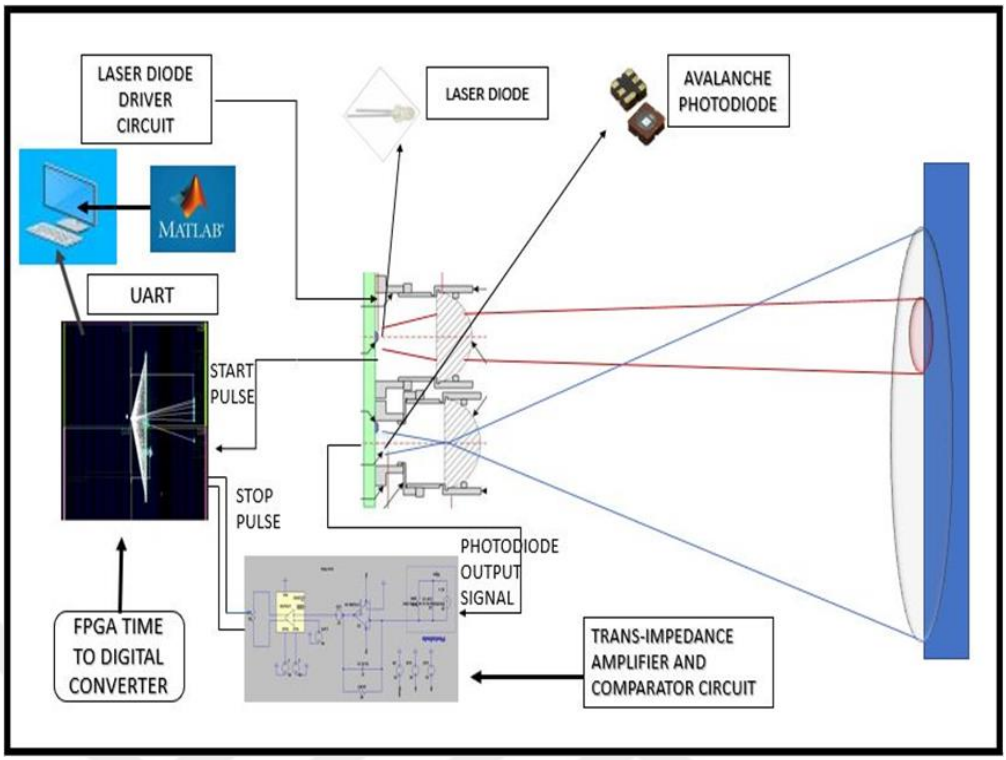

Figure 6.1. *The targeted LiDAR structure*

LiDAR bases on a very sensitive time measurement. The laser light travels in the air until it hits an object and then it is reflected towards the receiver circuit. 1 ns time of flight of the light corresponds to 30 cm. Since the light travels the same distance twice. 1 ns measured time corresponds to 15 cm. Therefore even 1 ns time calculation error results in a 15 cm distance measurement error. It is understood when studying on time of flight measurements that it is important to determine the processing time of the circuit behind the photodiode precisely. There is a trans-impedance amplifier circuit after photodiode in the receiver circuit to amplify the small photodiode currents to a processable voltage value. The opamp selected for the trans-impedance amplifier is LTC6268-10. Although LT6268-10 has 1500 V/μs slew rate and 4 GHz gain-bandwidth product, the propagation delay is more for small photodiode currents. For instance, if the output current of the photodiode is 1.4 μA as in the simulation of Figure 4.12. The time needed for the trans-impedance amplifier to amplify that current to the determined threshold of 25 mV is 3.47 ns. For 5.2 μA photodiode current, this time value is 1.6 ns as can be seen in Figure 4.13. Therefore, the time error is 1.87 ns which is unacceptable. The time error corresponds to 28 cm error if other components result in additional time error. But for relatively high

photodiode output currents, propagation delay difference is low. For example, the time needed for the trans-impedance amplifier to amplify that current to the determined threshold of 25 mV is 3.47 ns for 15.1 μA photodiode current in Figure 4.14. The time was 1.6 ns for 5.2 μA so the time difference is 270 ps. The objects in the short-range cause high photodiode current while objects in the long-range cause low photodiode current. Therefore, according to simulation results in Figure 4.12,4.13 and 4.14, the time error of the trans-impedance amplifier is more for long-range measurement.

A comparator circuit follows the trans-impedance amplifier in the receiver of LiDAR as can be seen in Figure 4.10. The comparator circuit compares the output voltage of the trans-impedance amplifier to a threshold voltage to create a stop signal for FPGA TDC to finish the time of flight calculations. The selected comparator opamp is LTC6754 is a low propagation delay with 1.8 ns. It also has a low overdrive dispersion of 1ns from 10 mV to 125 mV. The propagation time difference for 10 mV and 125 mV input overdrive voltages is 1 ns as shown in the simulations in Chapter 4. The selected comparator is compatible with LiDAR systems since it has low overdrive dispersion. Another comparator TLV3501 which is used LiDAR systems has 5 ns overdrive dispersion for 5 mV and 100 mV input overdrives. 6.49 ns time is elapsed in Figure 4.12 simulation between the signal appears on a photodiode with 1.4 μA current and comparator output voltage's %50 value. The time is 3.7 ns for 5.2 μA photodiode current and 3.1 ns for 15.1 μA photodiode current as can be seen in figures 4.13 and 4.14, respectively. There is 3.39 ns time difference. Therefore 3.39 ns time calculation error. It corresponds to approximately 50 cm of distance measurement error. As a result, with these simulation results, significant time calculation errors arising from electronic circuits were detected. Another important error is observed in the simulation results. An error called walk error occurs due to different reflectivities of targets as shown in Figure 4.6. To interpret these time errors of electronic components of LiDAR and walk error, a high-speed analog to digital converter (ADC) or fast peak detector circuits can be used as a future study. The output voltage of the trans-impedance amplifier can be connected to a ADC or fast peak detector circuit to calculate the photodiode current. If a photodiode current can be guessed, an equation that shows the time error can be established and this time error is substracted from total calculated time in the FPGA TDC to find the true time of flight time.

An FPGA TDC is designed in this thesis for the time of flight calculations. The tapped delay line method is used. Carry4 blocks are implemented as delay elements. In the first experiments, a constructed tapped delay line is tested with ordinary jumper cables. The number of the delay elements which propagated through by the start signal before the stop signal comes are counted by a decoder and sent to the computer using the UART protocol. A signal is given to two cables. One of them is start cable and the other is stop cable. By changing the stop cable length, the number of ones is observed on the screen of the Realterm program. As the stop cable length is increased, it is observed that the number of ones on the screen increase. Therefore, the experiments show that constructed delay lines are work. Since the velocity factors of jumpers are not the same and the cables are not calibrated, the exact resolution of time measurement did not be determined by these experiments.

To be able to determine the propagation delay of one carry delay line element and time measurement resolution of constructed tapped delay lines. Other experiments have done. Two 100 Mhz phase-locked loop (PLL) clocks are generated in the FPGA using Vivado Design Suite IDE. In every experiment, the phase of the second clock is incremented by 15º. 15º phase shift corresponds to 416 ps time delay. For 416 ps time delay,23 new carry elements have appeared on the screen. So, one carry delay element propagation delay is approximately 18 ps. But it changes in the different locations of the FPGA chip. A 100 ps resolution for 10 ns range is achieved. The Nutt interpolation method was used to increase the range. A coarse counter is made by a clock and fine time measurement is done by two parallel tapped delay lines which are shown in Image 5.33.

A simple and cheap analog time measurement circuit is designed in chapter 2. It is based on the charging time of capacitors. A simple and inexpensive analog timing circuit is designed in Chapter 2. When the capacitors are filled with a constant current source, the voltage formed on the capacitor per unit time becomes constant. The designed circuit is simulated by the LTspice simulation program. A 100 ps time measurement resolution is observed. 100 ps time interval causes approximately 0.9 mV voltage difference on the capacitor. It is measurable with cheap ADCs, but it needs buffer before the capacitor. The circuit shows good linearity as shown in figures 2.21 and 2.24. 30 ns time interval is measured at most in these simulations. But it can measure longer time intervals. The only limitation is the measurable voltage value on the capacitor.

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