

ENHANCED DIRECT QUADRATURE CONTROL IMPLEMENTATION FOR A THREE-PHASE INVERTER

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By
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January 2025

Enhanced Direct Quadrature Control Implementation for A Three-
Phase Inverter

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January 2025

We certify that we have read this thesis and that in our opinion it is fully adequate,
in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

ENHANCED DIRECT QUADRATURE CONTROL IMPLEMENTATION FOR A THREE-PHASE INVERTER

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Power electronics is widely utilized in various fields, such as the military, daily life, and industry. The efficiency of power conversion applications is important. Three-phase inverters are primarily used in motors and UPS systems. However, the design of a three-phase inverter requires advanced knowledge of software, hardware, and algorithms. The digital control of the three-phase inverter provides flexibility for the adjustment of output voltage and frequency. The combination of Sinusoidal Pulse Width Modulation (SPWM) and Direct Quadrature (DQ) control increases the stability of output voltage.

In this thesis, we present an implementation of a three-phase voltage source inverter using the Digital Signal Processor (DSP) based controller of TMS320F28379D. There are three electronic cards in the system. The first card includes Switched-Mode Power Supplies (SMPS), current sense circuits, and three half-bridges using discrete MOSFETs. The second card comprises of a low-loss filter and a voltage sensing circuit. The input voltage of the three-phase inverter is 30 V, and the output is a three-phase inverter with an output voltage that can be adjusted up to 12 V with an output frequency of 50 Hz. The maximum power of the inverter is 98.5 W. The efficiency of the inverter is 90.72 % at the full load.

Keywords: DSP in three-phase inverter, LCL filter, DQ control, SPWM, voltage source inverter.

ÖZET

ÜÇ FAZLI İNVERTÖR İÇİN GELİŞMİŞ DİREKT DÖRTLÜ KONTROL UYGULAMASI

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Güç elektroniği, askeri, günlük yaşam ve endüstri gibi çeşitli alanlarda kullanılmaktadır. Güç dönüştürme uygulamalarının verimliliği önemlidir. Üç fazlı invertörler büyük ölçüde motorlarda ve UPS sistemlerinde kullanılmaktadır. Ancak, üç fazlı invertörün tasarımı için, yazılım, donanım ve algoritma konusunda gelişmiş bir bilgi gerekmektedir. Üç fazlı invertörün dijital kontrolcü ile kontrol edilmesi, çıkış voltajı ve frekansının ayarlanması için esneklik sağlamaktadır. Sinüzoidal Darbe Genişlik Modülasyonu (SDGM) ve Direkt Dörtlü kontrolünün birleşimi, çıkış voltajının kararlılığını artırmaktadır.

Bu tezde, TMS320F28379D DSP'sini kullanarak üç fazlı invertörün bir uygulamasını sunuyoruz. Sistemde üç elektronik kart bulunmaktadır. İlk kart, ayrı Metal Oksit Yarı İletken Alan Etkili Transistörler kullanarak üç yarım köprüyü, anahtarlama güç kaynaklarını ve akım okuma devrelerini içermektedir. İkinci kart, düşük kayıplı filtre ve voltaj okuma devresinden oluşmaktadır. Üç fazlı invertörün giriş voltajı 30 V ve çıkış voltajı 12 V'a kadar ayarlanabilmektedir ve frekansı 50 Hz'dir. Invertörün maksimum gücü 98.5 W'tır. Invertörün verimliliği tam yükte %90.72'dir.

Anahtar sözcükler: Üç fazlı invertörde DSP, LCL filtre, DQ kontrol, SDGM, gerilim kaynaklı invertör.

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Chapter 1

Introduction

1.1 Power Electronics

Power electronics technology is employed in every aspect of life to illustrate the efficient charging of smartphones and laptops, home appliances, industrial machines, rail systems, and renewable energy. The improvement in efficiency and reliability is significant for power electronics. While designing a power electronic system, engineers should meet the requirements of voltage, current rating, thermal management, stability, and electromagnetic compatibility. Besides these, there should be some protection circuits in case of dangerous situations such as over-voltage and short-circuit [1].

Power electronics primarily consist of four types of conversion, including AC-DC converter, DC-DC converter, DC-AC, or AC-AC. AC-DC and DC-DC converters are considered to be switching mode power supplies. DC-AC and AC-AC converter are called inverters. The most common inverter is DC-AC, which converts direct current (DC) into alternating current (AC).

1.2 Inverters

Inverters are crucial for applications where AC output is required, such as in residential and commercial electrical systems, renewable energy installations, and various electronic devices. Modern inverters are designed for high efficiency. Although there is no clearly aimed efficiency in inverters, it is generally higher than 90 %. As the efficiency decreases, the operational cost and heat dissipation problems occur. Therefore, it is important to maintain high efficiency. The Total Harmonic Distortion (THD) is another critical concept in inverters. It quantifies the level of distortion at the output waveform, which arises from the harmonic frequencies. According to IEEE Standard 519-2014, the THD of the voltage should be restricted to less than 5 % for harmonic components up to the 49th order [2]. THD is highly dependent on the modulation technique, switching frequency, and low pass filter of the inverter.

The control algorithm of an inverter is significant for achieving the desired output. In inverters, there are advanced control algorithms such as Space Vector Modulation (SVPWM) and Sinusoidal Pulse Width Modulation. These algorithms generally monitor the output voltage and/or output current and create the switching signals accordingly. SPWM is the most popular technique, and it is widely used in industry. Although SVPWM demonstrates a distinct advantage over SPWM at low switching frequencies, the performance difference between these two techniques becomes smaller as the switching frequency increases since THD decreases considerably with an increasing switching frequency [3], and both SVPWM and SPWM can satisfy the requirements of THD specified by IEEE standard. In this thesis, the sinusoidal pulse width modulation technique is used.

There are two types of inverters: voltage source inverters and current source inverters. In the voltage source inverter, there is a restricted control of the output voltage while in the current source inverter, the output current is controlled. In the voltage source inverter, the working of the inverter should be independent of the load connected to the inverter. Uninterruptible power supplies and adjustable speed drivers are designed using voltage source inverters.

Voltage source inverters are effectively utilized in both single-phase and three-phase systems. Single-phase voltage source inverters use both half-bridge and full-bridge configurations. Three-phase voltage source inverters are generally employed in applications that require sinusoidal voltage waveforms and high power. Voltage source inverters can function in two modes: stepped wave or square wave mode and pulse width modulation mode. The square wave mode provides simplicity in operation, whereas the PWM mode results in a higher-quality output waveform [4].

The output voltage of an inverter can be adjusted by either changing the input DC voltage while keeping the inverter's gain constant or by altering the inverter's gain while maintaining a fixed DC supply voltage. When the DC supply voltage is maintained constant, the output voltage is modulated by adjusting the inverter's gain using the pulse width modulation technique [4]. In this thesis, the sinusoidal pulse width modulation technique is applied. The topology is elaborated in the next chapter.

The controller of inverters plays a significant role in the output quality, as the performance of an inverter substantially depends on the controller. The digital controllers are widely adopted in inverter applications. DSPs are especially well-suited for inverter applications because they can offer a superior computational performance for the real-time signal processing [5]. In this thesis, the DSP of TMS320F28379D from a member of the C2000 series from Texas Instruments is used. Further details regarding the specifications and functionalities of this DSP are presented in the following sections.

There are several notable studies that attract attention. These works mainly focus on a specific target, such as significantly enhancing efficiency, or they try to benefit from new technologies such as GaN transistors. A summary of these impactful studies is provided below.

The work [6] designs a GaN (GS66516T) based two-level three-phase inverter with a high power density. The rated power of this inverter is 10 kW with a power density of 17.5 kW/L. This design increases the switching frequency to

decrease the size of the system. They design a compact PCB so that the parasitic inductance and capacitance can be minimal. Therefore, the overshoot at the drain-to-source voltage is only 10 % of the bus voltage. The hardware design of the inverter considers the noise issues. They have three different grounds, namely DSP ground, inverter signal ground, and power ground. This isolation helps eliminate electromagnetic interference (EMI) problems.

Another work is [7]. This work presents a 50-kW SiC two-level, three-phase voltage source inverter. A commercial SiC power module, Wolf-speed CAS120M12BM2, is used in the design. There is a gate assisted circuit between the gate and source terminals of the power modules. This circuit reduces the switching loss and ringing of voltage and current. In addition, they benefit from the advantages of SiC using high switching frequency. At the high switching frequency, the dead time becomes substantially important. They perform a comparison between the dead time of 250 ns and 550 ns. When the dead time is 250 ns, The fifth and seventh-order harmonics reduce considerably.

Different work is [8] that uses a vertically stacked busbar design with SiC power modules CAS120M12BM2. They employ a high switching frequency. Therefore, This design aims to minimize the stray inductance. In addition to this, there are other benefits of busbar design, such as its capability to conduct high currents. The DC-link capacitors are equally divided at each phase along the busbar, which makes the parasitic power loop inductance of each phase equal. This special arrangement of DC-link capacitors requires a smaller amount of decoupling capacitors since DC-link capacitors offer a conductive path for currents at the switching frequency and its harmonics, and these capacitors also offer a low-impedance route for switching transients.

1.3 Motivation

The motivation of this thesis is to design a three-phase inverter using the DSP of TMS320F28379D. The three-phase inverter has the output of 12 V peak phase voltage with a frequency of 50 Hz. This system is designed for the purpose of balanced loads, such as motors. The three-phase inverter is designed such that it can work with a 28 V battery as a source. Although the mid-point voltage of this type of battery is generally 28 V, the battery voltage is increased to approximately 30 V as it is charged. The output quality decreases with a higher input voltage since the harmonic distortion increases. Therefore, the design must be carried out with an input voltage of 30 V. In the control algorithm, the combination of DQ and SPWM is used to increase output quality and efficiency. A low-loss filter called LCL filter is designed to attenuate the high-order harmonics. The simulation of the control algorithm and the low-loss filter is aimed at conducting. The over-voltage and over-current protections are also designed in case of any undesirable situation, such as a short-circuit at the output. The manufacturing and testing of the three-phase inverter are carried out.

1.4 Thesis Outline

This thesis discusses the design of a three-phase inverter using a DSP controller with an advanced control algorithm.

In Chapter 2, the topology of SPWM is discussed. The design of PCBs and selected components are explained. The simulations of the circuits are performed to validate the designed circuits.

In Chapter 3, the digital controller is explained. The selected DSP is introduced. The development board, which includes the specified DSP, is presented. The peripherals, such as ADC and ePWM, are introduced, and the implementation of these peripherals is explained. Then, the digital control algorithm is described. The simulation of the digital control algorithm is conducted.

In Chapter 4, the hardware implementation is carried out, and hardware results are examined. The working of protection circuits is demonstrated.

In Chapter 5, the thesis is concluded, and possible future works are discussed.

Chapter 2

Three-Phase Inverter Design

The design of a three-phase inverter requires consideration of various tasks such as the selection of components, efficiency, quality of AC output, and protective features. The selection of transistors such as Insulated Gate Bipolar Transistors (IGBT) or Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET) is the key aspect because it should handle the specified voltage and current without facing any thermal issues. Besides this, the switching loss and the conduction loss should be taken into account. Obtaining a high efficiency is valuable since thermal issues arise from a low-efficiency design. The primary components for the majority of power dissipation are the MOSFETs and the LCL filter elements. Besides the efficiency requirement, it is essential to obtain a high-quality AC output with minimal harmonic distortion, which depends mainly on the LCL filter and the control algorithm. In addition to these, the regulation of voltage and frequency is crucial. Safety issues also come up in power electronics. Therefore, the control algorithm should check the input voltage, phase voltages, and phase currents in case of over-voltage, over-current, or short-circuit situations. The block diagram of the three-phase inverter is exhibited in Figure 2.1.

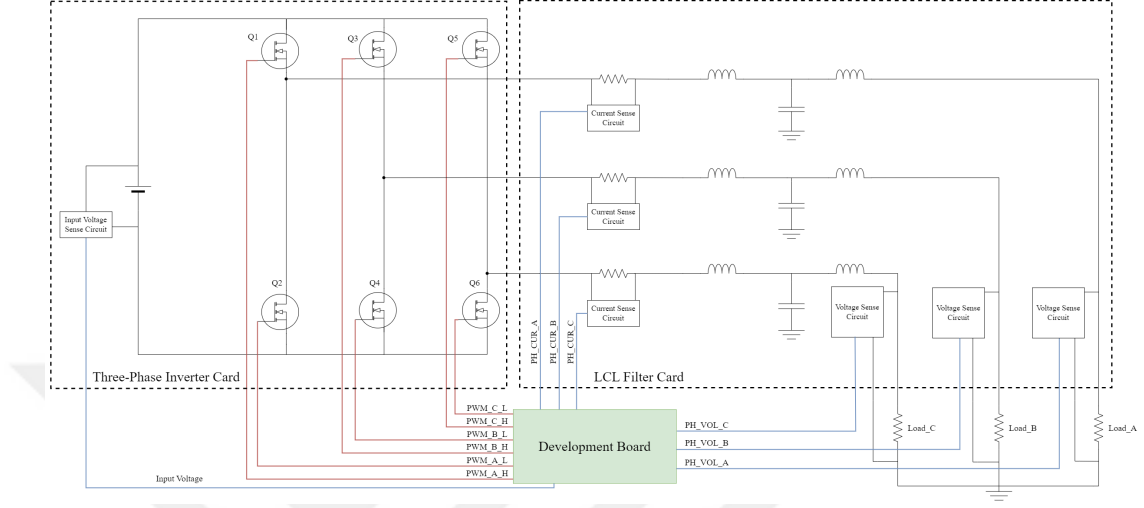


Figure 2.1: The Block Diagram of Three-Phase Inverter

The block diagram shows all the connections in the system. The connections marked in red represent the PWM signals, and the connections marked in blue represent the feedback signals. The schematics of the circuit boards are presented in the subsequent sections.

2.1 Topology

There are numerous inverter topologies, each of which has distinct features. Current Source Inverters (CSI) and Voltage Source Inverters (VSI) are extensively used in power conversion applications. The research concentrates primarily on voltage source inverters. This topology uses the constant DC voltage as a voltage source. By employing the Pulse Width Modulation (PWM) technique, a high-quality AC signal is generated at the output. There are more advanced topologies in inverter applications, such as the Neutral Point Clamped and Cascaded H-Bridge. These are capable of producing improved output waveform and overall efficiency. However, these topologies are challenging to design in terms of circuit design and control algorithm. In addition, the cost of inverters benefiting from these topologies increases substantially. Therefore, it is necessary to specify

the requirements of the inverter and select the topology accordingly.

In this thesis, the voltage source inverter topology is used. The phase voltages are measured, and these measurements are taken as inputs by the control algorithm. The sinusoidal pulse width modulation technique is utilized. Therefore, the DC link voltage needs to be at least twice the peak value of the phase voltage. There are distinct advantages of voltage source inverters over current source inverters. The required DC link capacitor is smaller in VSI. Therefore, the cost is reduced. VSI is also capable of providing better steady-state performance compared to CSI. The switching loss of VSI is higher, but the conduction loss is lower. Hence, as long as the switching frequency is not too high, the total power loss of VSI is lower than CSI [9].

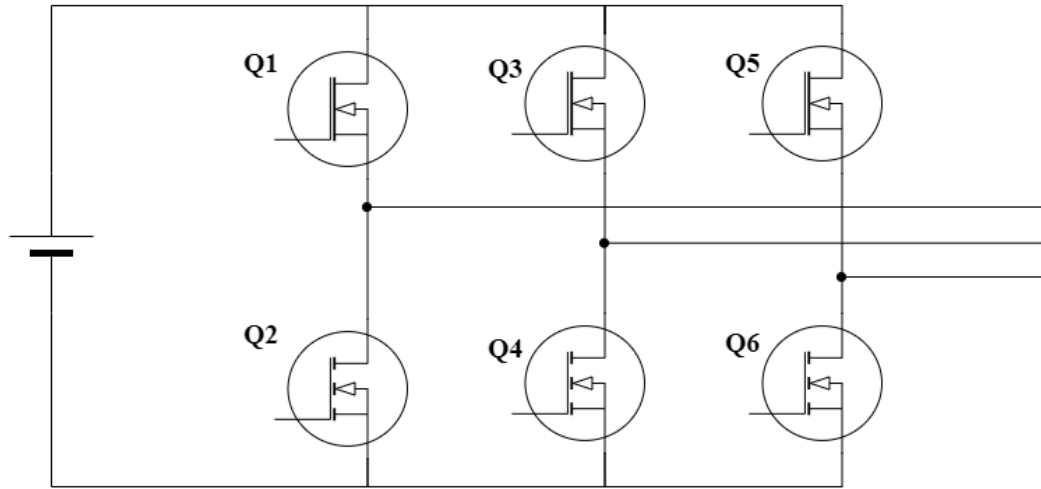


Figure 2.2: Voltage Source Inverter

In the SPWM technique, multiple pulses are generated, and each of these pulses has a different duty cycle according to the magnitude of the sine wave. The carrier wave is a triangular waveform, while the reference wave is sinusoidal. These two waves are compared to produce the pulse width modulation signal. The MOSFETs are switched with the generated PWM signals, and the unfiltered phase signals occur. After filtering these signals, sinusoidal output waveforms

are acquired. The number of pulses for each half-cycle is determined by the ratio between the carrier signal frequency (f_c) to the frequency of the modulating sinusoidal signal (f_m). The frequency of the modulating signal determines the inverter's output frequency (f_o), while the peak amplitude of the modulating signal affects the modulation index (m_a), which specifies output voltage [4].

The amplitude modulation index is defined as:

$$m_a = \frac{V_{\text{control}}}{V_{\text{carrier}}} = \frac{V_c}{V_{\text{carr}}} \quad (2.1)$$

2.2 Three-Phase Inverter Card

The three-phase inverter card includes step-down switching regulators, MOS-FETs, gate drivers, and current sense circuits. This is the main card in the thesis. The selection of each component plays a major role in achieving a high-quality output. The schematic of the three-phase inverter card is provided in Figures 2.3, 2.4, 2.5, 2.6. The gate driver and current sense circuits are the same for phases A, B, and C. In these circuits, additional headers and/or pins are located on the card in case of any problem on the solder layer.

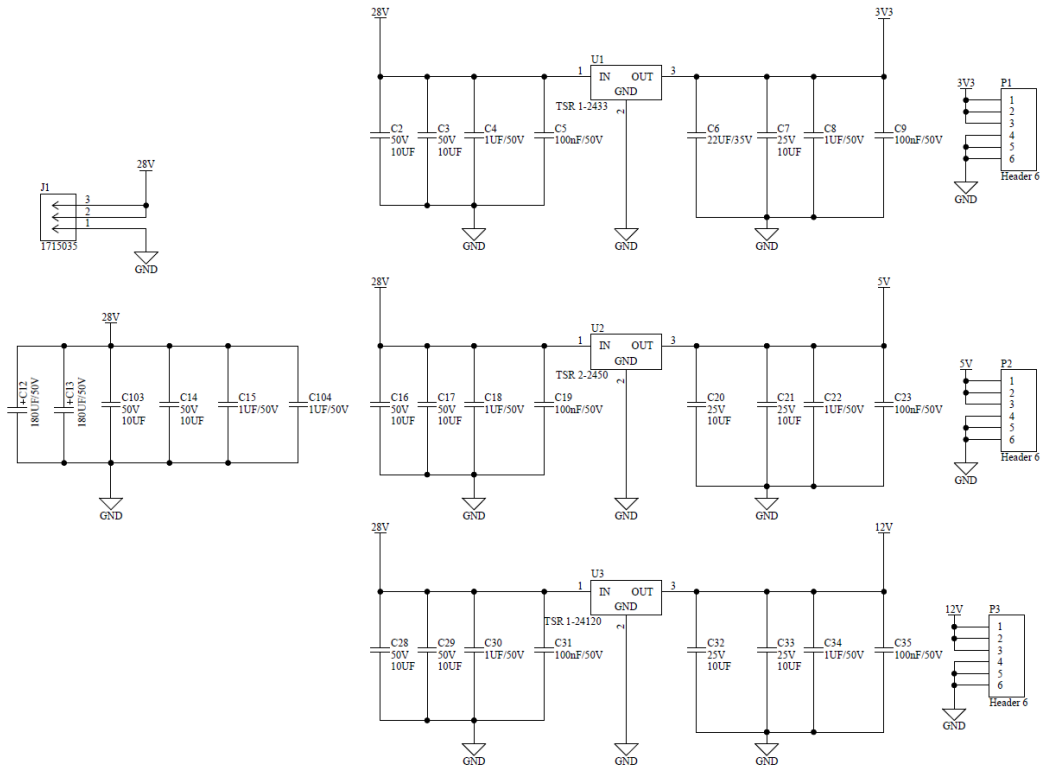


Figure 2.3: Power Architecture of Three-Phase Inverter Card

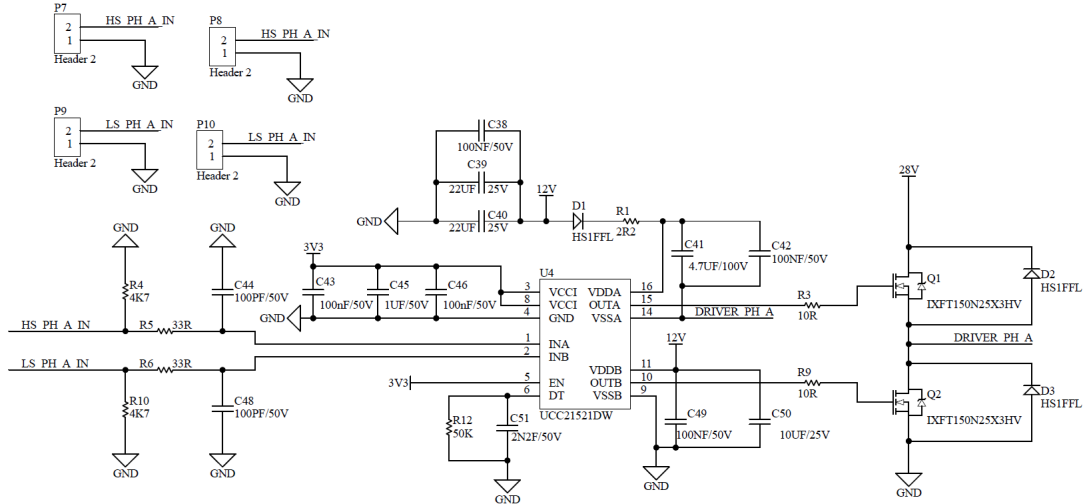


Figure 2.4: Gate Driver Circuit for Phase A, B, C

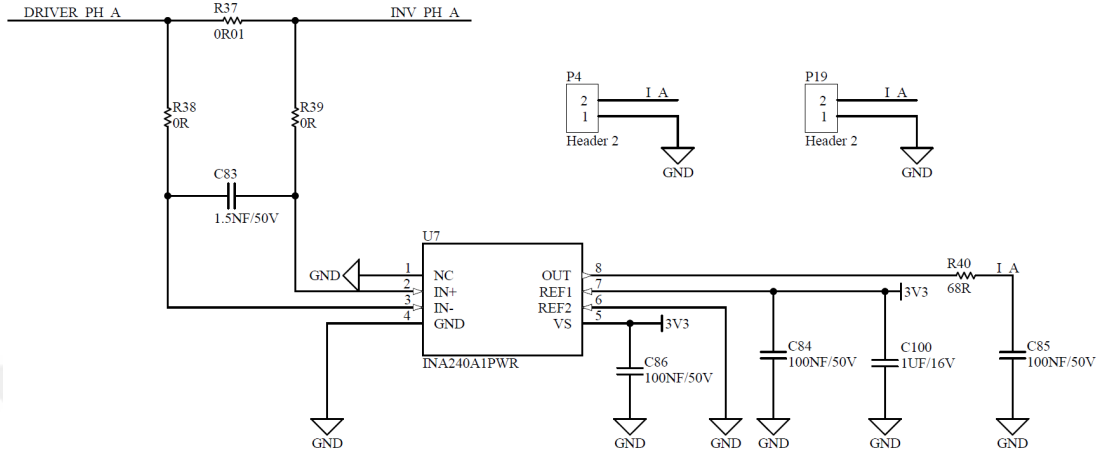


Figure 2.5: Current Sense Circuit for Phase A, B, C

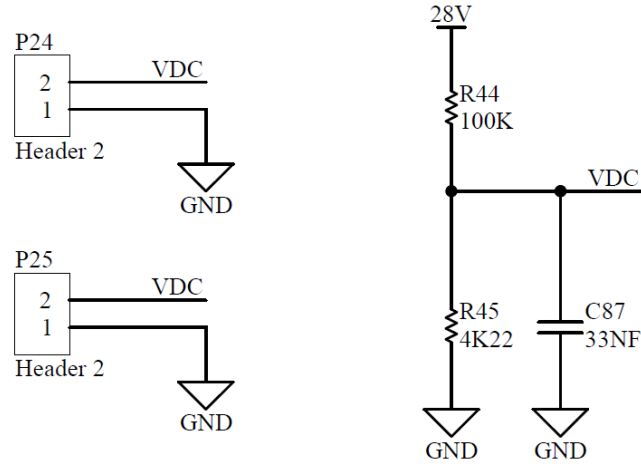


Figure 2.6: Input Voltage Sense Circuit

The component list of the three-phase inverter card is given in Table 2.1.

Component	Designator	Quantity
Ceramic Capacitor, 10 μ F, 50 V, 1206	C2, C3, C7, C14, C16, C17, C20, C21, C28, C29, C32, C33, C103	13
Ceramic Capacitor, 1 μ F, 50 V, 0805	C4, C8, C15, C18, C22, C30, C34, C104	8
Ceramic Capacitor, 100 nF, 50 V, 0603	C5, C9, C19, C23, C31, C35, C38, C42, C43, C46, C49, C53, C57, C58, C61, C64, C68, C72, C73, C76, C79, C84, C85, C86, C89, C90, C91, C92, C97, C98, C99	31
Ceramic Capacitor, 22 μ F, 25 V, 1206	C6, C39, C40, C54, C55, C69, C70	7
Ceramic Capacitor, 1 μ F, 50 V, 0603	C45, C60, C75, C100, C101, C102	6
Aluminum Polymer Capacitor, 180 μ F, 50 V	C12, C13	2
Ceramic Capacitor, 4.7 μ F, 100 V, 1210	C41, C56, C71	3
Ceramic Capacitor, 100 pF, 50 V, 0603	C44, C48, C59, C63, C74, C78	6
Ceramic Capacitor, 10 μ F, 25 V, 0805	C50, C65, C80	3
Ceramic Capacitor, 2.2 nF, 50 V, 0603	C51, C66, C81	3
Ceramic Capacitor, 1.5 nF, 50 V, 0603	C83, C88, C96	3
Ceramic Capacitor, 33 nF, 50 V, 0603	C87	1
Diode, 300 V, 1 A, HS1FFL	D1, D2, D3, D4, D5, D6, D7, D8, D9	9
3 pins terminal connector	J1, J2	2
Header, 6-Pin	P1, P2, P3	3

Component	Designator	Quantity
Header, 2-Pin	P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P24, P25	22
MOSFET, 250 V, 150 A, IXFT150N25X3HV	Q1, Q2, Q3, Q4, Q5, Q6	6
Resistor, 2.2 R, 0.25 W, 1206	R1, R13, R25	3
Resistor, 10 R, 0.4 W, 1206	R3, R9, R15, R21, R27, R33	6
Resistor, 4K7, 0.063 W, 0603	R4, R10, R16, R22, R28, R34	6
Resistor, 33 R, 0.063 W, 0603	R5, R6, R17, R18, R29, R30	6
Resistor, 0 R, 0.1 W, 0603	R8, R11, R38, R39, R42, R43, R47, R51, R52	9
Resistor, 69K8, 0.1 W, 0603	R12, R24, R36	3
Resistor, 100 K, 0.063 W, 0603	R44	1
Resistor, 4K22, 0.1 W, 0603	R45	1
DC-DC Converter, TSR 1-2433	U1	1
DC-DC Converter, TSR 2-2450	U2	1
DC-DC Converter, TSR 1-24120	U3	1
Gate driver, UCC21521DW	U4, U5, U6	3
Current Sense Amplifier, INA240A1PWR	U7, U8, U10	3

Table 2.1: Component List of Three-phase Inverter Card

The 3D appearance of a three-phase inverter card is exhibited in Figure 2.7.

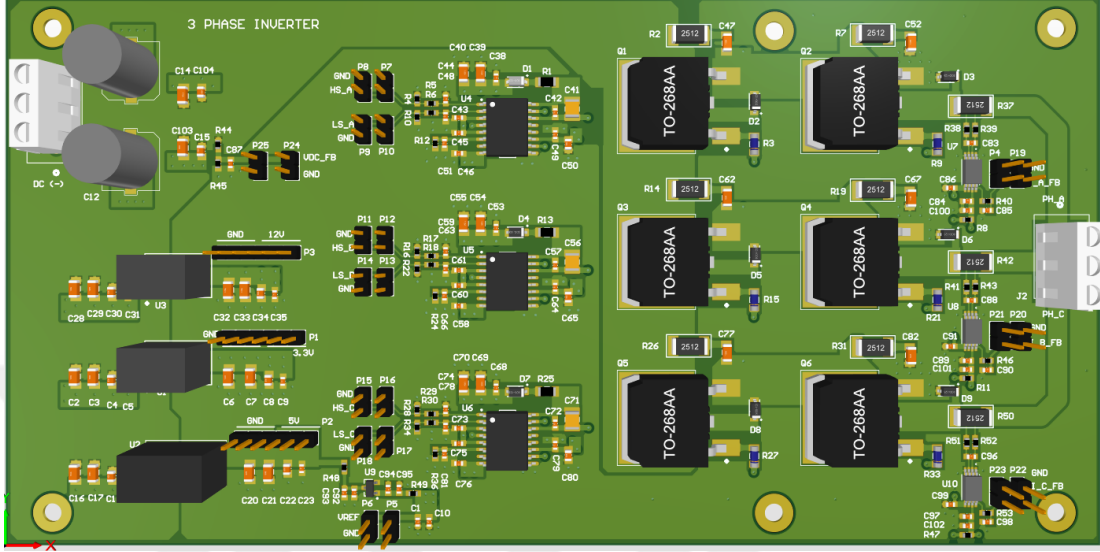


Figure 2.7: 3D of Three-Phase Inverter Card

There is a DC input located on the left side of the card. There are two DC-link capacitors, each of which has a capacitance of $180 \mu\text{F}$ with a voltage rating of 50 V. In the lower-left corner, there are three step-down switching regulators. The first one converts the DC input voltage to 12 V. The second one converts the DC input voltage to 3.3 V, and the third one converts the DC input voltage to 5 V. 12 V is used for supplying the inverter side of the gate driver to switch the MOSFETs. 3.3 V is used for supplying the development board that includes the DSP of TMS320F28379D. 3.3 V also supplies the current sense amplifier of INA240A1PWR. 5 V is used for supplying Op-amps located in the voltage sensing circuit. At the center of the three-phase inverter card, there are three gate drivers. Each one is responsible for controlling two transistors that are high-side and low-side MOSFETs of each phase. Before connecting the phase outputs to the connector, each phase current is sensed with the current sense amplifier. After this, the three-phase output is connected to the output connector. The DC input connector and three-phase output connectors are the same components. The components and circuits are described in the following sections.

In the design of the three-phase inverter card, the layout of the PCB is considerably important because there are two main grounds, namely power ground

and digital ground. The power ground is the reference for the high-power components in the circuit, while the digital ground is the reference for the low-power components, such as logic circuits. The consideration for current return loops is essential because, in the power ground, there is a high-current switching noise, which can affect the sensitive digital signals. Therefore, the layout should be designed so that digital ground and power ground cannot interfere with each other. Besides this, there are traces where di/dt is high; while designing these traces, it is important to minimize the inductance since it can have the capability of affecting the digital signal. To minimize the inductance of a trace, the trace width should be high while the trace length should be minimal.

2.2.1 Power Converters

There are three step-down switching regulators in the card. The first one is TSR1 - 24120. It fits the footprint of TO-220. This regulator is for converting the input voltage to 12 V that supplies the gate driver to satisfy the need for secondary-side power (i.e., MOSFETs' ON voltage). TSR1 - 24120 can deliver 1 A at the full load. The input voltage range of the regulator is from 15 V to 36 V. Its wide input operating range provides flexibility for the user. The maximum efficiency of TSR1 - 24120 is 96 % without any heat sink or active cooling. It has the capability of short-circuit protection at the output [10].

The second step-down switching regulator is TSR1 - 2433 which converts the input voltage to 3.3 V which supplies the current sense amplifier, and the development board of the specified DSP. The maximum current of TSR1 - 2433 is 1 A at the full load. The operating range of input voltage is from 4.75 V to 36 V. Its maximum efficiency is approximately 94 %. There is no need for any heat sink or active cooling. TSR1 - 2433 has the feature of short circuit protection at the output. The footprint and dimensions are the same as TSR1 - 24120 [10].

The third step-down switching regulator is TSR2 - 2450, which converts the input voltage to 5 V. The Op-amps located at the LCL filter need 5 V. Therefore, TSR2 - 2450 is used to supply these Op-amps. This switching regulator can give

a maximum current of 2 A with a typical efficiency of 94 %. Its input voltage range is from 6.5 V to 36 V. This regulator does not require any heat sink or active cooling, and it includes protection against short circuits. The footprint and dimensions are different from the previous ones. The dimensions of TSR2 - 2450 are $14 \times 7.5 \times 10.1$ mm [11].

2.2.2 Transistor

The selection of transistors is significant in inverter applications. IGBTs and MOSFETs are the common transistors for inverter applications and other power electronic circuits. Although the specifications of each transistor might change, IGBTs and MOSFETs generally have specific advantages. Power converters with IGBTs can work under higher DC supply voltage and higher load current compared to converters having MOSFETs. However, the turn-on delay and turn-off delay of IGBTs is much higher than MOSFETs, which indicates that MOSFETs generate smaller switching loss. MOSFETs can also work with a higher switching frequency, which decreases the harmonic distortion [12].

Dead-time is required for both transistors, but MOSFETs require less dead-time than IGBTs. The dead-time leads to problems such as output current distortion and voltage error. Thus, the control performance degrades. Since MOSFETs need shorter dead-time, inverters designed with MOSFETs exhibit lower voltage error and reduced output current distortion [13]. As a result of these reasons, MOSFET is preferred in this thesis.

Although MOSFETs possess countless parameters, the selection of MOSFET is based on several key considerations. These are drain-to-source voltage, continuous drain current, drain-source on-resistance, gate charge, maximum gate-to-source voltage, and the package of MOSFET. Drain-to-source voltage is the difference between the drain and source of the MOSFET, and it should be above the DC input voltage with an appropriate safety margin. In this case, the supply voltage is 30 V. Therefore, it should be considerably higher than 30 V. Continuous drain current specifies the maximum amount of current the MOSFET can

handle. The continuous drain current should be higher than the inverter's output current. Drain-source on-resistance is the on-state resistance of MOSFET. This resistance is directly related to the conduction loss. Therefore, a high drain-source on-resistance decreases the efficiency. Gate charge is another important parameter since it affects the duration of turn on and turn off of the MOSFET. Therefore, the switching loss is associated with the gate charge of the MOSFET. The higher the gate charge is, the more switching loss occurs. Maximum gate-to-source voltage should be compatible with the output specifications of the gate driver. Higher gate-to-source voltage decreases the drain-source on-resistance, which is an advantage in acquiring high efficiency. The package of MOSFET is also crucial because it is related to the capacity of heat dissipation. In inverter applications, two primary types of packages are commonly employed: through-hole packages and surface-mount packages. Through-hole packages might require an additional mechanical part for heat dissipation, while surface-mount packages generally dissipate the heat through the PCB. Therefore, it is easier to cool down surface mount packages. The selected MOSFET is IXFT150N25X3HV. The specifications of MOSFET from the datasheet are presented in Table 2.2 [14].

Specification	IXFT150N25X3HV
Drain to Source Voltage (V_{DS})	250 V
Continuous Drain Current (I_D)	150 A
MOSFET on-state Resistance ($R_{DS(on)}$)	9 m Ω
Total Gate Charge (Q_g)	154 nC
Internal Gate Resistance ($R_{G(int)}$)	1.5 Ω
Gate Threshold Voltage ($V_{GS(th)}$)	4.5 V
Gate-Source Voltage (V_{GS})	± 20 V
Turn-On Delay Time ($t_{d(on)}$)	30 ns
Rise Time (t_r)	30 ns
Turn-off Delay Time ($t_{d(off)}$)	115 ns
Fall Time (t_f)	10 ns
Package	D3PAK

Table 2.2: Specifications of IXFT150N25X3HV

IXFT150N25X3HV is highly sufficient for this application. This MOSFET is capable of conducting high currents with a surface mount package, which is one of the main advantages of this MOSFET. Therefore, the MOSFET can dissipate the power through the PCB without overheating.

2.2.3 Gate Driver Circuit

The gate driver controls the switching of MOSFET. Proper design of gate driver circuits is significant in inverter applications. This circuit consists mainly of a gate driver, decoupling capacitors, a bootstrap circuit, and a gate resistor. The trace length of this circuit needs to be minimal to decrease the oscillations. Since there is a high switching frequency, the trace between the gate driver and MOSFET should be especially minimized. Otherwise, there might be some voltage spikes and oscillations, which might affect the working of MOSFET [15].

There are two kinds of gate drivers: current source gate drivers and voltage source gate drivers. The voltage source gate drivers are considered more traditional, and their functionality is validated numerously. The current source gate drivers are relatively new in comparison to voltage source gate drivers. The current source gate drivers are highly resistive. This increases the damping effect on the switching of MOSFET. Therefore, the current source gate drivers are more stable against the injected voltages arising from stray inductance and high di/dt . However, the current source gate drivers are more complicated than the voltage source gate drivers, which increases the difficulty of the design. The voltage source gate drivers apply a constant voltage to the gate of MOSFET. This voltage charges the gate using internal and external gate resistors. This drive technique requires low resistive output of IC. However, if the design is not proper, this drive technique is prone to oscillations occurring from high dv/dt in switching of MOSFET [16].

Our gate driver is a voltage source gate driver. The driver circuit is specially designed. The gate driver is UCC21521DW. The specifications of the gate driver from the datasheet are given in Table 2.3 [17].

Specification	UCC21521DW
Isolation	Isolated (can be used as non-isolated)
Peak Source and Sink Currents	4 A peak source and 6 A peak sink
Output resistance at high state	5 Ω
Output resistance at low state	0.55 Ω
Rise / Fall Time (Typ)	6 ns, 7 ns
Pulse Width Distortion (Max)	6 ns
Number of Channels	2 (suitable with high-side and low-side drive)
Programmable Dead-Time	Yes, via resistor and capacitor
Supply Voltages	For controller side: 3 V to 18 V. For MOSFET side: 9.2 V to 25 V
Package	16-SOIC

Table 2.3: Specifications of UCC21521DW

While deciding the gate driver and switching frequency, it is necessary to validate the selected components. The formula for the peak value of gate current is given Equation 2.2 [15].

$$I_{g(peak)} = \frac{V_{GS}}{R_{G(int)} + R_G + R_O} \quad (2.2)$$

In the formula, $R_{G(int)}$ is the internal gate resistance of MOSFET, $R_G = 4 \Omega$ is the external gate resistance of MOSFET, and R_O is the output resistance of the gate driver.

When the parameters from Tables 2.2, 2.3 are plugged into the formula, the peak gate current is calculated as 1.98 A, which is well below the limits of the gate driver.

The second formula is for calculating the maximum switching frequency of MOSFET [15].

$$f_{sw(\max)} < \frac{1}{t_r + t_{d(\text{on})} + t_f + t_{d(\text{off})}} \quad (2.3)$$

When the values specified in Table 2.2 plugged, $f_{sw(\max)}$ is calculated as 5.40 MHz. The switching frequency is selected as 25 kHz, which is sufficiently lower than the maximum switching frequency.

After determining the gate driver, the bootstrap circuit should be designed. The bootstrap circuit is a cost-effective and efficient method. This circuit is required when employing a half-bridge configuration since it is essential to establish a high-side bias to control the gate of the high-side MOSFET with respect to the switch node. A bootstrap circuit comprises a capacitor, a diode, a resistor, and a bypass capacitor. Some gate drivers include a built-in bootstrap circuit, while others do not have this circuit internally. The external design of this circuit gives the user flexibility and reduces power dissipation, which makes it more favorable. UCC21521DW does not have an internal bootstrap circuit. Therefore, it is necessary to design this circuit.

The operational principle of a bootstrap circuit comprises of two stages: the charging of the bootstrap capacitor and the discharging of the bootstrap capacitor. When the high-side MOSFET is off and low-side MOSFET is on, the bootstrap capacitor is charged. This stage is depicted in Figure 2.8 [18].

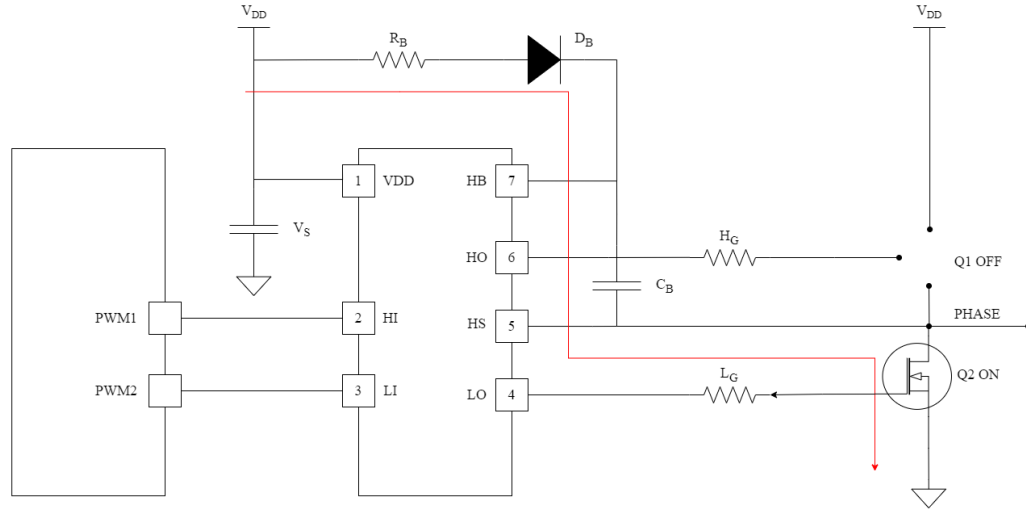


Figure 2.8: Bootstrap Capacitor Charging Path

When the high-side MOSFET is on, the bootstrap capacitor supplies the charged voltage to the gate of the high-side MOSFET. This makes the gate voltage of the high-side MOSFET exceed its source voltage. Hence, the MOSFET turns fully on. The discharging stage of the bootstrap capacitor is displayed in Figure 2.9 [18].

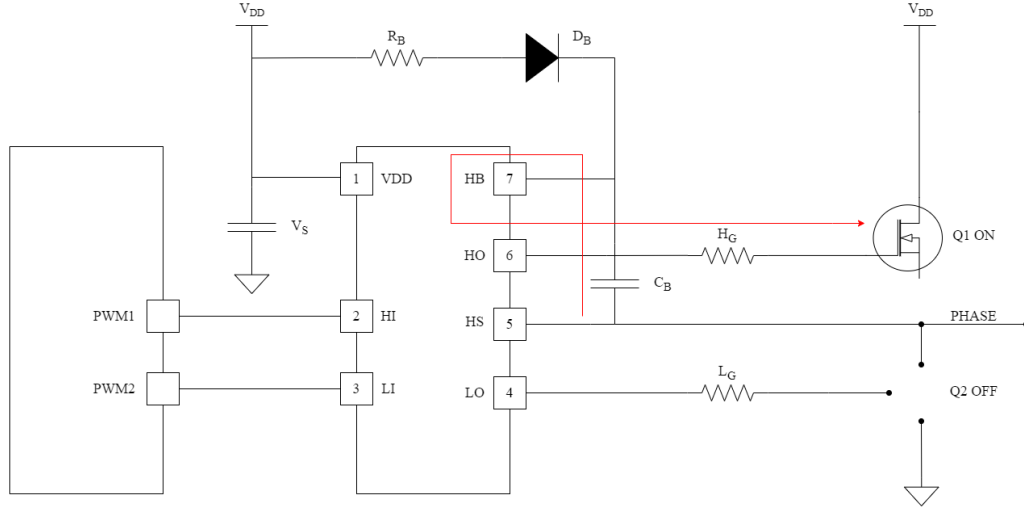


Figure 2.9: Bootstrap Capacitor Discharging Path

The bootstrap capacitor is one of the key components in the bootstrap circuit. This capacitor enables the gate driver to obtain a high amount of peak currents to drive the high-side switch. The size of the bootstrap capacitor is important to provide the necessary voltage to the high-side MOSFET without any issue. The bootstrap capacitance needs to be at least 10 times higher than the gate capacitance of the high-side MOSFET. This amount of capacitance prevents the impact of capacitance shift arising from DC bias and temperature. The formula for the calculation of gate capacitance is provided Equation 2.4 [18].

$$C_g = \frac{Q_g}{V_g} \quad (2.4)$$

where Q_g is the gate charge given in the MOSFET's datasheet and

$$V_g = V_{DD} - V_F \quad (2.5)$$

where V_F is the forward voltage of the diode in the bootstrap circuit. In this

case, V_{DD} is 12 V and V_F is 950 mV.

$$C_g = \frac{154 \text{ nC}}{12 \text{ V} - 0.95 \text{ V}} = 13.87 \text{ nF} \quad (2.6)$$

Therefore, the bootstrap capacitor should be higher than 139 nF. If the capacitance is lower than this value, this might cause the activation of the gate driver's Under Voltage Lockout (UVLO). Hence, the high-side gate might prematurely turn off. The higher capacitance values provide lower ripple voltage. Therefore, it is reasonable to select the bootstrap capacitance that is higher than the required value. In our case, the bootstrap capacitor is selected as 4.7 μF and 100 nF in a parallel connection. Bypass capacitor V_S should have a capacitance of at least ten times greater than the bootstrap capacitance. This prevents the bypass capacitor from being depleted during the charging period of the bootstrap capacitor. This ratio of ten to one ensures that the maximum ripple on the V_S capacitor does not exceed 10 % under worst-case conditions [18]. It is difficult to find a 47 μF ceramic capacitor. Therefore, V_S is selected as 44 μF . This capacitance is acquired with a parallel combination of two capacitors with a capacitance of 22 μF .

The bootstrap diode is another important component in the bootstrap circuit. A fast recovery diode is required to minimize the losses related to the reverse recovery. The selected diode is HS1FFL. This is a fast recovery diode, and it is suitable for this application. The repetitive peak reverse voltage of HS1FFL is 300 V. It can pass a surge current of 30 A for around 8 ms.

The bootstrap resistor is the component that limits the peak currents passing through the bootstrap diode during start-up. This resistor is selected as 2.2 Ω . The formula for calculating peak current passing through the diode is included in Equation 2.7.

$$I_{pk} = \frac{V_{DD} - V_{\text{BootDiode}}}{R_{\text{boot}}} \quad (2.7)$$

In our case, $V_{DD} = 12\text{ V}$ and $V_{\text{BootDiode}} = 950\text{ mV}$. Hence, $I_{\text{pk}} = 5.02\text{ A}$. This current is within the limits of diode HS1FFL.

2.2.4 Current Sensing

Current sense circuits are utilized in power electronic applications. They are used as the input of the control algorithm. Besides this, the current sensing is also important for safety issues. In the case of short-circuit situations, the over-current protection circuits are necessary. In addition, there are some cases where there is no complete short circuit situation. However, the system draws an inordinate amount of current. In such cases, over-current protection is also required to prevent the electronic devices from being damaged [19]. Over-current protection is generally achieved by a current sensor that samples the phase current. There are two main types of methods for in-line current sensing. The first method is to sense the in-line current through a shunt resistor. This method is cost-effective, simple, smaller, and highly accurate. However, the primary drawback of this method is efficiency. The shunt resistor located at each phase consumes power, which decreases the efficiency, especially in high-current applications. The second method is to sense the in-line current with a hall-effect current sensor. This method is costly compared to the previous method, and hall-effect current sensors generally provide less accuracy [20]. In our case, the maximum peak current is 5.45 A. Hence, the dissipated power is not too high. Therefore, in this thesis, it is appropriate to employ the shunt resistor method. Each phase current is sampled with the current sense amplifier of INA240A1PWR.

Specification	INA240A1PWR
Common-mode voltage (max)	80 V
Common-mode voltage (min)	-4 V
Voltage gain	20 V/V
CMRR (min)	120 dB
Bandwidth	400 kHz
Supply voltage (max)	5.5 V
Supply voltage (min)	2.7 V
Number of channels	1
Gain error	0.2 %

Table 2.4: Specifications of INA240A1PWR

Table 2.4 displays the specifications of INA240A1PWR from the datasheet [21]. The gain error is negligibly low to measure the phase current correctly. In addition to this, a sufficiently high bandwidth is also required since the digital control algorithm samples the current with a frequency of 50 kHz. This current sensor is compatible with sensing the current at this frequency. Therefore, it is suitable for this inverter application. In this application, the peak value of phase current is -5.45 A and 5.45 A. Hence, there are negative values that need to be sampled. The current sense circuit is exhibited in Figure 2.10.

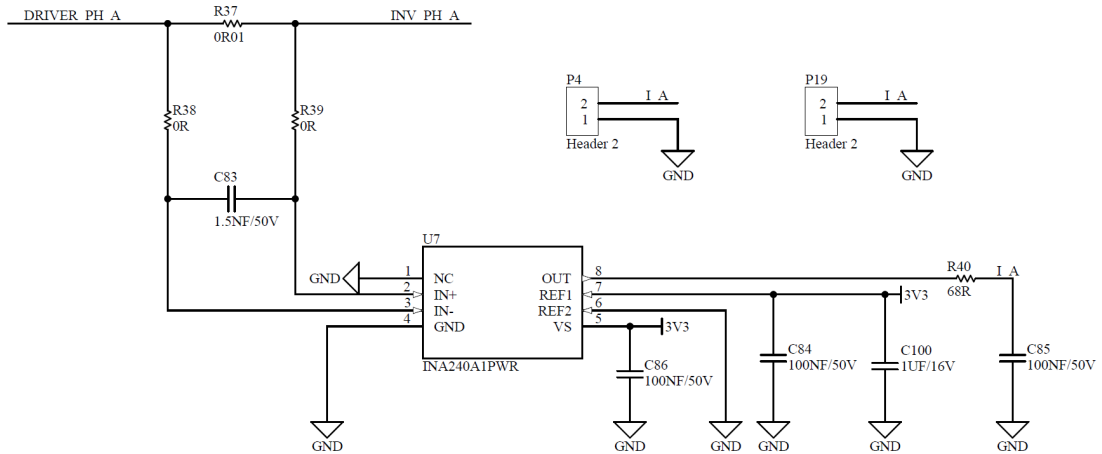


Figure 2.10: Current Sense Circuit

The input pins of the current sense amplifier are swapped to optimize the layout. At the output of the current sense amplifier, there is an RC filter whose cut-off frequency is 23.4 kHz, which eliminates the noise that might result from the switching of MOSFETs. The output voltage formula is given in the datasheet of INA240A1PWR. When the formula is adjusted according to our values, it is presented in Equation 2.8.

$$V_{\text{out}} = 1.65 + (-I_A[A] \times 10 \text{ m}\Omega) \times 20 \frac{\text{V}}{\text{V}} \quad (2.8)$$

When the values of -5.45 A and 5.45 A are plugged into Equation 2.8, the output of the current sense amplifier is in the range from 0.56 V to 2.74 V. In order to ensure the working of the circuit, the simulation should be performed. LTspice is used for the simulation.

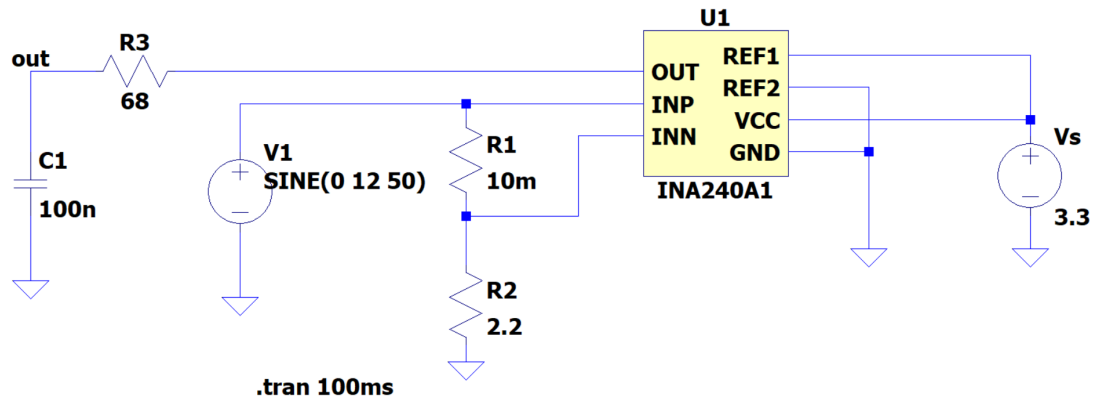


Figure 2.11: Current Sense Circuit on LTspice

The current sensing circuit on LTspice is provided in Figure 2.11. The result of the simulation is given in Figure 2.12.

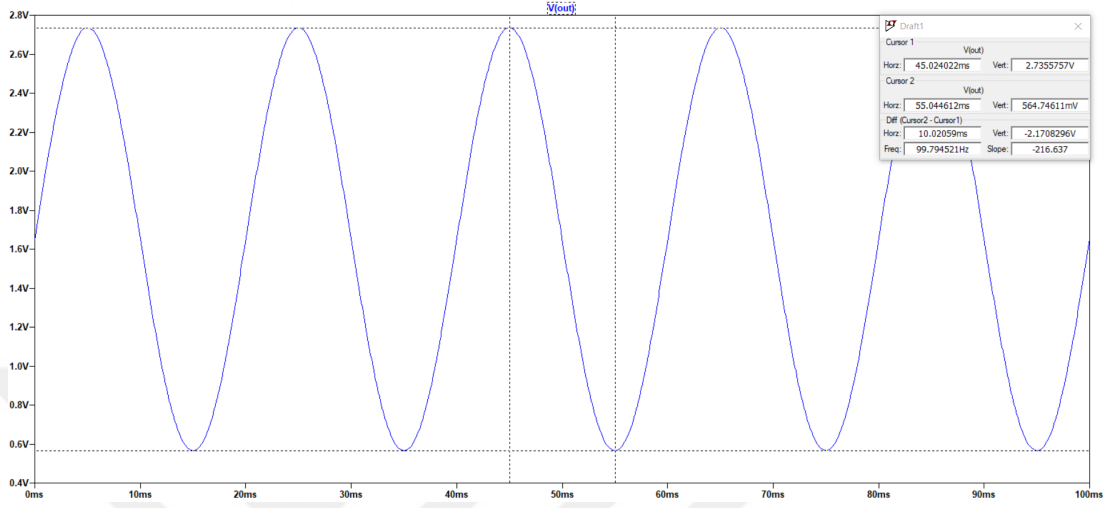


Figure 2.12: The Result of Current Sense Simulation

The result of the simulation is compatible with the theoretical calculations. The phase currents are sensed with the ADC of DSP. After sensing it, Equation 2.9 represents the analog signal as a current with the ampere unit.

$$I_A = (V_{\text{out}} - 1.65) \times 5 \quad (2.9)$$

The result shown in Figure 2.13 is acquired when this calculation is carried out on LTspice.

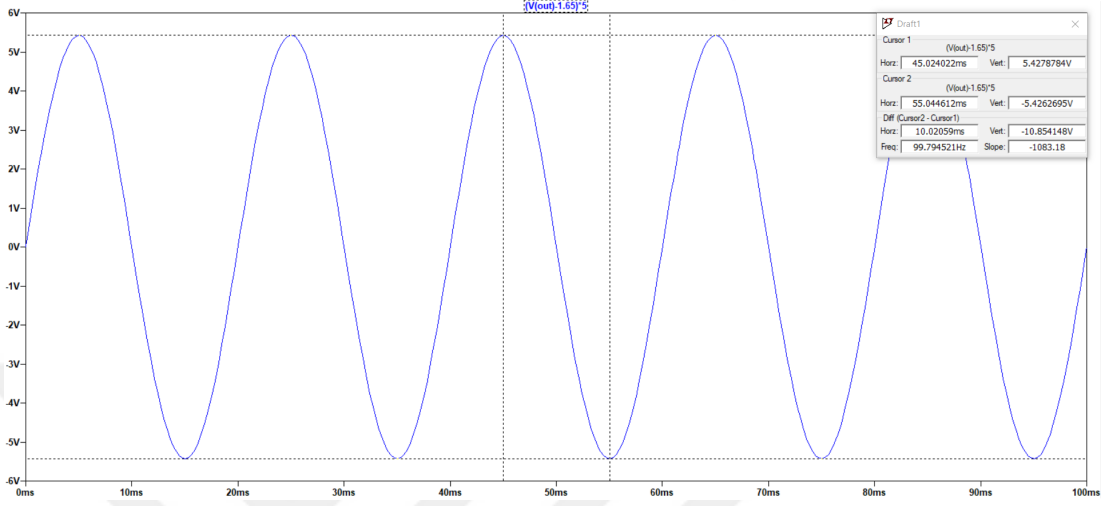


Figure 2.13: The Result of Simulation in terms of Current

The current sense circuit is verified with this simulation. In this thesis, this circuit is used for the over-current protection.

2.3 LCL Filter Card

LCL filter is utilized to filter the harmonics of the three-phase output, thereby acquiring a pure sinusoidal output. LCL filter card consists of LCL filters and voltage sensing circuits. On the front of the card, there are three LCL filters, each of which corresponds to one phase. A stability resistor is included at each phase. Three connectors are the same components. The connector located at the bottom is for the neutral signal. However, it is not used. The connector placed at the left is the input of three phases that come from the three-phase inverter card. After filtering, the connector located at the right gives the sinusoidal three-phase output. The schematic of the LCL filter card is given in Figures 2.14, 2.15, 2.16.

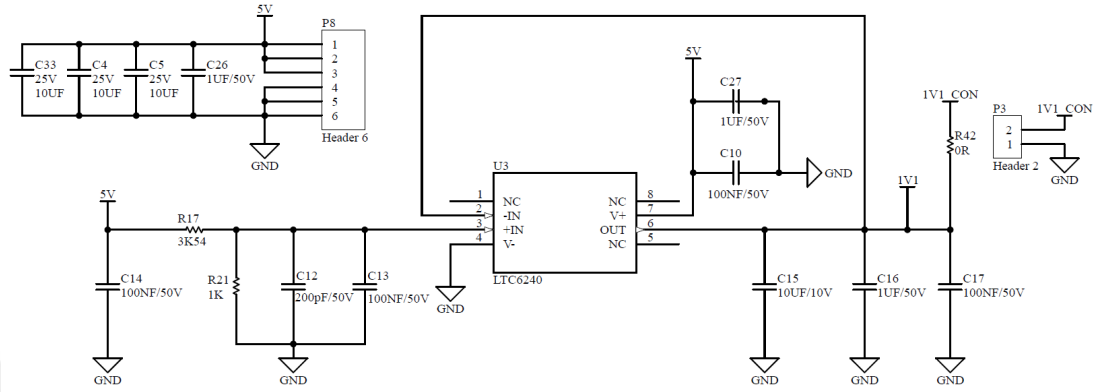


Figure 2.16: Acquisition of 1.1 V from 5 V

The component list of the LCL filter card is given in Table 2.5.

Component	Designator	Quantity
Ceramic Capacitor, 330 pF, 50 V, 0603	C1, C8, C19	3
Ceramic Capacitor, 100 nF, 50 V, 0603	C2, C3, C7, C9, C10, C11, C13, C14, C17, C18, C20, C21, C22	13
Ceramic Capacitor, 10 μ F, 25 V, 1206	C4, C5, C33	3
Ceramic Capacitor, 1 μ F, 50 V, 0805	C6, C16, C26, C27, C28, C29, C30, C31, C32	9
Ceramic Capacitor, 200 pF, 50 V, 0603	C12	1
Ceramic Capacitor, 10 μ F, 10 V, 0805	C15	1
Aluminum Polymer Capacitor, 47 μ F, 63 V	C23, C24, C25	3
3 pins terminal connector	J1, J2, J3	3
Fixed inductor 150 μ H 9.2 A 30.6 mohm, 74437529203151	L1, L2, L3, L4, L5, L6	6
Header, 6-Pin	P8	1
Header, 2-Pin	P1, P2, P3, P4, P5, P6, P7, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20	19
Resistor, 5 K, 0.063 W, 0603	R1, R9, R12, R22, R25, R33	6
Resistor, 33K3, 0.25 W, 1206	R2, R3, R4, R6, R7, R8, R13, R14, R15, R18, R19, R20, R26, R27, R28, R30, R31, R32	18
Resistor, 68 R, 0.1 W, 0603	R5, R16, R29	3
Resistor, 3K54, 0.1 W, 0603	R17	1
Resistor, 1 K, 0.1 W, 0603	R21	1
Resistor, 1 R, 1.5 W, 2512	R36, R37, R38, R39, R40, R41	6
IC OPAMP, LTC6240IS8	U1, U2, U3, U4	4

Table 2.5: Component List of LCL Filter Card

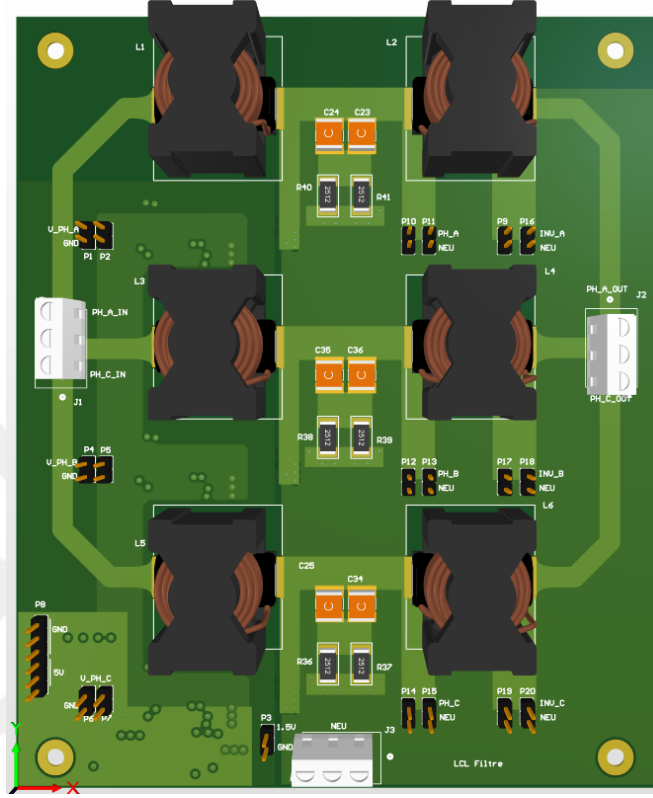


Figure 2.17: 3D Front View of LCL Filter Card

The design of the LCL filter is explained in the following sections. On the back of the card, there are three voltage sensing circuits, each of which is identical. At the bottom of the card, there is a circuit that provides an offset of 1.1 V to the voltage sensing circuits. These voltage sensing circuits are built with difference amplifier circuits that measure the difference between op-amp inputs. The component placement is conducted so that the high current cannot affect the sense of voltage. Therefore, it is not preferred to put the voltage sense circuit directly at the bottom of inductors.

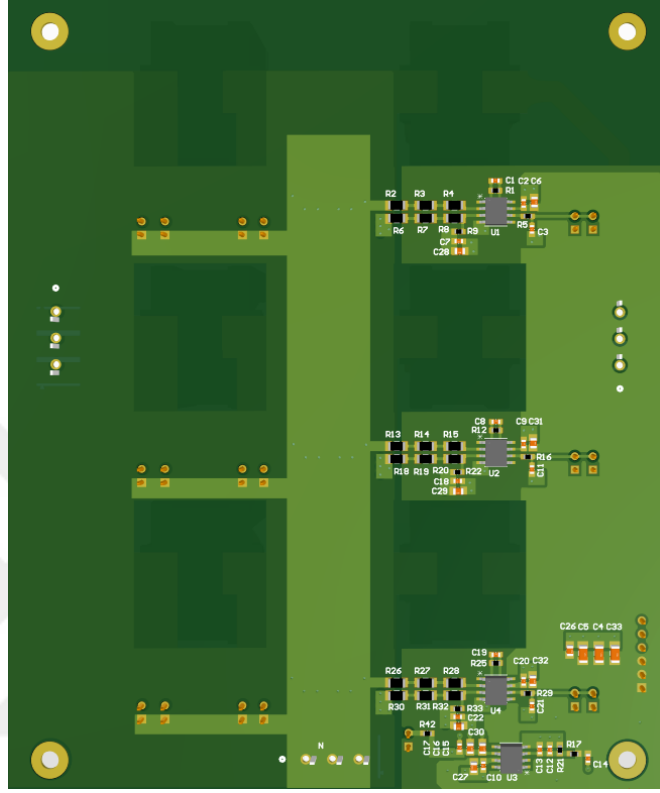


Figure 2.18: 3D Back View of LCL Filter Card

2.3.1 Filter Comparison and LCL Filter Selection

Inverters generate high-frequency switching signals that include undesired harmonics. The output filter of an inverter is required to attenuate these high-frequency components and reduce harmonic distortion, which results in a better-quality output signal. There are typically three types of output filters, namely L-filter, LC-filter, and LCL filter.

Initially, a single inductor L-filter is used due to its simplicity. However, this filter suffers from a low attenuation and requires a high inductance value. The voltage drop across the inductor leads to poor system dynamics, which results in a slow response time. To effectively attenuate harmonics using an L-filter, it is necessary to either apply the high-frequency switching signal or place a high value of inductor [22].

After that, a capacitor is added in the shunt connection since the L-filter provides an insufficient attenuation of the switching oscillations. This combination enhances the attenuation of these switching components since capacitors provide low reactance at the switching frequency, and so the high-frequency noise can be eliminated. Conversely, the capacitors present a high impedance at the control frequency range. Hence, the main signal is not affected. However, in this approach, the required value of L does not change considerably. To compensate for this, a high capacitor value is needed to acquire a good attenuation. On the other hand, it is not recommended since the inrush current and the reactive current increase substantially [22]. In addition to these, the direct connection of the capacitor to the system may lead to instability. [23].

Finally, despite the increased design complexity that comes from the third-order configuration of the LCL filter, this filter offers superior harmonic attenuation and a more cost-effective solution for decreasing current harmonics. LCL filter design needs the consideration of numerous constraints such as the resonance phenomenon, the current ripple through inductors, the current harmonics attenuation at the switching frequency, and the reactive power absorbed by capacitor [23]. In the next section, the design of the LCL filter is performed by taking these constraints into account.

2.3.2 Calculation of LCL Filter Values

After determining the filter type as an LCL filter, the values of the filter should be calculated. This calculation is critical for obtaining a high attenuation. The inverter side of inductor (L_{inv}) can be calculated using Equation 2.10 [24].

$$L_{inv} = \frac{V_{DC}}{8f_{sw}I_{rated}\%ripple} \quad (2.10)$$

In this application, $V_{DC} = 30 \text{ V}$, $f_{sw} = 25 \text{ kHz}$, $I_{rated} = 3.85 \text{ A}$, and ripple = 30 %. This amount of ripple is regarded as low enough for inverter applications. Using the specified values, the inverter side of the inductor is calculated as $L_{inv} =$

130 μH .

An inductor from Wurth Elektronik (74437529203151) with a rated current of 9.2 A and an inductance of 150 μH is used. The effective inductance of this inductor at the current of 5.45 A is approximately 135 μH , so it is appropriate to select this inductor.

After calculating the inverter side of inductance, the value of capacitance should be calculated. The formula for C_f is given by Equation 2.11 [24].

$$C_f = \frac{\%X Q_{\text{rated}}}{2\pi f_{\text{grid}} V_{\text{grid}}^2} \quad (2.11)$$

The total reactive power absorbed by the capacitor is limited to 3.5 %. Hence, $C_f = 50 \mu\text{F}$. It is required to use non-polarized capacitors in LCL filter, and two ceramic capacitors of 22 μF can be used in a parallel connection.

Base capacitance needs to be calculated to compute the attenuation factor.

$$C_b = \frac{C_f}{X\%} = \frac{47 \mu\text{F}}{3.5 \%} = 1343 \mu\text{F} \quad (2.12)$$

The grid side inductance should be calculated with Equation 2.13.

$$L_{\text{grid}} = r \times L_{\text{inv}} \quad (2.13)$$

As r increases, the attenuation also increases. To increase the attenuation and minimize the filter size, r should be selected as 1 [25]. Hence, $L_{\text{grid}} = 130 \mu\text{H}$. Therefore, the same inductor is selected for the grid side. The resonant frequency should be calculated with Equation 2.14 [24].

$$f_{\text{res}} = \frac{1}{\sqrt{\frac{L_{\text{grid}} L_{\text{inv}} C_f}{L_{\text{grid}} + L_{\text{inv}}}}} \cdot \frac{1}{2\pi} \quad (2.14)$$

When the calculation is carried out, f_{res} is found as 2681 Hz. To ensure that f_{res} is stable. The following criterion should be satisfied.

$$10f_g < f_{\text{res}} < 0.5f_{\text{sw}} \quad (2.15)$$

This criterion helps avoid issues in the upper and lower harmonic spectrums. In our case, $f_g = 50 \text{ Hz}$ and $f_{\text{sw}} = 25 \text{ kHz}$. Therefore, the criterion is fulfilled. After satisfying the requirements, the attenuation factor should be considered. This factor defines the allowable ripple between the grid inductor and the inverter inductor. The attenuation factor should be minimal to attenuate the harmonics substantially. The attenuation factor can be calculated in percent using Equation 2.16 [24].

$$\text{attenuation} = \frac{100}{|1 + r(1 - L_{\text{inv}}C_b(2\pi f_{\text{sw}})^2 X)|} \quad (2.16)$$

The attenuation factor is found as 0.54 %, which is sufficiently good. Finally, a damping resistor should be considered.

Resonance should be avoided through the use of passive damping methods since the rapid phase transition occurring at the resonance frequency, there might be an instability of controllers, which leads to an oscillation. The damping resistor can be computed using Equation 2.17 [24].

$$R_D = \frac{1}{6\pi f_{\text{res}}C_f} \quad (2.17)$$

When the values $f_{\text{res}} = 2681 \text{ Hz}$ and $C_f = 44 \text{ }\mu\text{F}$ are plugged, R_D is found as $0.43 \text{ }\Omega$. Two resistors with the value of $1 \text{ }\Omega$ are used in a parallel combination. To see the total harmonic distortion and the quality of the output, the simulation is performed on Simulink.

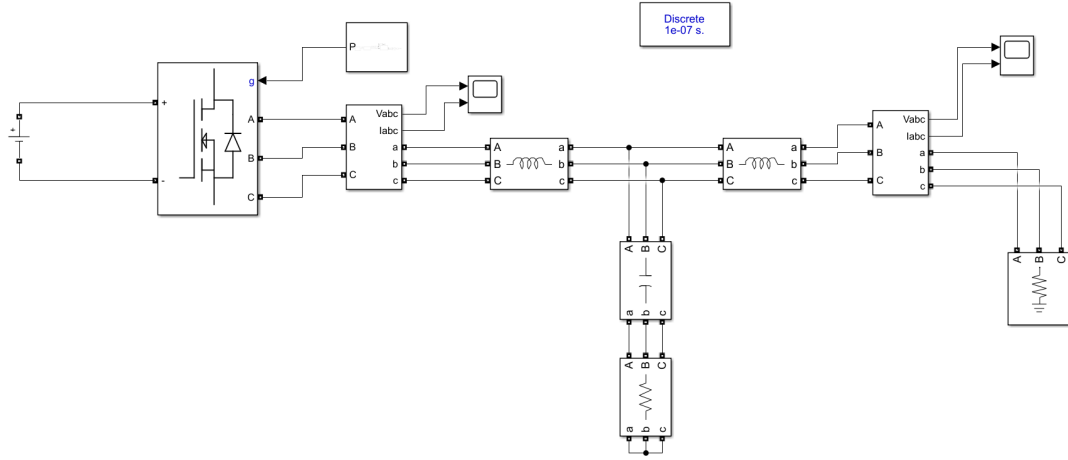


Figure 2.19: Schematic for LCL Filter Simulation

This simulation aims to verify the LCL filter. Therefore, a 2-level internal controller is used. The PI controller is implemented in the next chapter.

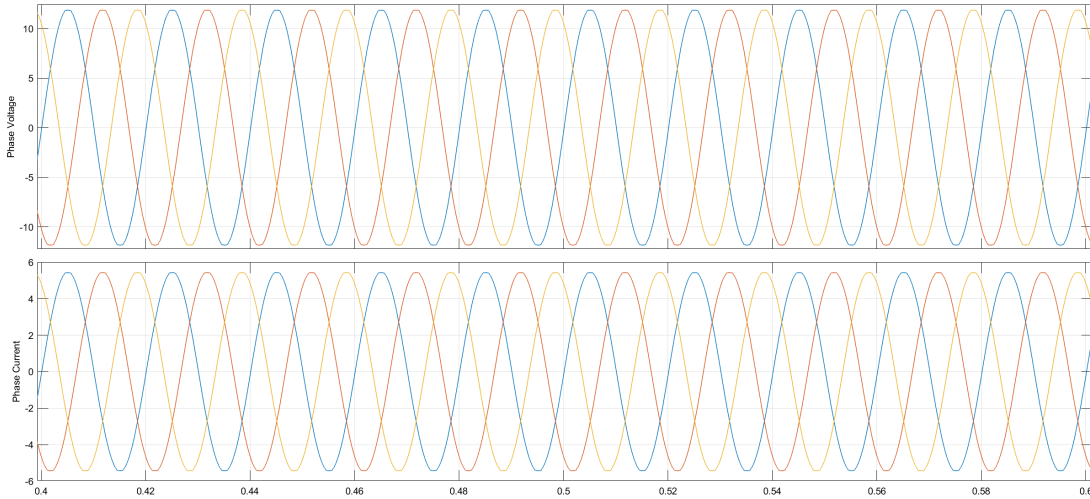


Figure 2.20: LCL Filter Simulation Result

The phase voltage and phase current can be seen in Figure 2.20. The peak value of phase voltage is 12 V, and the peak value of phase current is 5.45 A. The total harmonic distortion should also be examined.

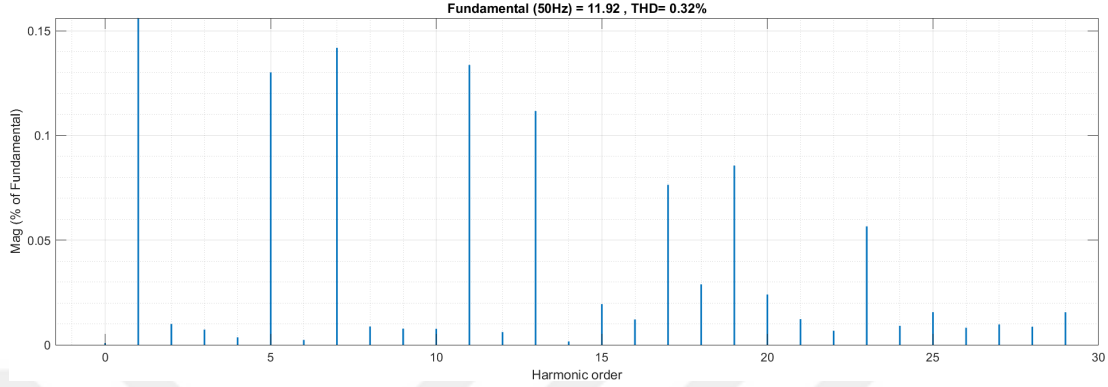


Figure 2.21: Total Harmonic Distortion of LCL Filter

The total harmonic distortion is 0.32 %, which is sufficiently low. The results of the LCL filter satisfy the requirements.

2.3.3 Voltage Sensing Circuit

The output voltage is a valuable measurement in the voltage source inverter. The accuracy of voltage sensing has an enormous impact on the performance, stability, and efficiency of the inverter. In the voltage source inverter, the output voltage is generally taken as the input of the control system. This voltage can be phase voltage or line-to-line voltage. The actual output voltage is compared to the desired reference voltage. Therefore, an accurate sensing of output voltage increases the accuracy of output voltage. Besides this, the harmonics are minimized with the correct voltage sensing since the output voltage waveform is closely followed by the desired waveform [26].

There are some measurement techniques for sensing the output voltage. In this thesis, the phase voltage is directly measured instantaneously. While measuring the phase voltage directly, dead-time and non-ideal properties of the inverter components are included in the measurements, which is one of the main advantages of the direct measurement technique. A difference amplifier circuit with the op-amps is used. It is crucial to connect the output of the difference amplifier

circuit to the low-pass filtering to eliminate the high-frequency switching signals produced by the PWM process while allowing the fundamental component of the phase voltage to pass [27].

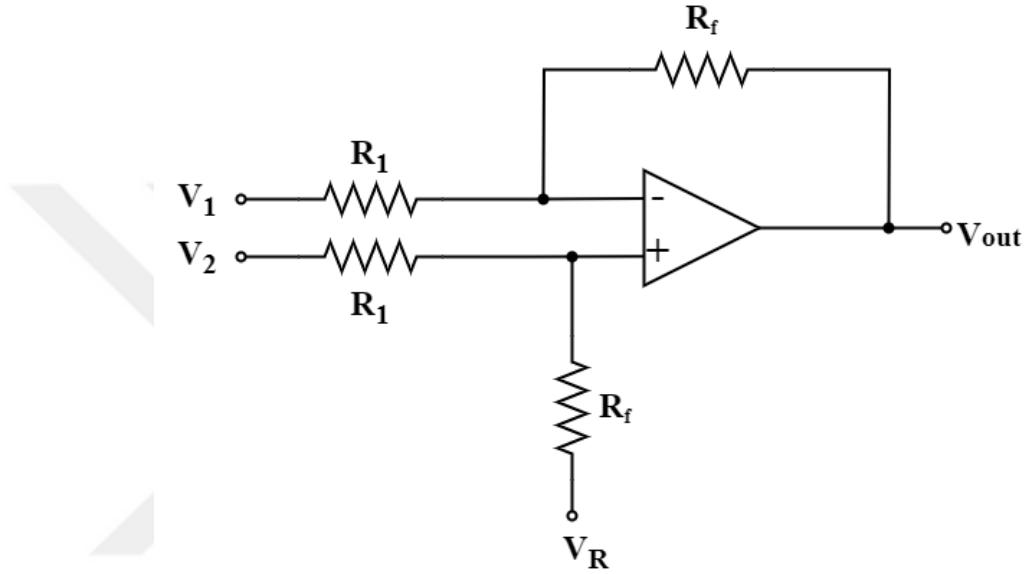


Figure 2.22: Difference Amplifier Circuit

The difference amplifier circuit is given in Figure 2.22. The main purpose of the difference amplifier circuit is to measure the voltage difference between two inputs of the op-amp. V_R is the offset of the difference circuit. So, the output voltage of this circuit can be calculated using Equation 2.18.

$$V_{\text{out}} = V_R + \frac{R_f}{R_1} \times (V_2 - V_1) \quad (2.18)$$

One of the key advantages of the difference amplifier is its ability to reject common-mode signals, which are the signals that are present on both input lines. The circuit passes only the difference between the inputs and ignores any common signal included in both. In this thesis, the inputs of op-amp are connected to the phase voltage and neutral. The noise coming from the switching of MOSFETs might affect both phase voltage and neutral. In this case, common-mode noise rejection of the circuit increases the accuracy of the measurements.

In this application, the phase voltage is in the range from -12 V to 12 V. While measuring the phase voltage, it is reasonable to provide some margin in case of over-voltage or oscillation. Otherwise, the DSP might be damaged permanently because of over-voltage at the ADC channel. Therefore, $R_f = 5\text{ k}\Omega$, $R_1 = 100\text{ k}\Omega$ and $V_R = 1.1\text{ V}$. When the values are plugged, Equation 2.18 becomes

$$V_{\text{out}} = 1.1\text{ V} + 0.05 \times (V_2 - V_1) \quad (2.19)$$

The selection of op-amp is significant. There are some parameters that need to be considered when an op-amp is selected [26].

The input offset voltage (V_{OS}) is the voltage required between the two input terminals of an operational amplifier to produce a zero-volt output. The input offset voltage affects the accuracy of measurements. Therefore, the lowest offset voltage is preferred.

Offset voltage drift in an operational amplifier refers to the change in the input offset voltage (V_{OS}) as the temperature. The lowest offset voltage drift is preferred.

Rail-to-rail input and rail-to-rail output are significant since the phase voltage is converted to a voltage in the range of 0 V to 3 V.

The common-mode rejection ratio is crucial because the switching frequency of the three-phase inverter is 25 kHz. The common-mode rejection ratio should be greater than 80 dB at 125 kHz, which is 5 times the switching frequency.

When these considerations are prioritized, LTC6240 is selected for this application. LTspice simulation is performed with this op-amp to ensure that the circuit works properly.

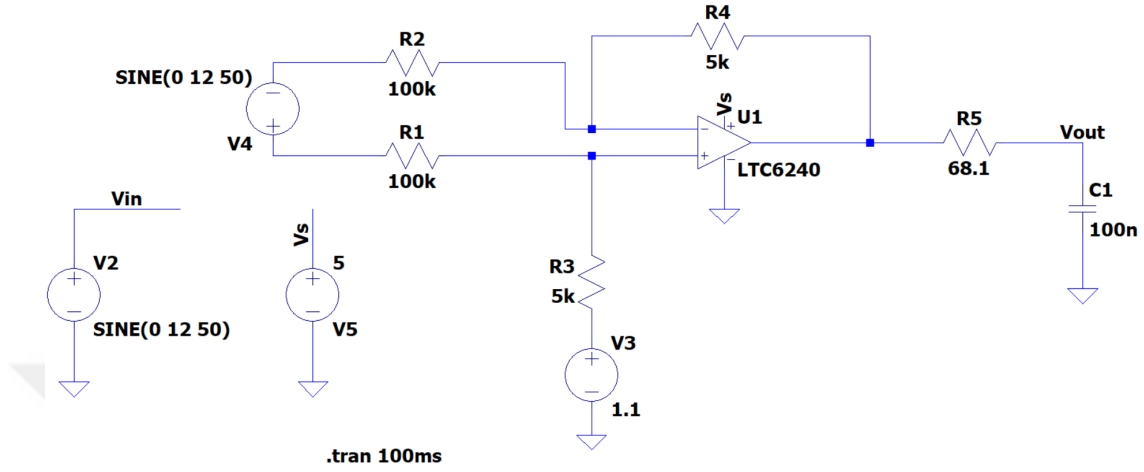


Figure 2.23: Difference Amplifier Circuit on Simulation

In the simulation, the input voltage is sinusoidal between -12 V and 12 V with a frequency of 50 Hz. This input is given in Figure 2.24.

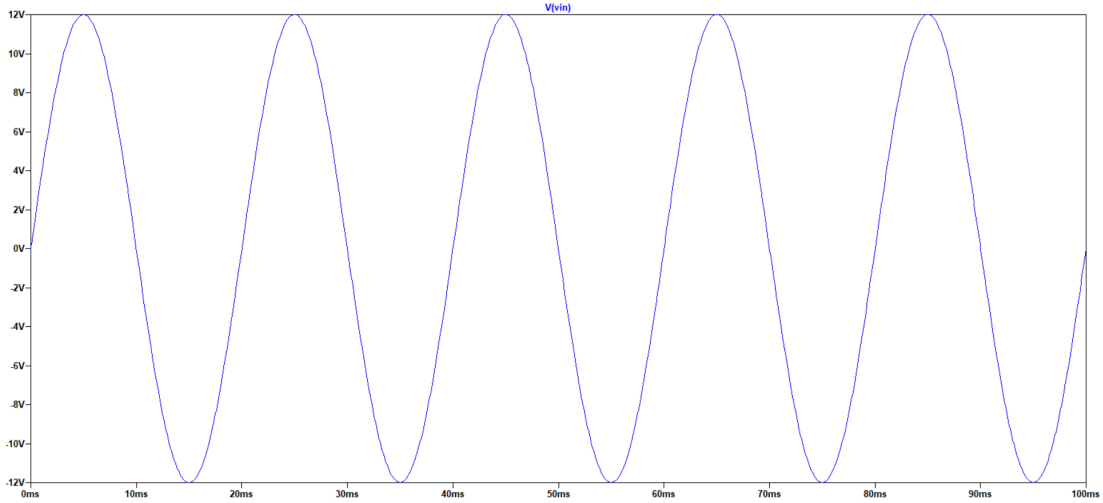


Figure 2.24: The Input Signal

The offset voltage is 1.1 V, and the equation of output voltage is given in Equation 2.19. In addition to this, there is a low-pass RC filter at the output. The main purpose of this filter is to filter the noise arising from the switching of MOSFETs. The cut-off frequency of this filter is 23.4 kHz, which is below the switching frequency. The corresponding output is given in Figure 2.25.

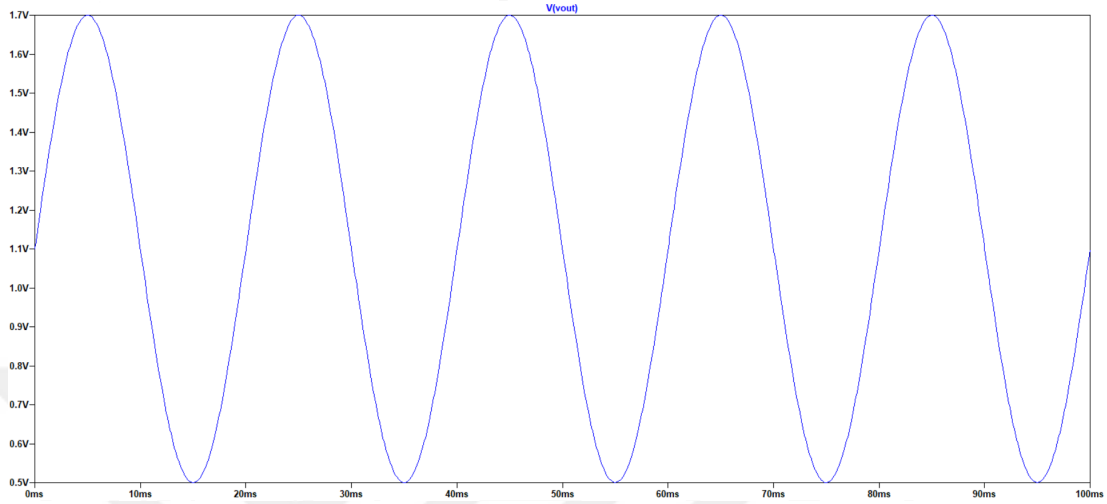


Figure 2.25: The Output Signal

In the DSP algorithm, 1.1 V is subtracted from the measured voltage and then multiplied by 20 to acquire the input voltage. When this adjustment is implemented, the result is given in Figure 2.26.

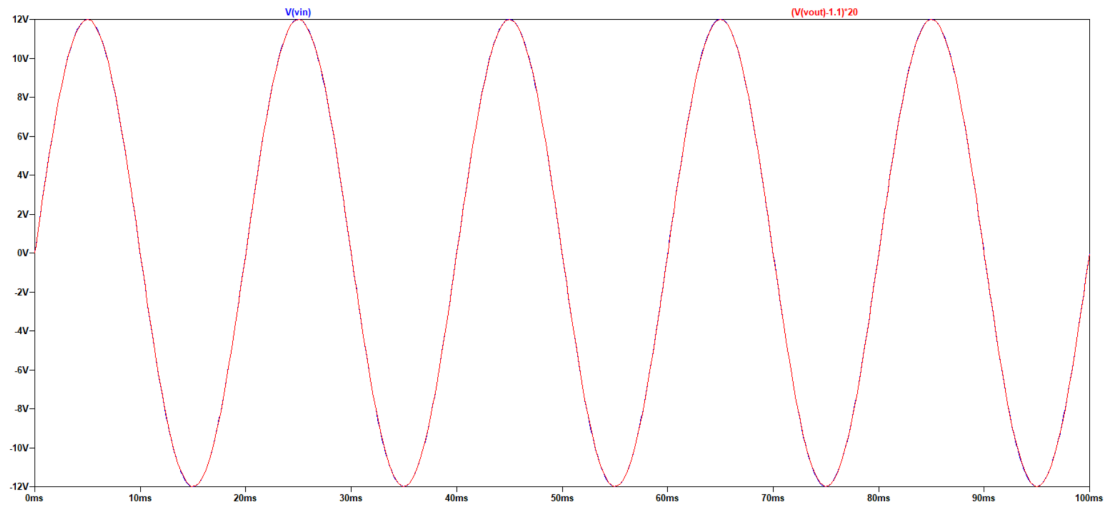


Figure 2.26: The Measurement of Input Signal

It is evident in Figure 2.26 that the input signal and the adjusted output signal overlap with each other, which means the input signal can be correctly sensed with this circuit.

Chapter 3

Digital Controller

Digital controllers in inverters are significant since they provide precise management and optimization of power conversion processes. Digital controllers might benefit from digital signal processors to implement sophisticated algorithms, which results in acquiring the required output voltage with sufficiently high accuracy. Although the stability of analog controllers is higher compared to digital controllers, analog controllers do not offer the same opportunity. Digital controllers continuously observe the output voltage, current, frequency, etc., so this control level increases the efficiency and output quality of the inverter. Besides these, digital controllers allow the user to easily change the output parameters, such as voltage and frequency, without changing any hardware configuration. As the sampling frequency of the digital controller increases, the stability issues can be overcome [28]. Therefore, the superiority of digital controllers becomes distinct with the increasing sampling frequency.

3.1 DSP Selection

DSPs are highly suitable for inverter applications since they are designed to handle real-time control, complex mathematical computations, and control algorithms [29]. Texas Instruments offers a comprehensive range of products, such as single-core and multicore DSPs. The C2000 series is ideal for inverter applications since they perform sophisticated computations and include advanced peripherals. In inverter applications, it is important to possess a high-precision pulse width modulation module to generate high-quality output. In order to create PWM, the sensing of output voltage is necessary. The analog-to-digital converter peripheral of C2000 enables sensing of voltage, current, and other signals at a high speed. Hence, the C2000 series fulfills the requirements of designing an inverter. There are numerous DSPs that belong to the C2000 series. The comparison is performed in Figure 3.1 [30].

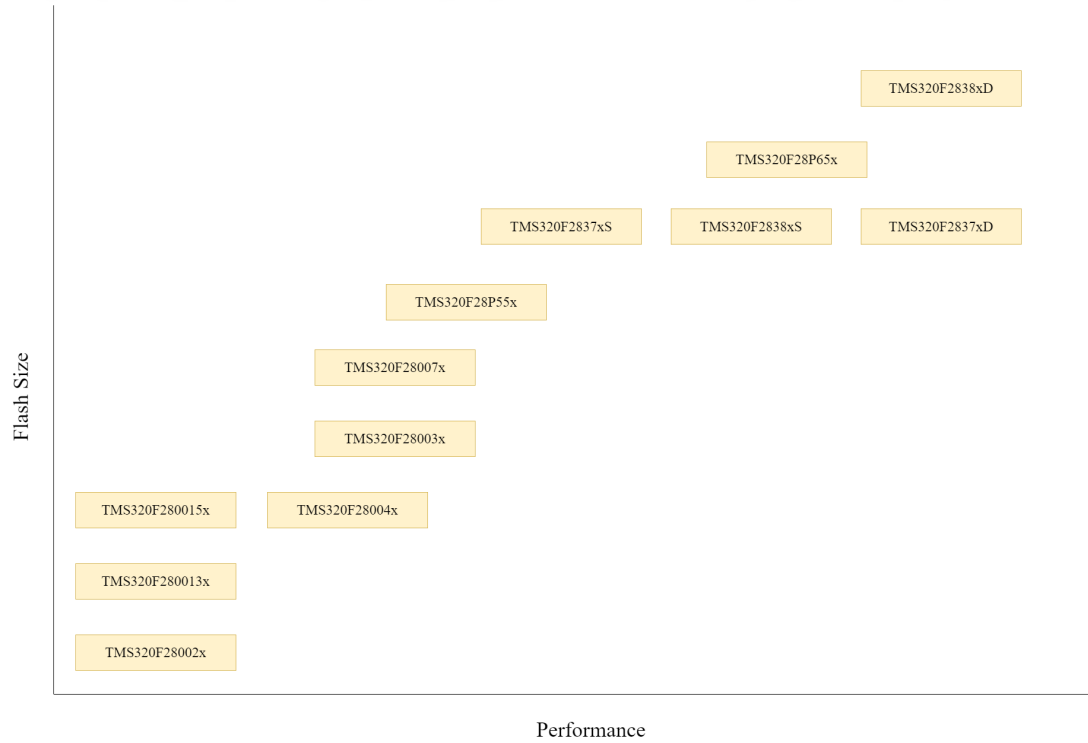


Figure 3.1: C2000 series Comparison of Memory and Performance

Along these DSPs, TMS320F2837xD is used in countless applications. There are a lot of DSPs that belong to this series. The frequency and total processing of all these DSPs are the same. However, Flash Memory, RAM, and ADC resolution change according to DSP. In this thesis, TMS320F28379D is used. The specifications of this DSP from the datasheet are provided in Table 3.1 [31].

Feature	TMS320F28379D
Frequency	200 MHz
Flash Memory	1024 kByte
RAM	204 kByte
ADC resolution	12, 16 bps
Total processing	800 MIPS

Table 3.1: Specifications of TMS320F28379D

ADC resolution depends on whether the signal conversion is single-ended or differential. When the single-ended signal conversion is used, the resolution is 12-bit, whereas when the differential signal conversion is used, the resolution is 16-bit. In this thesis, the single-ended conversion is used. There are 24 ADC channels that can be used as single-ended conversion [32].

3.2 Development Board

There are two boards that include the DSP of TMS320F28379D. These boards are TMS320F28379D controlCARD and LAUNCHXL-F28379D. TMS320F28379D controlCARD is costly, and there is a need for the second board to fit the control card. Therefore, in this thesis, the LAUNCHXL-F28379D development board is used.

This development board can be used in power conversion control focusing on DC-DC, AC-DC, and DC-AC. There are numerous inverter evaluation boards that are compatible with LAUNCHXL-F28379D. This board has an XDS100v2

JTAG debug probe that connects TMS320F28379D to a host computer via USB without requiring any additional interface card. XDS100v2 is also compatible with the Integrated Development Environment (IDE) of Texas Instruments called Code Composer Studio. Therefore, using XDS100v2, one can program the code and debug it. In this board, there is galvanic isolation between the PC and the DSP, which prevents the PC from being damaged in case of any unfavorable situation [33].

This board needs 3.3 V and 5 V. 3.3 V is required for DSP. 5 V is needed for Op-amps and reference IC that produces a reference voltage of 3 V for ADCs. The board can be supplied with both 3.3 V and 5 V. This adjustment is made according to the jumpers located on the board. There are three methods for supplying the board. The first configuration is to supply the board with a USB cable. When this method is employed, there is no isolation between PC and DSP. Therefore, it is not favorable in power conversion applications. The second configuration is to supply the board with an external 5 V. In this configuration, there should also be an additional 3.3 V. Since this configuration needs two different supply voltages, it is not useful for us. The third configuration is to supply the board with an external 3.3 V. In the development board, there is a boost converter that converts 3.3 V to 5 V, which satisfies the need for 5 V [33]. In this thesis, the third configuration is used. With this configuration, only 3.3 V is supplied to the board, and there is a galvanic isolation between the PC and DSP. Therefore, this configuration is reasonable for power conversion applications.

The development board has two LEDs that can be configured depending on the user's preference. They can be utilized as an indicator of the working of DSP. In our configuration, initially, one is not blinking, and the other is. Each second these LEDs toggle to indicate that there is no problem in the working of DSP. There are 12 available Enhanced Pulse Width Modulation (ePWM) pins physically connected to the connector of the development board, 6 of which are used in this thesis. There are 20 available ADC channels in the development board, 7 of which are used in this thesis [33].

3.3 DSP Peripherals

TMS320F28379D has various peripherals such as ADC, ePWM, communication, etc. These peripherals can be used in advanced applications. In this thesis, we benefit considerably from ADC and ePWM peripherals.

3.3.1 ADC Peripheral

There are four independent ADCs in TMS320F28379D: ADCA, ADCB, ADCC, and ADCD. Each ADC module utilizes a successive approximation (SAR) architecture that offers a selectable resolution of 16 or 12 bits with 16 configurable SOC's. The ADC comprises two main components, namely core and wrapper. The core includes various analog circuits such as the channel select MUX that selects the channel of the selected ADC, sample-and-hold (S/H) circuit that consists of a capacitor and resistor, voltage reference circuits that provide the reference voltage to ADC, and additional analog support components. The wrapper contains the digital circuitry responsible for the configuration and control of ADC, including result registers that have the results of conversion, connections to peripheral buses, and post-processing circuits that perform post operations such as adding an offset. Each ADC module features one sample-and-hold circuit, which means when an ADC samples multiple channels, there should be a sequential process of analog-to-digital conversion [32]. Although each ADC has 16 channels, all these channels are not physically connected. There are six channels available for ADC module A (ADCA). There are four channels available for ADC module B (ADCB). There are four channels available for ADC module C (ADCC). There are four channels available for ADC module D (ADCD). There are two channels available that can be used by any of the four ADCs [31]. In this thesis, the ADCs of ADCA, ADCB, and ADCC are used. The ADC of ADCD is not used in this application.

ADC	Channel	SOC	Description
ADCA	ADCINA2	SOC0	Sensing of Voltage across Phase A
	ADCINA3	SOC1	Sensing of Voltage across Phase B
	ADCINA4	SOC2	Sensing of Voltage across Phase C
ADCB	ADCINB4	SOC0	Sensing of Current through Phase A
	ADCINB5	SOC1	Sensing of Current through Phase B
	ADCIN15	SOC2	Sensing of Current through Phase C
ADCC	ADCINC5	SOC0	Sensing of Input Voltage

Table 3.2: ADC Channel Descriptions for Voltage and Current Measurements

There are multiple trigger options in TMS320F28379D. These are software immediate start, ePWMs for ADCSOCA or B, CPU Timers 0/1/2, GPIO XINT2, and ADCINT1/2. The reduced schematic of the ADC core is presented in Figure 3.2 [32].

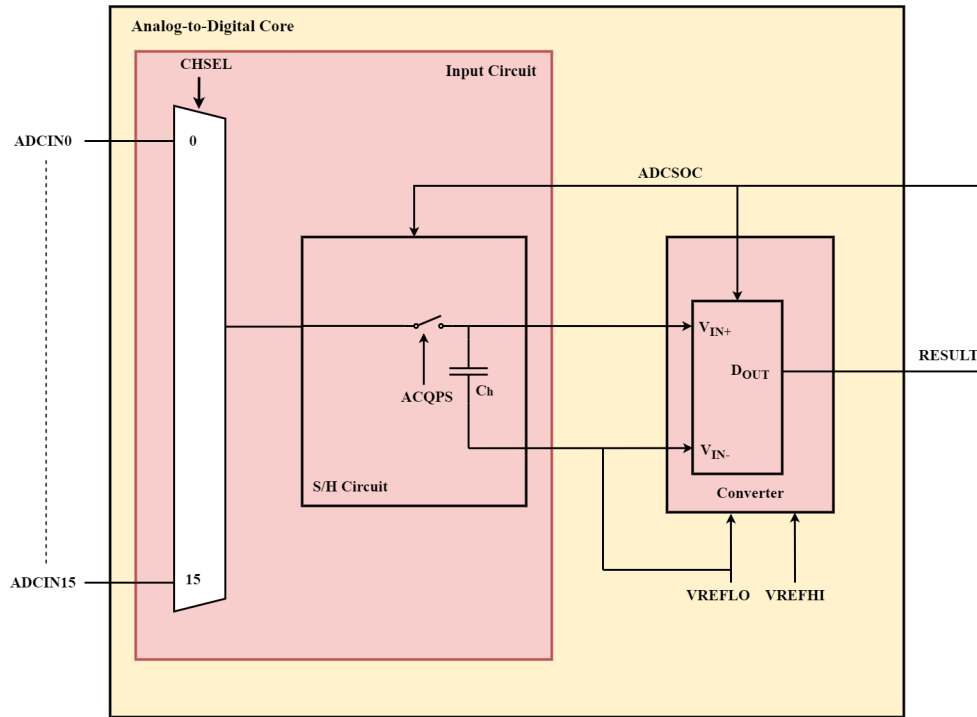


Figure 3.2: ADC Core

Conversion starts with an incoming Start of Conversion (SOC) trigger signal. In this thesis, the trigger signal of SOC comes from ePWM. After being triggered, the ADC samples the voltage on the selected channel. This selection is determined by CHSEL with the channel mux. This is necessary because each ADC can convert only one sample at a time. In this application, the configuration is established in such a way that when ePWM1 matches the zero or period, the trigger signal of SOCA is generated, and then the ADCA begins sampling channel ADCINA2 (SOC0), ADCINA3 (SOC1) and ADCINA4 (SOC2) sequentially, ADCB simultaneously begins sampling channel ADCINB4 (SOC0), ADCINB5 (SOC1) and ADCIN15 (SOC3) sequentially and ADCC also simultaneously samples the channel of ADCINC5 (SOC0). The conversion proceeds at the Sample and Hold (S/H) Circuit. The capacitor C_h located at the S/H Circuit is charged up with the duration stated by the Acquisition Pre Scalar (ACQPS) value. The determination of this value is critical for the accurate measurement of ADC. If ACQPS is too short, charging stops before reaching the real value, which causes reading the voltage to be lower than its actual value. If ACQPS is too long, there is an unnecessary delay in the conversion. In our case, there is a buffer in the voltage sensing circuit, which implies the input of ADC has a low impedance. Therefore, it is reasonable to keep the switch closed for a shorter amount of time.

According to the datasheet, the minimum sample duration should be 75 ns for performing 12-bit conversion. However, it is appropriate to calculate the value of ACQPS according to the used circuit. The input drive circuit of ADC is given in Figure 3.3.

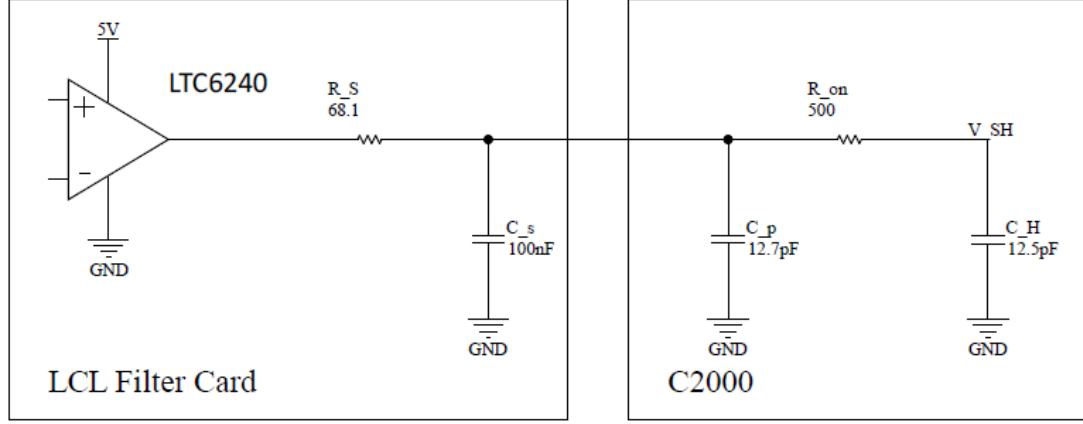


Figure 3.3: The Drive Circuit of the ADC

The time constant can be calculated with Equation 3.1 [32].

$$\tau = (R_s + R_{on})C_H + R_s(C_s + C_p) \quad (3.1)$$

C_H denotes the ADC sampling capacitor and C_p denotes the ADC channel parasitic input capacitance. In this case,

$$C_H = 12.5 \text{ pF} \quad \text{and} \quad C_p = 12.7 \text{ pF}$$

The number of time constant can be calculated using Equation 3.2 [32].

$$k = \ln \left(\frac{2^n}{\text{settling error}} \right) - \ln \left(\frac{C_s + C_p}{C_H} \right) \quad (3.2)$$

So, the approximate duration of the sample and hold time should be at least:

$$t = k\tau \quad (3.3)$$

When the values are plugged in the equations, $\tau = 6.81 \mu s$, $k = 0.0236$ and $t = 160.83 ns$. The system clock runs at 200 MHz. Therefore, each SYSCLK is 5 ns. ACQPS can be calculated with Equation 3.4 [32].

$$ACQPS = \frac{160.83}{5} - 1 = 32 \quad (3.4)$$

$$t_{(S+H)} = (ACQPS + 1) \times \left(\frac{1}{SYSCLK} \right) \quad (3.5)$$

After the S/H circuit, the converter calculates the digital representation of the voltage on C_H capacitor. The formula for this calculation is provided in Table 3.3 [32].

Analog Input	Digital Result
analog input $\leq$ VREFLO	ADCRESULT = 0
VREFLO $\leq$ analog input $\leq$ VREFHI	ADCRESULT = $4096 \times \left(\frac{ADCIN - VREFLO}{VREFHI - VREFLO} \right)$
VREFHI $\geq$ analog input	ADCRESULT = 4095

Table 3.3: Digital Result of ADC Conversion

In the development board, VREFHI is connected to 3 V, and VREFLO is connected to 0 V. Therefore, we cannot measure an analog signal greater than 3 V and lower than 0 V. Hence, the voltage range of measurement is from 0 to 3 V.

3.3.2 ePWM Peripheral

The Enhanced Pulse Width Modulation module is a versatile and advanced peripheral designed for precise timing and control applications. It provides high-resolution pulse-width modulation signals suitable for a wide range of tasks, such

as motor control and power conversion. The ePWM module features multiple channels, each of which is capable of generating up to two independent PWM signals, allowing for flexible and complex waveform generation.

There are three operating modes in the ePWM module, namely, up-count, down-count, and up-down count. We use the up-down count mode that is generally used in half-bridge topology. In this mode, the dead-time duration can be adjusted, and there is a symmetric operation among the three phases, which is important to obtain the phase difference of 120° . There are eight main submodules in the ePWM peripheral. These are Time-Base (TB), Counter Compare (CC), Action Qualifier (AQ), Dead-band (DB), PWM-choper (PC), Event-trigger (ET), Trip-zone (TZ), and Digital Compare (DC). In this thesis, five of these submodules are used: Time-Base, Counter Compare, Action Qualifier, Dead-band, and Event-trigger [32]. These are shown in Figure 3.4 [32].

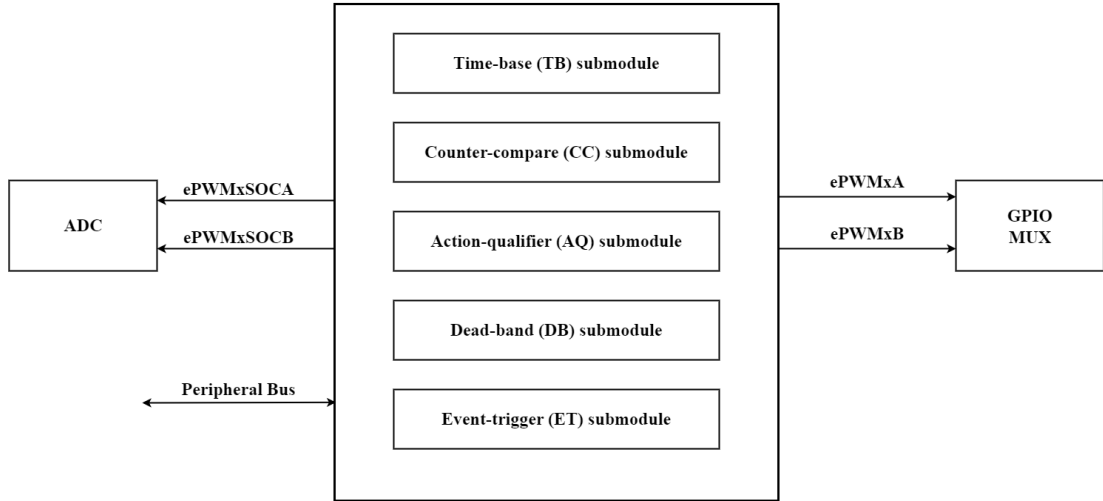


Figure 3.4: Submodules of ePWM Module

The Time-Base submodule configures the PWM time-base counter (TBCTR) to acquire the required frequency. This submodule specifies the mode of time-base counter such as up-count, down-count, or up-down-count. This submodule also adjusts the phase in relation to another the ePWM module. The count modes are exhibited in Figure 3.5 [32].

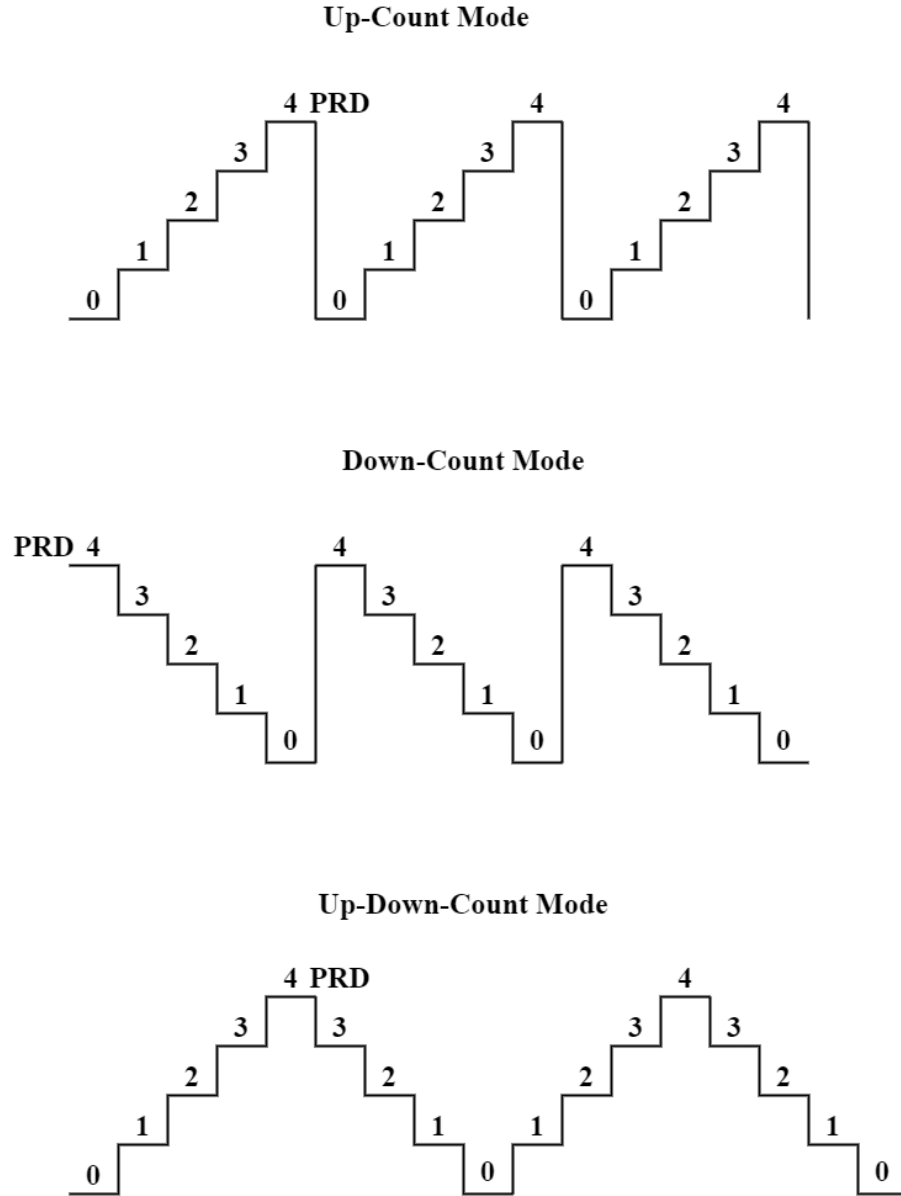


Figure 3.5: Count Modes

The Up-Down Count Mode is usually used in inverter applications. In order to adjust the switching frequency, the value of TBPRD should be calculated. The formula for this calculation is presented in Equations 3.6, 3.7 [32].

$$\text{TBPRD} = \frac{f_{\text{TBCLK}}}{2f_{\text{pwm}}} \quad (3.6)$$

$$f_{\text{TBCLK}} = \frac{\text{EPWMCLK}}{\text{HSPCLKDIV} \times \text{CLKDIV}} \quad (3.7)$$

EPWMCLK is equal to half of the system frequency, which implies 100 MHz. HSPCLKDIV and CLKDIV are equal to 1, which means that there is no additional division of EPWMCLK. Therefore, $f_{\text{TBCLK}} = 100 \text{ MHz}$. The switching frequency is 25 kHz. Hence, $\text{TBPRD} = 2000$.

The Counter Compare submodule receives the value of the time-base counter as input, and it continuously compares this value to the compare values of CMPA and CMPB. An event is triggered when the value of the time-base counter equals a compare value [32]. In our case, there is no fixed value of CMPA. This value is determined by the control algorithm of the inverter to acquire the required three-phase sinusoidal output.

The Action Qualifier submodule determines which action is taken when an event of the time base, counter compare, or comparator arises. The types of actions and their descriptions are described in Table 3.4 [32].

Action	Description
Set High	Configure the output of EPWMxA or EPWMxB to a high state.
Clear Low	Configure the output of EPWMxA or EPWMxB to a low state.
Toggle	Toggle output EPWMxA or EPWMxB
Do Nothing	Maintain outputs EPWMxA and EPWMxB at the same state

Table 3.4: Types of Actions

In our case, when there is a match between the time-base counter value and the compare value of CMPA, an action is triggered. When the value of the time-base counter equals zero or period, no action occurs. The events of action qualifier are depicted in Figure 3.6 [32].

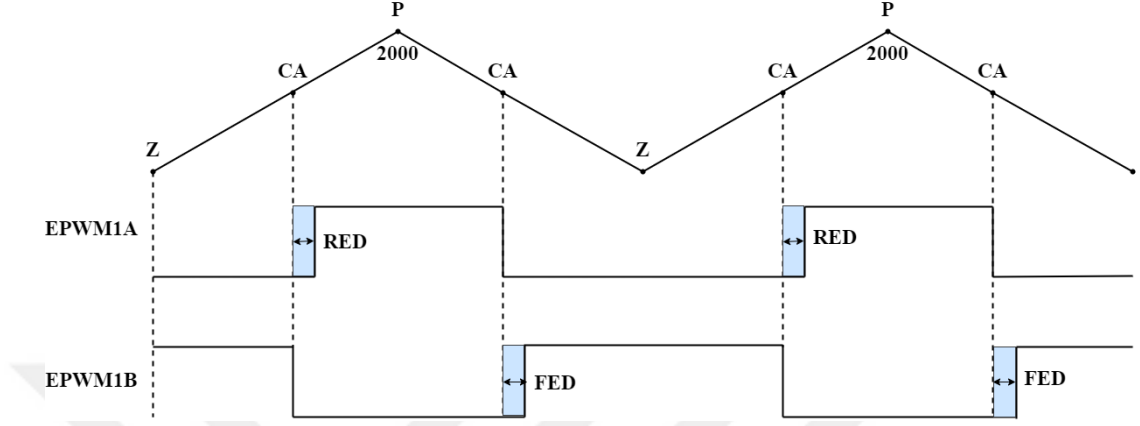


Figure 3.6: Events of Action Qualifier

When the value of the time-base counter increases and reaches the value of CMPA, EPWM1A is set to high. And, when the value of the time-base counter decreases and reaches the value of CMPA, EPWM1A is set to low. Unless these two events, there is no change in EPWM1A.

After creating the EPWM1A signal, its complimentary is generated using the Dead-band submodule. This submodule can be adjusted to create an active high complementary signal, and its rising-edge and falling-edge delays are configurable using the following equations [32].

$$\text{RED} = \text{DBRED} \times T_{\text{TBCLK}} \quad (3.8)$$

This equation is used to adjust the rising-edge delay. DBRED is the value of the register.

$$\text{FED} = \text{DBFED} \times T_{\text{TBCLK}} \quad (3.9)$$

This equation is used to adjust the falling-edge delay. DBFED is the value of the register.

In order for the inverter to work properly without any safety issues, rising-edge and falling-edge delays should be 500 ns. T_{TBCLK} is calculated as 10 ns. Therefore, $DBRED = DBFED = 50$.

Event Trigger submodule activates the ePWM events that initiate an interrupt and ADC start-of-conversion. The frequency of events that lead to triggering can be determined [32]. In our case, every event triggers the start-of-conversion, and the event occurs when the time-base counter equals zero or period.

3.4 Control Algorithm

In a three-phase inverter system, the control algorithm is essential for ensuring stable and efficient conversion of direct current into alternating current. This algorithm might involve sophisticated techniques such as pulse width modulation. These kinds of techniques provide a better regulation of voltage and current. The control algorithm continuously monitors the output and adjusts the switching patterns accordingly. Therefore, power quality, reduction of harmonics, and system efficiency are achieved.

Three-phase inverters employing the PWM switching technique typically operate with a constant DC input voltage (V_{DC}). The objective of the inverter is to convert this steady DC input into an AC output, where both the magnitude and frequency of the output can be regulated. There are various pulse width modulation techniques, and the performance of an inverter largely depends on the chosen modulation strategy [34]. SPWM and SVPWM are the most common modulation techniques. There are advantages and disadvantages of each technique. There are two main advantages of SVPWM. The first advantage of SVPWM is providing up to 15 % more utilization of DC bus voltage. This is an advantage in achieving a higher output voltage for the same DC bus voltage. The second advantage of SVPWM is to have a lower THD [35]. However, this modulation technique has some disadvantages. The switching loss of SVPWM is higher compared to SPWM. In addition to this, the SVPWM technique is more sensitive

to errors that might result from noise. On the other hand, the implementation of the SPWM technique is more straightforward than SVPWM, and this technique is less sensitive to errors. The combination of the SPWM technique with the LCL filter provides adequately low THD. In addition to the LCL filter, the switching frequency directly affects THD. As the switching frequency increases, THD decreases considerably, and in terms of output quality, the performance difference of these two modulation techniques becomes negligible. Besides this, in our case, there is no need for achieving higher output voltage with the same input voltage. Therefore, the SPWM technique is utilized in this design. The total harmonic distortion will be examined in the Simulink simulation.

The sinusoidal pulse width modulation technique allows for the direct regulation of both the output voltage and frequency. SPWM technique is defined by the pulses having a constant amplitude, but the duty cycle varies for each cycle. The pulse widths are adjusted to control the inverter's output voltage and minimize harmonic distortion. While employing SPWM, three sinusoidal waves and a high-frequency triangular carrier wave are utilized to produce the PWM signals. These waves are reference signals, and there is a phase difference of 120° between the sinusoidal waves. The frequency of these sinusoidal waves is selected based on the desired output frequency of the inverter. The frequency of the triangular carrier wave is high, and the switching signals are generated by comparing the sinusoidal waves to the triangular wave. The output of the comparator is high when the sine voltage is greater than the triangular voltage. The working principle of SPWM is depicted using MATLAB.

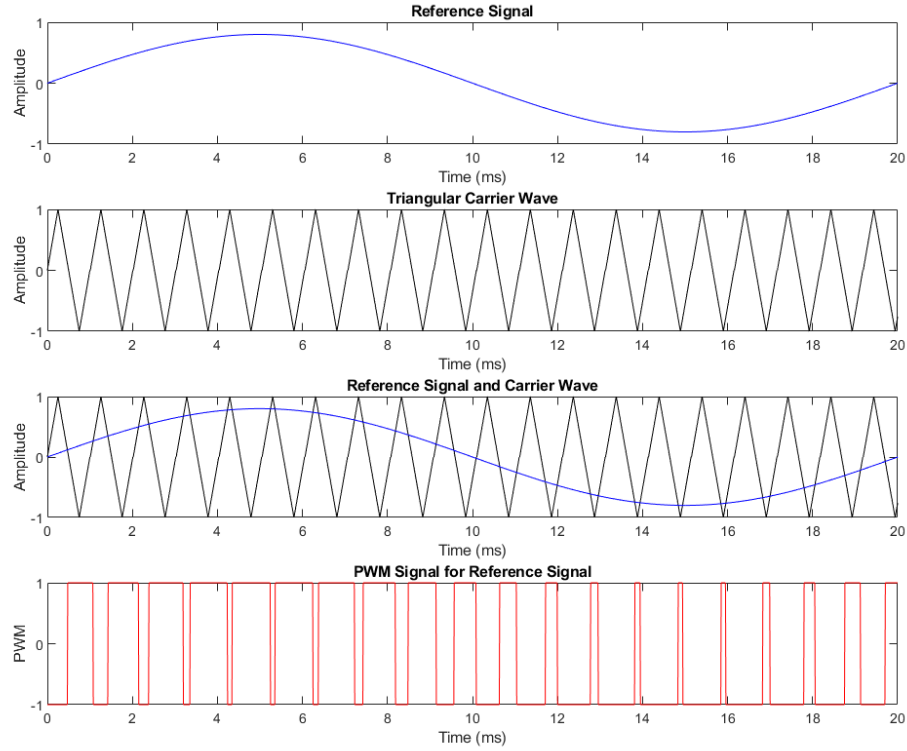


Figure 3.7: SPWM Technique for Single Phase Inverter

It is seen in Figure 3.7 that the first subplot is the reference signal whose frequency should be the same as the inverter's output frequency. The second subplot is the triangular carrier wave with a high frequency. On the third subplot, the reference signal and carrier wave are displayed together so the comparison can be performed. On the fourth subplot, the corresponding PWM signal is shown. After examining the SPWM technique for a single-phase inverter, the SPWM technique for a three-phase inverter is displayed in Figure 3.8. The main difference is the generation of three reference signals, each of which has a phase difference of 120° .

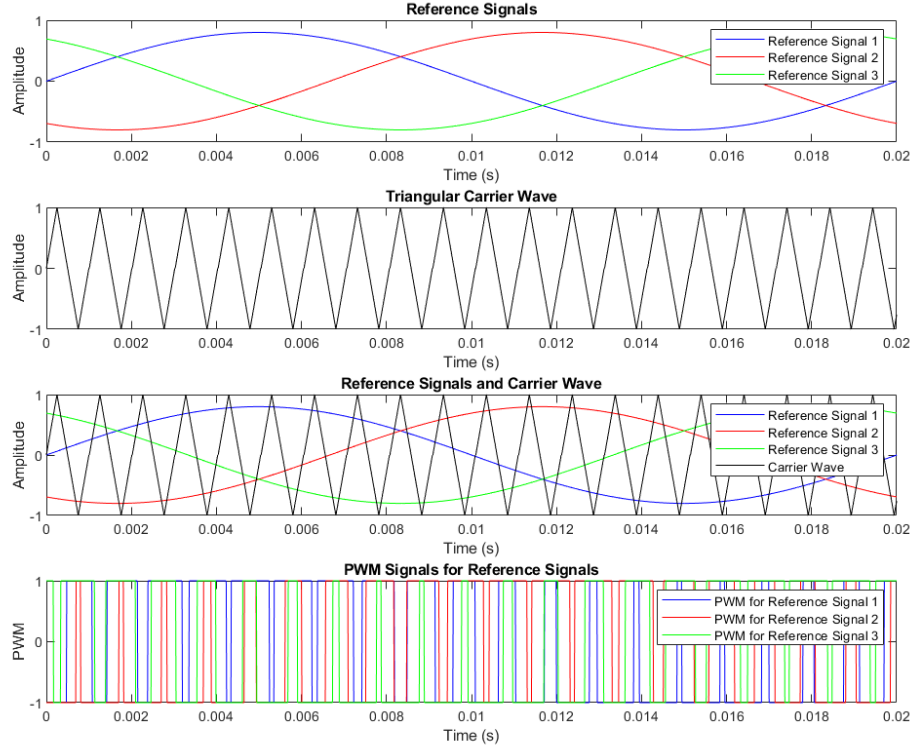


Figure 3.8: SPWM Technique for Three-Phase Inverter

The first subplot shows three reference signals. The frequency of each reference signal is the same as the output frequency. The second subplot is the triangular carrier wave. On the third subplot, the reference signals and carrier wave are exhibited together. The comparison between reference signals and triangular carrier wave is carried out, and the PWM signal is created accordingly on the fourth subplot.

Another advantage of SPWM is the attenuation of low-order harmonics. Larger filters are generally required to attenuate lower-order harmonics. However, these filters can be both bulky and costly. Conversely, filters designed to address higher-order harmonics are typically more compact and economical. Therefore, sinusoidal pulse width modulation techniques are employed to eliminate the lower-order harmonics, whereas an LCL filter circuit is utilized for the

attenuation of higher-order harmonics [36].

A PI (Proportional-Integral) controller is widely used in the control of three-phase inverters to regulate the output voltage and frequency. In the context of a three-phase inverter, the PI controller operates by minimizing the steady-state error. The actual voltage is monitored and compared to the inverter's target output voltage. If any error is detected, the PI controller generates the necessary modulation signals to correct and control the output voltage. The proportional term of the controller ensures a fast response to errors while the integral term decreases or even eliminates the steady-state error, resulting in smooth and stable inverter operation. In three-phase inverter applications, the PI controller is often used in the DQ reference frame to increase the voltage stability of the inverter [37]. In this thesis, the proportional term and integral term of the PI controller are found with the method of fine-tuning.

In the DQ reference frame, the AC signals appear as DC-like quantities, making them easier to regulate using the PI controller. The DQ reference frame can be obtained using Clarke-Park Transformations. These transformations are utilized to conduct a dynamic analysis of three-phase systems. Clarke-Park Transformations generate a new geometrical representation for three-phase systems. The Clarke transformation converts the three-phase AC quantities (usually voltages or currents) into two orthogonal α and β components, which are represented in a stationary reference frame. This simplifies the analysis of three-phase systems by reducing the complexity from three variables to two variables [38].

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad (3.10)$$

$$V_\alpha = \frac{2}{3}V_A - \frac{1}{3}V_B - \frac{1}{3}V_C \quad (3.11)$$

$$V_\beta = \frac{1}{\sqrt{3}}V_B - \frac{1}{\sqrt{3}}V_C \quad (3.12)$$

After benefiting from the Clarke transformation, the Park transformation converts the α and β components into DQ components [38].

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (3.13)$$

$$V_d = \cos \theta V_\alpha + \sin \theta V_\beta \quad (3.14)$$

$$V_q = -\sin \theta V_\alpha + \cos \theta V_\beta \quad (3.15)$$

In the DQ control method, the peak voltage of the three-phase inverter is determined from the d-axis of the Park transformation, and it is compared to a constant reference voltage to maintain a steady output voltage [37]. The peak of the phase voltage is 12 V. The difference between the measured voltage and the reference voltage is sent to the PI controller, which generates the necessary modulation index. The modulation index determines the amplitude of sinusoidal pulses to produce the gate signals that increase or decrease the output voltage of the inverter. The schematic of the control algorithm using the DQ frame is provided in Figure 3.9.

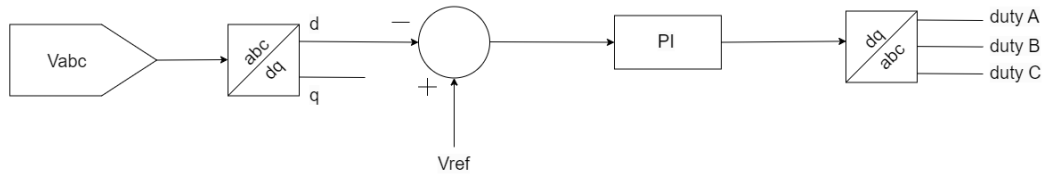


Figure 3.9: The Control Algorithm of Three-Phase Inverter

The simulation of the control algorithm can be carried out on Simulink. The LCL filter and controller schematics are given in Figure 3.10, 3.11.

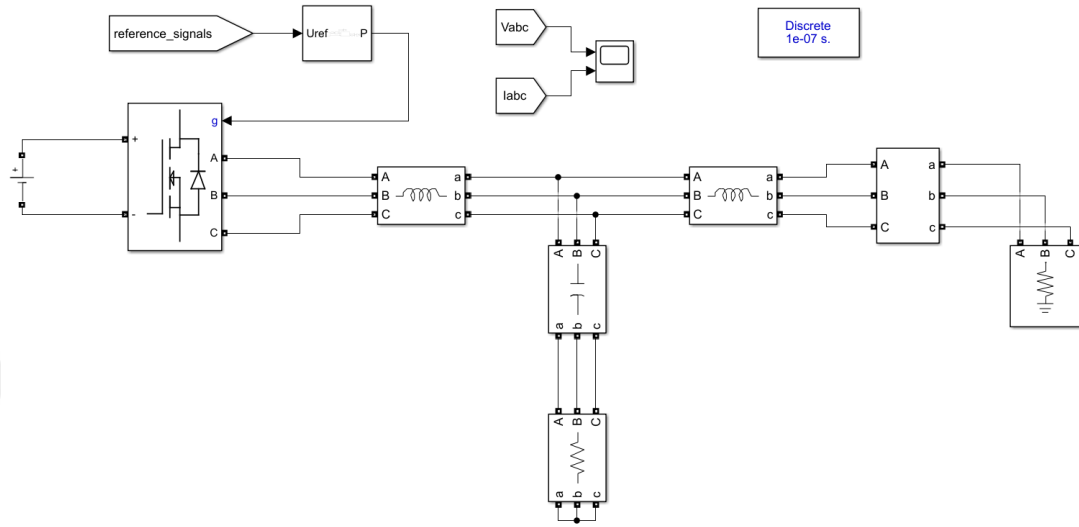


Figure 3.10: The LCL Filter and Measurements of Voltage and Current

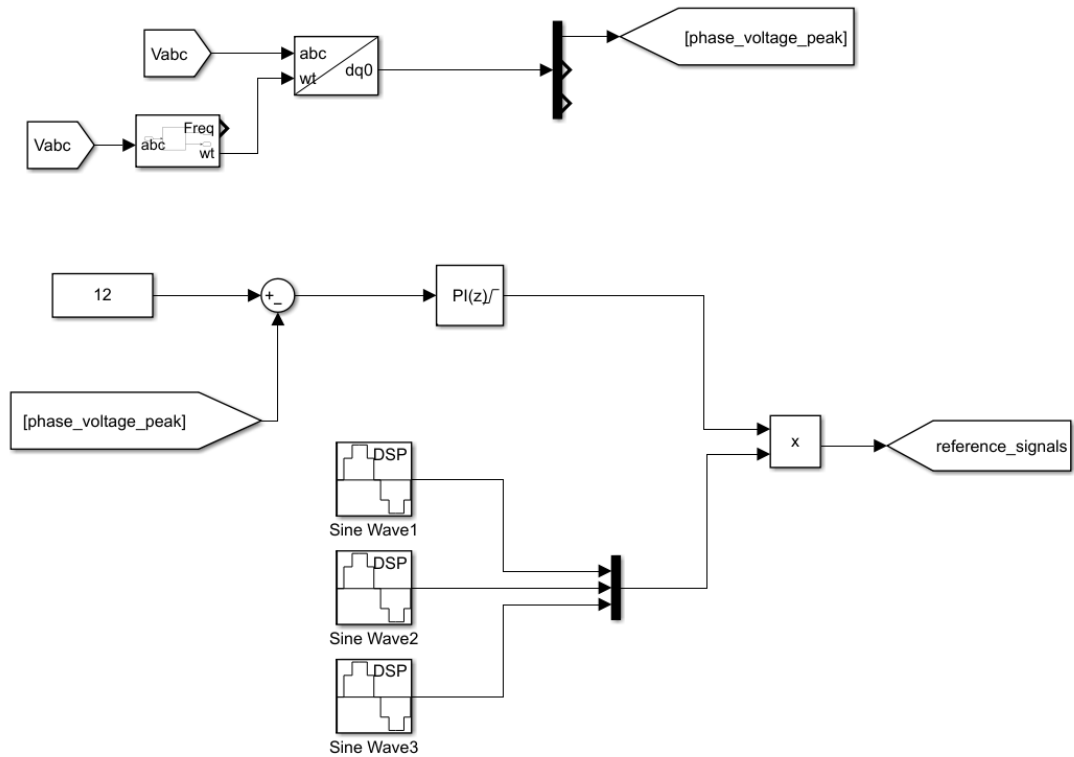


Figure 3.11: The Controller with DQ Transformation and SPWM

The result of the simulation is provided in Figure 3.12.

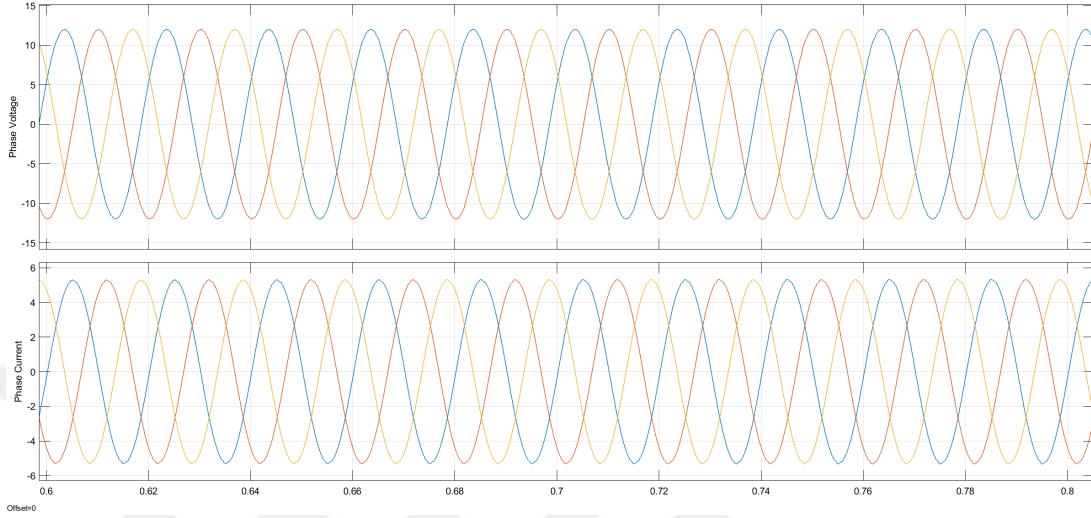


Figure 3.12: The Simulation Result of Controller

The phase voltage and phase current of each phase are shown in Figure 3.12. The quality of the output voltage is adequately high. The total harmonic distortion should also be investigated.

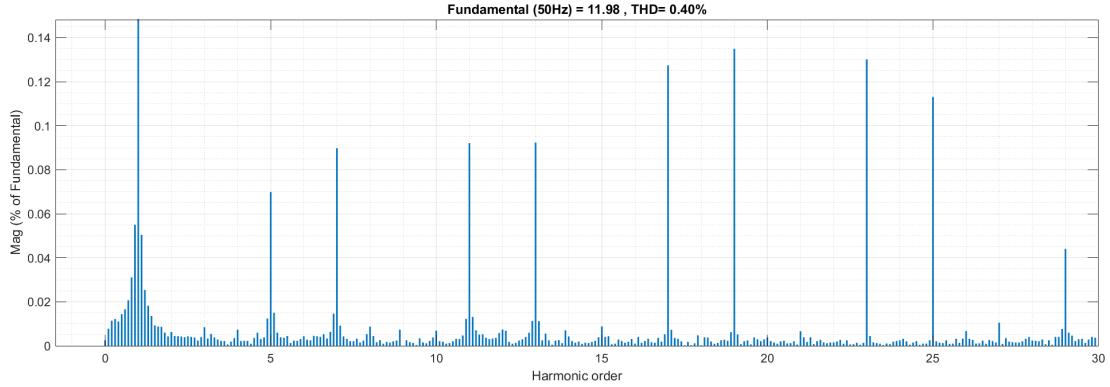


Figure 3.13: The Total Harmonic Distortion Result of Controller

The total harmonic distortion is 0.40 %, which is sufficiently good. Therefore, the controller can be implemented on hardware. This implementation is performed using DSP.

To implement the controller on DSP, the structure of the control algorithm

should be designed. In this application, the digital control algorithm receives inputs from both the user and the circuit. The user states whether the PWMs are enabled or not, and what the peak value of the phase voltage is. On the other hand, The phase voltages come from the circuit located at the LCL filter card. Besides this, the algorithm decides whether the PWMs are generated by sensing the phase currents and input voltage, which satisfies the over-voltage and over-current protections. Over-voltage protection is performed with an input voltage higher than 35 V, and over-current protection is fulfilled with a phase current higher than 7 A. When these conditions occur, the PWMs are not generated. When there is no such situation, the percentage of the duty cycle is determined by the control algorithm. The algorithm flow chart is presented in Figure 3.14.

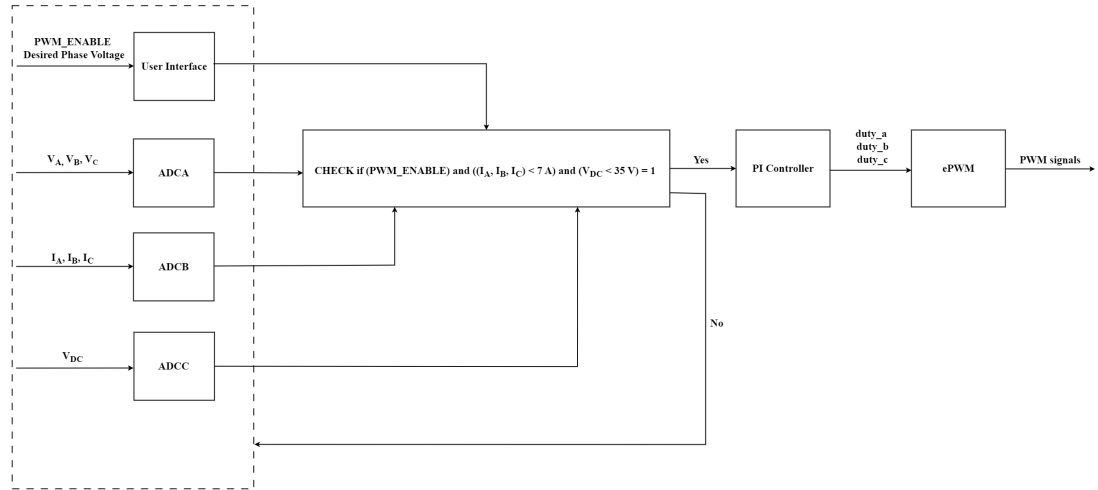


Figure 3.14: Algorithm Flow Chart

Chapter 4

Hardware Implementation and Measurement Results

The hardware implementation of the designed inverter is performed with three main cards. The first one is the main card which contains SMPSSs, gate drivers, and MOSFETs. The second one is the LCL filter card that includes LCL filters and voltage sensing circuits. The third one is the development board called LAUNCHXL-F28379D, and there is also an aluminum plate that includes three loads of $2.2\ \Omega$. Each load can handle a maximum power of 150 W.

4.1 Hardware Implementation

Three-phase inverter card, LCL filter card, development board, and aluminum plate with the load are shown in the following figures.

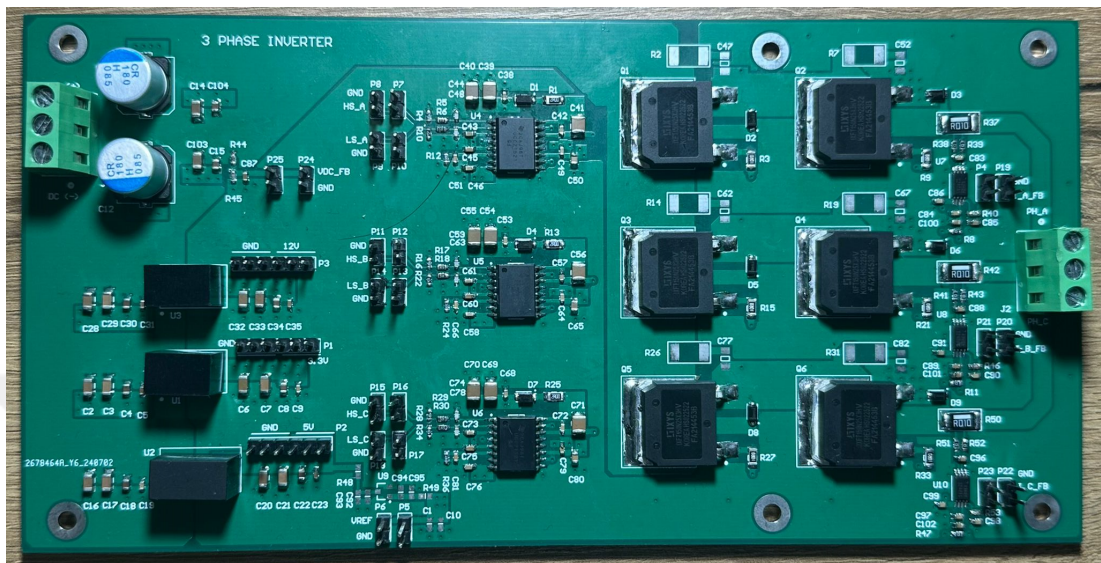


Figure 4.1: Three-Phase Inverter Card

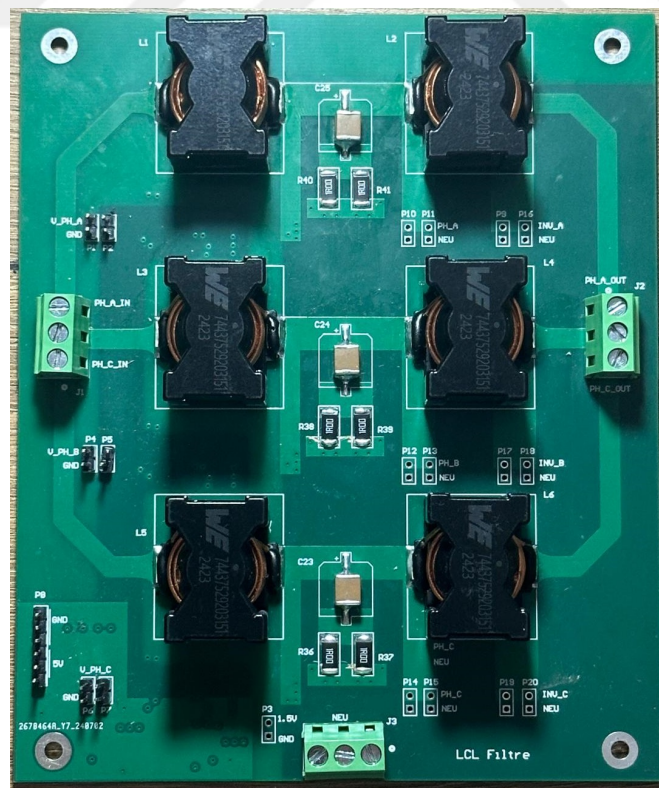


Figure 4.2: LCL Filter Card

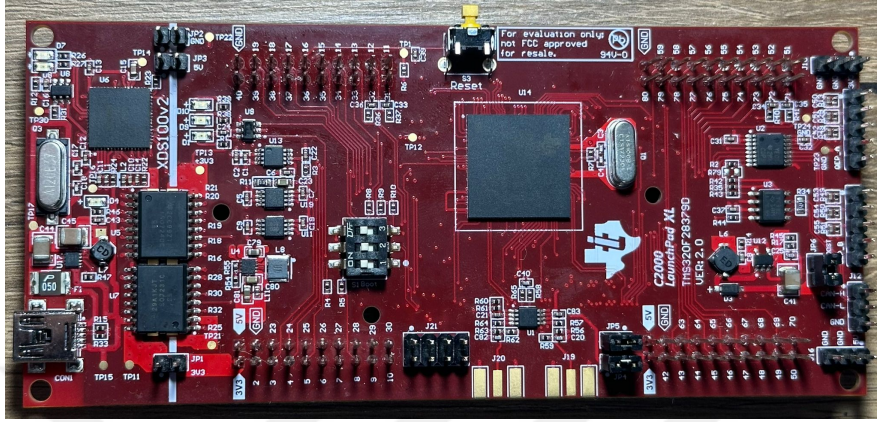


Figure 4.3: Development Board LAUNCHXL-F28379D



Figure 4.4: Three-Phase Load

The hardware setup is built using these three cards and loads. The hardware setup is displayed in Figure 4.5.

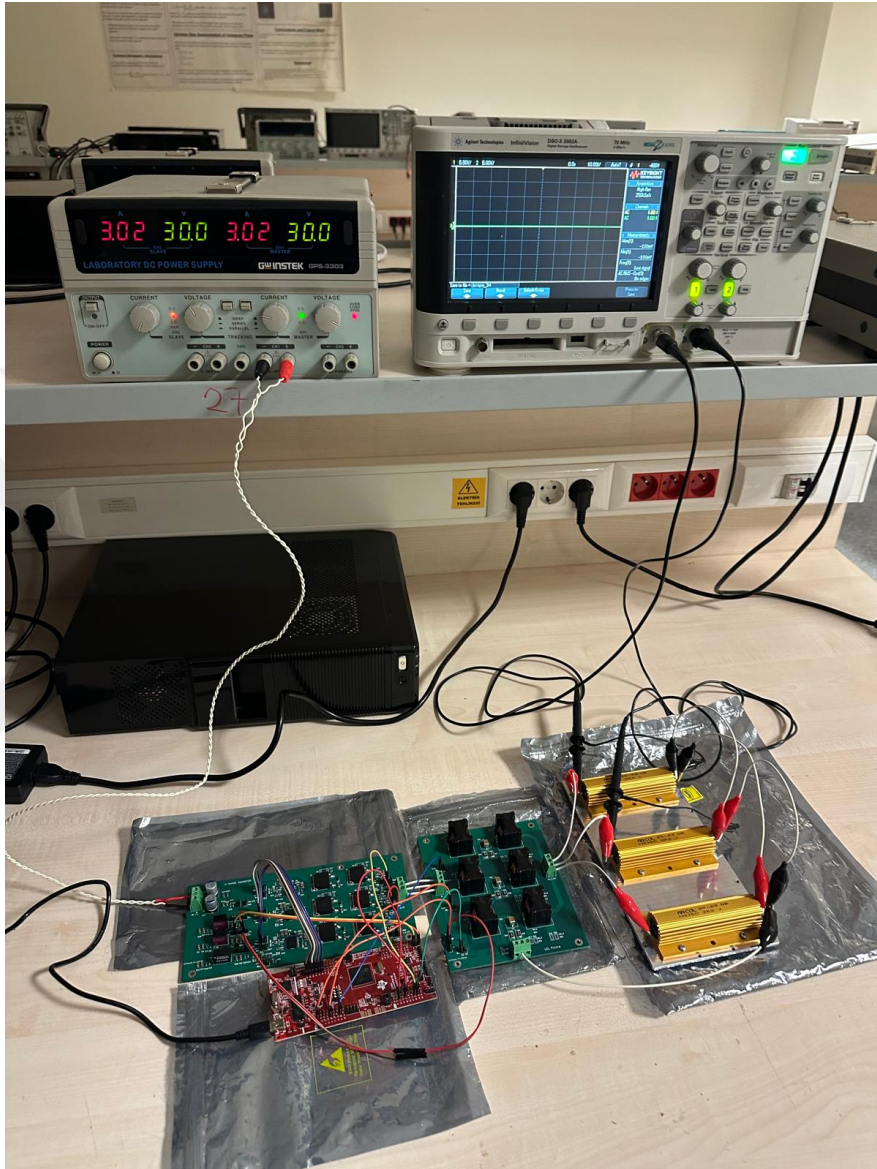


Figure 4.5: Hardware Setup

The results of hardware implementation are shown in the following section.

4.2 Measurement Results

The measurement results contain the no-load current drawn by the DSP and other ICs, phase voltages, efficiency calculations, the Code Composer Studio interface, and the phase current sensed by the current sense amplifier.

The no-load current is shown in Figure 4.6. This current is mainly drawn by DSP.



Figure 4.6: No-load Current

The no-load power is 1.5 W. The phase voltages are shown in the following figures.

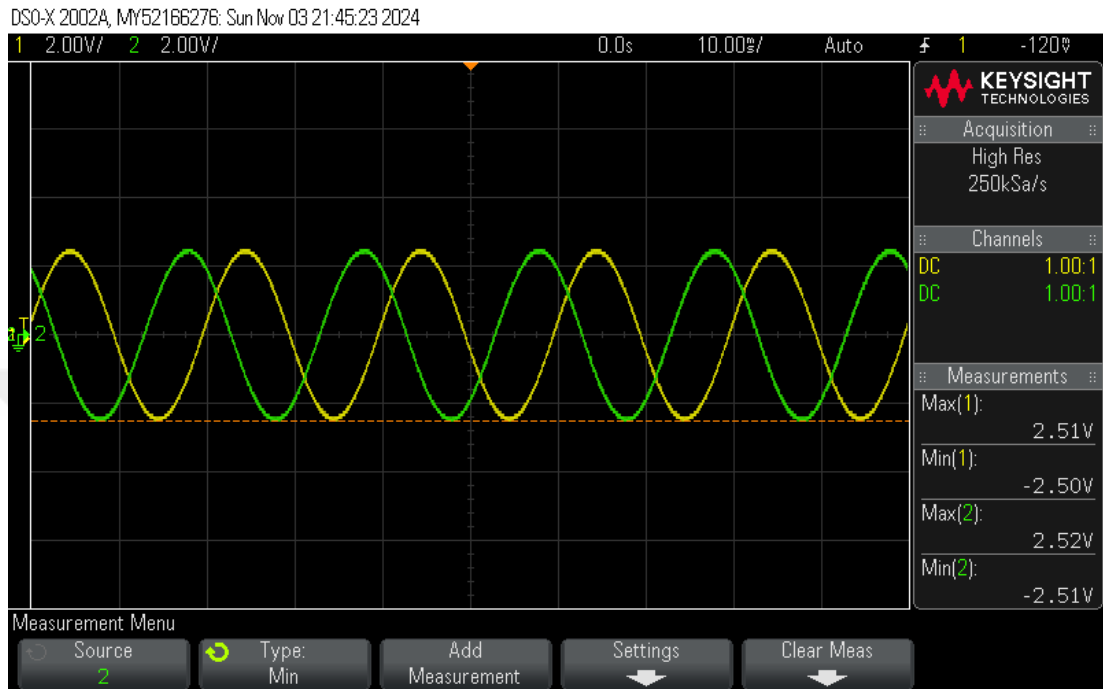


Figure 4.7: 2.5 V Peak Phase Voltage of Phase A and B

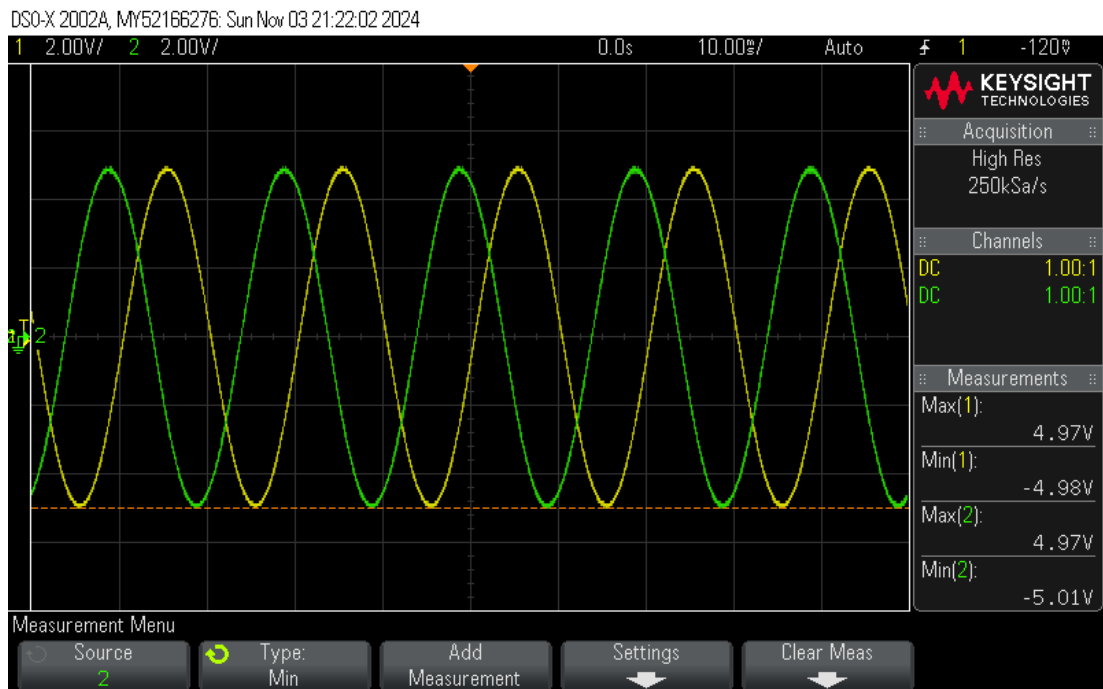


Figure 4.8: 5 V Peak Phase Voltage of Phase A and B

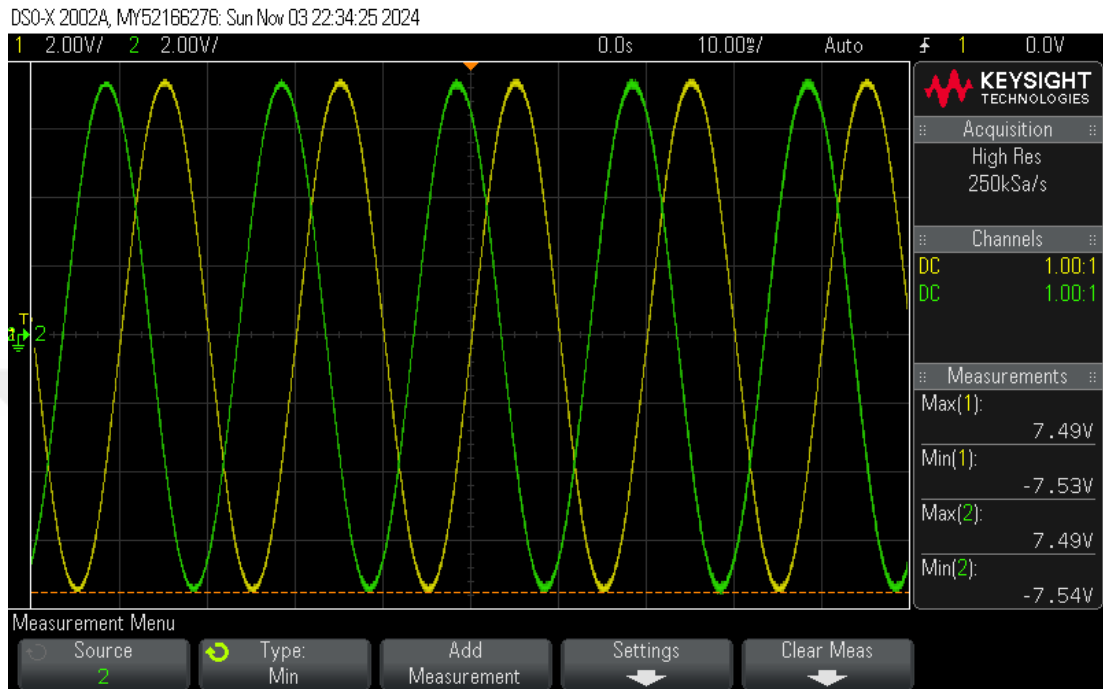


Figure 4.9: 7.5 V Peak Phase Voltage of Phase A and B

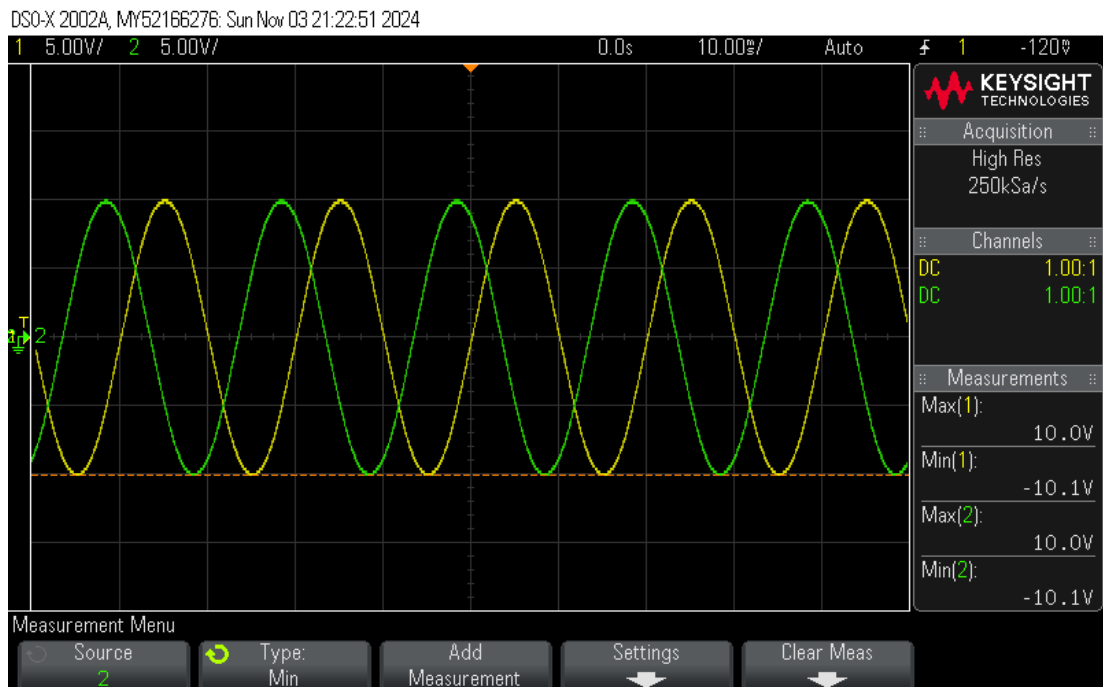


Figure 4.10: 10 V Peak Phase Voltage of Phase A and B

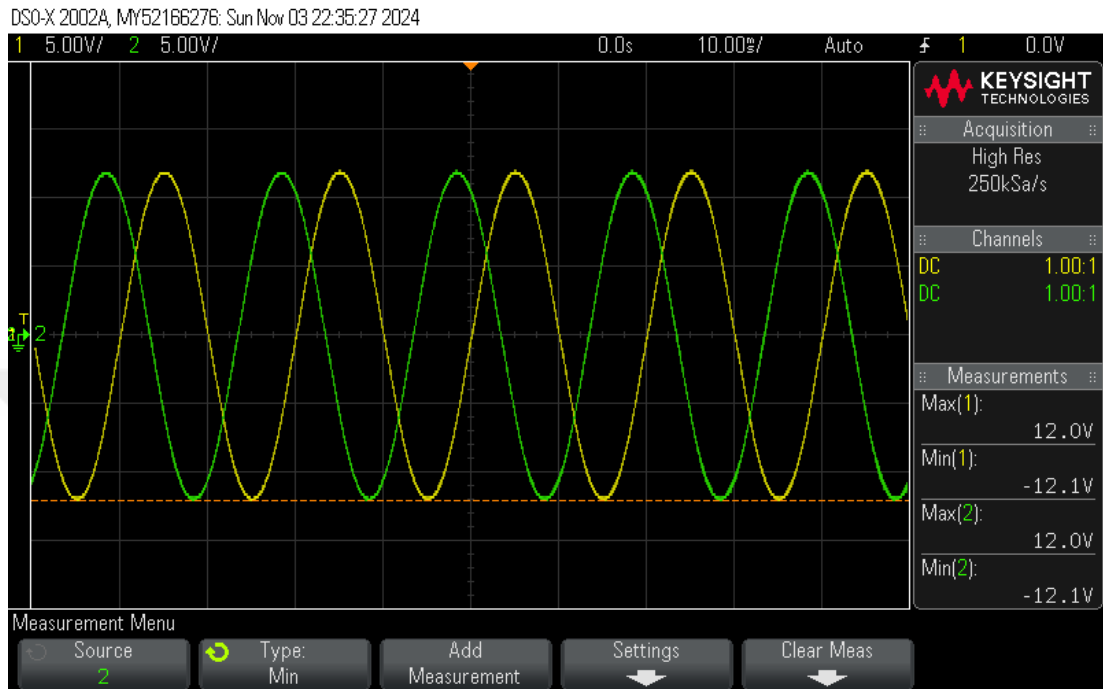


Figure 4.11: 12 V Peak Phase Voltage of Phase A and B

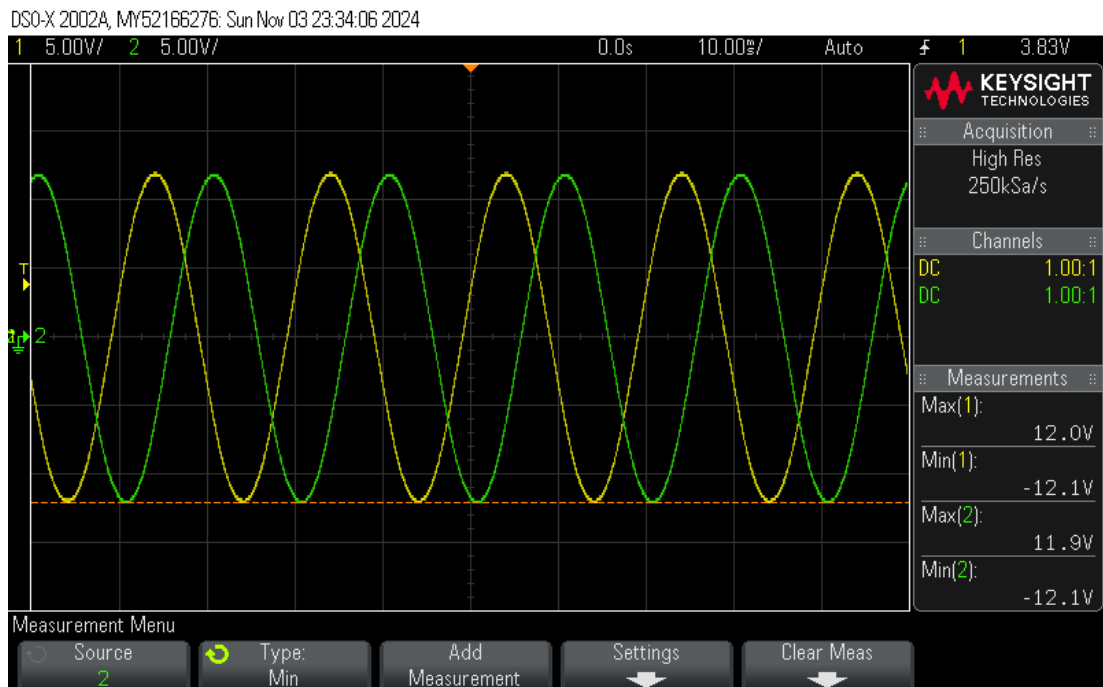


Figure 4.12: 12 V Peak Phase Voltage of Phase B and C

The phase voltage measurements shown with 5 V division include a measurement of offset that results from the oscilloscope. This offset is displayed in Figure 4.13, where there is no output voltage.

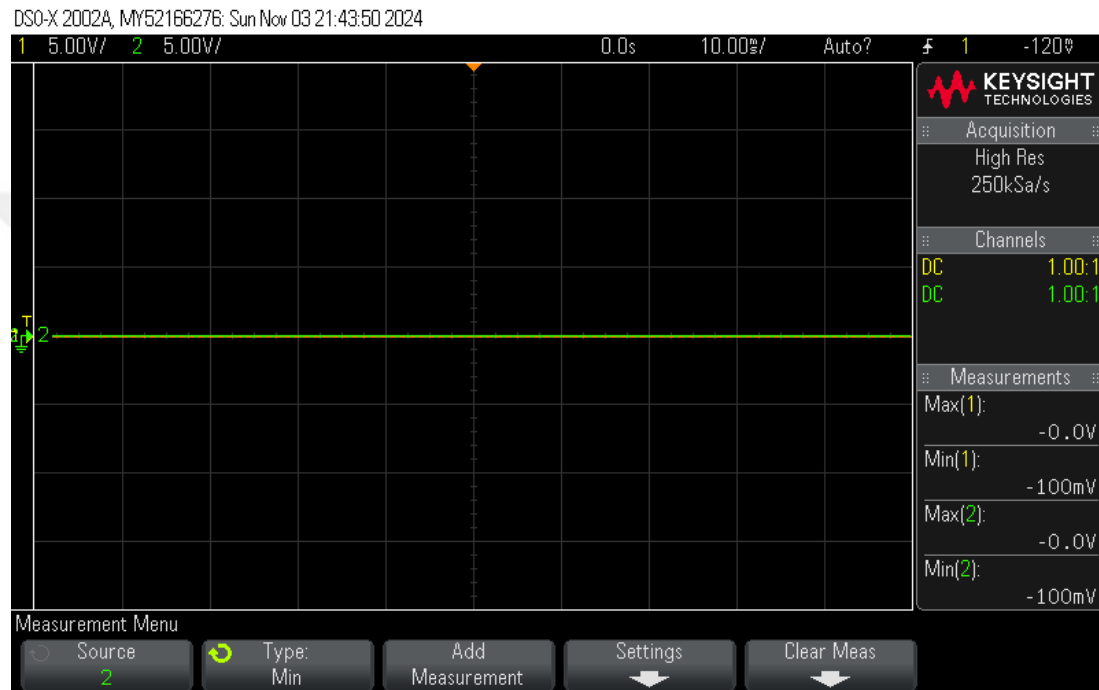


Figure 4.13: Offset from Oscilloscope in 5V Division Measurements

The validation of frequency should be performed for these voltages. This is accomplished with Figures 4.14, 4.15, 4.16, 4.17, 4.18.

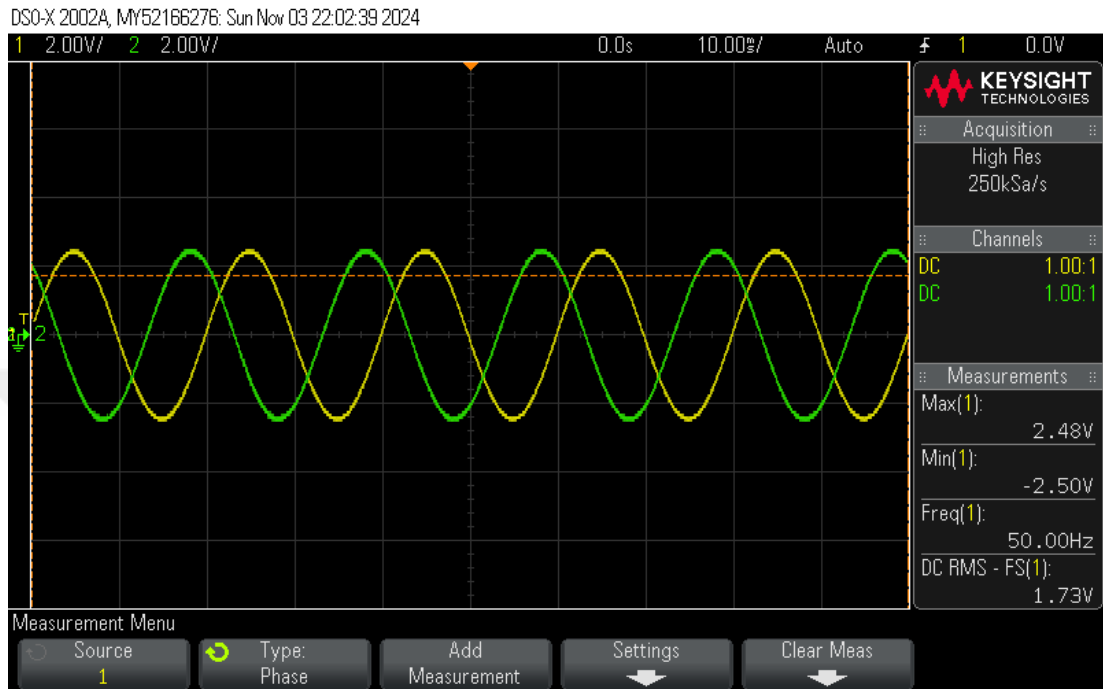


Figure 4.14: 2.5 V Peak Phase Voltage of Phase A

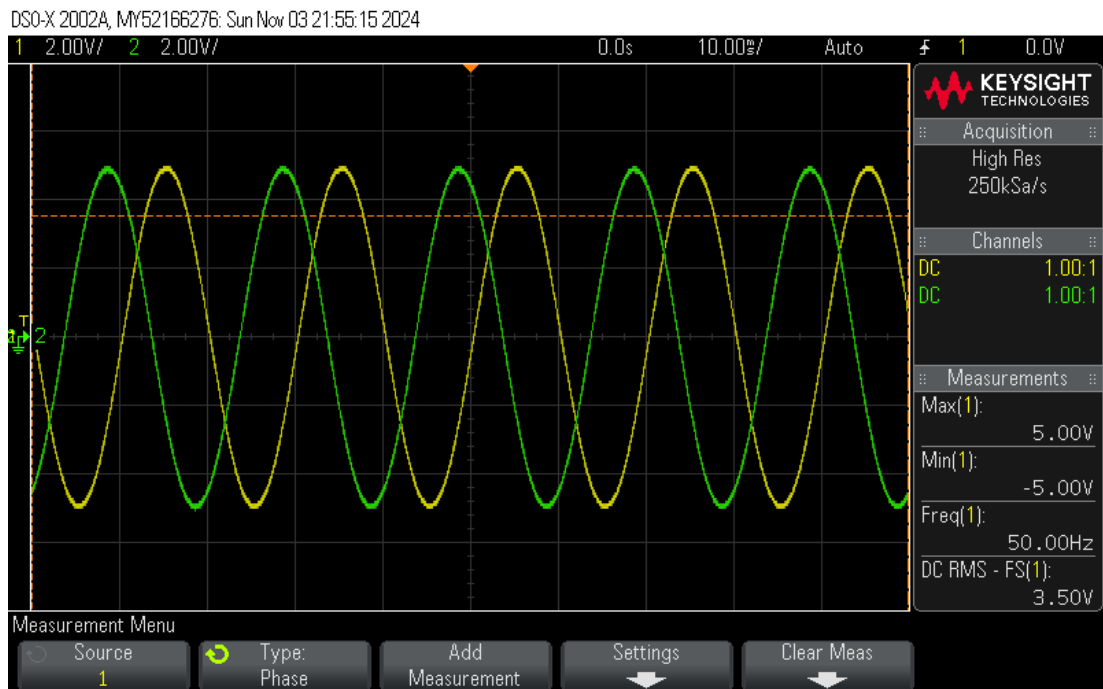


Figure 4.15: 5 V Peak Phase Voltage of Phase A

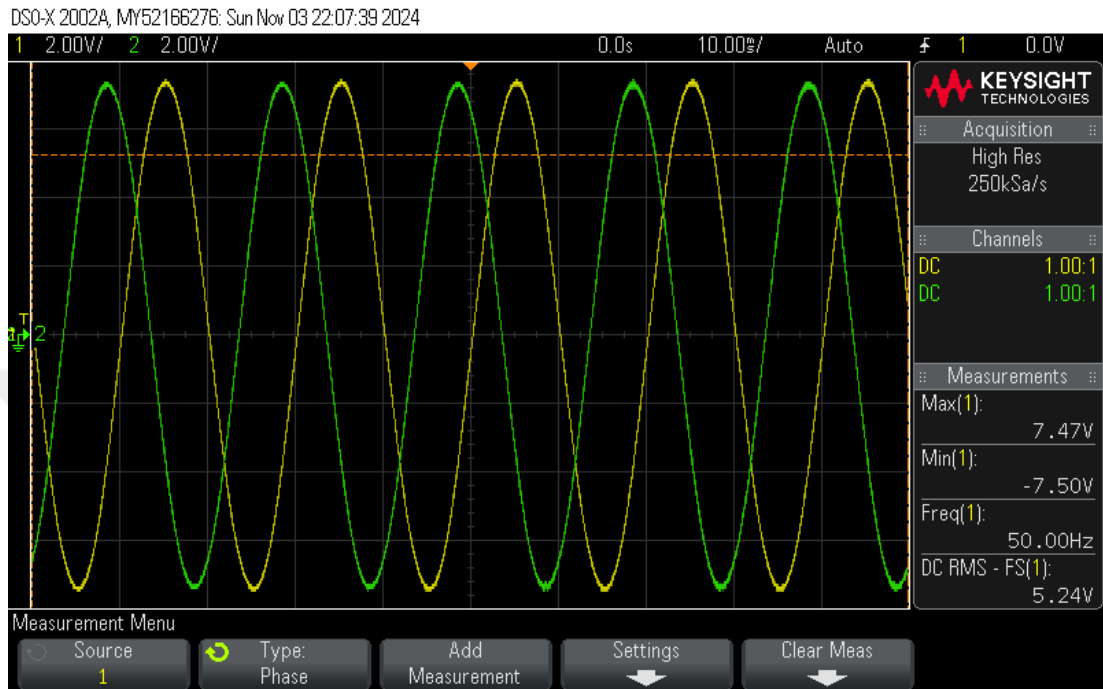


Figure 4.16: 7.5 V Peak Phase Voltage of Phase A

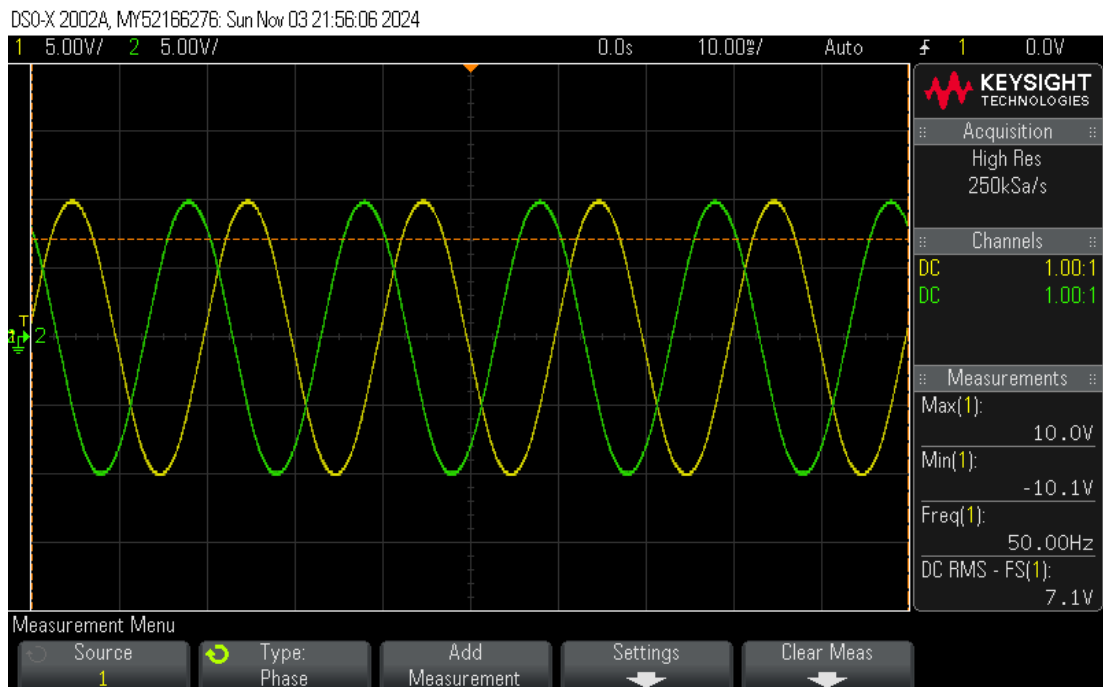


Figure 4.17: 10 V Peak Phase Voltage of Phase A

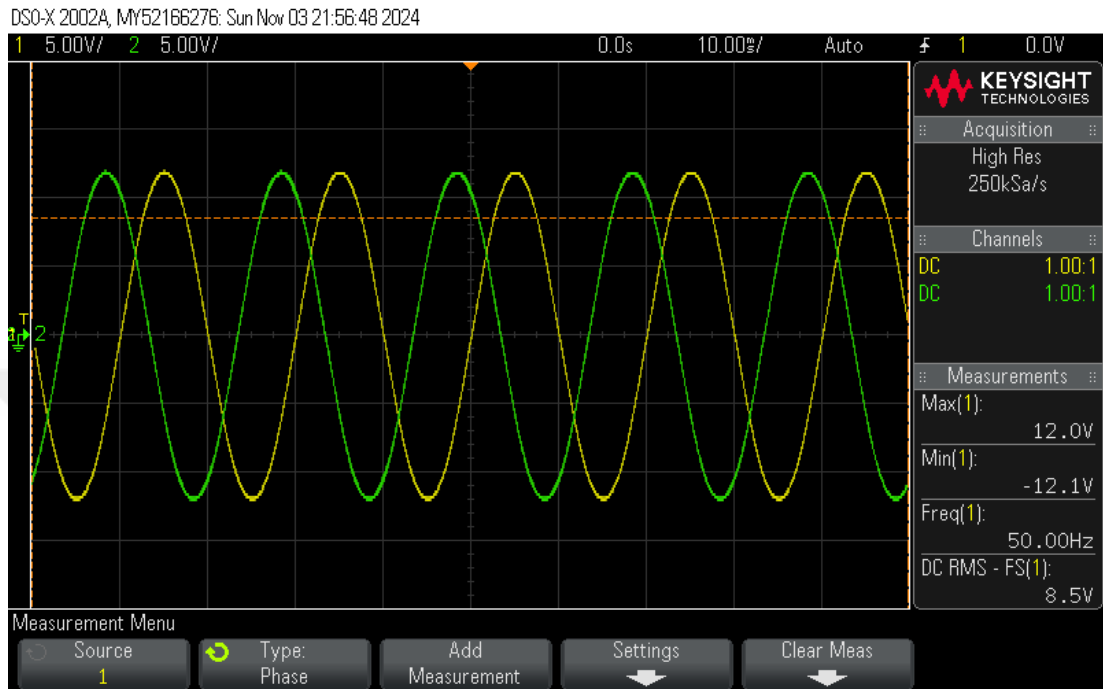


Figure 4.18: 12 V Peak Phase Voltage of Phase A

The system is tested with the nonlinear load in which there is a series diode and a resistor of $2.2\ \Omega$ in each phase. The results of this test are shown in Figures 4.19, 4.20.

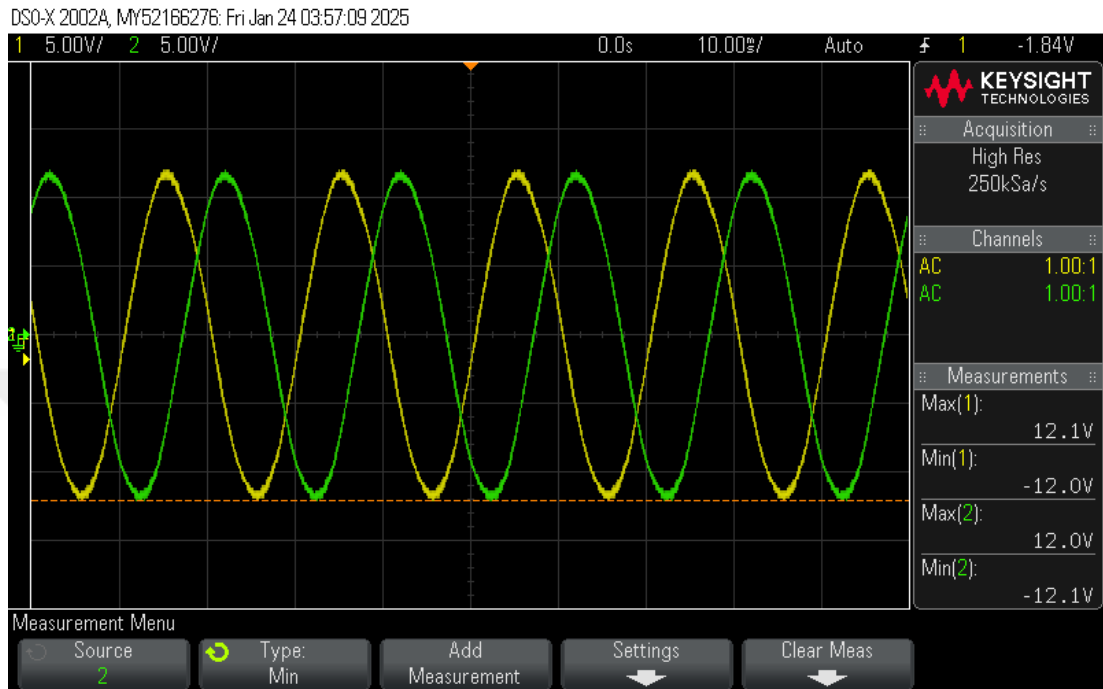


Figure 4.19: 12 V Peak Phase Voltage of Phase A and B

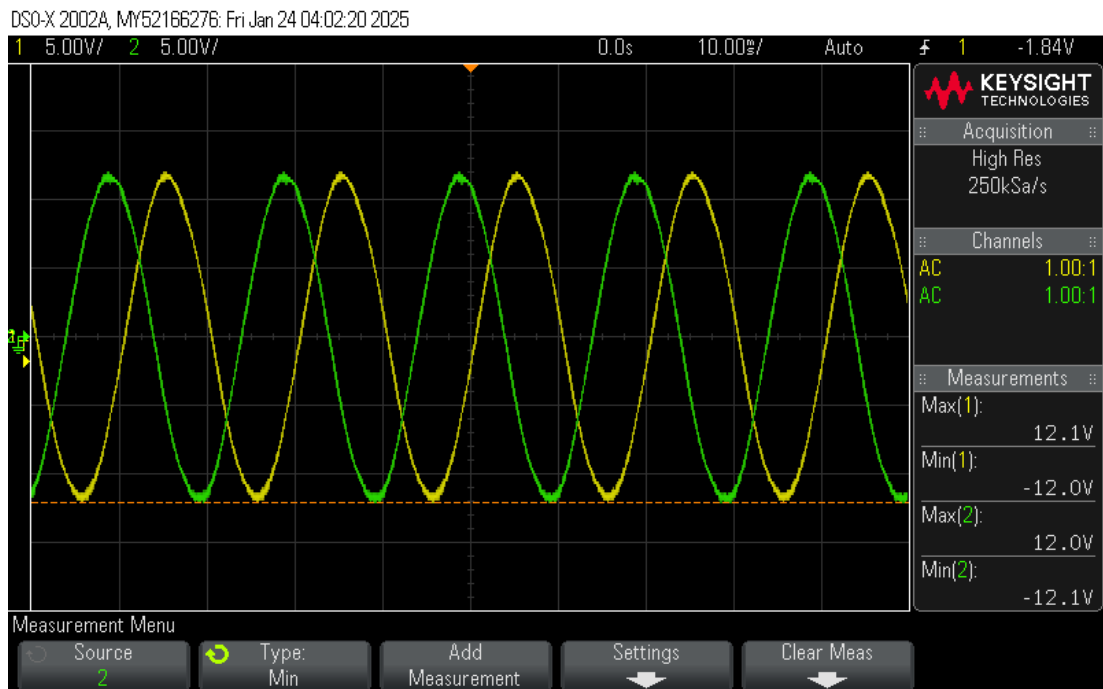


Figure 4.20: 12 V Peak Phase Voltage of Phase B and C

The system is tested with no load. The results of this test are provided in Figures 4.21, 4.22.

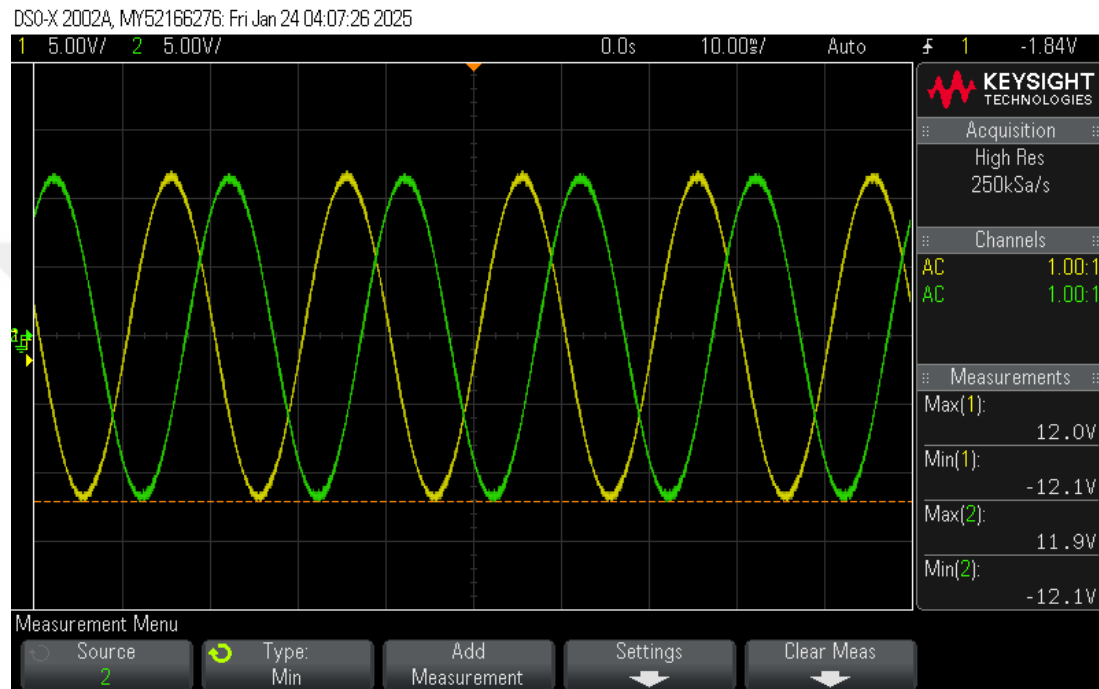


Figure 4.21: 12 V Peak Phase Voltage of Phase A and B

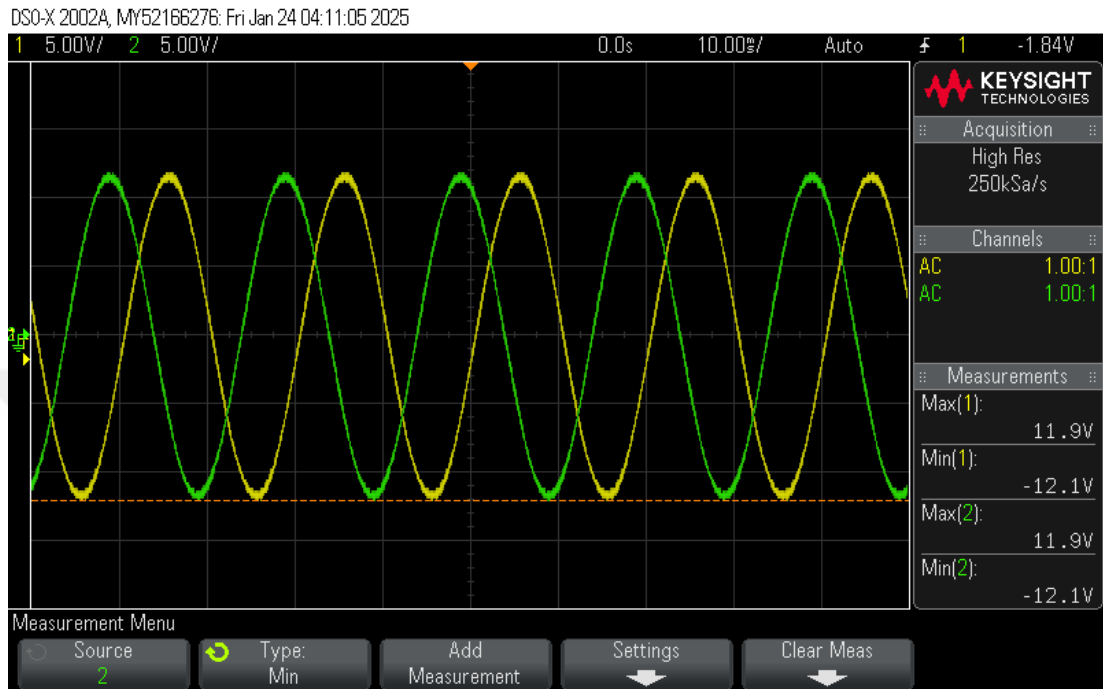


Figure 4.22: 12 V Peak Phase Voltage of Phase B and C

The system is tested with an imbalanced load in which Phase A and Phase B are connected to $2.2\ \Omega$ and Phase C is connected to $3.3\ \Omega$. The results of this test are provided in Figures 4.23, 4.24.

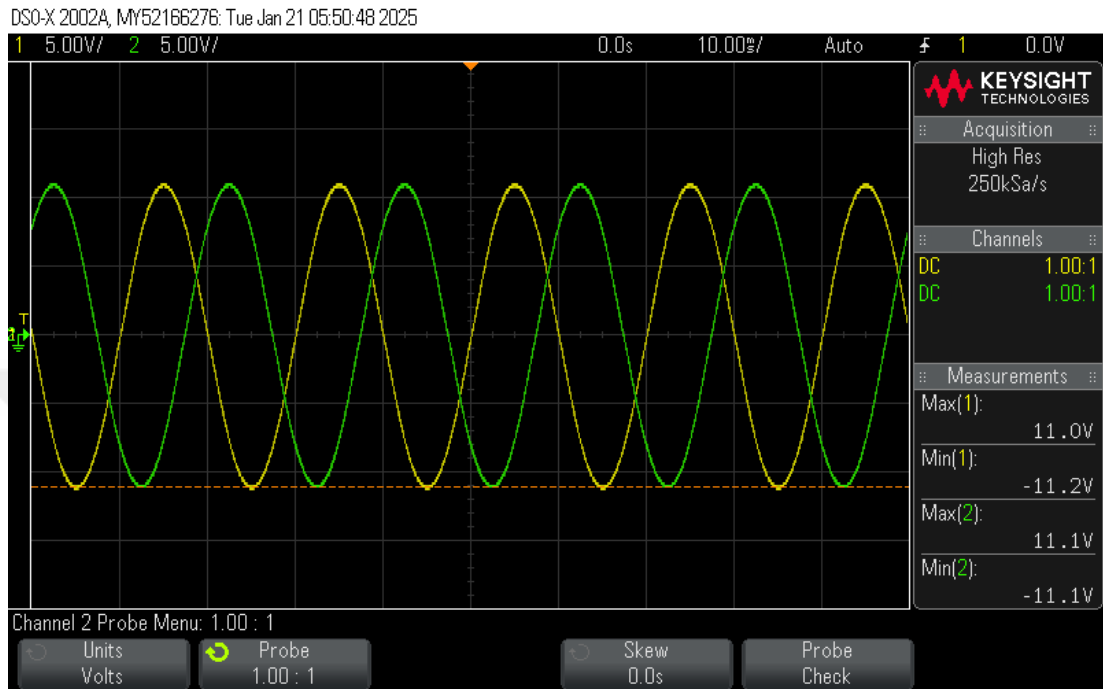


Figure 4.23: 12 V Peak Phase Voltage of Phase A and B

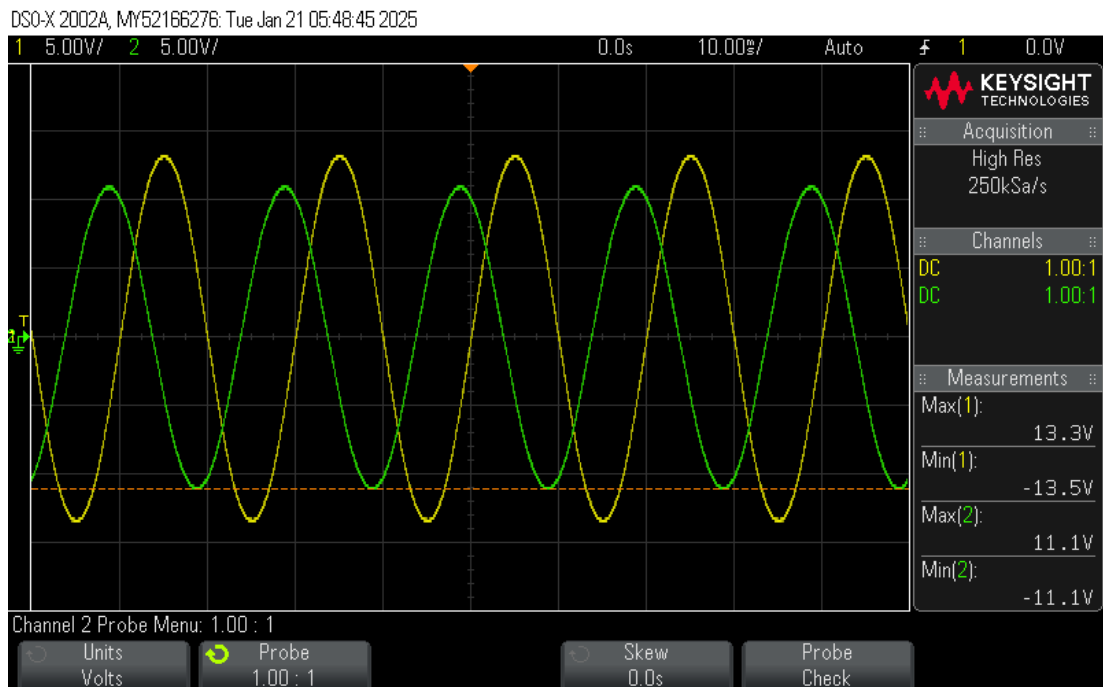


Figure 4.24: 12 V Peak Phase Voltage of Phase B and C

These results indicate that when there is an imbalanced load at the output, the controller attempts to equalize the phase voltage with the reference voltage. However, in this system, there is no neutral pin obtained through the division of capacitors at the input. Therefore, the current lacks a complete path to flow, and an imbalance in voltage occurs. The phase voltage of the phase with the higher load increases.

The efficiency calculation should be performed using Figures 4.14, 4.15, 4.16, 4.17, 4.18.

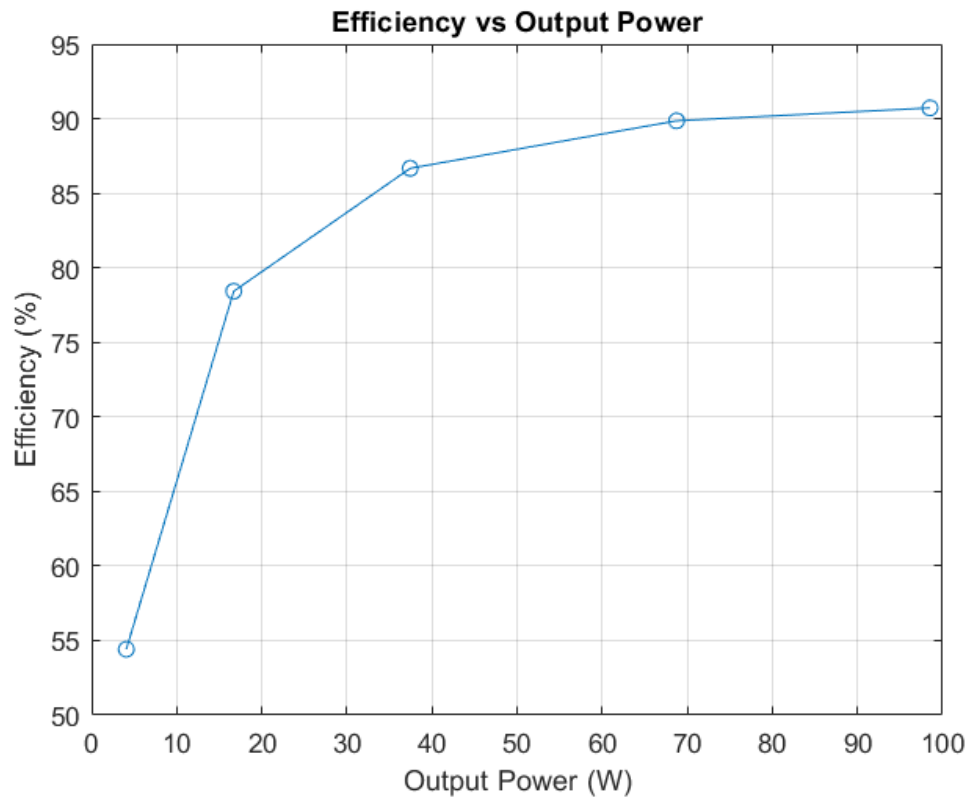


Figure 4.25: Efficiency vs Output Power

The efficiency of the three-phase inverter is shown in Figure 4.25. This calculation includes the no-load power mainly drawn by the DSP. The no-load power is 1.5 W; this power is shown in Figure 4.6. When this power is not included, efficiency increases. Especially at low output powers, the power of DSP becomes

critical for efficiency. As the output power increases, this power becomes negligible and changes the efficiency to only 1 or 2 %. When a MOSFET with a lower drain-to-source voltage is used, the efficiency can be improved further since drain-source on-resistance becomes lower.

The Code Composer Studio interface is given in Figure 4.26. Using this interface, the input and output parameters of the three-phase inverter can be determined and/or monitored.

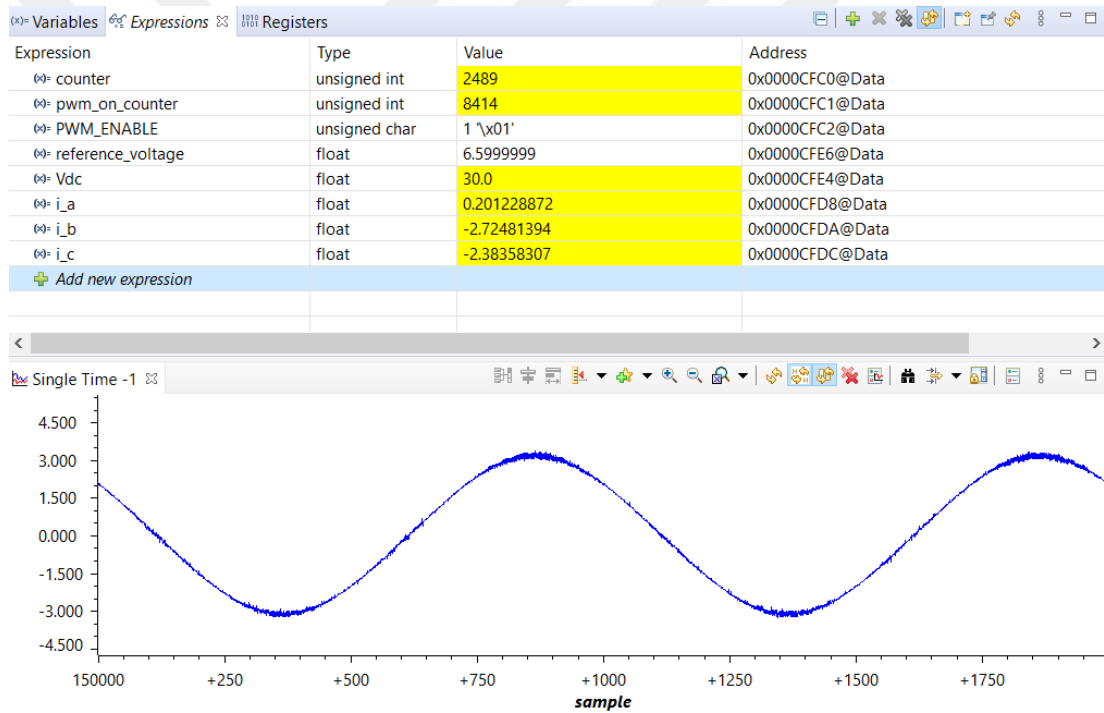


Figure 4.26: CCS Interface

The reference voltage and PWM enabling can be adjusted on Code Composer Studio. The phase current can also be examined on the interface. When the peak value of phase current is 3 A, two periods of cycles are shown in Figure 4.26. The input DC voltage can also be monitored on the interface. If the input voltage exceeds 35 V, PWMs are disabled, which implies input over-voltage protection. The short-circuit protection circuit is also tested.

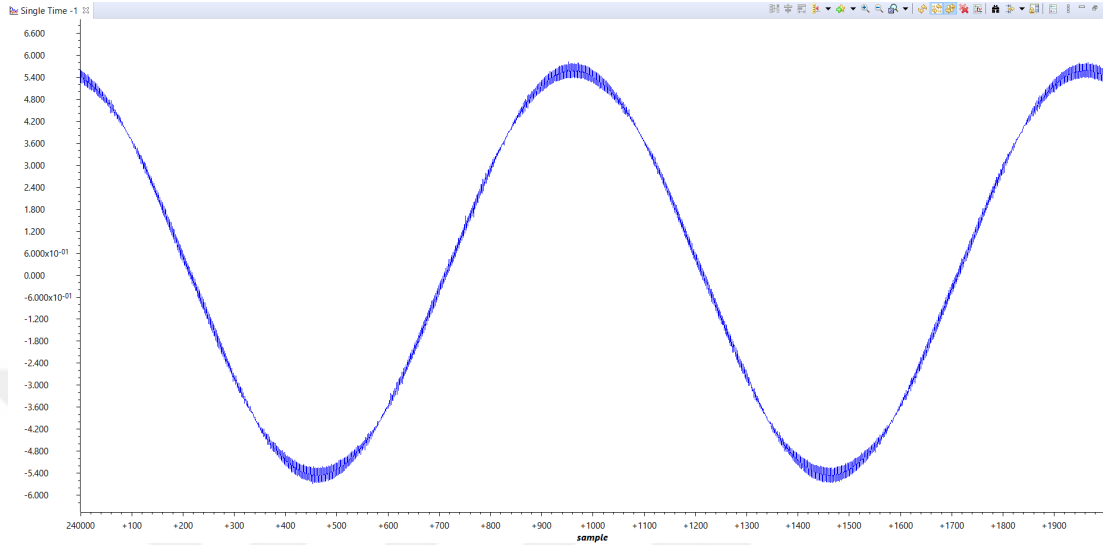


Figure 4.27: Phase Current on CCS Interface

The phase current on the CCS interface is shown in Figure 4.27. At the full load, the peak value of phase current is 5.45 A, which is sensed correctly by the current sense circuit. When the current is above 7 A, PWMs are disabled, which verifies the over-current protection circuit. The limits of over-voltage and over-current protections can be adjusted.

Chapter 5

Conclusion

In this thesis, a three-phase inverter is designed using the DSP of TMS320F28379D on which an advanced control algorithm with the combination of SPWM and DQ reference frame is implemented. To attenuate harmonics in the phase outputs, various filter topologies, namely L, LC, and LCL, are evaluated based on existing literature. Provided its superior attenuation, the LCL filter is selected for implementation.

In the design process of the three-phase inverter, we first start with the decision on the digital controller. TMS320F28379D is included in a common development board, and it is well-suited for inverter applications. The second task is to determine the control algorithm. Then, the type of passive filter is specified. The LCL filter provides a high attenuation for harmonics. After that, the design of a voltage sense circuit is critical since the control algorithm takes the phase voltages as input and generates the modulation index and so PWMs accordingly. Finally, the protection circuits are designed. These are over-voltage and over-current protections. To fulfill over-voltage protection, the input voltage is monitored continuously. Over-current protection is satisfied with the sense of output phase currents. These currents are sensed by a current sense amplifier located at each phase.

The peak output voltage of the three-phase inverter is 12 V with a frequency of 50 Hz. The maximum output power is 98.5 W with an efficiency of 90.72 % without any heat sink or additional cooling components. This system works properly with a balanced load, and the inverter also works with nonlinear loads as long as the load is balanced.

In the future, we plan to design a heat sink and mechanical design, which will enable an increase in the output power. Besides this, to increase the output power, the value of components in the LCL filter needs to be calculated again. The new components might have to be selected.

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discrete_mosfets_n-channel_ultra_junction_ixf_150n25x3_datasheet.pdf.pdf, [Accessed: Nov. 15, 2024].

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