X-BAND LOW PHASE NOISE MMIC VCO & HIGH POWER MMIC SPDT DESIGN

A THESIS

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND

ELECTRONICS ENGINEERING

AND THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

MASTER OF SCIENCE

By

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June, 2014

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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June, 2014

Generally the tuning bandwidth (BW) of a VCO is smaller than the tuning BW of the resonant circuit itself. Using proper components with right topology can handle this problem. In order to overcome this problem and improve the tuning BW of the VCO, common-base inductive feedback topology with Gallium Arsenide (GaAs) Heterojunction Bipolar Transistor (HBT) is used and an optimized topology for tank circuit is selected to minimize the effect of bandwidth limiting components. Designed VCO with this topology achived -117 dBc/Hz at 1 MHz offset phase noise with 9-13 dBm output power between 8.8-11.4 GHz band. Second part of the thesis composed of Single Pole Double Throw (SPDT) RF Switch design. From mesa resistors to SPDT fabrication, everything is fabricated using Bilkent University NANOTAM Gallium Nitride (GaN) on Silicon Carbide (SiC) process. Switching HEMTs are fabricated to generate a model to design SPDTs and the final design works between DC-12 GHz with less than 1.4 dB insertion loss (IL), -20 dB isolation and 14.5 dB return loss (RL) at worst case. The power handling of the switches are better than 40 dBm at output with 0.2 dB compression, which is measured with continuous wave (CW) signal at 10 GHz.

Keywords: MMIC, VCO, Phase Noise, SPDT, GaAs, GaN, CPW, HEMT, HBT.

ÖZET

X-BANT DÜŞÜK FAZ GÜRÜLTÜLÜ VCO & YÜKSEK GÜÇLÜ SPDT TASARIMI

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Düşük faz gürültülü osilatörler resonatör devresinin bant genişliği ile karşılaştırıldığında genellikle daha dar bir banda sahiptirler. Doğru bir topoloji ve uygun devre elemanları ile bu sorun çözülebilmektedir. Galyum Arsenit (GaAs) temelli HBT' nin base ucuna bir bobin eklenerek elde edilen yapı ile uygun bir resonans devresi sayesinde bant genişliğini kısıtlayan devre elemanlarının etkisi en aza indirilebilmektedir. Bu yapı ile tasarlanan VCO ile 8.8-11.4 GHz aralığında 9-13 dBm çıkış gücünde, 1 MHz ofsette -117 dBc/Hz faz gürültüsü elde edilmiştir. Tezin ikinci kısmı ise Single Pole Double Throw (SPDT) RF anahtar tasarımından oluşmaktadır. Mesa dirençlerinden SPDT üretimine kadar tüm işlemler Bilkent Üniversitesi NANOTAM' da Silikon Karbid (SiC) üzerine Galyum Nitrat (GaN) işlemi kullanılarak üretilmiştir. Öncelikle anahtarlama transistörleri üretilerek SPDT tasarımı yapabilmek için model çıkarılmıştır. Bu model ile üretilen anahtar yapıları DC-12 GHz aralığında 1.4 dB' den az araya girme kaybı (IL), -20 dB' den iyi yalıtım ve en kötü durumda 14.5 dB geriye dönüş kaybı ile çalışabilmektedir. Ayrıca 10 GHz' de sürekli sinyal altında 0.2 dB' den az kompresyon ile 40 dBm' lik çıkış verebilmektedir.

Anahtar sözcükler: MMIC, VCO, Phase Noise, SPDT, GaAs, GaN, CPW, HEMT, HBT.

Acknowledgement

I would like to thank my advisor Dr. Tarık Reyhan for the continuous support of my study and research, for his patience, motivation, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis.

I would like to thank Prof. Dr. Ekmel Özbay for his support and guidance in the projects.

I would like to thank Dr. Özlem Şen for her support in RF Switch project.

I would like to thank the rest of my thesis committee: Prof. Dr. Yusuf Ziya İder and Prof. Dr. Atilla Aydınlı for being a part of my thesis committee.

I would also like to thank my family: my parents Gülbiye and Seyfi Osmanoğlu and my elder brother Kamuran Osmanoğlu. They were always supporting me and encouraging me with their best wishes.

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Chapter 1

Introduction

Any RF/Microwave system requires a signal source to operate. The quality of the signal source is very important to process the received/transmitted data successfully. There are some properties of a signal source like linearity, stability, signal purity, bandwidth, phase noise etc.

In a transceiver system, an RF switch which is a front-end component has crucial importance. An RF switch has to be capable of switching high powers at higher frequencies with low loss and high isolation. When system receives a relatively low power signal, the loss of the RF switch is critical and isolation is crucial when transmitting a high power signal to prevent damage to the receiver part.

This thesis is focused on designing both a VCO (voltage controlled oscillator) and an SPDT (single pole double throw) switch which are the critical components of both receiver and transmitter parts of an RF/microwave system. The characteristics of these components directly effects the quality of the whole system. In this thesis, low phase noise property of a VCO and low loss-high isolation properties of an SPDT switch in X-band are studied. Low phase noise VCO is designed using a commercial GaAs based HBT foundry process of WIN semiconductors. For the SPDT switch, GaN based HEMT on SiC process with CPW (Coplanar Waveguide) technology of Bilkent University Nanotechnology Research Center

(NANOTAM) is preferred.

1.1 Organization of Thesis

This thesis is composed of two main sections. First part is the Low Phase Noise VCO and the second main section is about SDPT switch.

Chapter 2 revisits the basic theory of phase noise starting with the definition of long term and short term stability. Then describes common noise terms.

Chapter 3 presents the design steps of low phase noise VCO using a CAD tool. Layout and EM simulations are added in this part with the results like bandwidth, output signal, phase noise and etc. Besides, resonator design with quality factor is discussed in this chapter.

Chapter 4 presents a summary of the phase noise measurement techniques along with their advantages and drawbacks. General block diagrams of the measurement setups are depicted in this chapter.

Chapter 5 is allocated to switch theory, modelling and design. Starting with a single series HEMT, modelling is explained with measurement methods. Using this model, SPST switches are fabricated to optimize the model and SPDTs are designed at the end.

Chapter 6 contains the comparison of the designs with other state-of-the art designs and the discussion of the contributions of this thesis with possible future suggestions.

Chapter 2

Background

2.1 Phase Noise

Phase noise is an important performance criterion for the state-of-the-art systems. In many cases, designers may not notice the effect of phase noise on the system, because they have no familiarity with phase noise. In a system with multiple subcarriers with a limited bandwidth, effect of the LO with average phase noise performance can be observed clearly.

In any oscillator design, there are some criteria which are of critical importance. These are headed by frequency stability which can be observed as long-term and short-term stability. Frequency variations that occur over hours, days, months, or even years on the output signal related with long-term frequency stability. Short-term stability, on the other hand, is describing the variations that occur over a period of seconds or less. These variations can be random or periodic and are called as phase noise.

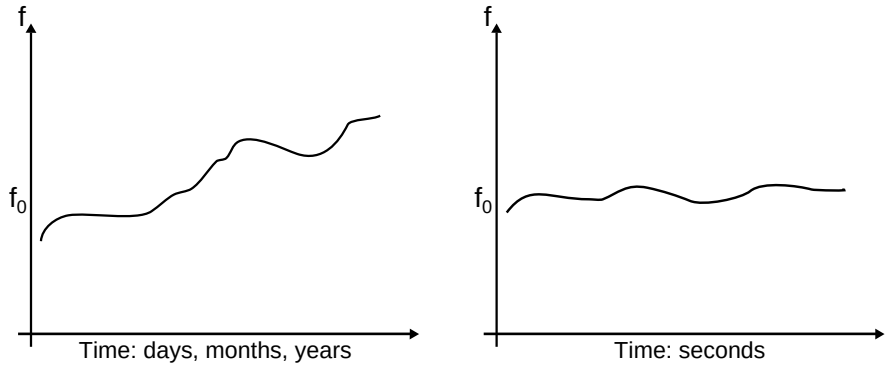


Figure 2.1: Long-term (left) and short-term (right) stability

Output signal of an ideal oscillator can be represented by Eq.2.1 and its spectrum is expected to have an impulse at the frequency of oscillation as in Fig.2.2. However the spectrum of practical oscillator does have skirts around the oscillation frequency due to phase noise and can be represented as in Eq.2.2 and Fig.2.3.

$$V(t) = A_0 sin(\omega_0 t) \tag{2.1}$$

$$V(t) = (A_0 + \epsilon(t))sin(\omega_0 t + \varphi(t)) \tag{2.2}$$

where;
A_0: nominal amplitude,
ω_0: nominal frequency,
$\epsilon(t)$: random amplitude changes,
$\varphi(t)$: random phase changes

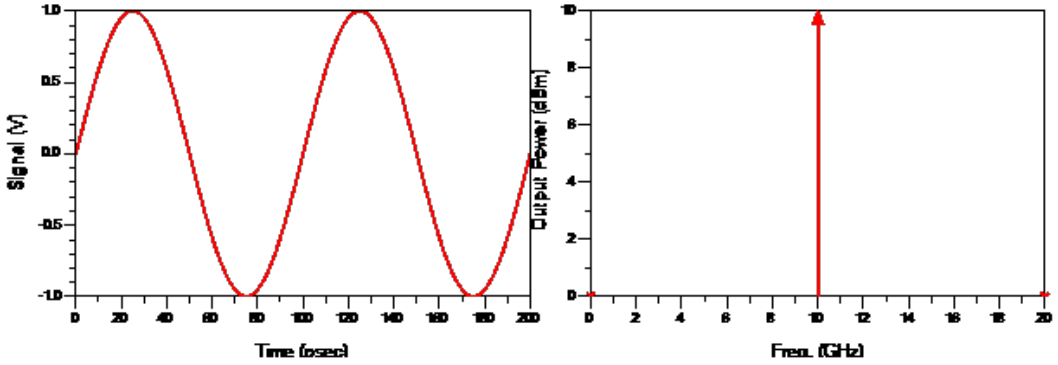


Figure 2.2: Ideal sine wave (left), Frequency spectrum (right)

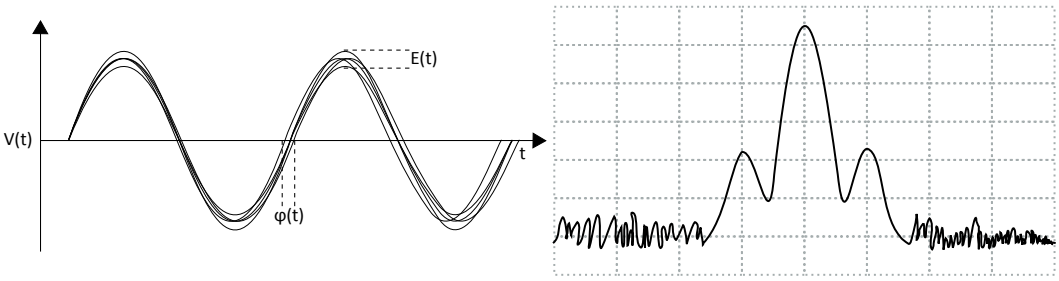


Figure 2.3: Real-world sine wave

In this thesis, short-term stability which is commonly referred as phase noise is primarily studied. Phase noise is random fluctuations in the phase of a signal, contributed by the various components and circuits within a generator, which disperses the output power to the surrounding frequencies. Ideally, the power of a synthesized continuous wave (CW) signal is all located at a single frequency. This can be modeled as random phase modulation. The units of phase noise (referred to as $L(f)$) are measured in dBc/Hz or dB down from the measured carrier power in a 1 Hz bandwidth for frequency offsets from the CW output.

$$S_{\varphi}(f_m) = \frac{\Delta^2_{\varphi}(f_m)}{BW}[\frac{rad^2}{Hz}] \tag{2.3}$$

where;

$S_{\varphi}(f_m)$: double sideband (DSB) phase noise,

f_m: offset frequency

Most of the time phase noise is described as single sideband (SSB) and it is the half of DSB noise. SSB phase noise, $L(f_m)$, can be shown by Eq.2.4.

$$L(f_m) = \frac{1}{2} S_\varphi(f_m) \tag{2.4}$$

As defined earlier SSB phase noise is likewise expressed in relation to the carrier power normalized to a 1Hz BW:

$$L(f_m) = \frac{P_{SSB}}{P_{carrier}}(dBc/Hz) \tag{2.5}$$

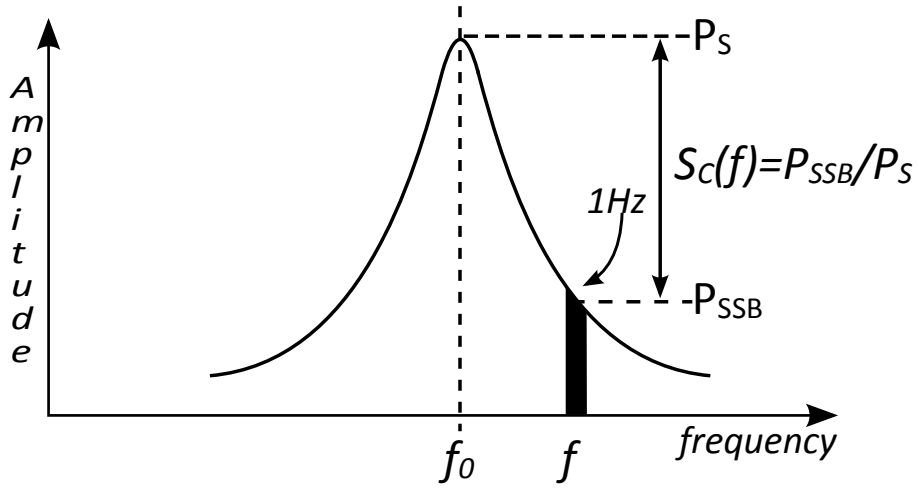


Figure 2.4: Single Sideband Phase Noise

2.2 Thermal Noise and Noise Figure

Thermal noise, Johnson noise or Nyquist noise, is the electronic noise generated by thermally agitated charge carriers inside an electrical conductor [1]. Because of the random nature of the noise, the value of voltage cannot be identified at a specific time, only statistical concepts like the expected value of υ^2 which is equal to the rms under certain conditions is possible [2]. Available noise power at absolute temperature is given by

$$P_{NA} = kT\Delta f \tag{2.6}$$

where k is the Boltzmann's constant ($1.38 \times 10^{-23} J/K$), T is the absolute temperature in Kelvins and Δf is the noise bandwidth in Hertz over which the measurement is made. From Eq.2.6 one can calculate the available noise power over a 1Hz BW is about 4×10^{-21} W or -174 dBm at room temperature. This level is also known as thermal noise floor. This power level includes both amplitude and phase noise portions of the thermal noise [3]. As we are interested with just the phase noise part, we can exclude the amplitude noise part from the power by dividing it two as their contributions are considered equally. Then, thermal noise level from the phase noise part is

$$P_{NA-phase} = \frac{P_{NA}}{2 \times \Delta f} = \frac{kT}{2} \tag{2.7}$$

result is -177dBm/Hz and it can be used as the thermal limit [3]. As it was stated previously that phase noise is measured in dBc/Hz, it will be convenient to use $P_{NA-phase}$ in dBc/Hz.

In a network, any active component like amplifier will contribute to thermal noise floor. This contribution can be represented as

$$P_{NA-phase} = \frac{kT\Delta f}{2}(dB) + NF(dB) \tag{2.8}$$

where NF is the noise figure of the noise figure of the associated amplifier. One can relate the noise floor to the input power and express in terms of $L(f_m)$,

$$L(f_m) = \frac{kTF}{2P_{in}}(dBc/Hz) \tag{2.9}$$

where f_m is the offset frequency and F is the noise figure. Eq.2.9 represents the phase noise floor according to thermal noise relating with the input power, P_{in}, in dBm. Once the P_{in} is 0 dBm, then the phase noise floor stays at -177dBc/Hz. Each increase in input power level, also improves the phase noise floor level.

2.3 Flicker Noise

Noise near DC stays unconverted, with coefficient c_0, so 1/f noise becomes $1/f^3$ noise near the carrier; noise near the carrier stays there, weighted by c_1; and white noise is downconverted which is near higher integer multiples of the carrier, turning into noise in the $1/f^2$ region. Fig.2.5 represents both upward and downward frequency translations of noise into the noise near the carrier [2][4].

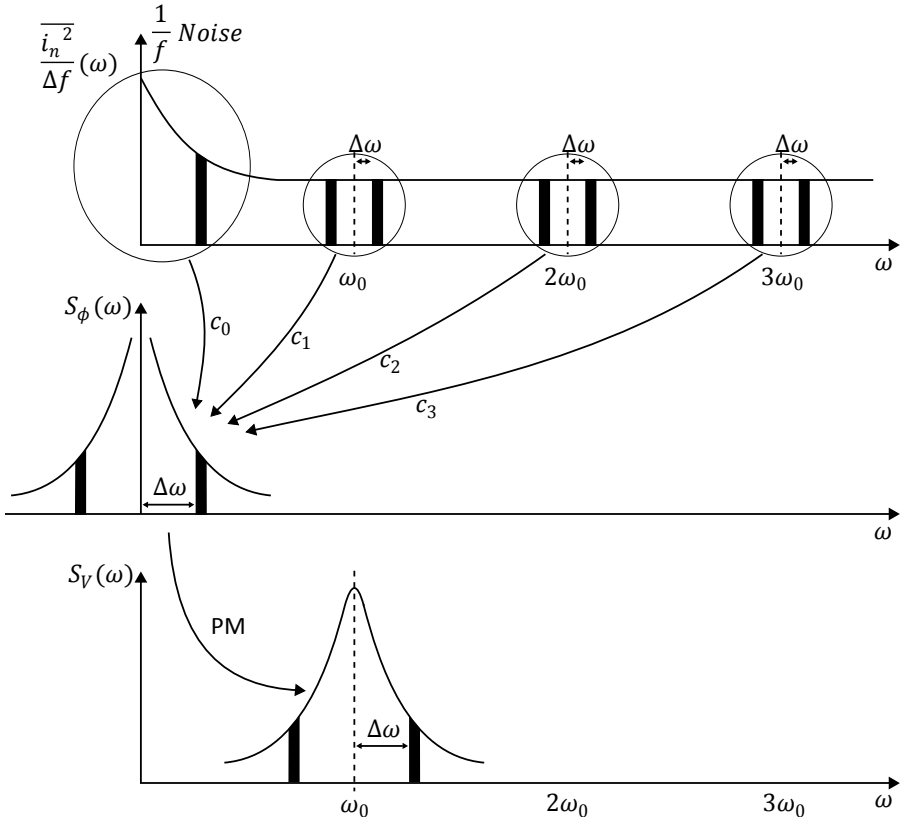


Figure 2.5: Coversion of Noise

The flicker noise affects the spectral purity of the carrier at frequencies close to the carrier and shows a 1/f component with a corner frequency known as f_c. With the effect of flicker noise $L(f_m)$ may be re-written by adding the f_c factor;

$$L(f_m) = 10\log_{10}[(\frac{kTF}{2P_{in}})(1+\frac{f_c}{f_m})](\frac{dBc}{Hz}) \tag{2.10}$$

2.4 Phase Noise in Oscillators

2.4.1 Oscillator Basics

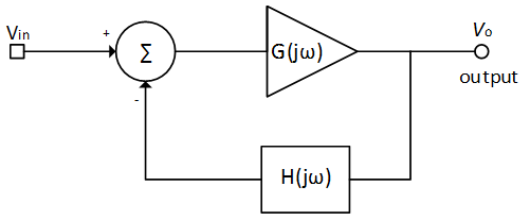


Figure 2.6: Basic Oscillator Block Diagram

An oscillator is a kind of electronic device which is capable of producing periodic AC signals. Oscillators convert dc power to RF signals. There is a well-known linear technique to describe the oscillator analysis and design, which is called as Barkhausen Criteria.

The block diagram of a simple feedback system is represented in Fig.2.6 and it represents all necessary blocks for an oscillator. In this block diagram, $G(jw)$ represents the frequency dependent gain of an amplifier and H(jw) represents the frequency dependent feedback network. In oscillator case, $H(jw)$ is the resonator and $G(jw)$ is the frequency dependent amplifier.

In this thesis a parallel resonator is introduced, so it can be modeled with a parallel resonance circuit like in Fig.2.7 where L is the inductor, C is the capacitance. These two components determine the resonance frequency ω_0 and the resistor R is used to indicate the losses in the resonant circuit.

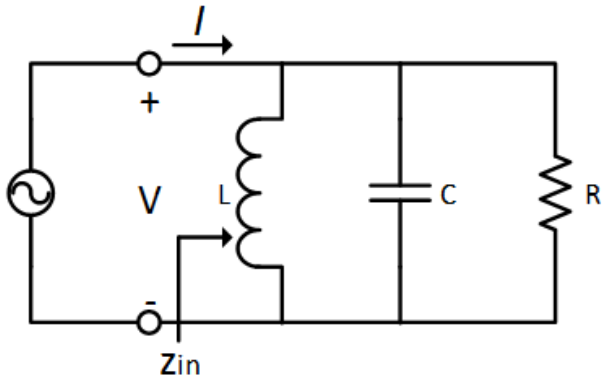


Figure 2.7: Parallel Resonance Circuit

The Q (quality factor) of the resonator is strictly related with the value of the resistor R and the input impedance of the circuit is:

$$Z_{in} = (\frac{1}{R} + \frac{1}{j\omega L} + j\omega C)^{-1} \tag{2.11}$$

From Eq.2.11, resonance frequency can be found by equating the imaginary part of the equation to zero. When the imaginary part is zero, stored energy oscillates between the capacitor and inductor. If there is no loss, this oscillation lasts forever but the losses deteriorate the oscillation. When the imaginary part is zero:

$$\frac{1}{\omega_0 C} = \omega_0 L \tag{2.12}$$

then the oscillating frequency is:

$$\omega_0 = \sqrt{\frac{1}{LC}} \tag{2.13}$$

The quality of the resonator then can be defined as in Fig.2.8 with the bandwidth of the resonance curve as it has direct relation with the losses. then Q is represented by:

$$Q = \frac{R}{\omega_0 L} = \omega_0 C \tag{2.14}$$

Now it is time to derive to relation between the input and output of Fig.2.6, which is called as the transfer function of the network.

$$\frac{v_o}{v_i} = \frac{G(j\omega)}{1 + G(j\omega)H(j\omega)} \tag{2.15}$$

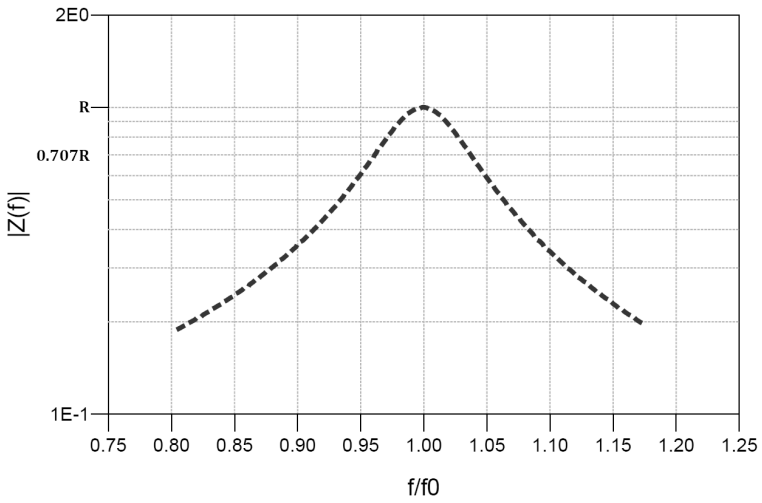


Figure 2.8: Normalized bandwidth

In an oscillator circuit, output voltage v_o is nonzero when v_i is zero and this only possible if the $G(j\omega)$ is infinite and this phenomena can be represented by:

$$1 + G(j\omega)H(j\omega) = 0 \tag{2.16}$$

At the specific frequency ω_0:

$$G(j\omega)H(j\omega) = -1 \tag{2.17}$$

$$|G(j\omega)H(j\omega)| = 1 \tag{2.18}$$

Eq.2.18 represents that the magnitude of the open loop gain should be one at the steady state and the phase shift should be:

$$\arg[G(j\omega)H(j\omega)] = \pm n360^\circ \qquad (n = 0, 1, 2, \ldots) \tag{2.19}$$

Eq.2.18 and Eq.2.19 explains the oscillation condition also called as Barkhausen (Nyquist) Criterion. These equations also show under what conditions a feedback system can start to oscillate. Namely; the open-loop gain must be greater than unity at the point at which the total phase shift is 360° in order to start oscillation. For a stable oscillation Eq.2.18 and Eq.2.19 must be fulfilled.

2.5 Leeson Phase Noise Model

Leeson Model is used to estimate the output spectral density of phase noise of an oscillator. The main components of the system are the noiseless amplifier, phase modulator and the resonator as depicted in Fig.2.9. As described in basics of oscillator part, resonator is assumed to be a parallel resonant circuit. The phase noise at the input of the noise-free amplifier is bandwidth limited and determined by the Q of the resonator.

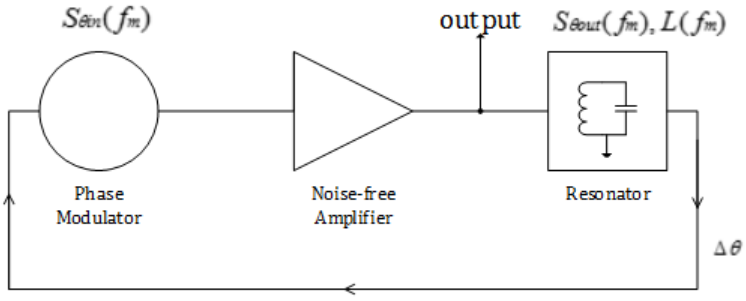


Figure 2.9: Model of an oscillator for noise analysis

As the resonator modeled by a parallel resonant circuit, the resonator has a low-pass transfer function described with the following equation:

$$L(\omega_m) = \frac{1}{1 + j(2Q_L\omega_m/\omega_0)} \tag{2.20}$$

where Q_L is the loaded Q of the resonator, ω_0 (rad/s) is the resonance frequency and ω_m is the carrier offset (rad/s), and $\omega_0/2Q_L$ is the half-bandwidth of the resonator. From Eq.2.20, the closed loop response of the phase feedback can be written by the following equation:

$$\Delta v_{out}(f_m) = (\frac{1}{1 + j(2Q_L\omega_m/\omega_0)})\Delta v_{in}(f_m) \tag{2.21}$$

Then the power transfer function is:

$$S_{v_{out}}(f_m) = [1 + \frac{1}{f_m^2}(\frac{f_0}{2Q_L})^2]S_{v_{in}}(f_m) \tag{2.22}$$

where;

$$S_{v_{in}}(f_m) = \frac{FkT}{P_{s,av}}(1 + \frac{f_c}{f_m}) \tag{2.23}$$

then;

$$L(f_m) = \frac{1}{2}[1 + \frac{1}{f_m^2}(\frac{f_0}{2Q_L})^2]S_{v_{in}}(f_m) \tag{2.24}$$

$$L(f_m) = \frac{1}{2}[1 + \frac{1}{f_m^2}(\frac{f_0}{2Q_L})^2]\frac{FkT}{P_{s,av}}(1 + \frac{f_c}{f_m}) \tag{2.25}$$

$L(f_m)$: Phase Noise (dBc/Hz)
Q_L: Loaded Q
f_m: carrier offset frequency (Hz)
f_0: carrier center frequency (Hz)
f_c: flicker corner frequency of the active device (Hz)
T: temperature $(^\circ K)$
$P_{s,av}$: average power through the resonator (W)
F: noise factor of the device
k: Boltzman constant (J/K)
kT: $4 \times 10^{-21} W$

Reordered case Eq.2.24 becomes:

$$L(f_m) = \frac{FkT}{2P_{s,av}}[1 + \frac{f_c}{f_m} + (\frac{f_0}{2f_mQ_L})^2(1 + \frac{f_c}{f_m})] \tag{2.26}$$

$$L(f_m) = 10\log_{10}\{\frac{FkT}{2P_{s,av}}[1 + \frac{f_c}{f_m} + (\frac{f_0}{2f_mQ_L})^2(1 + \frac{f_c}{f_m})]\} \tag{2.27}$$

Eq.2.27 is known as Leeson phase noise equation. It identifies the most significant causes of phase noise in oscillators.

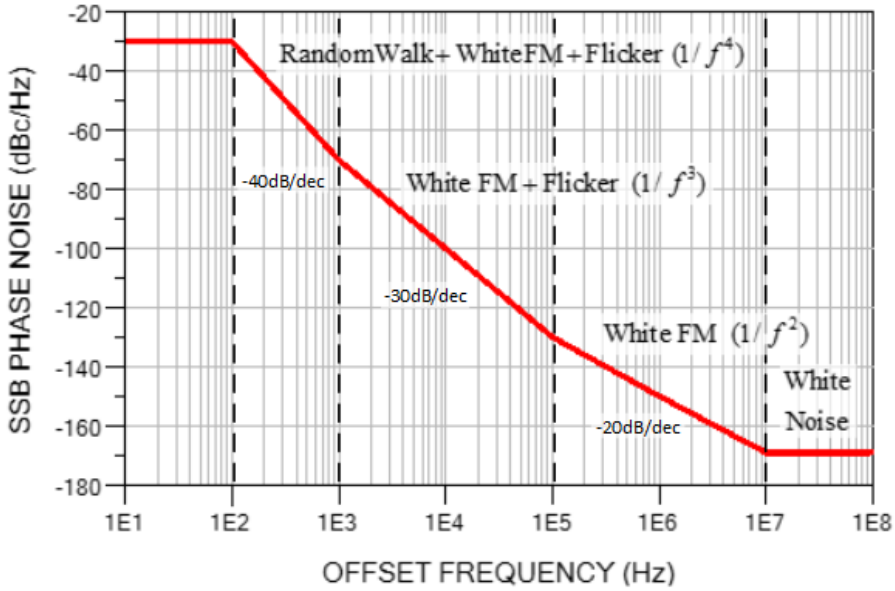


Figure 2.10: An example phase noise plot for an oscillator

2.6 LC Resonators

The simplest L-C networks are the basic series L-C and parallel L-C resonators shown in Fig.2.11.

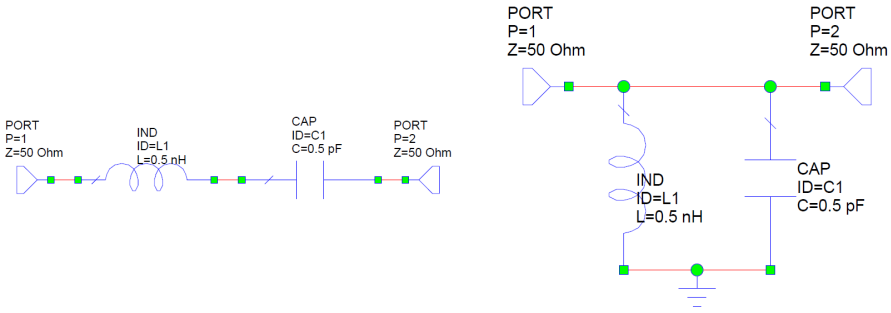


Figure 2.11: Series (on the left) and parallel (on the right) resonators

The values of the components are chosen to give same response and the transmission magnitude and phase of both resonators are shown in Fig.2.12. The

amplitude of S21 peaks at 0-dB and at the resonant frequency phase is 0°. Below the resonant frequency series network is capacitive and phase lags, while parallel network is inductive and phase leads. Above resonance the response is counterpart of the below resonance case.

Because of these networks are lossless, at resonance the impedance at the input is equal to the load impedance, so when the output is terminated in the reference impedance and the S11 passes through the center of the smith chart with zero magnitude.

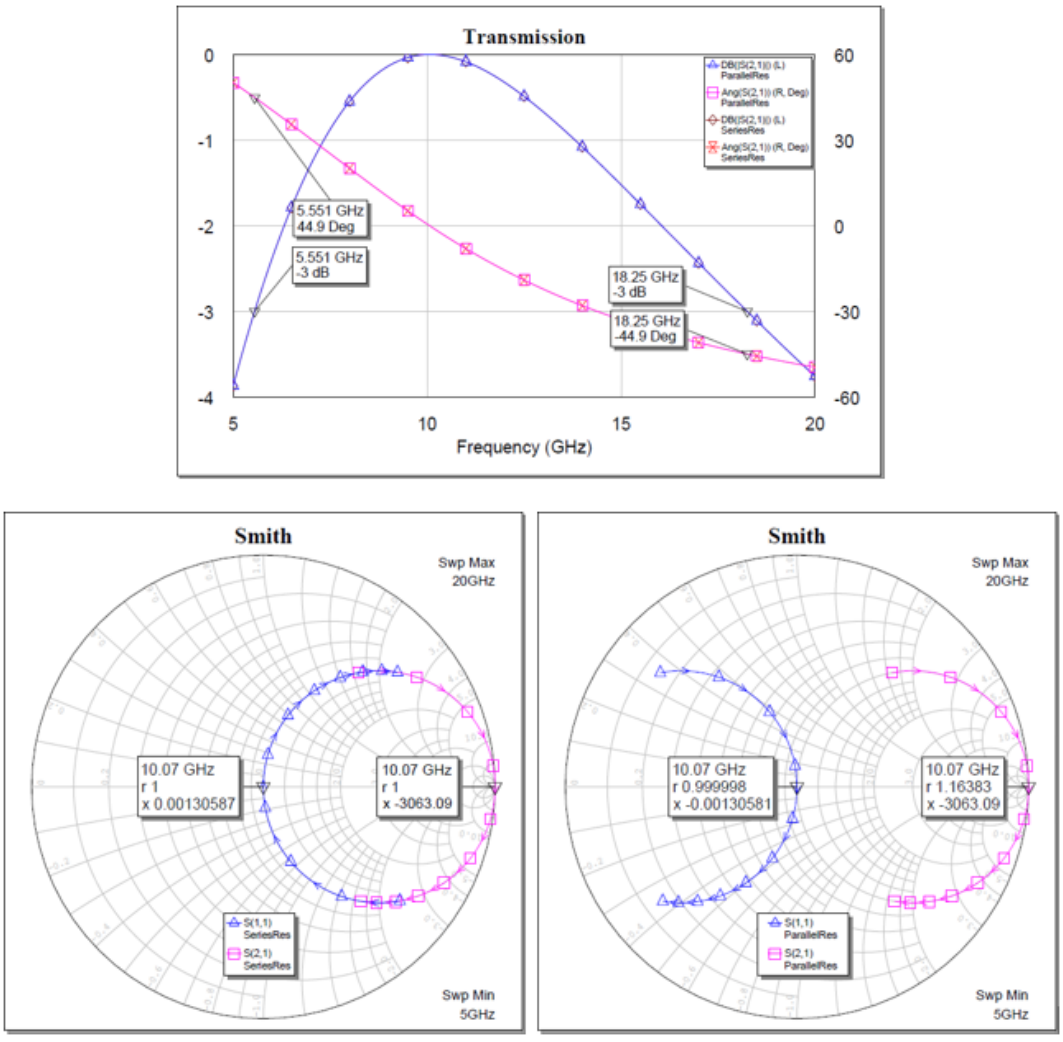


Figure 2.12: Response of series and parallel resonators

The resonance frequency of the tank can be calculated by

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad and \qquad f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \tag{2.28}$$

2.6.1 Loaded Q

Loaded Q (Q_L) represented by the following formula:

$$Q_L = \frac{f_0}{BW_{3dB}} \tag{2.29}$$

where f_0 represents resonant frequency and BW_{3dB} is the 3-dB down bandwidth of the amplitude of S21. The 3-dB BW of the resonators in Fig.2.11 is 12.7 GHz and Q_L is very high. Moreover, 3-dB BW represents the $\pm 45°$ BW as in Fig.2.11.

In this thesis, parallel resonant network is used and therefore the following equations just given for parallel network and detailed formulations for series resonant network is given in [5]. For the parallel resonator with no loss, Q_L may be defined by

$$Q_L = \frac{R_{parallel}}{X} = \frac{X}{2Z_0} \tag{2.30}$$

where X is the reactance of either the capacitor or inductor at the resonant frequency and $R_{parallel}$ is the parallel resistance.

The slope of the phase depends on Q_L. Control of Q_L means control of steepness of the phase. Additionally, the oscillation frequency depends on the transmission phase not the amplitude of S21. Thus, Q_L can also be defined as

$$Q_L = -\frac{\omega_0}{2}\frac{\partial\varphi}{\partial\omega} \tag{2.31}$$

where the unit of φ in radians. By the group delay definition

$$t_d = -\frac{\partial\varphi}{\partial\omega} \tag{2.32}$$

Q_L can be rewritten as

$$Q_L = \frac{\omega_0 t_d}{2} \tag{2.33}$$

The group delay and the resulting Q_L of the Fig.2.11 parallel resonator are in Fig.2.13.

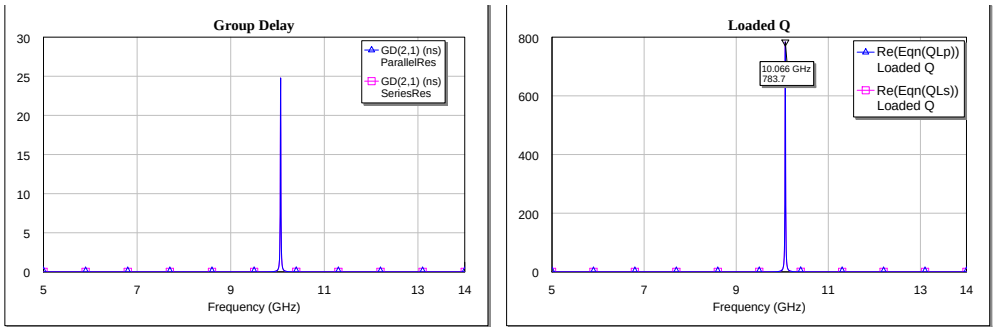


Figure 2.13: t_d and Q_L of both series and parallel resonators (Port impedances are scaled by 1000, 50e3Ω for parallel and 50e-3Ω for series)

2.6.2 Unloaded Q

Unloaded Q is related with the stored and dissipated energy in the resonator per cycle. For the parallel resonator it may be written as in Eq.2.34 by the definition of loss mechanisms.

$$Q_U = \frac{R_p}{X} \tag{2.34}$$

where R_p represents the parallel loss resistance in the network. Most of the time, these losses are directly related with core losses in an inductor and dielectric losses in a capacitor. Developments in the technology and usage of modern dielectrics shifted the source of dominant loss mechanisms to metal losses.

As the unloaded Q directly related with the components, for the resonator it can be modified by associating with individual component Qs as in Eq.2.35.

$$Q_{U-R} = \frac{1}{\frac{1}{Q_{ind}} + \frac{1}{Q_{cap}}} \tag{2.35}$$

From these mechanisms, it is possible to define insertion loss (IL) as in Eq.2.36 and the equation says that IL is minimum when unloaded Q is much greater than loaded Q.

$$IL = 20\log(\frac{Q_{U-R}}{Q_{U-R} - Q_L}) \tag{2.36}$$

Chapter 3

VCO Design

Design procedure starts with the selection of the proper technology. It may be GaAs, SiGe etc. based HBT, MESFET, BiCMOS, FET etc. Each technology has its own advantages, so preferred technology has to satisfy the requirements of the project. Besides, the design is totally based on the technology. As each foundry process has characteristic features, the design has to change with the change of the technology and process. This thesis aims to design low phase noise VCO, so we need to choose a device with low $1/f$ noise corner. At this point, HBT devices are superior to their opponents. Then the processes are eliminated with this criteria. Moreover, this VCO is a space type and it must be tolerant to 100krad total dose radiation as the VCO is intended to work at GEO (Geosynchronous Orbit). Thus a wide band-gap material would be proper for the process selection. With this general limitations, a GaAs based HBT process would be a logical choice. Moreover, the VCO operating frequency is about 10GHz. A suitable process with high enough f_t is needed to be able sustain oscillation at these frequencies. The foundry is also chosen with the considerations given above.

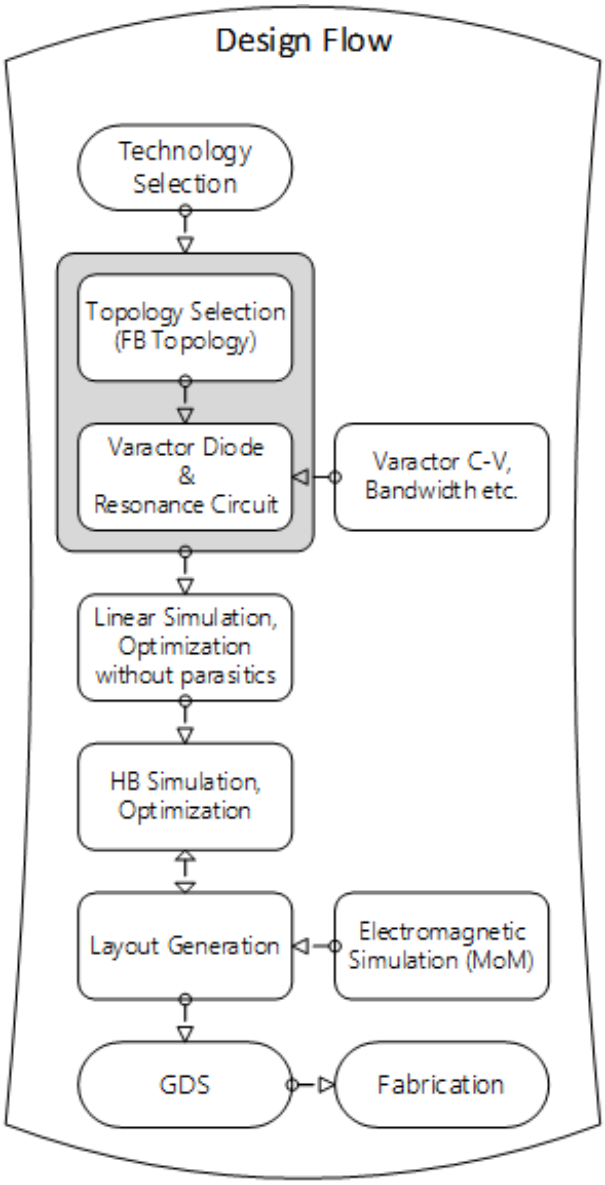


Figure 3.1: Oscillator Design Diagram

3.1 H01U-10 InGaP/GaAs HBT Process

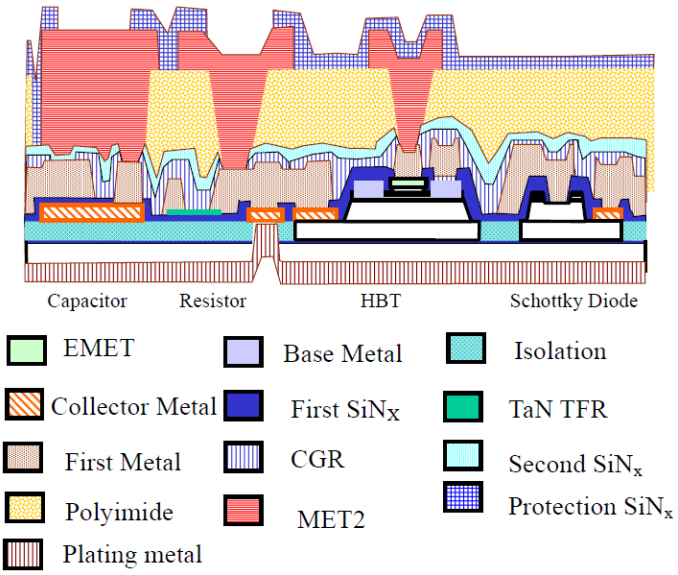


Figure 3.2: Oscillator Design Diagram

As the result of the considerations given above, 1μm InGaP/GaAs (H01U-10 process) based HBT process from WIN Semiconductors is chosen to design the VCO. The foundry was contacted to obtain the libraries with the initial intension of actually building and testing the chip. But, unfortunately, the funding of the project turned out to be insufficient to support the fabrication. InGaP is used as emitter material. 1μm represents the width of the emitter. Fig.3.3 depicts the basic HBT and shows where the emitter material (InGaP) is located.

This process consists of four HBT with different emitter mesa length (5, 10, 15, 20μm), TFR resistor, PN and Schottky diodes, inductors and MIM capacitors.

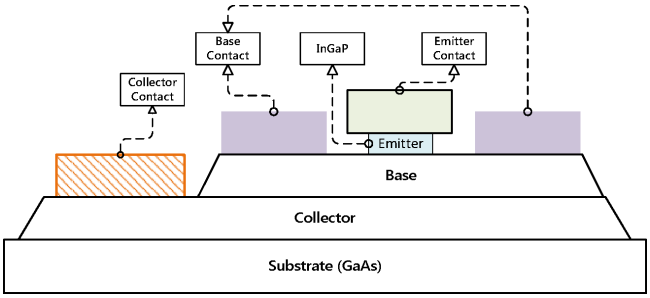


Figure 3.3: HBT Representation

3.1.1 HBT Transistor

Heterojunction bipolar transistors are kind of bipolar junction transistors, which are composed of at least two different semiconductors like InGaP/GaAs. In this thesis, used HBT has 1μm emitter width and 20μm emitter length.

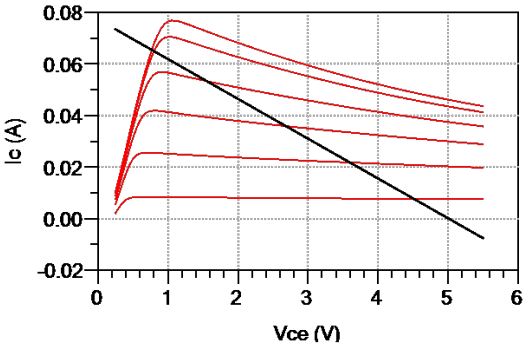


Figure 3.4: Dynamic load line superposed on IV curve

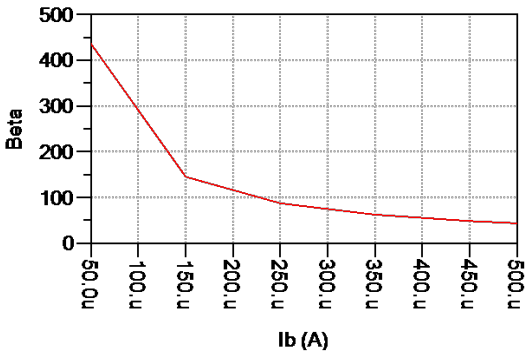


Figure 3.5: Beta vs. Base Current

HBT biased at $V_{CE} = 3.6V$ and $I_C = 20mA$, so f_t is $58GHz$ and f_{max} is $49GHz$. These values are appropriate to design a VCO in X-band.

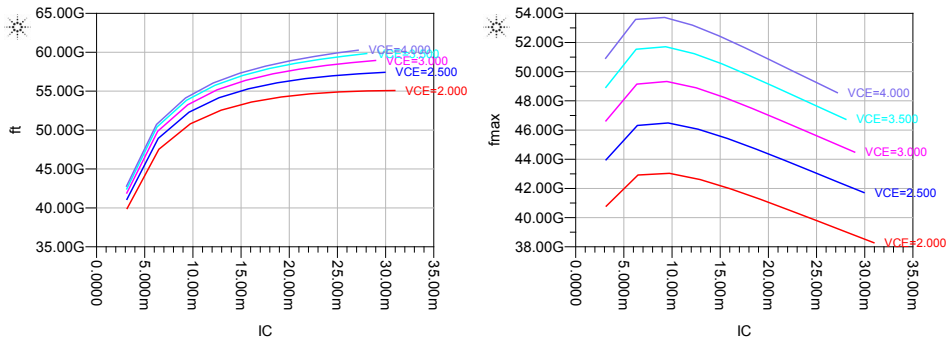


Figure 3.6: ft vs. Collector Current (left), fmax vs. Collector Current (right)

3.2 Resonator Design

To design a resonator for VCO, a varactor which has variable capacitance values under different DC bias values is needed. It has to satisfy the required BW for the VCO. Consequently, with the change in DC condition, circuit gains the ability of producing signal at different frequencies.

3.2.1 Varactor

It is a component that has different capacitance values under different DC biases. There are some kind of structures to form a varactor like schottky diodes or PN B/C junction diodes. The varactor used in the design of the VCO is a multifinger PN B/C junction type diode and the configuration of the varactor like in Fig.3.7. The model of the varactor is in Appendix A.

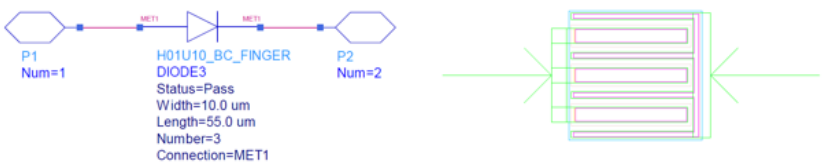


Figure 3.7: PN B/C Junction Diodes with fingers symbol on the left and layout on the right

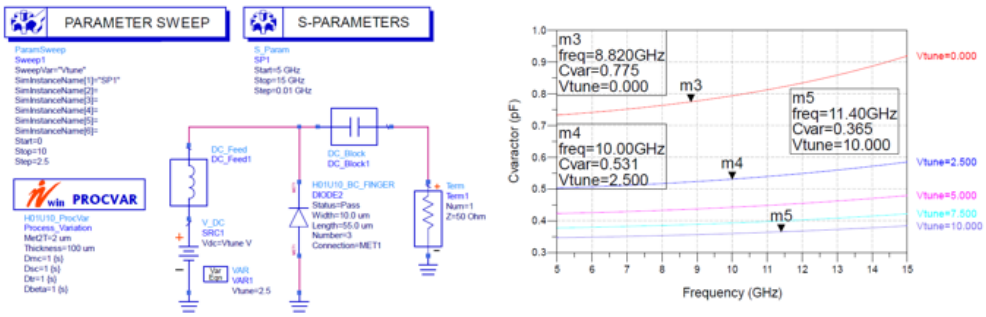


Figure 3.8: Varactor test circuit on the lest and Capacitance vs Freq. on the left

To ensure that the varactor is suitable for designing a VCO at X-band, it is necessary to test the capacitance values under different DC conditions. The test circuit and change in the capacitance value in Fig.3.8. The value of the capacitance should be between 0.2-1pF to design a inductor with reasonable size and results in Fig.3.8, supports that. With the Eq.2.28 in resonator part the resonance frequency can be calculated.

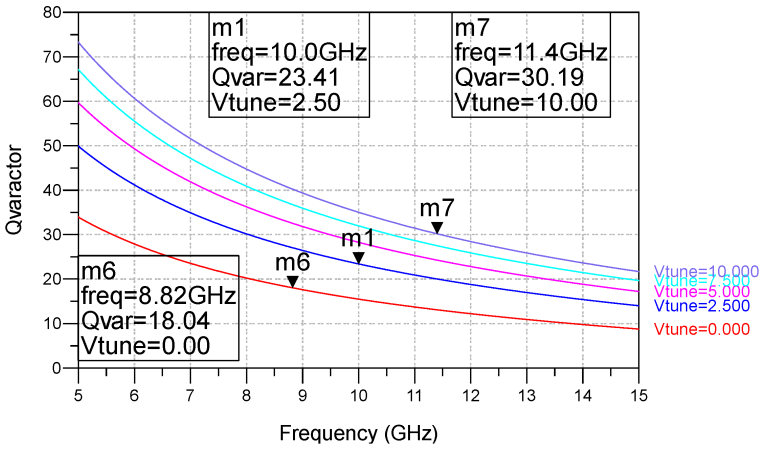


Figure 3.9: Varactor Q vs Freq.

For the phase noise consideration, quality factor of the varactor is an important parameter. The resulting Q of the varactor as in Fig.3.9. Unloaded Q of the varactor is between 20-30 in the band. Markers are located to represent actual values of unloaded Q of the varactor in the action.

3.2.2 Inductor

One of the challenging part is to get a high Q inductor. To get the best phase noise result, good quality of inductor is a need. Using Eq.2.28 and data in Fig.3.8, the amount of the inductor for the resonator can be calculated. The symbol and the layout view of the inductor are in Fig.3.10 and Fig.3.11 depicts the two-port test structure of the inductor. Fig.3.12 gives the test results of the inductor. As it is tested as a two-port structure, results can be calculated by both Y11 and Y12 parameters and each result has close relation. The value of the inductor in the band is ∼0.5nH which is a good value for the resonator. Because both the size of the inductor is compact and it has relatively high Q which is more than 25 in the band.

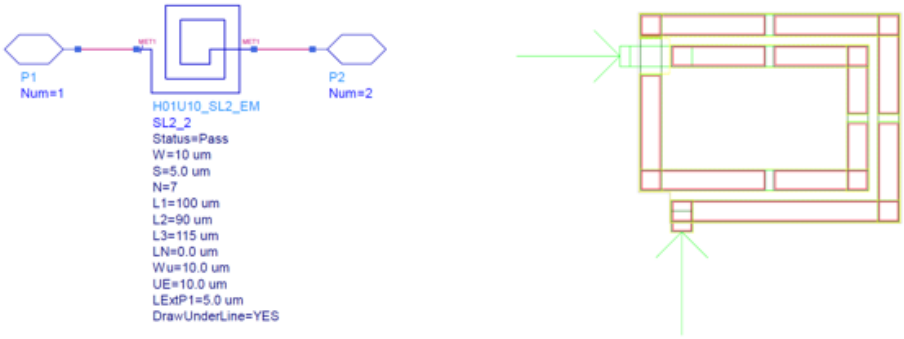


Figure 3.10: Inductor symbol on the lest and layout on the right

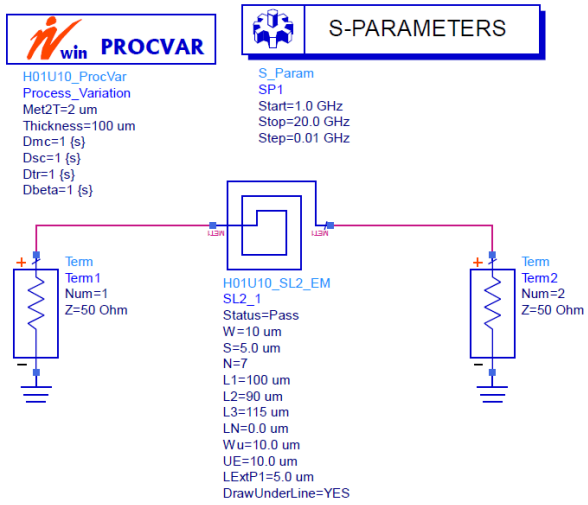


Figure 3.11: Inductor test structure

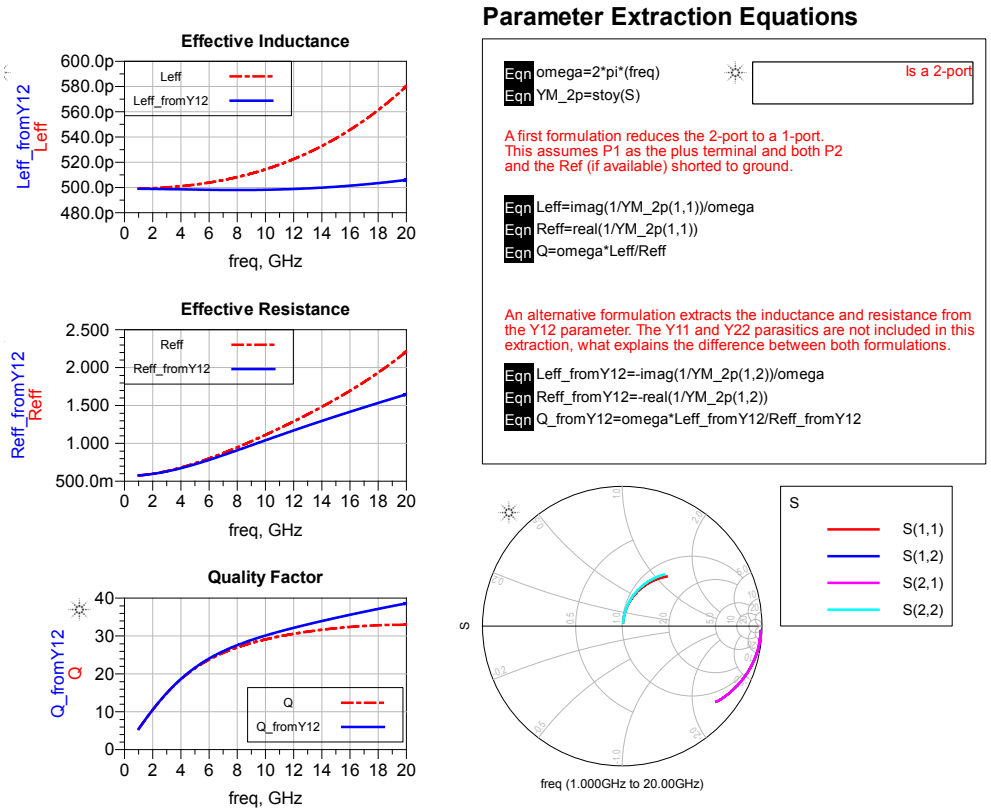


Figure 3.12: Inductor test results

3.2.3 Resonator Test

It is necessary to test the resonator response to see if it satisfies the necessary bandwidth for the oscillator or not. The test circuit is given in Fig.3.13 and the result is in Fig.3.14. It is obvious from the Fig.3.14 the resonator is capable of resonating from 7.6 GHz to 10.5 GHz. It can be observed by the phase response of the resonator. Zero crossings are the resonance point with the change in tuning voltage level of varactor. In Fig.3.14 also the active resistance part is depicted to show that it has the ability to generate negative resistance from 6.5 GHz to 13.5 GHz. Therefore, active part of the circuit covers the resonator operation band. Thus, a signal at the output can be observed.

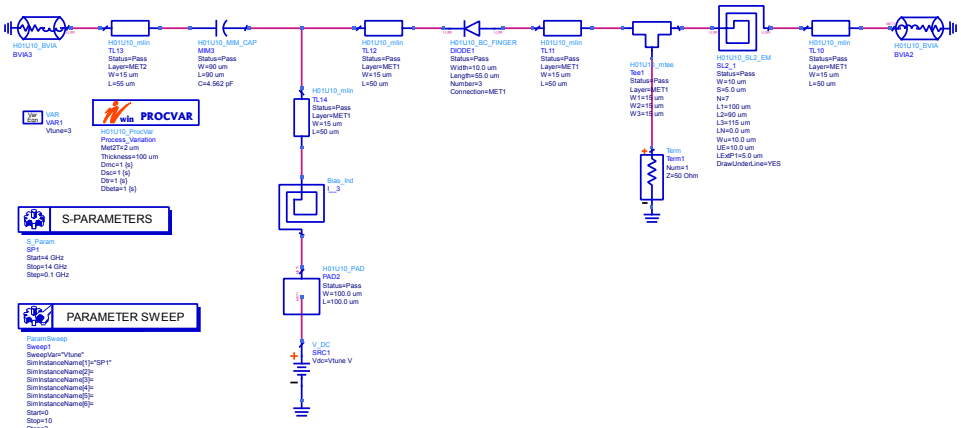


Figure 3.13: Resonator test configuration

As it was stated previously, loaded and unloaded Qs are important parameters. In Fig.3.15 and Fig.3.16, actual results of this resonator are given. Unloaded Q of this resonator is more than 10 with a peak at 5 GHz ($Q_{@5GHz} = 14$) and loaded Q is calculated from 1-port impedance parameters and equals to 13.3.

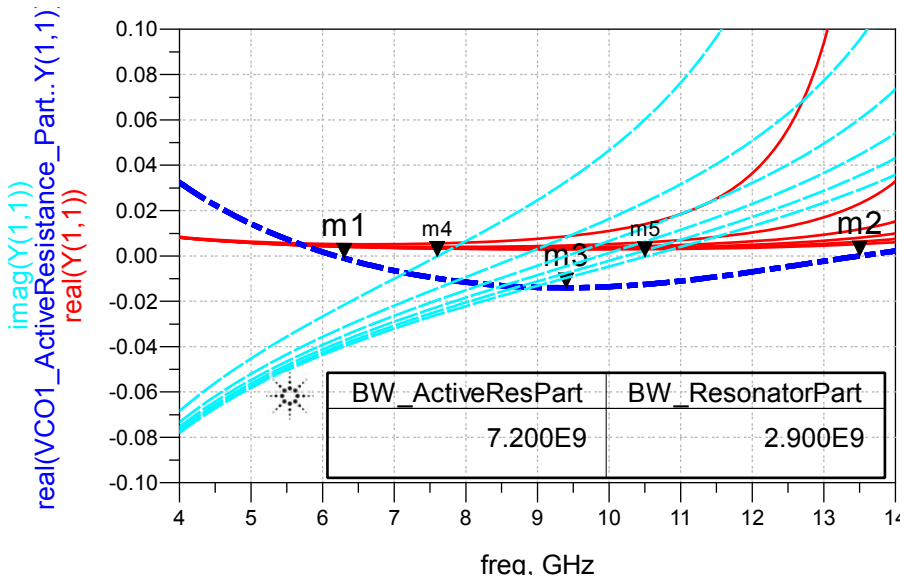


Figure 3.14: Resonator response

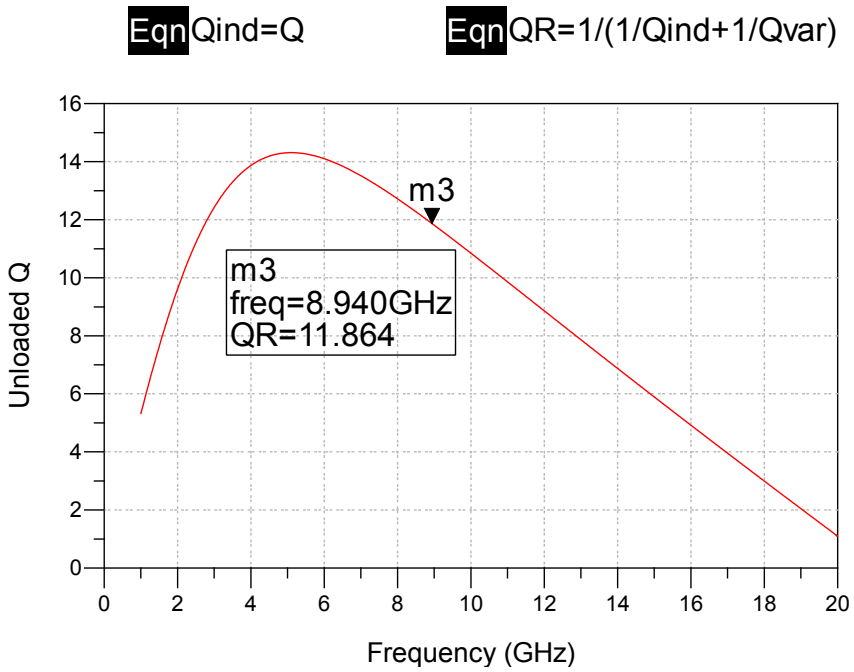


Figure 3.15: Unloaded Q

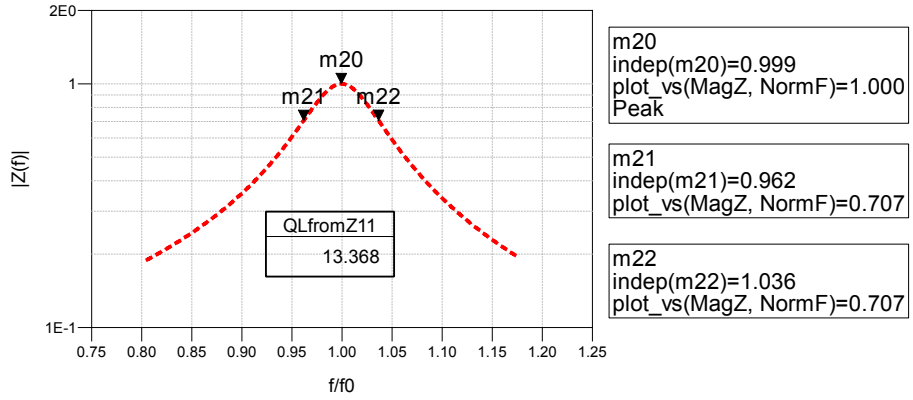


Figure 3.16: Loaded Q

As the losses in the resonator are compansated with the negative resistance, the resonator is not loaded with any load. Loaded Q value changes from 11.6 to 15.8 where the resonance frequency of the resonator is between 7.6 GHz to 10.86 GHz as in Fig.3.17.

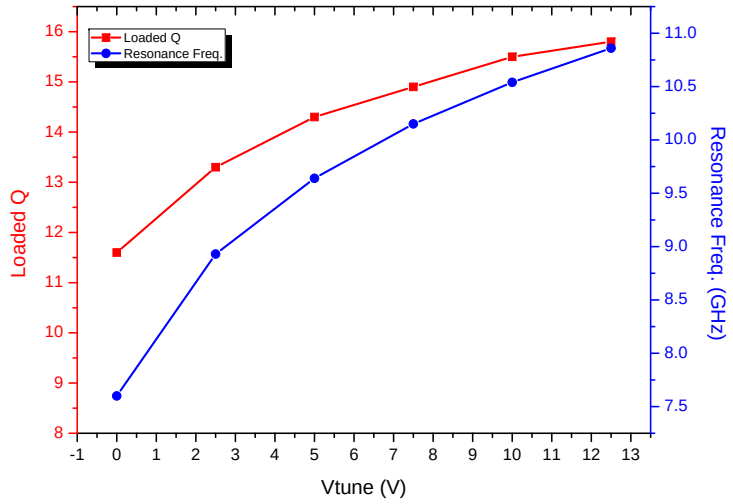


Figure 3.17: Loaded Q and Resonance Freq. vs Tuning Voltage

3.3 Topology Selection

There are three possible configuration as in Fig.3.18. These are CE, CB and CC configurations. CE configuration has high input and output impedances, but its high frequency response is poor due to miller capacitance. CB configuration has low input and high output impedance and also has good high frequency response. On the other hand, CC configuration has high input and low output impedance.

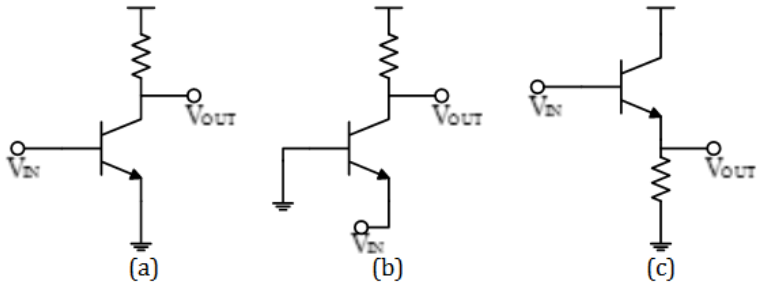


Figure 3.18: (a) Common Emitter (CE), (b) Common Base (CB), (c) Common Collector (CC) Configurations

Common-base (CB) configuration is suitable for high frequency applications, because its input impedance does not suffer from miller capacitance, which degrades the bandwidth. There is also little feedback from the output to the input, which ends up with high isolation. Therefore, changes at the output (like voltage or load changes) effect less the input, then network has high stability.

In comparison of these configuration, common-base configuration has approximately unity current gain which means it may has voltage gain but not necessarily power gain. However, CE and CC configurations have voltage and current gain respectively and both have power gain.

VCOs may have different impedance values at resonator side and this loss is compensated by the active part. In the operation range, stable output power with slight changes is preferred. Because, serious power changes may damage the system.

From the possible reasons stated above, common-base configuration is a suitable one to design a wide-bandwidth VCO with stable output power.

3.4 Negative Resistance Generation

Active part of the network is used to compensate the loss in the resonator to sustain the oscillation. To do so, a series inductive feedback is appropriate to generate the instability. There is a stability factor for the load which is defined as μ with the following formula:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^2| + |S_{12}S_{21}|} \tag{3.1}$$

where $\Delta = S_{11}S_{22} - S_{21}S_{12}$. If μ is less than unity then the 2-port network is unstable. By adding the inductor as in Fig.3.19, the circuit can be tested as it is stable or not under variable feedback inductor values.

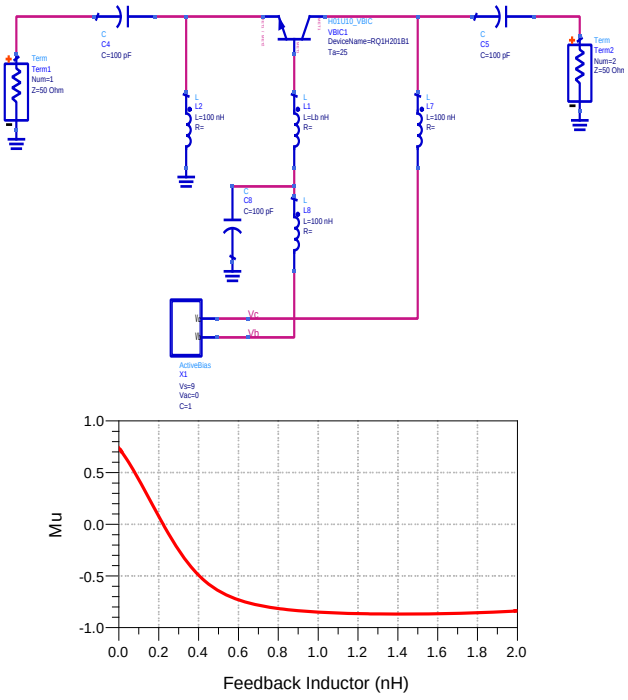
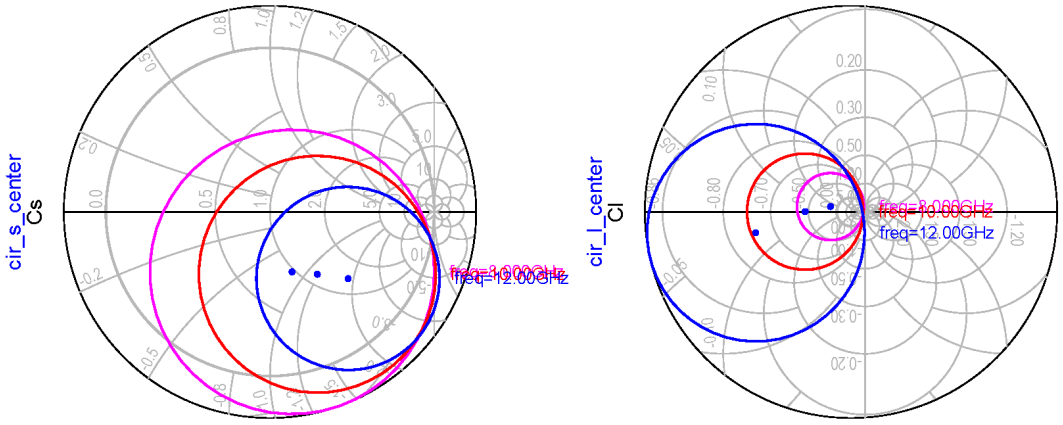


Figure 3.19: Stability Test

From the results, with or without feedback inductor the network is unstable at 10 GHz. However, with the inductor, instability is increased with the increase in the value of the feedback inductor. Fig.3.19 shows that instability increased at 1.2nH at 10 GHz. With that value, stability circles are plotted as in Fig.3.20.



freq	cir_s_center	cir_s_radius	cir_l_center	cir_l_radius
8.000 GHz	0.389 / -69.776	0.866	1.493 / 165.395	2.365
10.00 GHz	0.477 / -52.773	0.722	3.234 / 179.630	4.099
12.00 GHz	0.625 / -40.447	0.558	6.865 / -167.658	7.667

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
8.000 GHz	2.092 / 144.311	0.841 / 131.645	2.822 / -50.232	1.625 / -47.439
10.00 GHz	2.829 / 97.581	1.584 / 86.453	2.854 / -102.500	1.685 / -97.597
12.00 GHz	2.005 / 54.879	1.432 / 45.069	1.387 / -154.242	0.847 / -144.819

freq	K
8.00 GHz	-0.92
10.0 GHz	-0.90
12.0 GHz	-0.83

freq	mag_delta
8.00 GHz	1.28
10.0 GHz	1.32
12.0 GHz	0.68

Figure 3.20: Stability Circles

On the same plot with stability circles, also the center points of the circles at each frequency is marked with dots. Source stability circle on the left and the load stability circle is on the right. Small-signal results also represent that if the impedance value of the terminating network is selected inside value of stability circles, then instability is achieved. If we look closely to the load stability graph, then it is possible to say that terminating the network with 50Ω results with instability in X-band. To test the results, also the center values and the radiuses

of both load and source stability circles are given.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.2}$$

Eq.3.2 is the stability factor. If $K < 1$ then the network is unstable. Results in Fig.3.20 represents that the network is unstable in X-band and it is possible to generate negative resistance.

The value of the feedback inductor determines the potential oscillation frequency. As the feedback inductance value is increased, the potential oscillation frequency gets lower with narrower bandwidth. Fig.3.21 represents the effect of feedback inductor on both oscillation frequency and bandwidth. If $|S_{11}| > 1$, then it is possible to start oscillation.

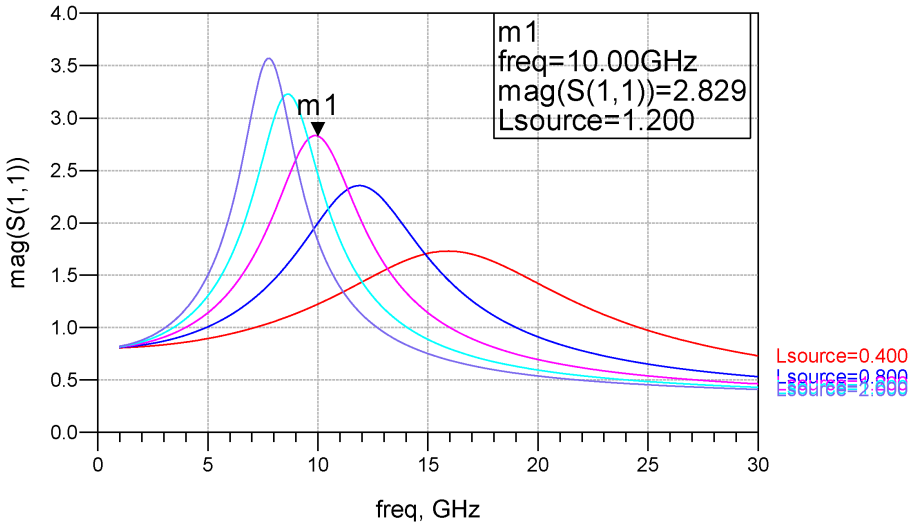


Figure 3.21: S_{11} vs Feedback Inductance

3.5 Oscillation Test

There are linear and non-linear techniques for testing a network for oscillation. Using ADS some techniques can be employed to check for oscillation. This tool can be used in linear analysis to test the small signal criteria also in harmonic-balance to test the large signal operation. Linear simulations (small signal) indicate whether the network starts the oscillation or not. Harmonic-balance simulations which study the large signal operation, give the output power, generated waveform and phase-noise. Additionally, time domain simulations can be performed to find the time to start oscillation and oscillation amplitude and waveform.

3.5.1 Linear Techniques

Small-signal conditions can be performed using the direct OscTest port tool or an ideal transformer can be introduced to network to break into closed loop oscillator and test the oscillation condition.

3.5.1.1 Ideal Transormer

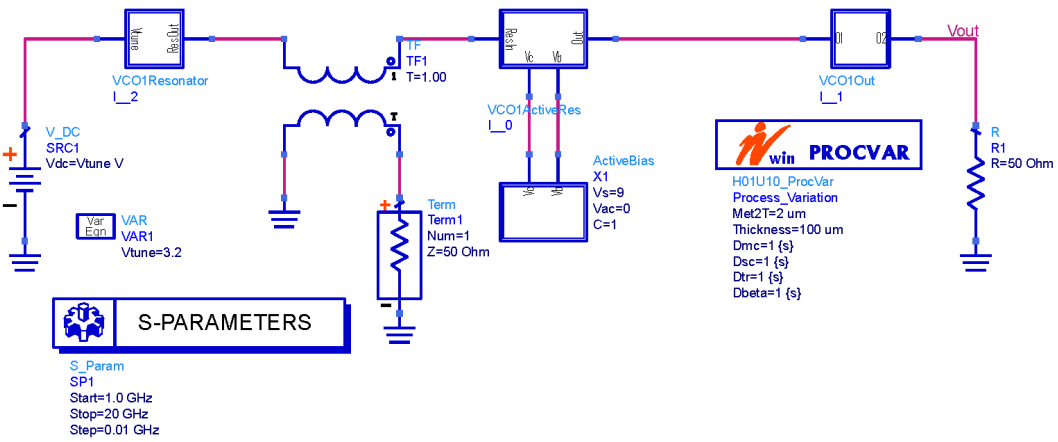


Figure 3.22: Linear test with ideal transformer

Ideal transformer breaks the loop and give access to test the oscillation condition and excess negative resistance.

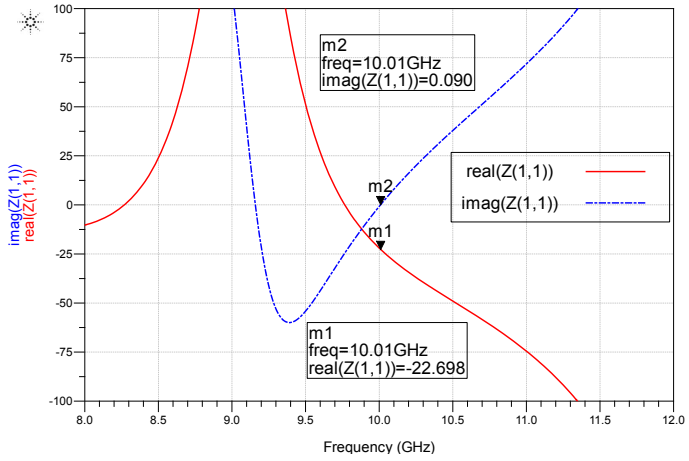


Figure 3.23: Small-Signal oscillation condition

Fig.3.23 represents the excess negative resistance with the real part of Z(1,1). This is not the absolute negative resistance. From the figure, can be seen that multiple zero crossing occurs for imaginary part. The critical point here is the negative resistance. At 9.16 GHz there is another zero crossing for imaginary part, but there is no negative resistance at that frequency. Since the network oscillates at the point where the negative resistance is introduced and there is no possibility for the network to oscillate at 9.16 GHz.

3.5.1.2 OscTest

OscTest port is replaced with the ideal transformer. This time there is no need to add an s-parameter controller, because simulation range is directly entered on OscTest port. Fig.3.24 shows the test setup and Fig.3.25 gives the result of the simulation. From the result, one can understand that loop gain is more than unity with zero phase at 10 GHz. This simulation tests Barkhausen criterion and results support that the network can start oscillation at 10 GHz [6].

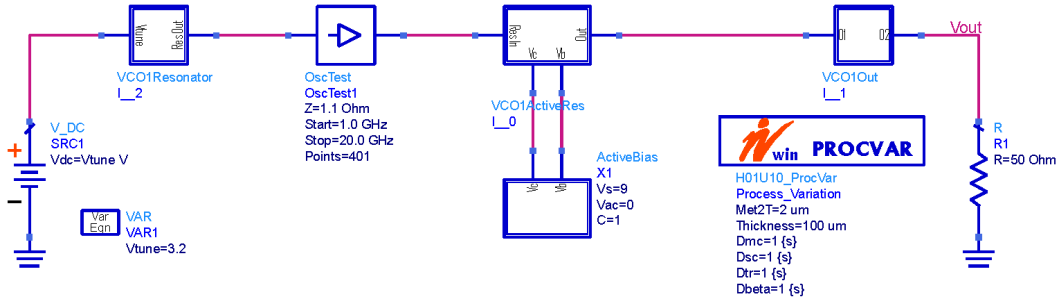


Figure 3.24: Linear test with OscTest setup

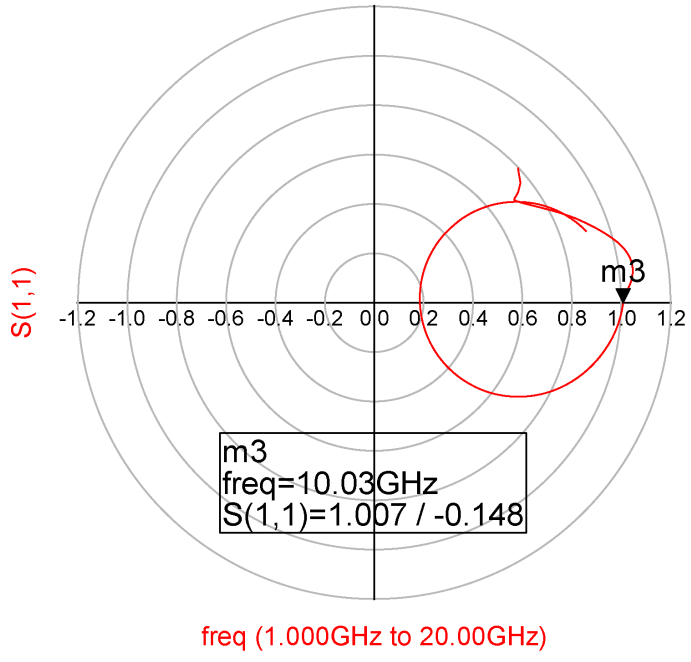


Figure 3.25: Linear test with OscTest result

3.5.2 Non-Linear Technique

Non-linear (Harmonic-Balance) simulations follows the linear simulations. By the aid of linear simulation the oscillation conditions are tested. Thus, it is time to determine the output power and waveform, and most importantly phase noise. To test the network an OscPort from Harmonic-Balance (HB) palette has to be added to network as in Fig.3.26.

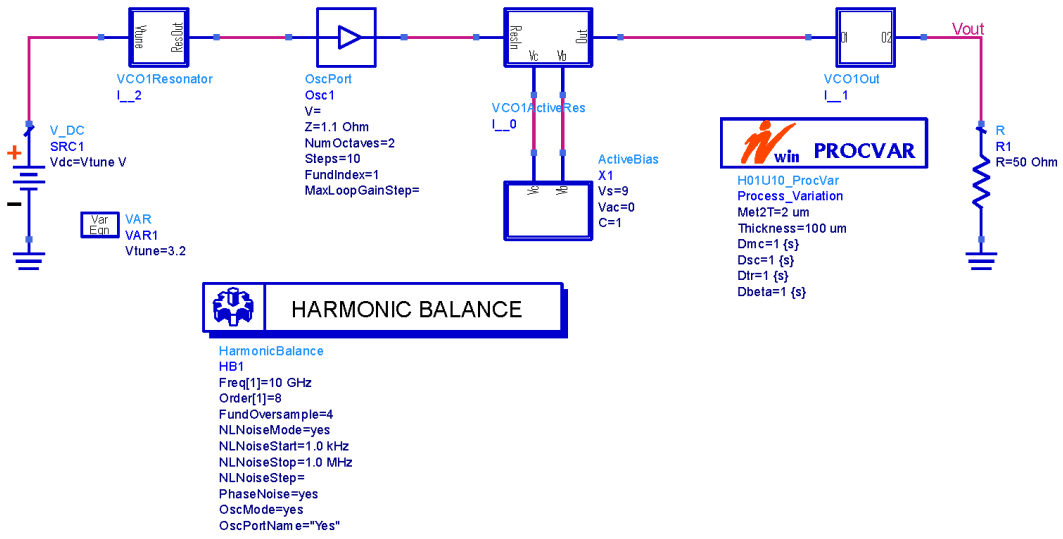


Figure 3.26: Harmonic-Balance test setup

From HB test, a lot of useful data can be taken. Fig.3.27 represents the simulation results of HB. Simulation results show that $f_{min} = 8.3GHz$ and $f_{max} = 11.2GHz$, so the BW is 26% with change of tuning voltage from 0V to +10V. Output power is more than 7.2dBm in the operation range. Phase noise is less -95dBc/Hz at 100 KHz offset and less than-115dBc/Hz at 1 MHz offset in the band. Also SSB phase noise is plotted at +5V tuning voltage at that operating point phase noise is -97.2dBc/Hz at 100 KHz offset. Moreover, harmonics suppression is represented. From the result, it can be clearly seen that second harmonic is -30dB suppressed. Fig.3.28 represents the output waveform at different tuning voltages. At any tuning voltage, output is a good sinusoidal signal.

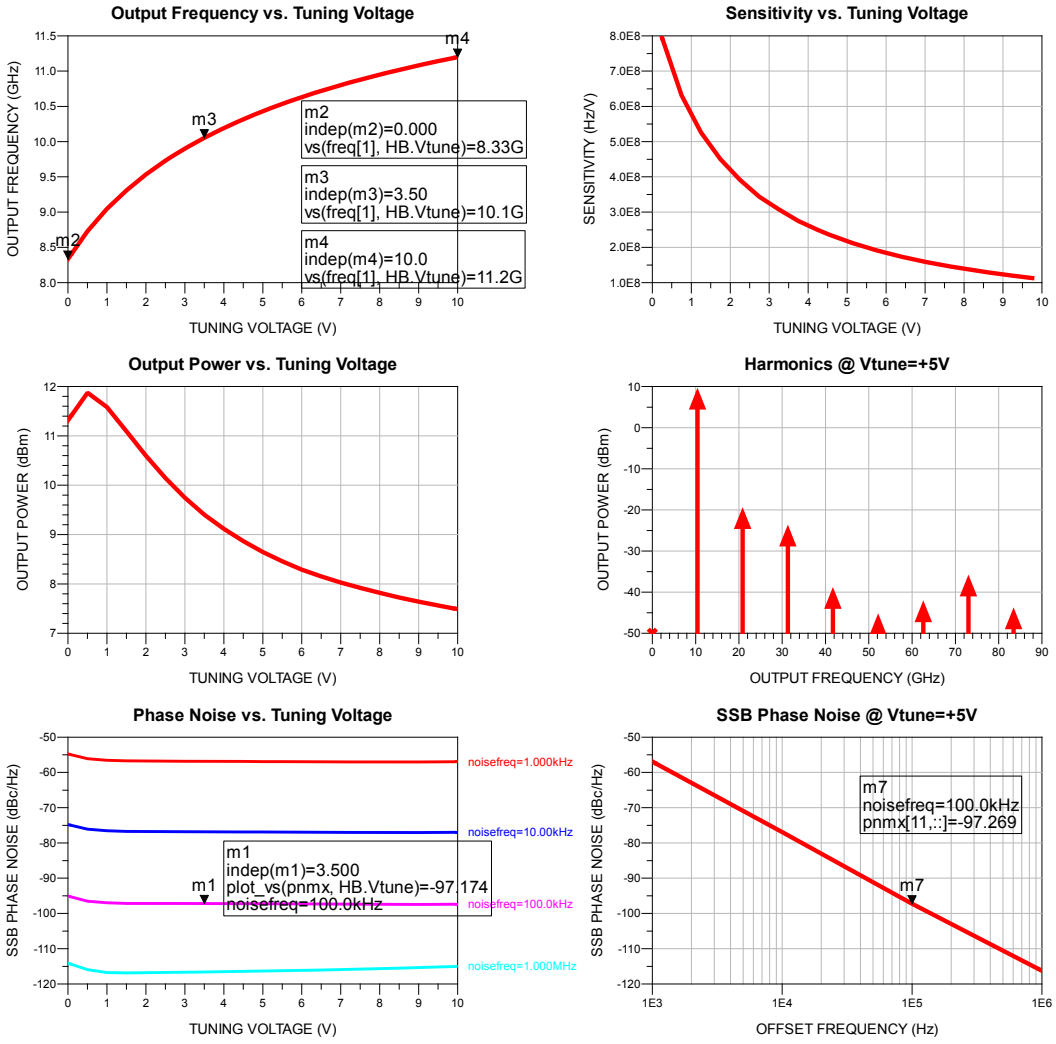


Figure 3.27: Harmonic-Balance test results

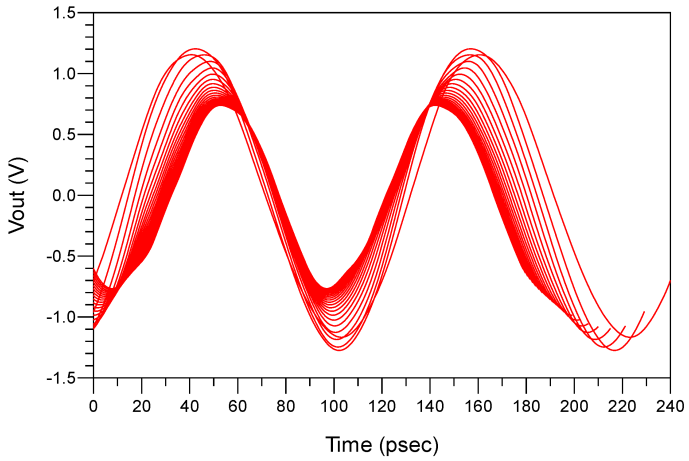


Figure 3.28: Output waveform

3.5.3 Time Domain

Time domain analysis which is also called transient analysis is performed to observe time to start oscillation and amplitude of generated signal. Fig.3.29 represents the transient analysis results. Less than 10ns network starts oscillation and nearly 14ns signal reaches maximum amplitude.

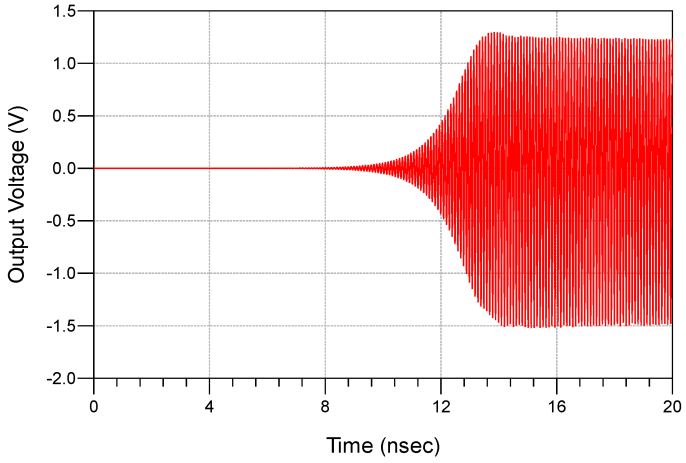


Figure 3.29: Transient analysis

3.5.4 Layout Generation and HB Simulations

When desired conditions are satisfied with linear and non-linear simulations, layout can be generated. Then, method of moments simulations are performed to take into account all parasitic effects. Increasing meshing frequency and density brings better data but simulation consumes much more time. EM simulations is valid for only metal work and passive components, no active component can be simulated in MoM simulations. Therefore, generated layout and consequent meshing is represented in Fig.3.20.

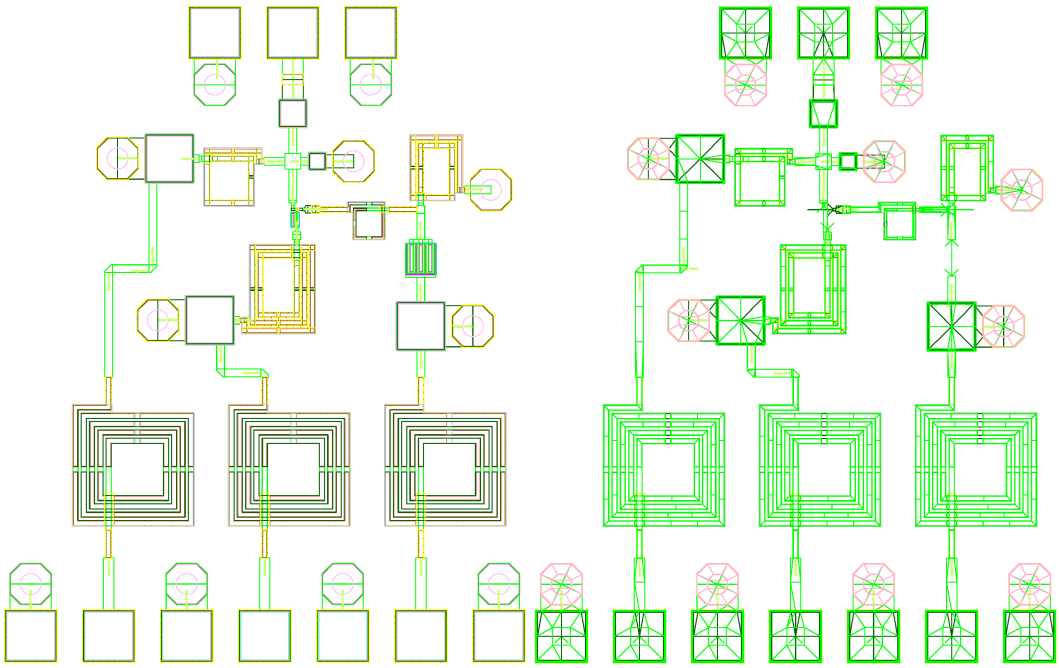


Figure 3.30: Layout (on the right) and Meshing (on the left)

EM simulations produce S-parameters. After that, S-parameters are used in CoSim as is Fig.3.31. Since EM simulation just gives S-parameters of metal work, active components, HBT and varactor are added to corresponding ports to test the resulting performance of the network. If the results are not good enough then the optimization of the layout continues until reaching the desired performance.

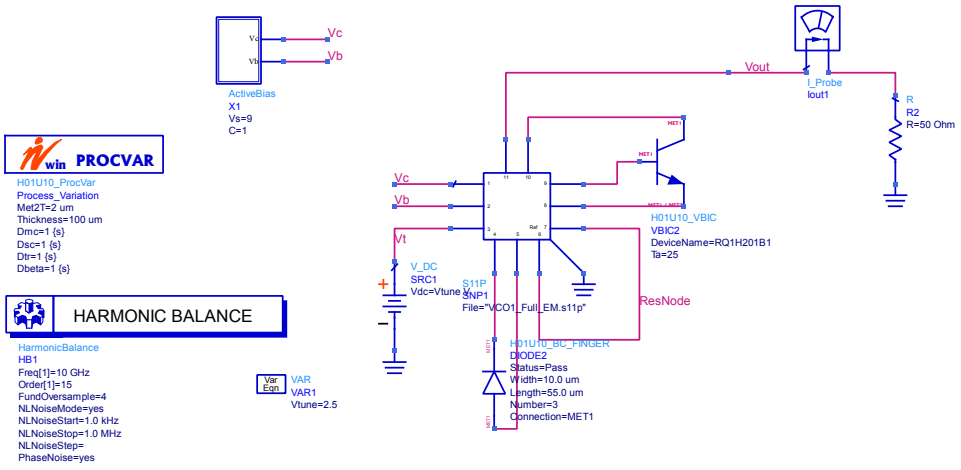


Figure 3.31: CoSim test bench

Results of final design is represented in Fig.3.32 and Table 3.1 is the summary of the results in Fig.3.32.

Table 3.1: Summary of final design

Parameters	Design Goal	Simulation
Phase Noise @ 100KHz offset	$< -90\ dBc/Hz$	$\sim -97\ dBc/Hz$
Phase Noise @ 1MHz offset	$< -100\ dBc/Hz$	$\sim -117\ dBc/Hz$
Tuning Range	$> 10\ \%$	$\sim 26\ \%$
Output Power	$> 0\ dBm$	$> 9\ dBm$
FOM_T @ 100KHz offset		-186.5
FOM_T @ 1MHz offset		-186.2
DC Power		$75\ mW$

FOM is a unitless quantity and can be calculated with the following formula.

$$FOM_T = Loffset = -20\log(\frac{f_0}{f_{offset}}) - 20\log(\frac{FTR}{10}) + 10\log(\frac{P_{diss,DC}}{1mW}) \quad (3.3)$$

where,

f_0: the oscillation frequency

f_{offset}: the offset from the carrier

L_{offset}: the phase noise at the specified offset

$P_{diss,DC}$: the DC power consumed by the VCO core

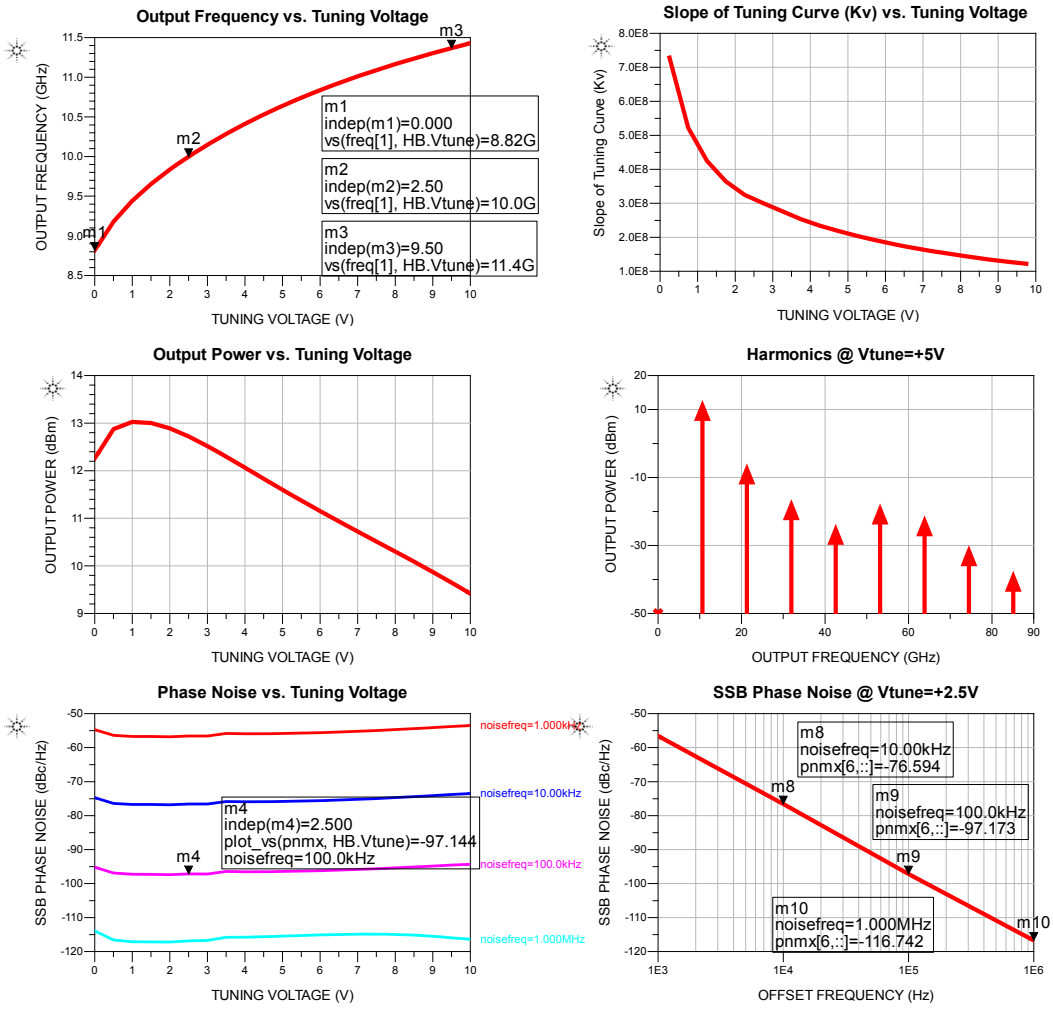


Figure 3.32: Harmonic-Balance test results (with EM)

Chapter 4

Phase Noise Measurement

Phase noise measurement is a challenging area and the measurement technique has to be studied carefully. Comparing the phase noise measurements with the other measurements at microwave frequencies, the most sensitive one is probably the phase noise measurement. In this chapter, several common measurement techniques are discussed.

4.1 Direct Measurement Technique

The simplest method used to measure the phase noise of a VCO is the direct connection of VCO with spectrum analyzer as shown in Fig.4.1. Spectrum analyzer and DUT (device under test) have to be tuned at the same frequency and spectrum analyzer measures the power spectral density of the DUT. As a carrier needed to measure the spectral density, the limiting parameter of this technique is the analyzer' s dynamic range and the selectivity of the spectrum analyzer [7][8]. Therefore, this method is not useful for measuring very close-in phase noise.

This technique is also limited by the phase noise of the local oscillator inside the analyzer. It has to have better phase noise performance than DUT. Moreover, it is not possible to distungish amplitude (AM) noise from the phase noise (PN).

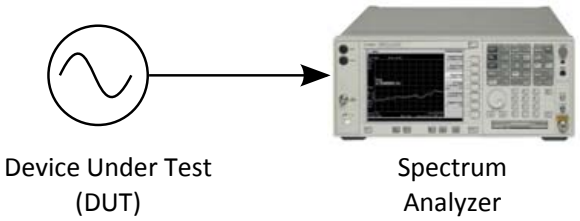


Figure 4.1: Direct Measurement Technique

4.2 Phase Detector Techniques

Phase detector technique is used to seperate PN from AM. A double balanced mixer can be used as a phase detector and the phase detector converts the phase difference of two signals into a voltage as in Fig.4.2. The voltage output is zero when the phase difference is in quadrature (90°) and it also rejects AM modulation because of 90° phase shift. Phase flactuations around quadrature will result in a voltage change at the phase detector output. Using this building block several phase noise measurement methods have been developed.

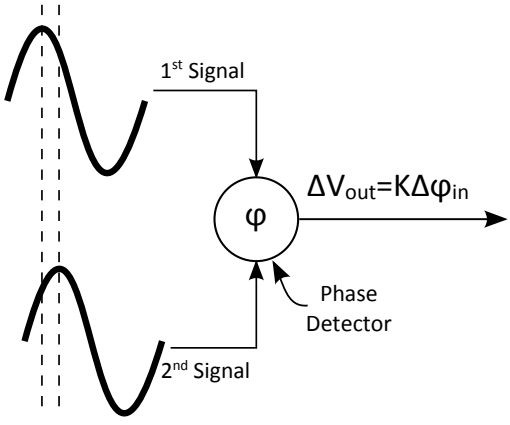


Figure 4.2: Phase Detector Concept

4.2.1 Phase Locked Loop (PLL) Method

PLL method is depicted in Fig.4.3. This method is adapted from phase detector method. As a phase detector, a double balanced mixer is prefered. DUT and reference source (RS) are the inputs of the double balanced mixer. RS and DUT are in quadrature at the same carrier frequency (f_0) and the the phase difference ($\varphi_i - \varphi_o$) is converted into voltage ($\nu_d = k_d(\varphi_i - \varphi_o)$) by the mixer [7]. The mixer sum ($2f_0$) component is filtered out by the low pass filter and the difference component is 0V with an average voltage of 0V. For the best performance, phase noise of the RS should be well characterized [8]. Aditionally, this method is insensitive to AM noise. Here, the variable DC bias at the input of the RS VCO is adjusted for 90° phase shift as a PLL having a mixer as phase detector naturally locks to 90° phase shift and the DC bias can be used to compansate for phase errors introduced by the components in the PLL circuit. This DC bias also helps to pull the PLL into lock-in range.

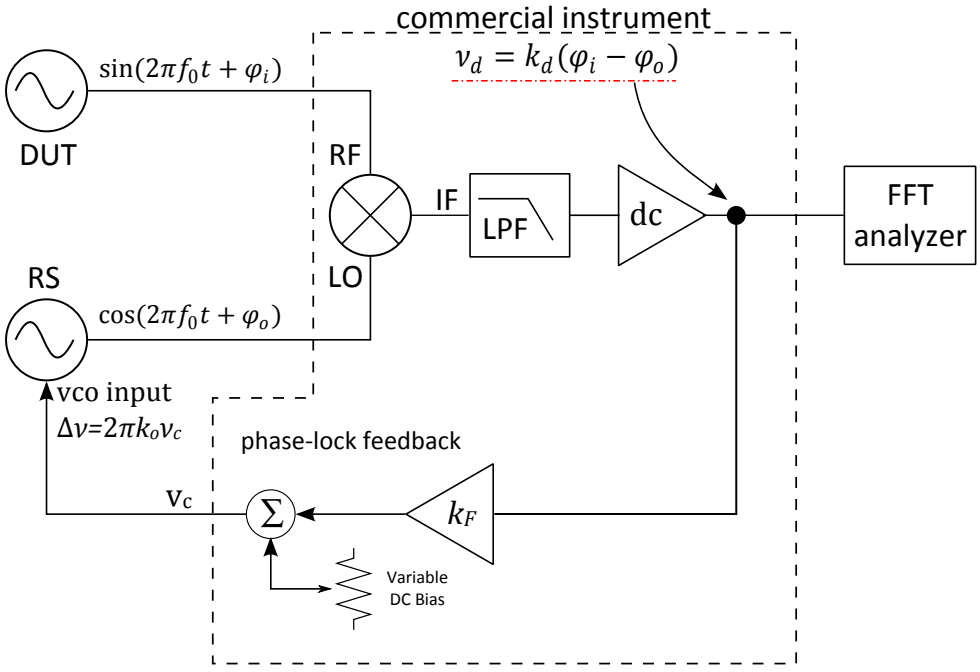


Figure 4.3: PLL Method

4.2.2 Delay Line Method

Delay-line discriminator technique is an another variaton of phase detector method. This method just requieres the DUT and with the delay line as in Fig.4.4, frequency flactuations are converted to phase flactuations [8]. 90° phase difference can be determined by adjusting the delay line or the phase shifter. Then the mixer converts the phase difference into voltage.

The advantage of this method is the elemination of the RS. It is also useful for measuring noisy oscillators that have poor phase noise performance with high close-in spurs which can cause problems for the PLL technique [8]. With the presence of close-in spurs, PLL may not be locked.

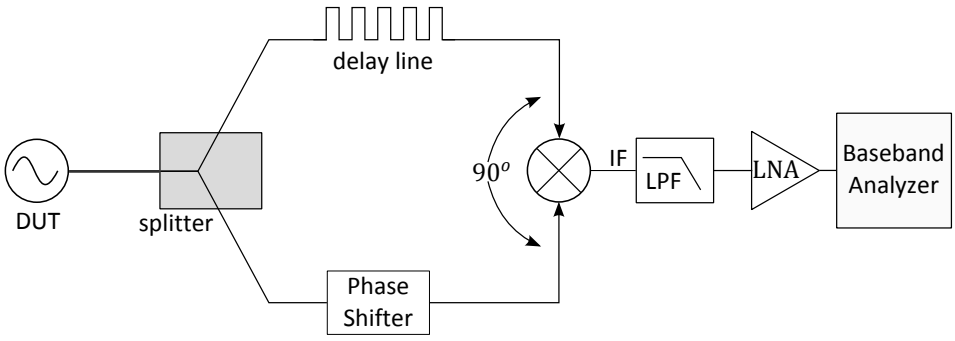


Figure 4.4: Delay Line Discriminator Method

4.3 Cross-Correlation Technique

By the combination of two single channel PLL systems, cross correlation operation can be performed between the outputs of the mixers as shown in Fig. 4.5. Noise from DUT is coherent in both channel but the internally generated noises in channels are incoherent and are diminished by the cross-corrolation operation. The cross-correlation operation is applied at the rate of $M^{1/2}$ as follows:

$$N_{meas} = N_{DUT} + (N_1 + N_2)/M^{1/2} \tag{4.1}$$

where N_{meas} is the total measured noise and N_{DUT} is the noise from DUT, N_1 and N_2 are the internally generated noise from channel 1 and channel 2 respectively and M represents the degree of correlations.

This method has the best measurement sensitivity and requires no extra performance of hardware components [8]. Nevertheless, increasing number of correlations extends the measurement period. It must also be stated here that in all the configurations using PLL, the PLL close-loop BW must be smaller than the minimum frequency of phase noise measured [9].

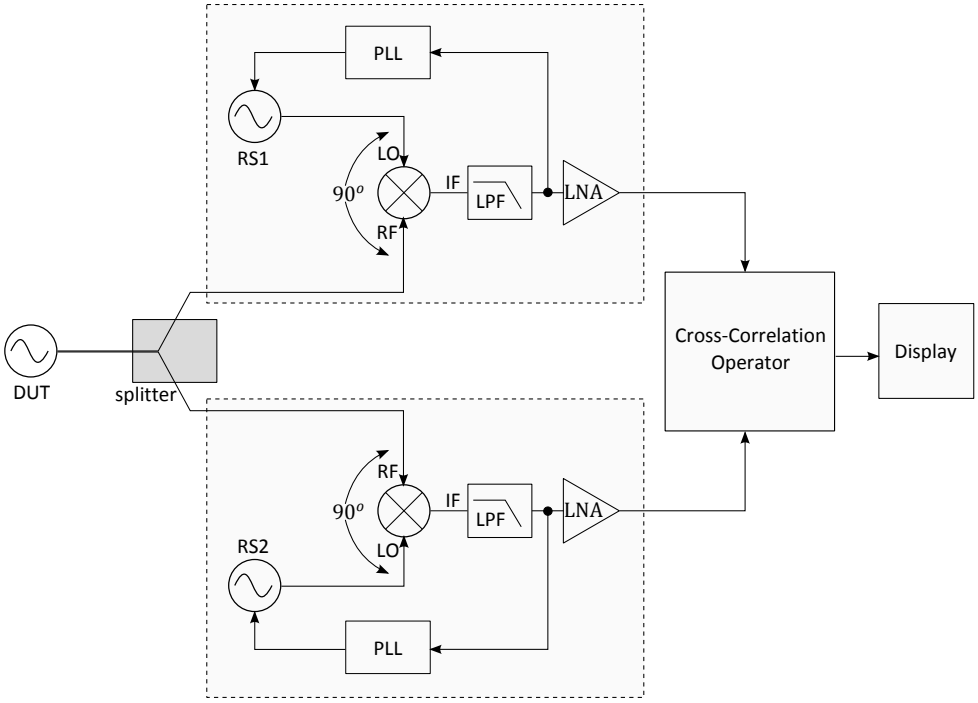


Figure 4.5: Cross-Correlation Method

Chapter 5

RF Switch

Solid state switches are one of the key components of modern RF/microwave systems. They are used to control signal flows, change signal sources and various other applications. Therefore, they have to be low loss for the receiver side and have to be capable of handling high power with low compression for transceiver side. Moreover, good isolation is required in order to minimize the effect of transmitter on receiver.

By comparison with both p-i-n diode switches and GaAs switches, GaN technology has its own advantages. While PIN diode switches consume DC power, GaN-HEMT switches require no DC power for switching operation. Instead of GaAs technology, GaN technology offers higher breakdown voltage levels for transistors. Using GaN technology ends up with higher power handling. In GaAs technology to improve the performance of the switches, the periphery of the transistors have to be increased, but it is not necessarily required in GaN, due to its high breakdown characteristic.

In this work, GaN-HEMT CPW SPST and SPDT switches are developed with different drain-source spacing, different drain-source size and different number of fingers both in series and shunt HEMTs. Actual measurement results of insertion loss, isolation, return loss and power compression level are presented with the effect of changing the control voltage for the OFF-state.

5.1 SPST Switch Design Considerations

Several Kohms resistors are needed to increase the isolation between RF and control pads. These resistors is used at the gates of the HEMTs. If the value of resistors are less than 1.5-2Kohm, the isolation between RF and control pads of the switches significantly changes with the value of the resistor. It is important that to fabricate these resistors in compact sizes, because of the area considerations. Common resistor types like Tantalum resistors require much space, so it is not a logical choice for several Kohm resistor.

To find the required and optimum value of the resistors, test patterns are designed and fabricated. To fabricate the patterns a photo-mask of the mesa resistors as in Fig.4.1 is designed and fabricated using E-Line and fabricated MESA resistors are represented in Fig.4.2. These resistor are used to calculate the sheet resistance of mesa resistors. Resulting sheet resistance is found by linear fitting as in Fig.4.3. The slope of the line gives the sheet resistance. In this fabrication, sheet resistance found as 350 ohm/sq.

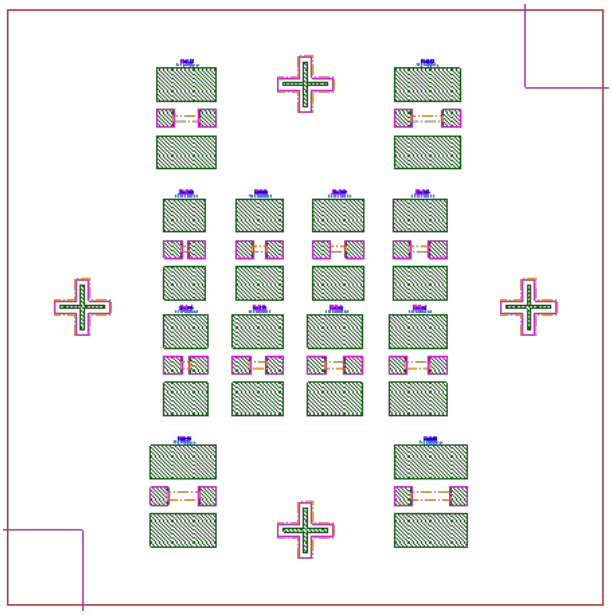


Figure 5.1: Mesa Resistor photo-mask

Figure 5.2: Fabricated Mesa resistors

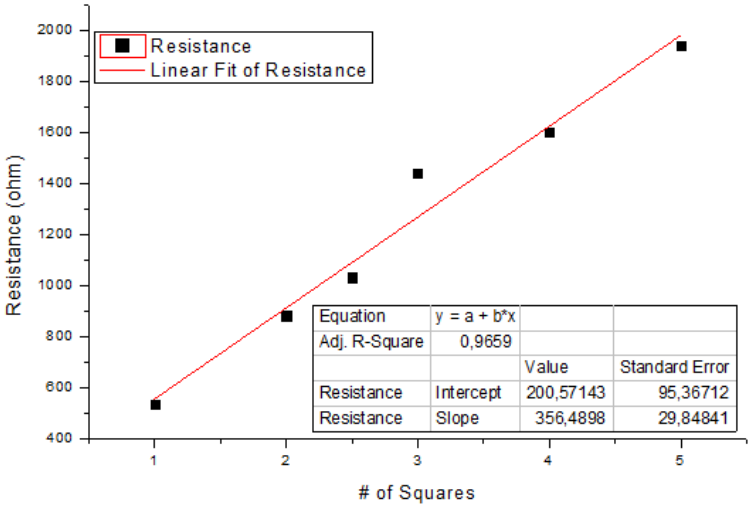


Figure 5.3: Mesa Resistor Measurements

These fabricated MESA resistors are the basis of the switch HEMT design. According to the measurement results, series HEMTs like in Fig.4.4 are designed and fabricated. The fabricated HEMTs are used to generate a model to design SPSTs and SPDTs.

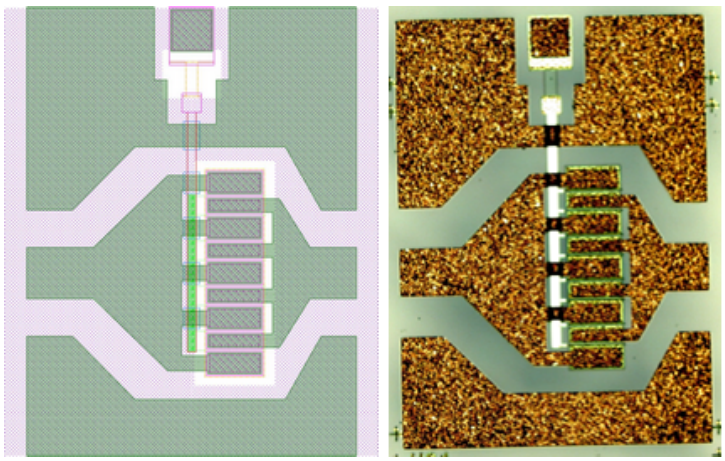


Figure 5.4: HEMT photo-mask (left), Fabricated HEMT (right)

5.2 RF Switch Design

The HEMTs are suitable for switch design, because of their drain-source resistance characteristic. They behave as a variable resistor with the gate-source (V_g) voltage change. When $V_g = 0V$, HEMT is ON and shows low resistance. For Vg below pinch-off, HEMT is OFF and shows high resistance and OFF capacitance present. The value of the capacitance changes with the voltage change. To control the resistance value, bias is applied from gate terminal and gate-source voltage adjusts the resistance value. In switching application, drain-source voltage of the HEMT is zero volt DC. Therefore, in ON state HEMT has constant resistance. RF signal is applied from drain-source path and DC voltage is applied to gate terminal to switch ON and OFF to RF path. These characteristics of HEMTs are suitable to model a HEMT with a resistance in ON state and a capacitance in OFF state as in Fig.4.5.

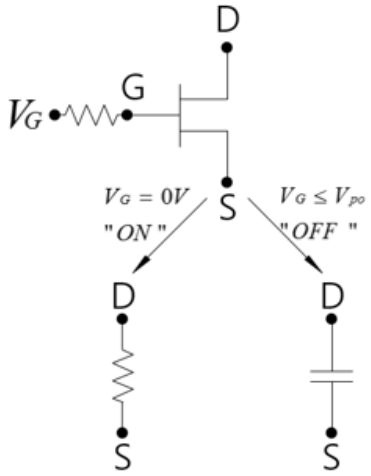


Figure 5.5: HEMT representation

In Fig.4.5, resistor represents the R_{ON} and capacitance represents the C_{OFF}. If 0V DC is applied to gate terminal, ON resistance is present. When a negative voltage is applied to gate terminal, lower than pinch-off voltage, then HEMT is OFF and C_{OFF} is present.

Using R_{ON} and C_{OFF}, a common term can be defined as in Eq.4.1, which is known as figure-of-merit. The unit of FOM is Hz. This term is used as a comparison criteria for switches. Higher the FOM, higher the upper operation frequency limit.

$$FOM = \frac{1}{2 \times C_{OFF} \times R_{ON}} \tag{5.1}$$

5.2.1 Switch Model

Fig.4.6 represents the basic SPDT configuration with four transistors. In this configuration, one arm is in ON state (series HEMT is ON and shunt HEMT is OFF), and the other is in OFF state (series HEMT is OFF and shunt HEMT is ON). As described before, these HEMts can be replaced by equivalent ON resistance and OFF capacitance as in Fig.4.7. It is possible to introduce off-resistance to OFF HEMT but in Fig.4.7 they are just for representation and the

value of OFF resistance is so high that it can be neglected.

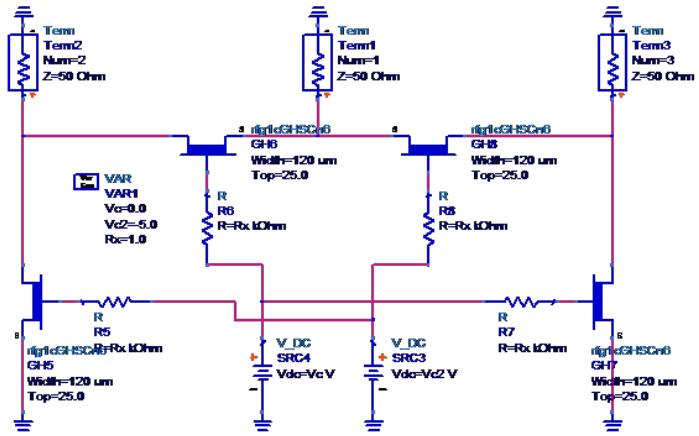


Figure 5.6: SPDT configuration

From Fig.4.7, it can be seen that left side of the switch is ON and right side is OFF. By sweeping R_{ON} and C_{OFF} values; insertion loss, return loss, isolation and FOM can be observed and optimum values can be found for desired design. With proper HEMT design required R_{ON} and C_{OFF} can be engineered. Fig.4.8 represents the corresponding simulation results of analyzed structure in Fig.4.7.

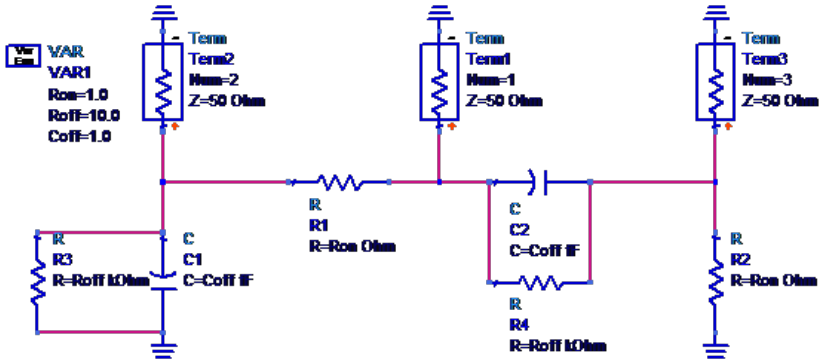


Figure 5.7: Equivalent SPDT model

Results in Fig.4.8 show that higher RON results with degraded insertion loss

and higher COFF degrades the isolation. Therefore, an optimum point for design goals has to be found by designing proper HEMTs and applying optimum voltages.

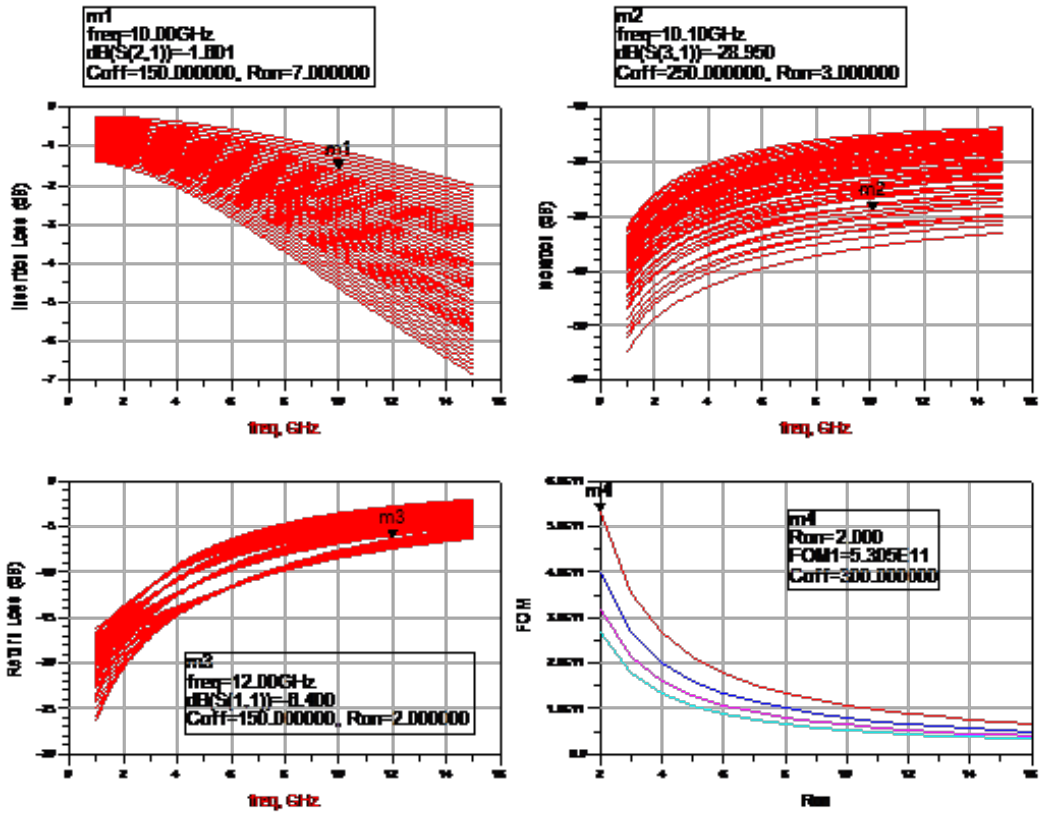


Figure 5.8: Switch model analysis

5.3 Switch Power Handling

As HEMTs used as both series and shunt elements, both power capability is important. When HEMT is used as a series element ON-state power handling, otherwise OFF-state power handling is critical.

Power handling term of switches means the power level that will correspond to the onset of gain compression. Exceeding calculated power handling introduces extra insertion loss and this is not a desired result. To avoid this situation, switches can be operated without compression.

5.3.1 ON-state power handling

In ON-state passing current limits the HEMT, then the power handling can be calculated by the maximum current the device can pass

$$P_{H-ON} = \frac{I_{MAX}^2 Z_0}{2} \tag{5.2}$$

5.3.2 OFF-state power handling

OFF-state power handling is related with the breakdown voltage:

$$P_{H-OFF} = \frac{(V_{BR} - V_{PO})^2}{2Z_0} \tag{5.3}$$

To increase the power handling, the difference between pinch-off and breakdown has to be increased. The optimum value of gate bias for the OFF-state can be calculated with the following equation:

$$V_{g_{opt}} = \frac{V_{br} + V_p}{2} \tag{5.4}$$

where V_{br} is the breakdown voltage of the drain-source and V_p is the pinch-off voltage.

5.4 HEMT Modelling

In previous sections it was stated that HEMTs act as a variable resistor under different gate-source voltage. In switching applications, 0 V gate bias applied and drain-source voltage is always zero volt in ON-state. When the HEMT is OFF then an off capacitance exists. Therefore, it is possible to model HEMTs as in Fig.4.5. To generate a model, linear S-parameters of the HEMT in Fig.4.4 measured by grounding the gate pad of the HEMT [10]. This time device is biased by applying positive voltage to the source and drain through bias tees. With that method drain-source voltage difference is kept at zero volt. Fig.4.9 shows the measured configuration of the HEMTs. On-state resistance and OFF-

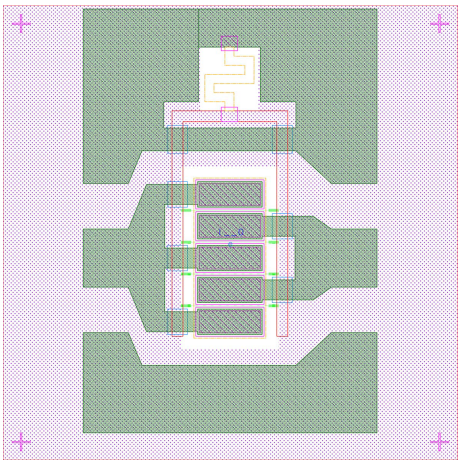


Figure 5.9: HEMT measurement configuration (gate grounded)

state capacitance for the HEMTs are estimated from low frequency s-parameters. Following equations are used to calculate resistance and capacitance values [10].

$$R_{on} = 2Z_0(10^{-\frac{S_{21}(dB)}{20}} - 1) \tag{5.5}$$

$$C_{off} = -\frac{1}{2Z_0\omega\sqrt{10^{-S_{21}(dB)/10} - 1}} \tag{5.6}$$

The DC transfer characteristics of control transistors are measured at $V_{DS} = +10V$ and $V_{GS} = -6V$ to $+1V$. Measured pinch-off (V_p) voltage was -4.2V. Maximum DC transconductance was 330 mS/mm and maximum drain current

at $V_{GS} = +1V$ is 1.2A/mm. Typical three-terminal breakdown voltage BV_{DS} is greater than 70V at $I_{DS} = 1mA$ ($200\mu m$ device). Fig.4.10 represents the I-V relationship of the HEMT and Fig.4.11 shows the transconductance of the same HEMT according to gate voltage change.

To extract a model for transistors, single series transistor is measured with network analyzer. On-state resistance (R_{ON}) and off-state capacitance (C_{OFF}) values are calculated from s-parameters at 3 GHz. Calculated values are shown in Table.4.1. Results show that source-drain spacing has major effect on on-state resistance but has minor effect on off-state capacitance. Figure of merit (FOM) for switch transistors in Table 4.1 calculated by Eq.4.1.

Table 5.1: GaN switch HEMT circuit parameters

Source-Drain Spacing (um)	Gate Bias (V)	R_{ON} (Ω-mm)	C_{OFF} (pF/mm)	FOM (GHz)
3	-30	2.2	0.3	241
5	-30	3.2	0.3	166

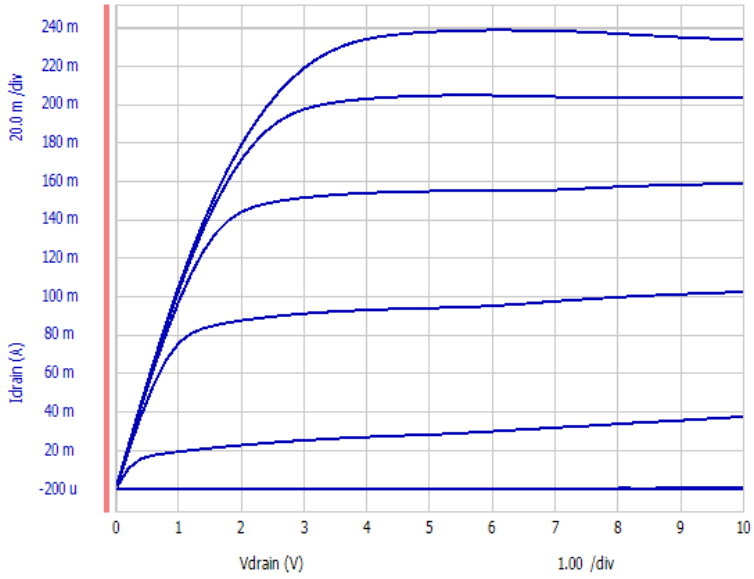


Figure 5.10: I-V of a HEMT (2x100um)

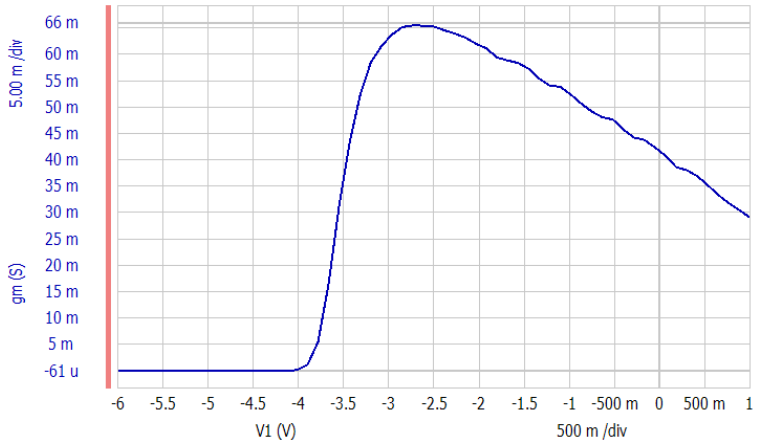


Figure 5.11: g_m vs. gate voltage (2x100um)

5.5 SPST Design

From the results in Table 4.1, a model for RF switch transistors is generated and to verify the accuracy of the model, several types of SPST switches with different combinations of HEMTs fabricated. Fig.4.12 depicts the design of the test SPSTs and Table 4.2 shows the design parameters of the SPSTs in detail. Fig.4.13 shows one of the fabricated SPST.

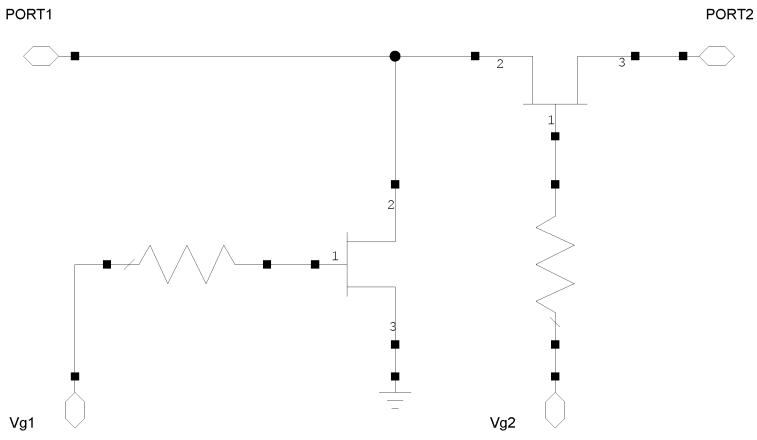


Figure 5.12: Circuit topology for the Single-Pole Single-Throw switches

Table 5.2: Summary of Design Parameters

	SPST1	SPST2	SPST3	SPST4	SPST5
Series HEMT	$4 \times 75\mu m$	$6 \times 75\mu m$	$6 \times 75\mu m$	$4 \times 100\mu m$	$2 \times 6 \times 75\mu m$
Parallel HEMT	$4 \times 75\mu m$	$6 \times 75\mu m$	$4 \times 75\mu m$	$4 \times 100\mu m$	$2 \times 4 \times 75\mu m$
D-S Spacing (μm)	5	3	3	5	3
Drain Size (μm)	32	25	25	32	25
Source Size (μm)	32	40	40	32	40

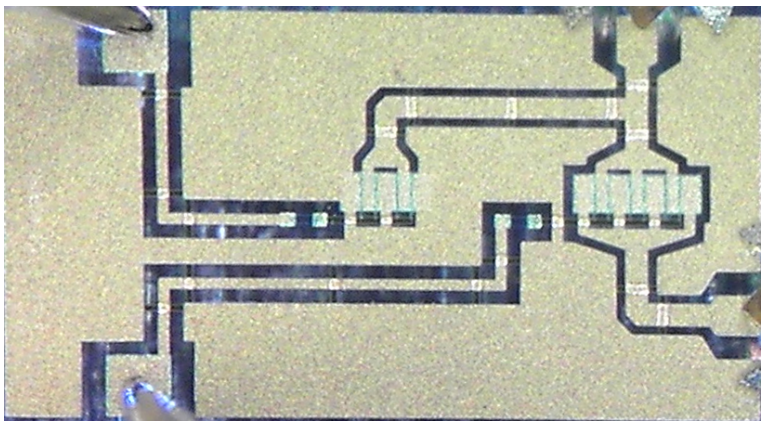
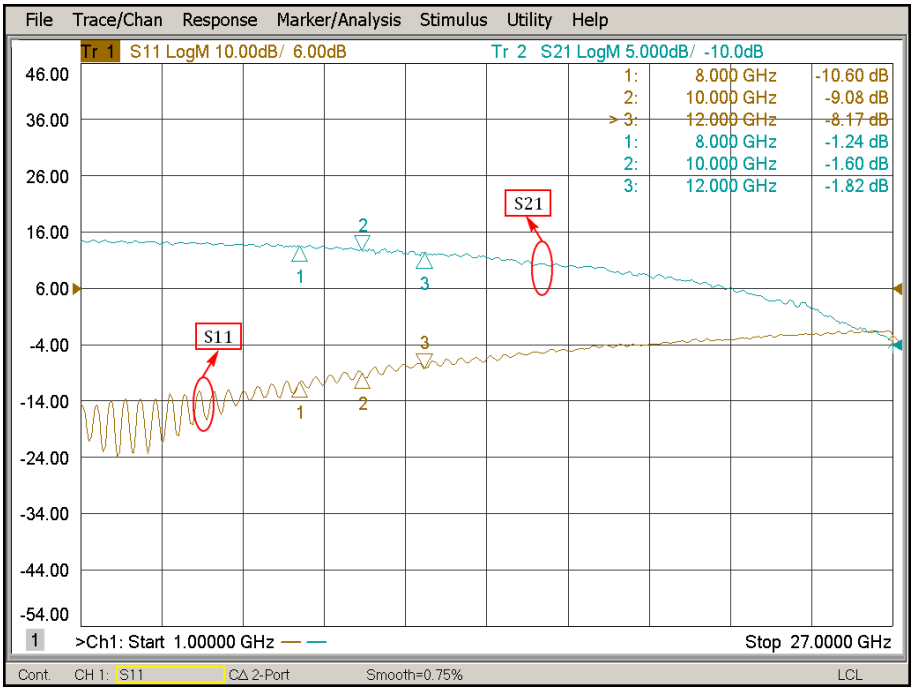
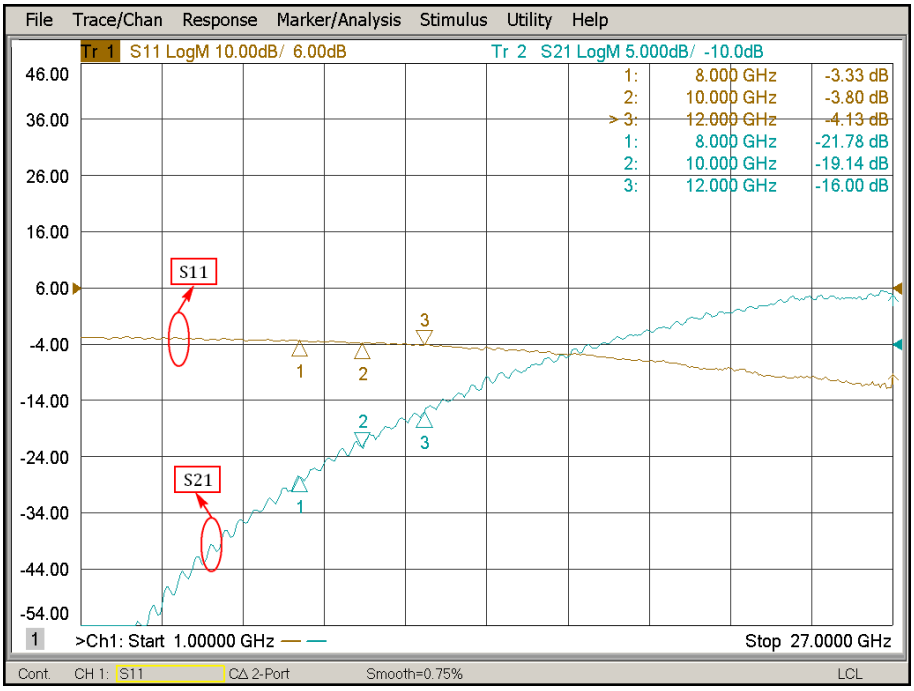


Figure 5.13: Photograph of a fabricated CPW SPST switch

For all five SPST design, small-signal S-parameter measurements performed and the results are as in following figures and the summary of them in Table 4.3. All of the measurements are performed at 0 and -25V gate voltages. In the following figures, ON-state and OFF-state responses are given. Fig.4.19 represents the power measurement results taken at 10 GHz with continous wave (CW). 40dBm output power is possible with less than 0.2dB compression.

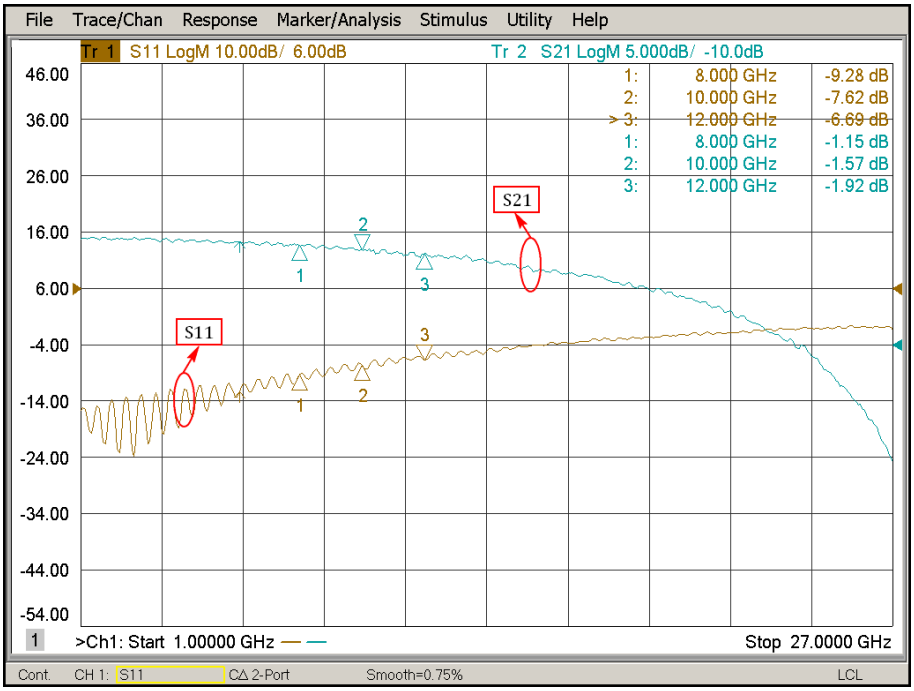


(a) ON-state S-parameters

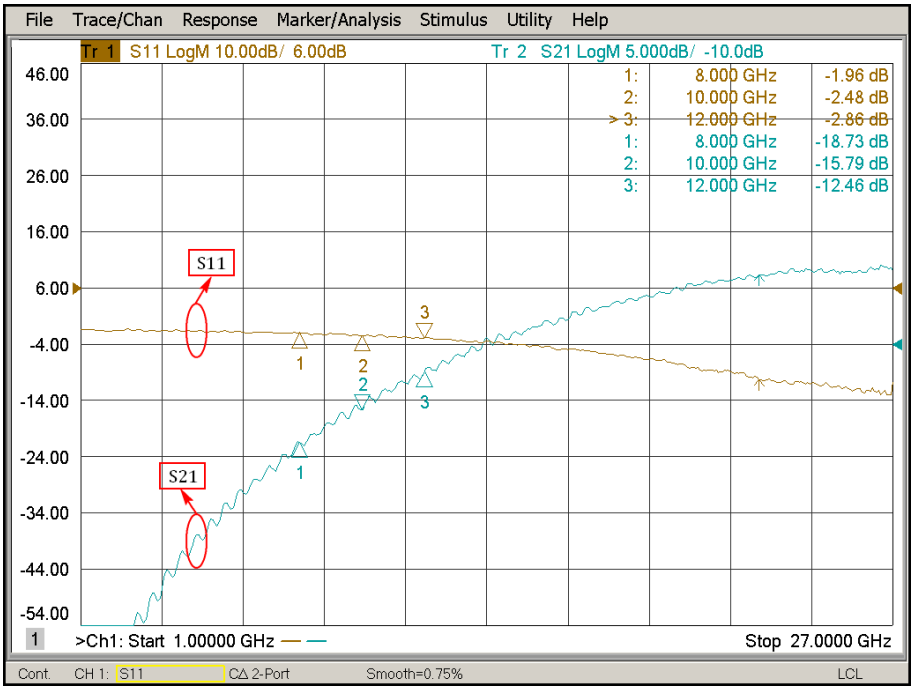


(b) OFF-state S-parameters

Figure 5.14: SPST1 S-parameters

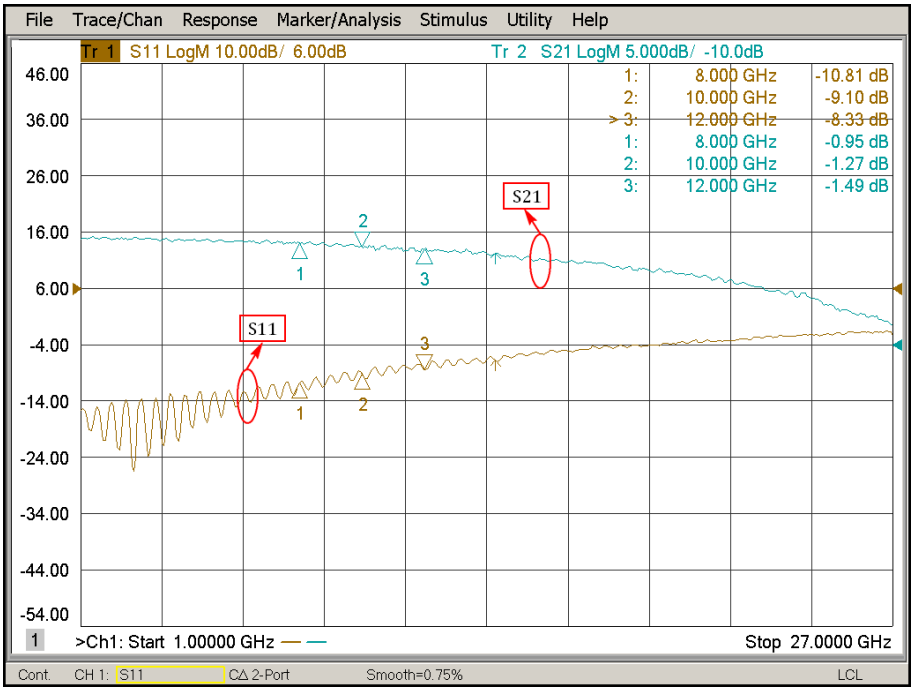


(a) ON-state S-parameters

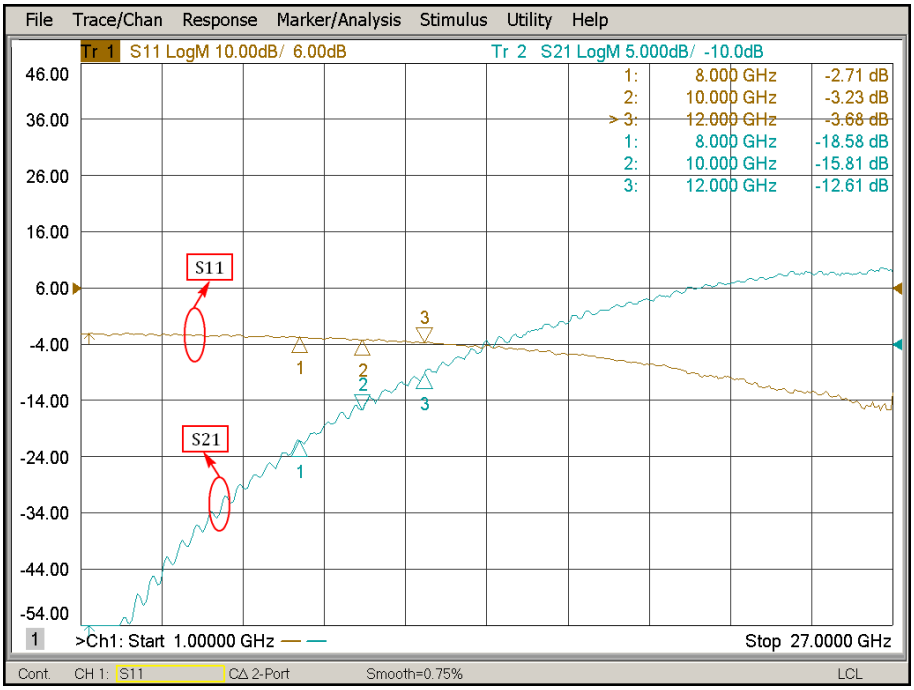


(b) OFF-state S-parameters

Figure 5.15: SPST2 S-parameters

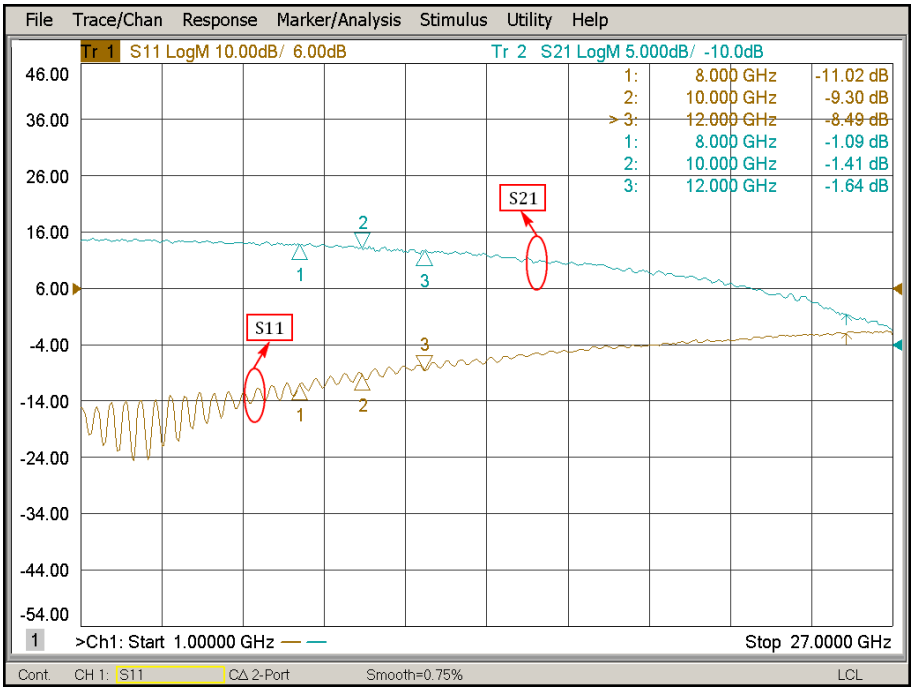


(a) ON-state S-parameters

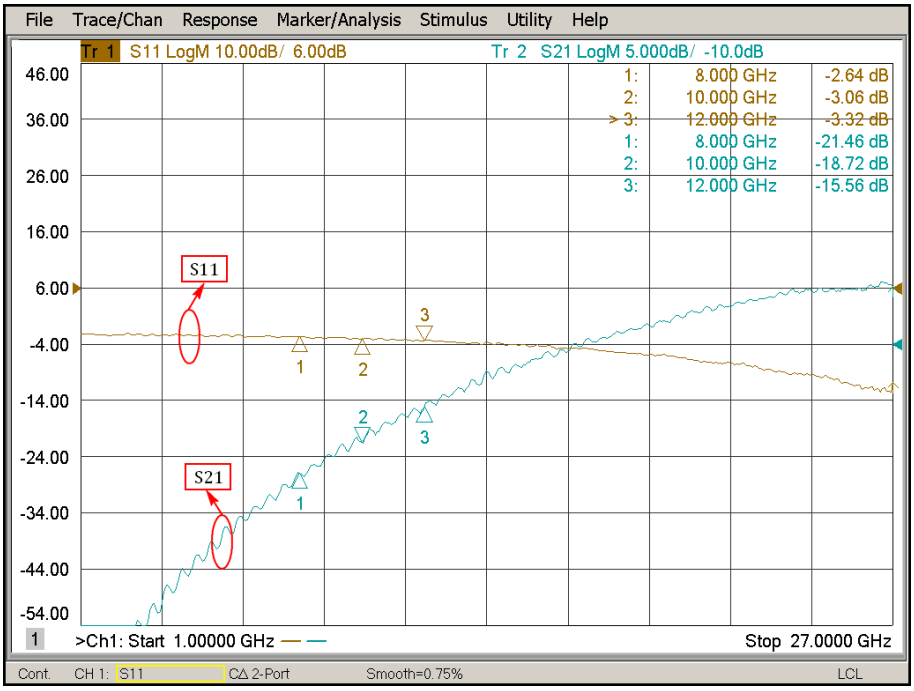


(b) OFF-state S-parameters

Figure 5.16: SPST3 S-parameters

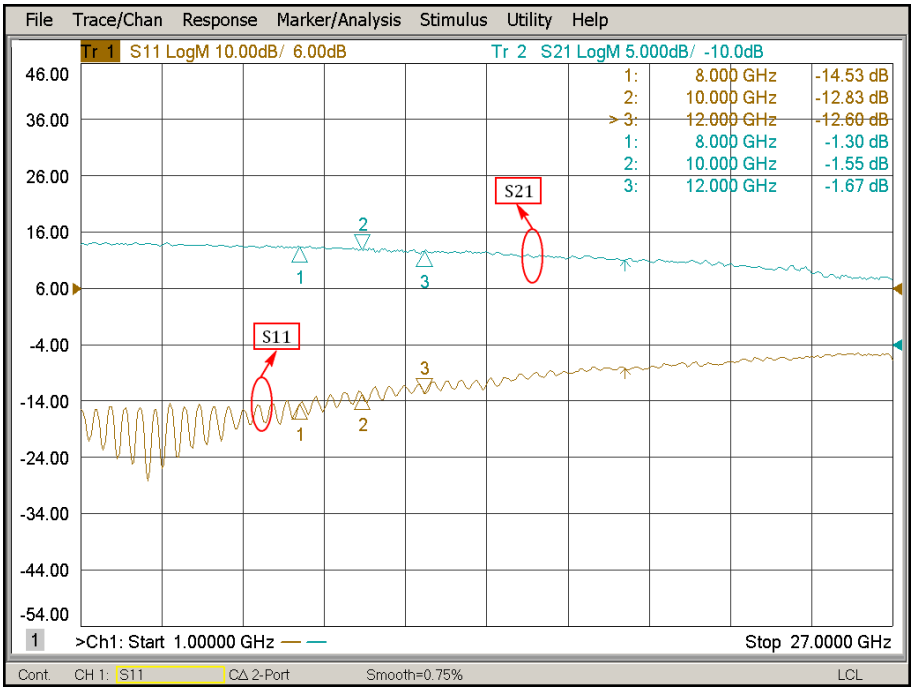


(a) ON-state S-parameters

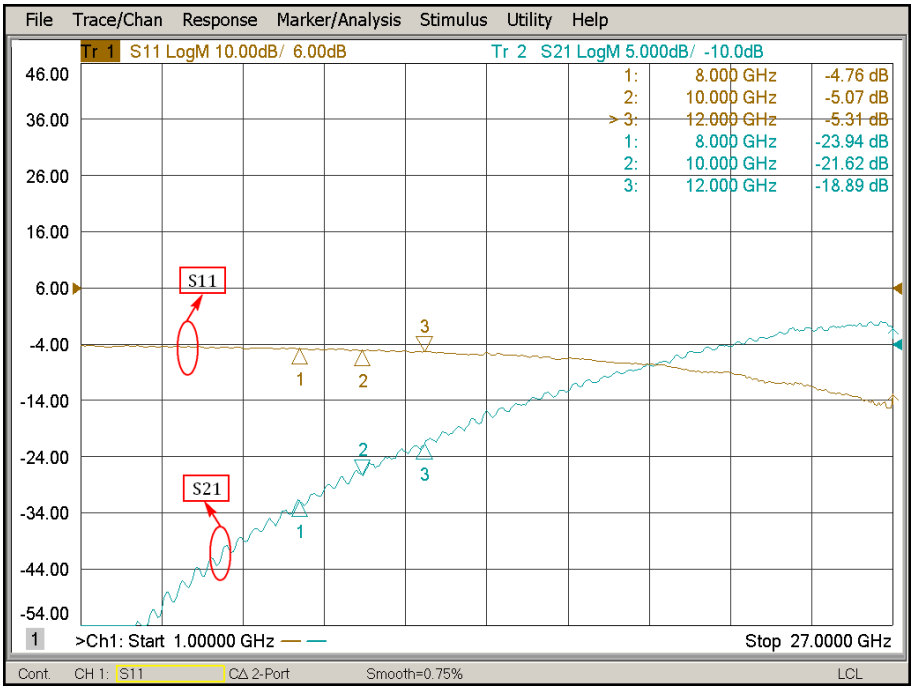


(b) OFF-state S-parameters

Figure 5.17: SPST4 S-parameters



(a) ON-state S-parameters



(b) OFF-state S-parameters

Figure 5.18: SPST5 S-parameters

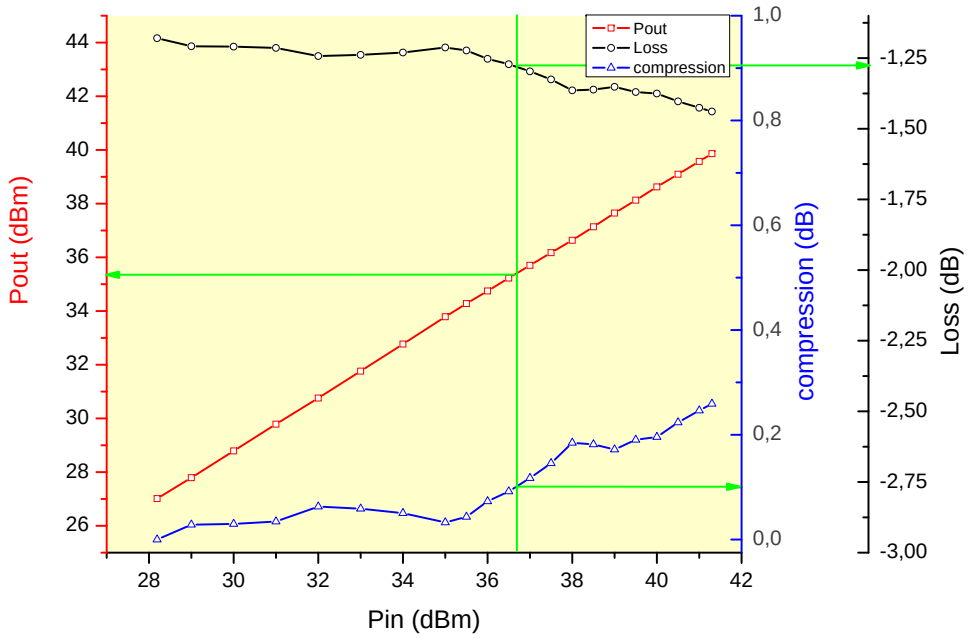


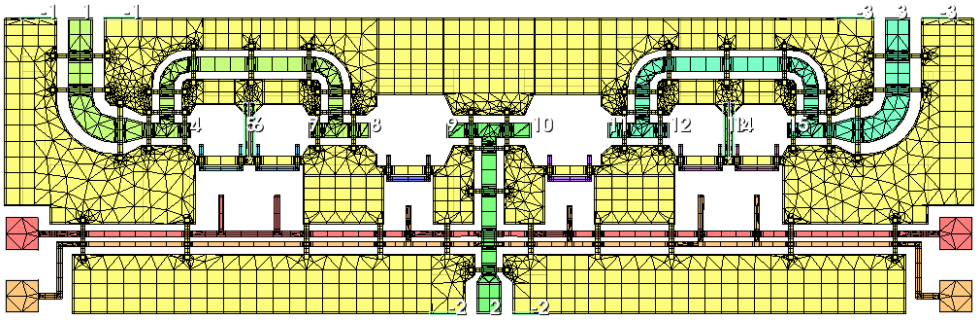
Figure 5.19: Large-Signal Compression and Loss vs Input Power

Table 5.3: SPST Measurement summary

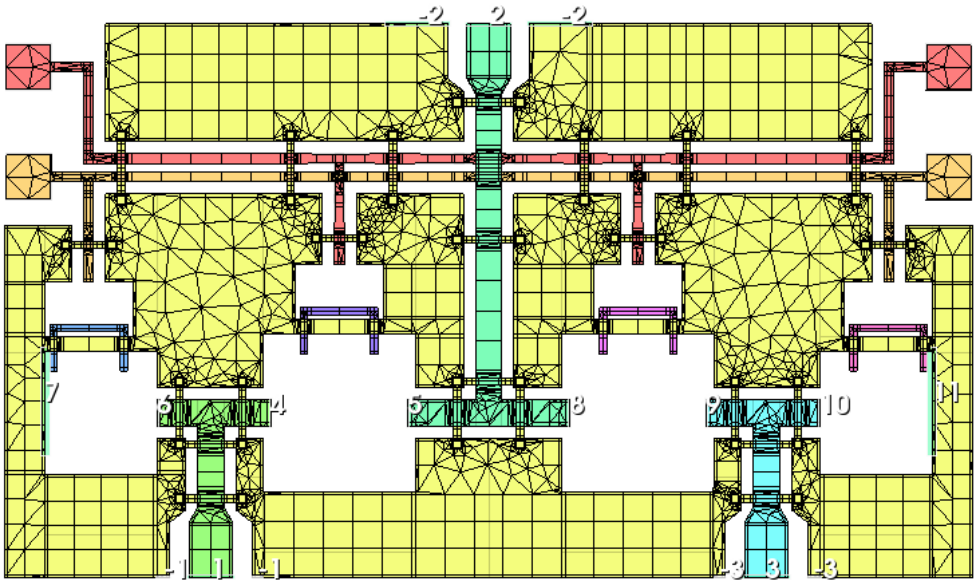
	Applied Voltages: 0V – ON, -25V – OFF														
	SPST1			SPST2			SPST3			SPST4			SPST5		
	f (GHz)			f (GHz)			f (GHz)			f (GHz)			f (GHz)		
	8	10	12	8	10	12	8	10	12	8	10	12	8	10	12
RL (ON) (dB)	-10.6	-9.0	-8.1	-9.2	-7.6	-6.6	-10.8	-9.1	-8.3	-11.0	-9.3	-8.4	-14.5	-12.8	-12.6
RL (OFF) (dB)	-3.3	-3.8	-4.1	-1.9	-2.4	-2.8	-2.7	-3.2	-3.6	-2.6	-3.0	-3.3	-4.7	-5.0	-5.3
IL (dB)	-1.2	-1.6	-1.8	-1.1	-1.5	-1.9	-0.9	-1.2	-1.4	-1.0	-1.4	-1.6	-1.3	-1.5	-1.6
Isolation (dB)	-21.7	-19.1	-16.0	-18.7	-15.7	-12.4	-18.5	-15.8	-12.6	-21.4	-18.7	-15.5	-23.9	-21.6	-18.8
RL: Return Loss ON&OFF are the states IL: Insertion Loss															

5.6 SPDT Design

With the fabrication of the SPSTs, the model optimized and SPDT are designed according to this model. To make the probing easier, all ports are located on north-south direction. Two different type of layout generated, one of them has positive effect on isolation and the other is optimized for insertion loss. Fig.4.20 (a) shows the layout of the SPDT which is optimized for isolation and Fig.4.20 (b) for the other SPDT.



(a) optimized for isolation

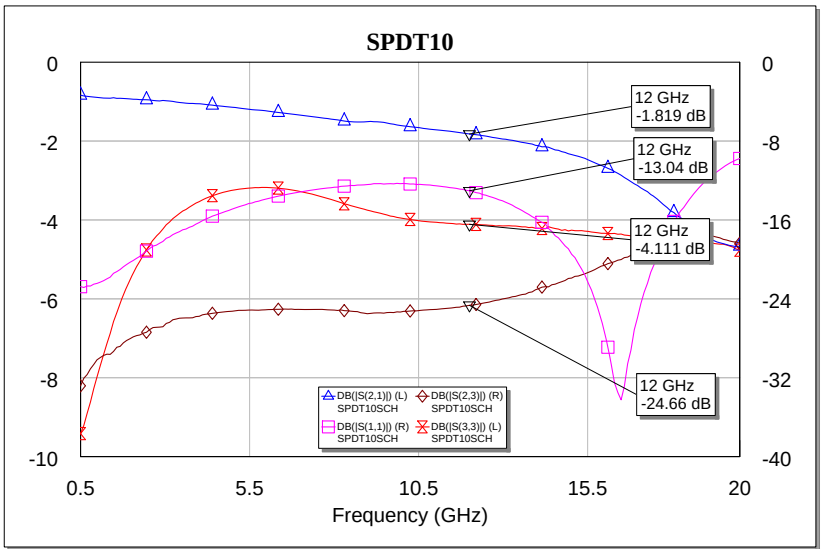


(b) optimized for insertion loss

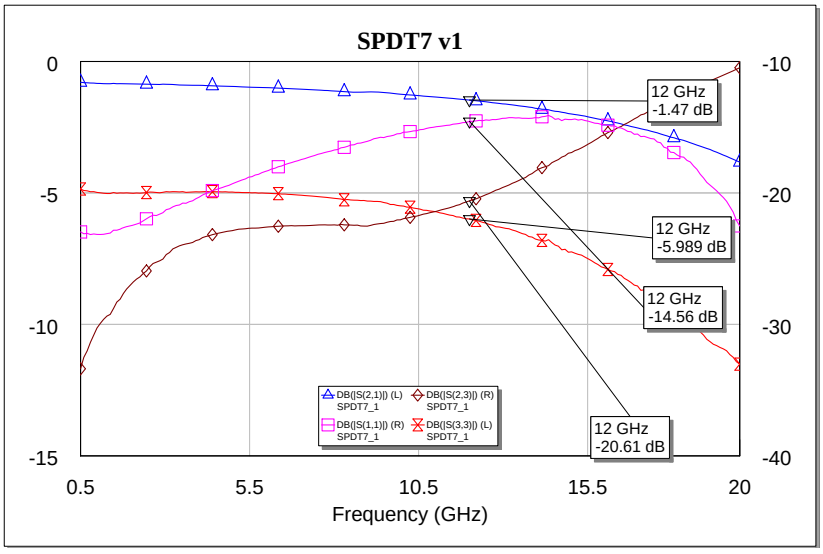
Figure 5.20: SPDT Layouts

Also the meshing and required ports for EM simulation represented in Fig.4.20. In these layouts, HEMTs are extracted for EM simulation. The pads

on east-west direction are the DC pads for biasing the HEMTs first layout has 15 ports while the second layout has 11 ports. EM simulation results for both layout are represented in Fig.4.20.



(a) optimized for isolation



(b) optimized for insertion loss

Figure 5.21: EM simulation results

The comparison table of designed SPDTs with design goals are summarized in Table 4.4.

Table 5.4: Summary of SPDT design

	Applied Voltages: 0V – ON, -25V – OFF		
	Design Goal @ 10GHz	SPDT1 @ 10GHz	SPDT2 @ 10GHz
RL (OFF-State)	10 dB	12.30	15.40
Insertion Loss	2 dB	1.60	1.20
Isolation	20 dB	25.30	22.00

Results show that first layout has 3dB better isolation and second layout has 0.4dB better insertion loss.

Chapter 6

Conclusion

Design of low phase noise VCO and high power SPDT switch at X-bant has been presented. To design the VCO a commercial foundry process is used but SPDT designed with Bilkent University GaN-SiC process in NANOTAM.

Designed MMIC VCO requires single HBT and one varactor and achives 26% (8.8∼11.4GHz) tuning range with output power 9-13dBm. The architecture used in the design with properly selected components, the tuning range of the MMIC VCO is close to the resonant frequency range with the resonator (7.6∼10.5GHz). A comparison table of several VCOs in GaAs HBT is given in Table 5.1. Considering the tuning range, the phase noise of the designed VCO is really low with acceptable power consumption and area requirements. As the rf chokes are located on the MMIC, size is increased, but it is possible to reduce the size by excluding them.

To design the SPDT, first mesa-resistors designed and fabricated to be used in switch type HEMTs. Switch type HEMTs are manufactured, modeled and tested in SPST switch structures. Switch HEMT model is optimized with the results of SPSTs and at the end, two types of SPDT designed; one for better isolation, one for better insertion loss (IL) by using the HEMT models. With these configurations; 12.3dB RL, 1.6dB IL and 22dB isolation at worst case achieved. A comparison table of several SPDT in GaN is given in Table 5.2. The proposed

SPDTs have the best power features with 0.2dB compression at 40.5dBm (CW) at the output. Moreover, the sizes are less than hlaf the size of the smallest SPDT in Table 5.2.

In these projects, the idea is not to design the lowest phase noise VCO and the state-of-the-art SPDT. The main purpose is to design and fabricate the MMICs in Turkey to reduce the dependancy on imported RF circuits. The VCO project is supported by UYAK project and because diminishing financial support at the end of the project, the VCO was not fabricated.

As a future work, VCO can be fabricated and it is possible to customize the design for other frequency ranges. With one of the suitable phase noise measurement techniques in chapter 4, the performance of the VCO will be tested. On the other hand, SPDTs will be fabricated in Bilkent University and both small-signal and large-signal measurements will be performed.

Table 6.1: Comparison Table of Recent VCOs in GaAs HBT

	Freq. (GHz)	Tuning Range (%)	PN (dBc/Hz@1MHz offset)	DC Power (mW)	Area (mm^2)	FOM_T	Technology
[11]	5.6∼16.8	69.8	-112	228.3	8.6×6.8	-186	InGaP-GaAs HBT
[12]	11.7∼12.28	4.75	-113.8	36	0.7×0.82	-173	InGaP-GaAs HBT
[13]	11.65∼12.1	3.78	-108	25.7	0.73×0.74	-167	InGaP-GaAs HBT
This Work	8.8∼11.4	26	-117	75	1×1	-186	InGaP-GaAs HBT

Table 6.2: Comparison Table of Recent SPDTs on GaN

	Freq. (GHz)	IL (dB)	Isolation (dB)	RL (dB)	Power (dBm)	Compression (dB)	Area (mm^2)	Technology
[14]	8∼11	3.5	-30	10	44 (pulsed)	-	4×1.8	CPW GaN-SiC
[15]	up to 13	1.2	-30	-	39.2 (-)	1	1.8×2.4	Microstrip GaN
[16]	2∼18	4	-15	-	34.4 (CW)	1	3.1×3.2	CPW GaN
This Work	DC∼12	1.4	-20	14.5	40.5 (CW)	0.2	1.7×0.94	CPW GaN-SiC

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Appendix A

Varactor

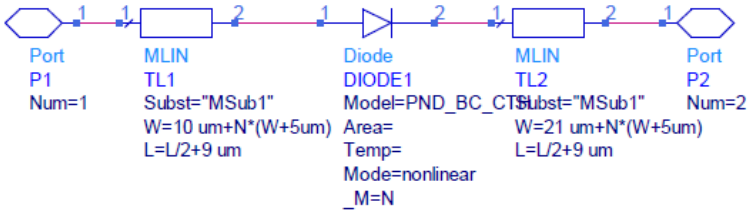

Figure A.1: Varactor Model

Table A.1: Varactor Parameters

Name	Description	Unit	Default
ID	Name		BC Finger Type
W	B-Metal Width	μm	10
L	B-Metal Length	μm	10
N	# of Fingers		1

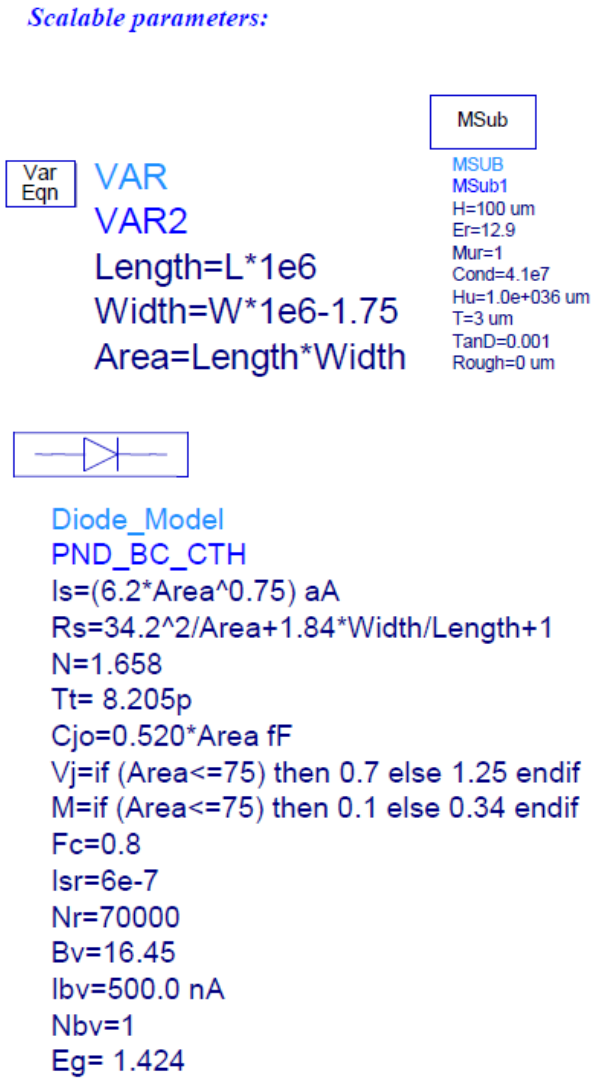

Figure A.2: Varactor Model (Detailed)