DESIGN AND DEVELOPMENT OF *X*-BAND GaN-BASED LOW-NOISE AMPLIFIERS

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By
Salahuddin Zafar
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Design and Development of X-band GaN-based Low-Noise Amplifiers
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We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Doctor of Philosophy.

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ABSTRACT

DESIGN AND DEVELOPMENT OF X-BAND GaN-BASED LOW-NOISE AMPLIFIERS

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December 2022

Gallium nitride (GaN) high electron mobility transistor (HEMT) technology emerged as a preferable candidate for high-power applications. GaN HEMTs on silicon carbide (SiC) substrate provide the best combination of speed and power due to high power density, escalated saturated carrier velocity, high efficiency, enhanced electrical breakdown, and superior thermal conductivity. Over the years, GaN technology also started to take its place in low-noise applications due to built-in power handling capability at the receive end of transceivers for compact designs and high linearity.

For GaN-based low-noise amplifiers (LNAs), improving the noise figure (NF) and getting it close to other competitive technologies is always challenging. Moreover, further improvement in the robustness of GaN-based LNAs in terms of survivability and reverse recovery time (RRT) is needed. For this purpose, NANOTAM's 0.15 µm GaN on SiC HEMT process is used to realize LNAs, one with survivability as high as 42 dBm and the other having NF as low as 1.2 dB. Survivability is investigated in terms of gain compression and forward gate current, while RRT is explored in detail with respect to the RC time constant of transistor and trap phenomenon. In the LNA design, the significance of inductive source degenerated HEMT, and the role of stability networks towards NF improvement are discussed in detail.

Furthermore, thermal simulations and infrared (IR) thermographic measurements of the LNA monolithic microwave integrated circuit are correlated to unveil the maximum channel temperature buried inside the two-dimensional electron gas of HEMT.

Keywords: GaN on SiC, low-noise amplifier, reverse recovery time, survivability, inductive source degeneration, IR imaging, finite element analysis.

ÖZET

X-BANT GaN TABANLI DÜŞÜK GÜRÜLTÜLÜ YÜKSELTEÇ TASARIMI VE GELİŞTİRİLMESİ

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Galyum Nitrür (GaN) Yüksek Elektron Hareketlilikli Transistör (HEMT) teknolojisi yüksek güçlü uygulamalar için tercih edilen bir aday olarak ortaya çıktı. Silisyum karbür (SiC) alttaş üzerine üretilen GaN HEMT'ler, yüksek güç yoğunluğu, artırılmış doymuş taşıyıcı hızı, yüksek verimlilik, gelişmiş elektriksel bozulma ve üstün termal iletkenlik sayesinde en iyi hız ve güç kombinasyonunu sağlar. Yıllar geçtikçe, GaN teknolojisi, kompakt tasarımlar ve yüksek doğrusallık için yüksek güç taşıma kapasitesi nedeniyle alıcı-vericilerin alıcı ucunda kullanılan düşük gürültülü uygulamalarda da yerini almaya başladı.

GaN tabanlı düşük gürültülü yükselteçler (LNA'lar) için, gürültü faktörünü (NF) iyileştirerek rakip teknolojilere yaklaştırmak zorlayıcıdır. Ayrıca, GaN tabanlı LNA'ların dayanıklılığında, hayatta kalma ve geri dönüş süresi (RRT) açısından daha fazla iyileştirmeye ihtiyaç vardır. Bu amaçla, NANOTAM'ın 0.15 µm SiC tabanlı GaN HEMT fabrikasyasonu kullanılarak beka kabiliyeti 42 dBm'ye kadar çıkabilen ve NF'si 1.2 dB kadar düşük olan LNA'lar gerçekleştirilmiştir. LNA'nın beka kabiliyeti, kazanç kısılması ve ileri kapı akımı açısından incelenirken, RRT, transistörün RC zaman sabiti ve tuzak fenomeni ile ilgili olarak ayrıntılı olarak araştırılmıştır. LNA tasarımında, endüktif kaynak dejenere HEMT'nin önemi ve kararlılık devrelerinin NF'de sağlanan iyileştirmelere yönelik rolü ayrıntılı olarak tartışılmaktadır.

Ayrıca, LNA monolitik mikrodalga tümleşik devresinin termal simülasyonları ve kızılötesi termografik ölçümleri, HEMT'nin iki boyutlu elektron gazının içinde görülen maksimum kanal sıcaklığını ortaya çıkarmak için ilişkilendirilmiştir.

Anahtar sözcükler: SiC tabanlı GaN, düşük gürültülü yükselteç, geri dönüş süresi, beka kabiliyeti, endüktif kaynak dejenerasyonu, kızılötesi görüntüleme, sonlu eleman analizi.

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List of Abbreviations and Acronyms

2DEG Two-dimensional electron gas

AlN Aluminum nitride

CS Common source

FEA Finite element analysis

FoM Figure of merit

GaAs Gallium arsenide

GaN Gallium nitride

HEMT High electron mobility transistor

IR Infrared

IRC Input reflection coefficient

ISD Inductive source degenerated

LNA Low-noise amplifier

MIM Metal-insulator-metal

MMIC Monolithic microwave integrated circuit

MOCVD Metal organic chemical vapor deposition

MTTF Median-time-to-failure

NF Noise figure

$\mathbf{NF_{min}}$ Minimum noise figure

OIP3 Output third-order intercept point

ORC Output reflection coefficient

$\mathbf{P_{1dB}}$ Output power at 1-dB gain compression

PECVD Plasma-enhanced chemical vapor deposition

RRT Reverse recovery time

SiC Silicon carbide

SiGe Silicon-germanium

$\mathbf{T_{max}}$ Maximum channel temperature

Chapter 1

Introduction

Gallium nitride (GaN) high electron mobility transistor (HEMT) technology has emerged as a preferable candidate for defense, space, and commercial applications [1–4]. GaN HEMTs have high power density, escalated saturated carrier velocity, high efficiency, enhanced electrical breakdown, and superior thermal conductivity [5–7]. Table 1.1 summarizes the comparison of GaN with other commonly used semiconductors [8–11]. The parameters compared are band-gap energy (E_g), breakdown field (E_c), electron mobility (μ_n), saturated velocity (v_{sat}), and thermal conductivity (k). Preferred choices of substrates for GaN HEMT technology are Si, SiC, and sapphire, depending on the application [5, 12–16]. SiC is used for power performance due to its high thermal conductivity [17–20]. Diamond is also used as a substrate for high-power RF applications [19, 21–23].

CMOS technology is advantageous in terms of cost and integration density [24], whereas Silicon-germanium (SiGe) [25] and Gallium arsenide (GaAs) [26] have been reported as better choices in terms of noise performance. Although GaN HEMT technology was initially oriented towards power performance, using the same technology for both transmit and receive chains had become desirable for compact and efficient transceiver modules. Moreover, robust and highly survivable GaN-based low-noise amplifiers (LNAs) are realizable due to GaN's built-in power handling capability without complex protection circuitry at the receive

Table 1.1: A comparison of RF semiconductors' physical properties.

Material	E_g **(eV)**	E_c **(MV/cm)**	μ_n **(cm²/(V.s))**	v_{sat} **(10^7 cm/s)**	k **(W/(K.cm))**
Si	1.12	0.3	1350	1.0	1.5
SiGe	0.84-1.12	0.3	1350-4315	2.4	0.8-1.3
GaAs	1.42	0.4	8500	2.0	0.5
GaN	3.39	3.3	2000	2.5	1.3
Diamond	5.45	5.6	1900	2.7	20
4H-SiC	3.26	2.0	720^a 650^c	2.0	4.5
6H-SiC	3.0	2.4	370^a 50^c	2.0	4.5

[a]mobility along the a-axis, [c]mobility along the c-axis

end [27–29]. Numerous GaN HEMT LNAs covering a wide frequency range have been reported in recent years [30–42]. These include sub-2 dB noise figure (NF) LNA designs in X-band [42–46].

1.1 Thesis Motivation and Goals

The LNA is the first and critical component of the receiver in an RF transceiver system. The NF parameter of an LNA determines the weakest detectable signal. Moreover, the robustness of LNA defines its power handling capability. This thesis addresses the critical parameters related to the robustness of GaN-based LNAs and achieving a low NF comparable with competitive technologies. Moreover, one of the fabricated LNAs has been used to unveil the maximum channel temperature (T_{max}) buried inside the two-dimensional electron gas (2DEG) region of HEMT.

For high-power applications, the robustness of LNA is a critical factor that is the main focus of GaN HEMT technology. Robustness is mainly defined in terms of two important figures of merit (FoMs), namely survivability and reverse recovery time (RRT). LNAs are supposed to survive high input powers and regain normal operating conditions in a very short time after removing high-input drives.

Various reports cover robustness in terms of survivability in the literature, but only a few works address RRT and related aspects. Therefore, the motivation of the thesis is to explore RRT with respect to the RC time constant and trap phenomenon. Moreover, improving the survivability and addressing it in terms of gain compression and forward gate current are also the goals of the thesis.

For GaN-based LNAs, improving the NF and getting it close to GaAs technology are challenging. There have been reports for sub-1.5 dB NF for K- and Ka-bands [47–51], lower NF at X-band remained a challenge. Therefore, to address this challenge, a design approach using inductive source degenerated (ISD) HEMT in all the stages of a multi-stage LNA is adopted. The criticality of stability networks towards NF contribution and their design is discussed in detail.

Another aspect of the thesis is to propose a method to reveal the channel temperature profile of HEMTs in a multi-stage monolithic microwave integrated circuit (MMIC). Infrared (IR) thermography that measures surface temperature has a diffraction-limited resolution. Moreover, using IR thermography, the measurement of T_{max} inside 2DEG of HEMT is impossible. A correlation method, using IR measurements and finite element analysis (FEA) simulations, is proposed to find the hotspots inside the MMIC accurately, thus revealing the T_{max} of the HEMTs. One of the designed LNAs is chosen for IR thermographic measurements and FEA thermal simulations.

1.2 Thesis Organization

This thesis uses NANOTAM's in-house 0.15 µm AlGaN/GaN fabrication technology to realize X-band LNAs. Fabrication process steps and device characterization are discussed in Chapter 2.

Three LNA MMICs have been designed and fabricated using the above-mentioned process. One of these LNAs is designed to improve survivability. RRT

measurements are performed on the same LNA. These aspects have been addressed in Chapter 3.

Chapter 4 addresses the design, fabrication, and characterization of the other two LNAs and the role of ISD HEMTs and stability networks towards NF improvement.

Chapter 5 contains the IR thermographic measurements and FEA simulations of one of the LNA MMICs. A correlation method is devised to unveil the T_{max} of the HEMTs in the MMIC, critical for accurate median-time-to-failure ($MTTF$) calculations.

Finally, the thesis is summarized in Chapter 6 with a discussion and conclusion.

Chapter 2

Fabrication Process and Device Characterization

2.1 Device and MMIC Fabrication Process

2.1.1 Epitaxial Structure

NANOTAM's 0.15 µm AlGaN/GaN on SiC process is used for X-band low-noise applications. Epitaxial growth of HEMT, shown in Fig. 2.1, is performed using in-house metal organic chemical vapor deposition (MOCVD) on a 3-inch SiC substrate. SiC is chosen as a substrate because of its high thermal conductivity and lattice mismatch of only +3.5% with GaN [7]. The X-band process considers breakdown voltages and power ratings along with noise performance.

Epitaxial growth starts with the deposition of a 100 nm aluminum nitride (AlN) nucleation layer over a 3-inch diameter, 300 µm 4H-SiC substrate. The AlN layer improves the surface roughness and provides a smooth transition to the following GaN buffer layer by reducing the effect of lattice mismatch. Moreover, it acts as an insulating dielectric layer in the structure, thereby improving the vertical breakdown of the device.

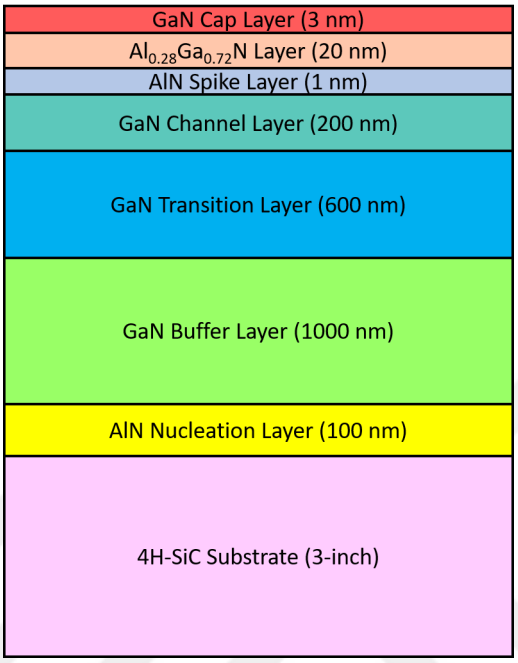

Figure 2.1: Cross-sectional view of epitaxial structure.

The next step is the growth of a 1000 nm iron-doped highly resistive GaN buffer layer. This is a high-quality layer with low defect density, thereby minimizing the buffer leakage and traps. The thickness of this layer is kept higher to obtain a lower dislocation interface, which improves the 2DEG quality. Although an undoped buffer layer would have a lower trap density [52], it is intentionally doped to make it highly resistive. Proper doping concentrations to achieve the high resistivity of the GaN layer minimizes the buffer-induced current collapse [53–55]. Fe-doping is preferred over C-doping to decrease the deep-acceptor traps and buffer leakages. Unlike Fe-doping, a high voltage-dependent current collapse results in a C-doped buffer because of the deep-acceptor traps [53]. Moreover, a higher energy barrier between the Fe-doped buffer layer and channel ensures a smaller buffer leakage current [56].

In order to cater for the diffusion tail of the Fe-doped buffer, a 600 nm thick GaN transition layer is grown on top of the buffer. The growth continues with a highly smooth low defect density, 200 nm thick un-doped GaN channel layer. A thin spike layer on top of the channel layer provides enhanced charge confinement and mobility in the channel [57]. In order to form a heterojunction and 2DEG in

the channel region, a wider bandgap 20 nm thick AlGaN (28% Al) layer is grown after the spike layer. The epitaxial growth concludes with a 3 nm thin GaN cap layer, which serves the purpose of better ohmic contact formation and physical isolation of the AlGaN layer from external effects.

The quality of the grown wafer is ensured by characterizing various parameters, such as electron mobility, sheet charge density, mesa sheet resistance, and surface roughness. Using Hall effect measurements, the sheet charge density and 2DEG electron mobility for the grown wafer are greater than 1 x 10^{13} cm^{-2} and 2000 $cm^2/(Vs)$, respectively. Mesa sheet resistance value is measured as lower than 250 $\Omega/\square$. The surface roughness measured using atomic force microscopy turns out to be less than 1 nm.

2.1.2 Active and Passive Device Fabrication Steps

Active and passive devices are fabricated over the grown wafers. Active device fabrication involves ohmic contact formation, mesa isolation etching, gate formation, passivation, and metallization. Passive device fabrication steps include thin-film resistor (TFR) and capacitor formation.

Active device fabrication starts with ohmic contact formation, performed by depositing a 120 nm thick metal stack of Ti/Al/Ni/Au using an electron beam (e-beam) evaporator (Fig. 2.2). Annealing of the metal stack is performed at a temperature of around 850 °C in a nitrogen atmosphere. Ohmic contacts ensure the electrical connection between the channel and the upper part of the wafer.

The next step is mesa isolation etching, which includes the removal of epitaxial layers containing 2DEG from areas other than active device regions (Fig. 2.3). This leads to the electrical isolation of all on-wafer active devices. The mesa etching step is performed in an inductively coupled plasma reactive ion etching (ICP-RIE) system using a plasma-based dry etch process. Mesa-etched regions also serve the purpose of high-value resistances having a density of 250 $\Omega/\square$.

Figure 2.2: Cross-sectional view of the structure after ohmic contacts formation.

Figure 2.3: Cross-sectional view of the wafer after mesa etching.

After the mesa isolation and before the gate formation, coating a 100 nm Si_3N_4 dielectric passivation layer is the intermediate step. This layer is grown using a plasma-enhanced chemical vapor deposition (PECVD) system. Passivation minimizes the defects on the surface and neutralizes the surface states, thereby reducing electron trapping and virtual gate formation. The patterning of the gate foot regions of the T-gate structure is carried out by dry etching using the ICP-RIE system with a gas mixture of CHF_3, CF_4, and SF_6. Fig. 2.4 shows the cross-sectional view of the wafer after dielectric deposition and etching.

A 50 nm thick gate foot and 450 nm thick gate head consisting of Ni/Au stack are defined by e-beam lithography (Fig. 2.5). Ni forms the Schottky contact, and Au above Ni provides better conductivity and prevents oxidation. The gate foot length is 150 nm, and the gate head length is 500 nm for the T-gate structure.

On-chip TFR having a density of 30 $\Omega/\square$ are realized by depositing 80 nm of TaN by RF magnetron sputter system (Fig. 2.6). To use as interconnections

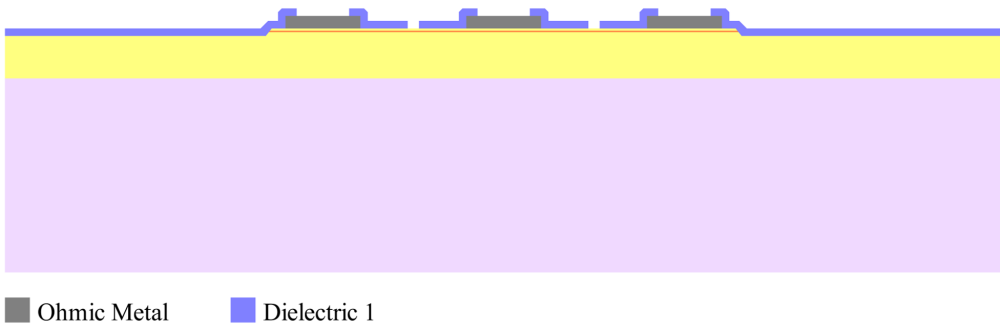

Figure 2.4: Cross-sectional view of the wafer after first dielectric deposition.

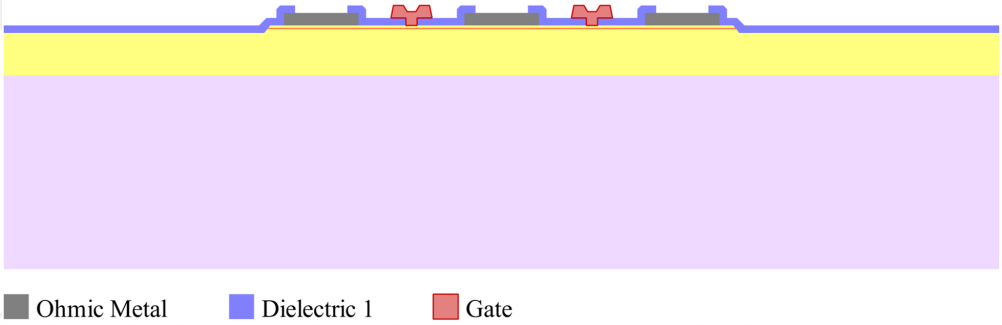

Figure 2.5: Cross-sectional view of the wafer after T-gate formation.

and form capacitors, two metal layers are deposited in the process. After patterning through photolithography, the Ti/Au first metal layer stack is coated using an e-beam evaporator system. Ti and Au in this stack have 100 nm and 1000 nm thicknesses, respectively. This layer serves the purpose of drain and source contacts of the transistors and the first metal of metal-insulator-metal (MIM) capacitors.

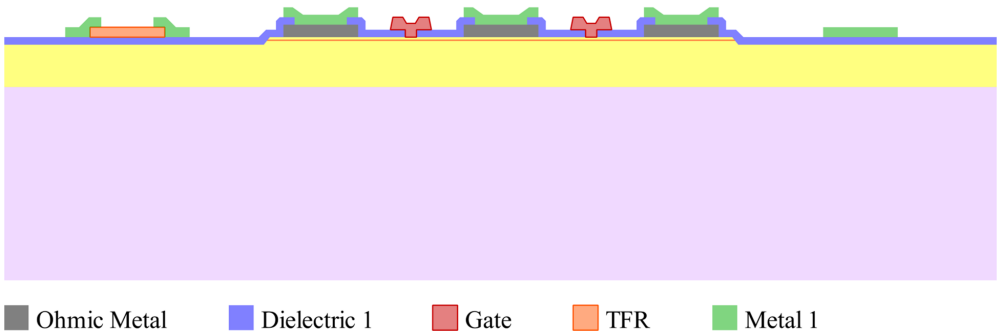

Figure 2.6: Cross-sectional view of the wafer after TFR and metal 1 deposition.

The second 220 nm thick Si_3N_4 layer is deposited with PECVD forming the

dielectric material for the capacitors (Fig. 2.7). In order to prevent the short circuits at metal-metal crossovers and reduce the parasitics, air bridges are formed (Fig. 2.7). A second 4 µm thick metal layer, used as the main interconnection layer, is coated with an electroplating system (Fig. 2.7). This metal layer also completes the MIM capacitor structure. On-chip capacitance density value is 270 pF/mm^2. The fabrication process of inductors is similar, having two metal layers and air bridges. The front-side process is concluded at this step.

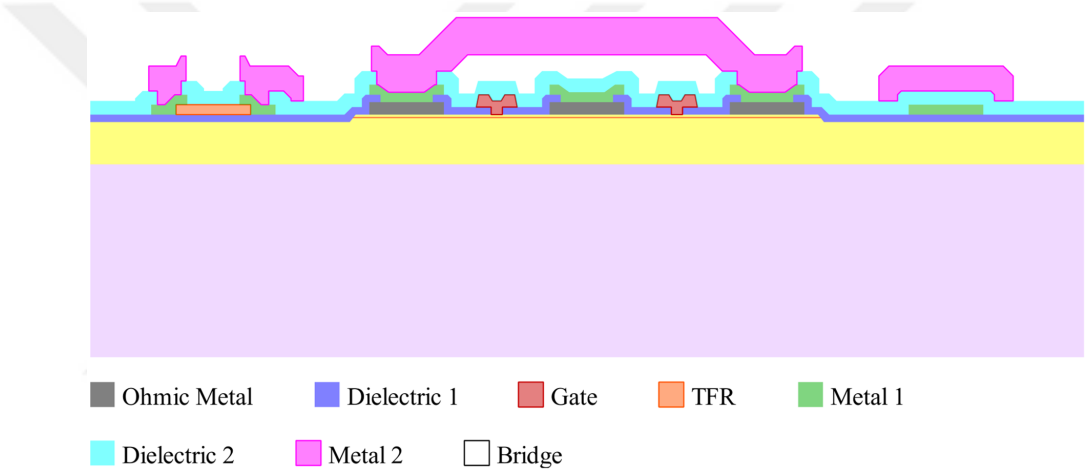

Figure 2.7: Cross-sectional view of the wafer after second dielectric passivation, air-bridge formation, and metal 2 layer coating.

The last step of the fabrication is the backside process. It includes 100 µm backside thinning, back-via holes opening through SiC substrate (using ICP-RIE dry etching), and 5.5 µm thick Au layer coating (using an electroplating system). Au layer coating is performed on the back side and the walls of via holes. These back-vias provide ground connections for microstrip transistors and circuits. The final cross-sectional view of the wafer, after the back-via process, containing a transistor and passive components is demonstrated in Fig. 2.8.

2.2 DC and RF Characterization

The characterization of active devices is performed using DC, small-signal, and large-signal measurement setups.

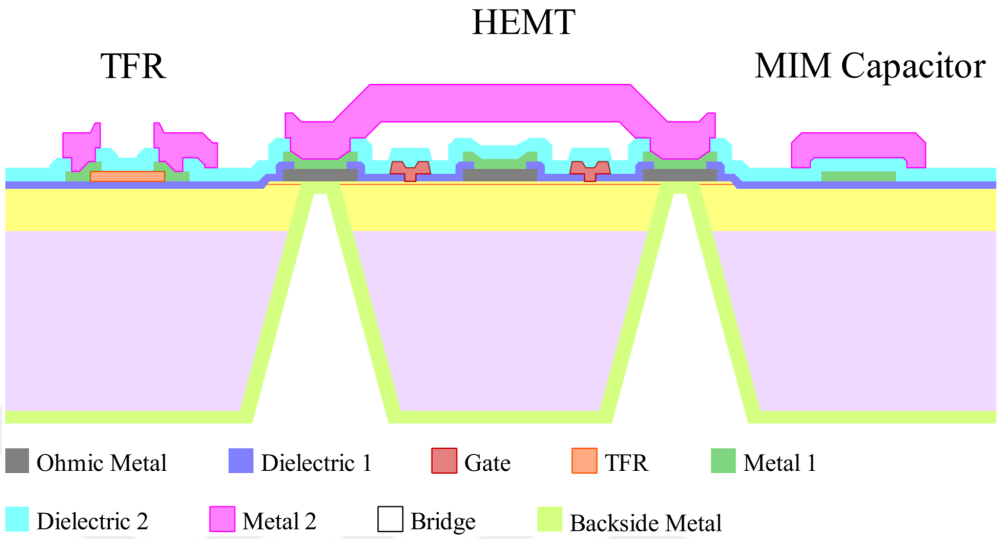

Figure 2.8: Cross-sectional view of the wafer after the backside process.

2.2.1 DC Characterization

Some of the DC FoMs for HEMTs are maximum saturated drain current (I_{dss}), maximum transconductance ($g_{m,max}$), pinch-off voltage (V_p), and breakdown voltage (V_{br}). B1505A Power Device Analyzer from Keysight Technologies[1] is used to perform DC measurements. On-wafer DC measurement setup is shown in Fig. 2.9.

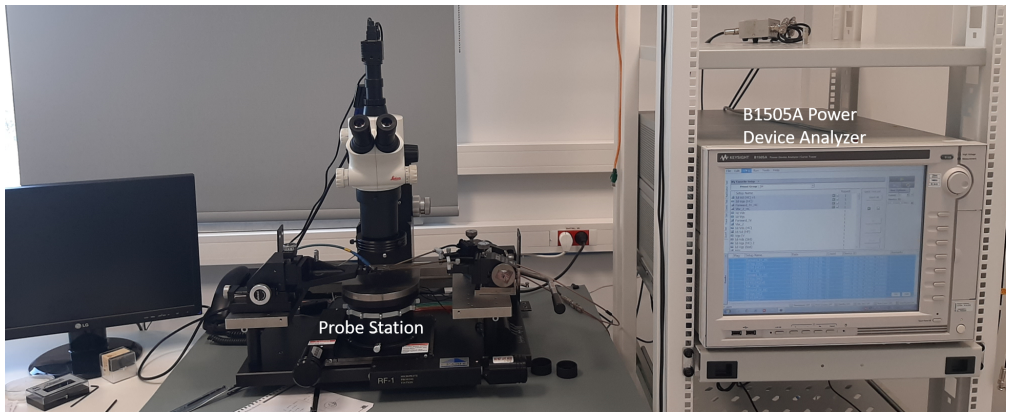

Figure 2.9: DC measurement setup.

The device's overall small-signal and large-signal performance is anticipated

[1]Keysight Technologies, Inc., Santa Rosa, CA 95403, USA

using the results of DC measurements. Higher values of I_{dss} and V_{br} are the indicators of higher RF power because of maintaining large current and voltage swings at the output of the device [58]. Moreover, the reliability of the device under DC and RF stress is predicted by drain and gate leakages. I-V measurements also demonstrate the knee voltages (V_{knee}). Fig. 2.10 shows a typical I-V measurement of a 4x75 µm common source (CS) HEMT. The values of I_{dss} and V_{knee} are obtained as 1.12 A/mm ($V_{drain} = 10$ V, $V_{gs} = 2$ V) and 5.10 V, respectively.

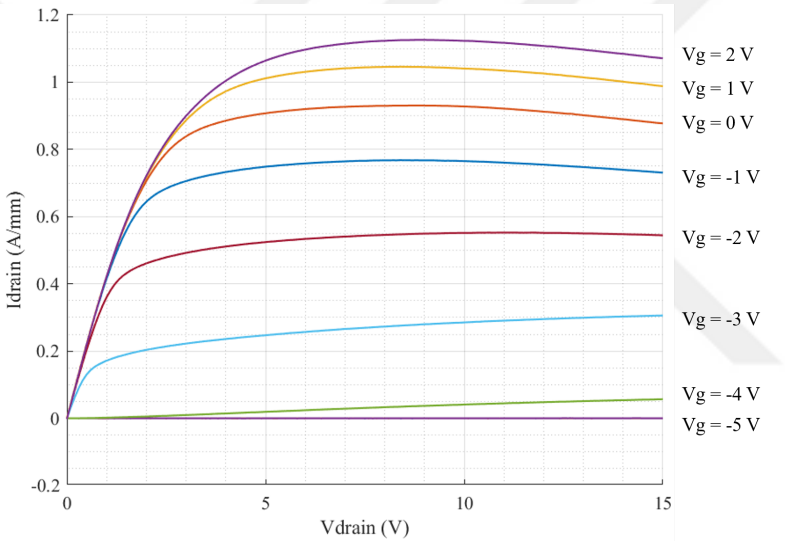

Figure 2.10: IV curves of 4x75 µm CS HEMT, using V_{gs} from -8 V to 2 V.

DC transconductance is defined as the ratio of the change in the drain current (I_d) to the change in the gate-to-source voltage (V_{gs}), given by the equation

$$g_m = \frac{\partial I_d}{\partial V_{gs}}. \tag{2.1}$$

It is a measure of predicting a small-signal gain of the transistor at higher frequencies without taking parasitic effects into account.

Fig. 2.11 shows the I_d-V_{gs} and g_m graph for drain voltages from 6 V to 10 V. The $g_{m,max}$ is measured as 270.8 mS/mm for $V_{drain} = 10$ V. The value of V_p, a valuable FoM in the characterization and MMIC design is -3.73 V. GaN HEMT is normally on, and a negative V_{gs} less than the V_p is required to turn the device off.

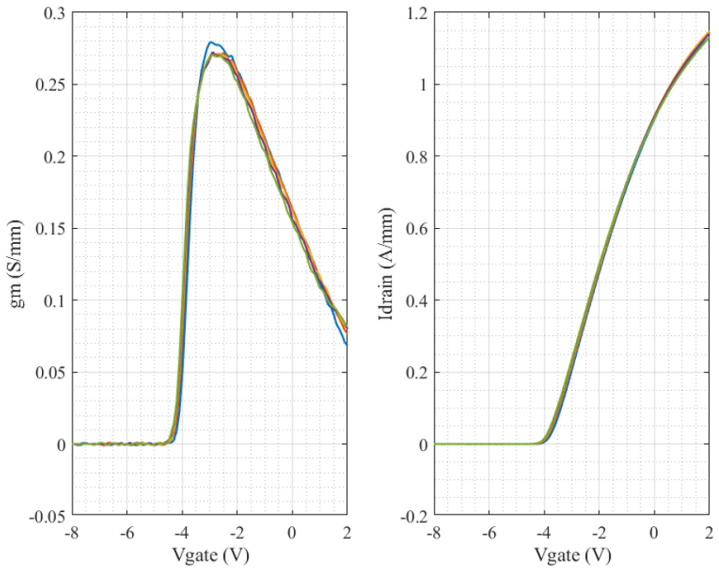

Figure 2.11: I_d-V_{gs} and g_m curves of 4x75 µm CS HEMT for V_{drain} from 6 V to 10 V.

Fig. 2.12 shows the DC breakdown measurements of the HEMT. Keeping the gate at a pinch-off level of −8 V, the drain voltage is swept to 25 V. For V_{drain} at 25 V, the drain and gate leakage currents are measured to be 510 µA/mm and 17.1 µA/mm, which are acceptable limits for the GaN HEMTs.

2.2.2 Small-signal Characterization

The small-signal analysis of the device refers to the region where input signal power is small enough that the device is assumed to be operating linearly [59]. Important FoMs to analyze the small-signal performance of a device are stability factor (K-factor), maximum available gain (MAG), maximum stable gain (MSG), cut-off frequency (f_T), and maximum frequency of oscillation (f_{max}). These FoMs are based on small-signal parameters (S-parameters), i.e., input reflection coefficient (IRC), output reflection coefficient (ORC), forward transmission, and reverse transmission.

Fig. 2.13 shows a small-signal characterization setup, where a network analyzer is a major instrument to measure the on-wafer S-parameters of the device under

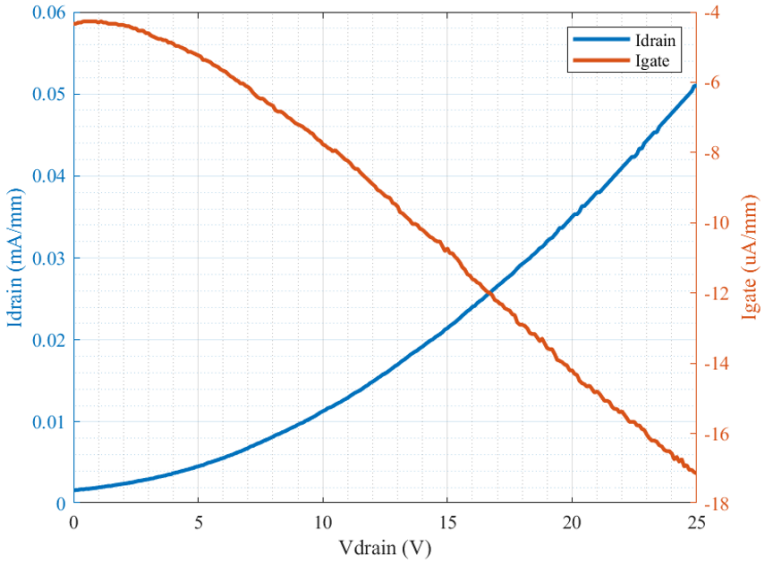

Figure 2.12: Breakdown characteristics of 4x75 µm CS HEMT showing the gate and drain leakage currents for $V_{gs} = -8$ V.

test (DUT). The probe station has a temperature-controlled chuck, and bias voltages are applied through either DC power supplies or pulsers for CW or pulsed measurements, respectively.

A device is unconditionally stable if Rollet's condition (given by Eq. 2.2) along with an auxiliary condition (given by Eq. 2.3) are satisfied at the same time [59].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.2}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.3}$$

A single parameter μ or its companion parameter μ' (given by Eq. 2.4 and 2.5) is enough alone to show the stability of any two-port network without any auxiliary condition [60].

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}{}^*| + |S_{12}S_{21}|} > 1 \tag{2.4}$$

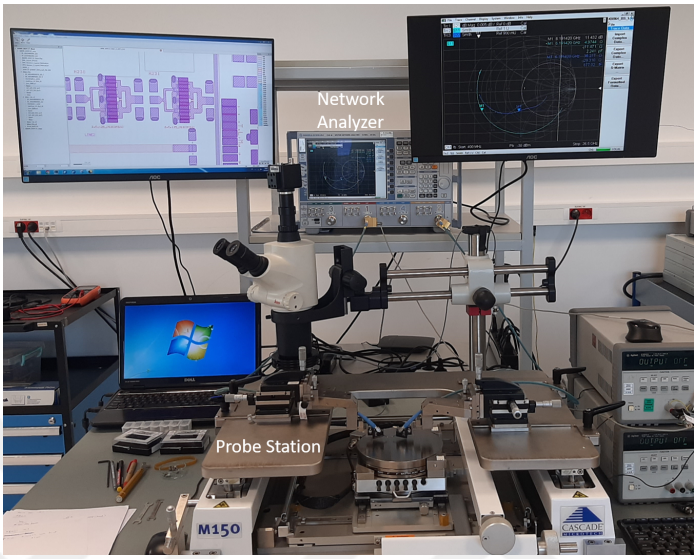

Figure 2.13: On-wafer small-signal characterization setup.

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{21}S_{12}|} > 1 \tag{2.5}$$

Two important FoMs, MAG and MSG, in the small-signal analysis are based on transducer power gain (G_T) given by Eq. 2.6 and 2.7.

$$G_T = \frac{Power\ delivered\ to\ the\ load}{Available\ power\ from\ the\ matched\ source} = \frac{P_L}{P_{AVS}} \tag{2.6}$$

$$G_T = \frac{(1 - |\Gamma_S|^2)|S_{21}|^2(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L)| - S_{12}S_{21}\Gamma_S\Gamma_L} \tag{2.7}$$

Setting $|S_{12}| = 0$ simplifies G_T expression to give unilateral transducer gain (G_{TU}) [61–63], given by Eq. 2.8.

$$G_{TU} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{2.8}$$

Small-signal gain of the transistor is typically defined by the terms MAG and MSG. MAG, referred to as maximum transducer power gain (G_{Tmax}), is given

by Eq. 2.9, where the transistor is unconditionally stable ($K > 1$) [59]. For conditionally stable transistors (K < 1), the term MSG is used and defined as MAG with $K = 1$ and given by Eq. 2.10.

$$MAG = G_{Tmax} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \tag{2.9}$$

$$MSG = G_{Tmax} = \frac{|S_{21}|}{|S_{12}|} \tag{2.10}$$

S-parameters measured for 4x75 µm CS HEMT are shown in Fig. 2.14. Fig. 2.15 illustrates MSG and MAG in the context of the K-factor.

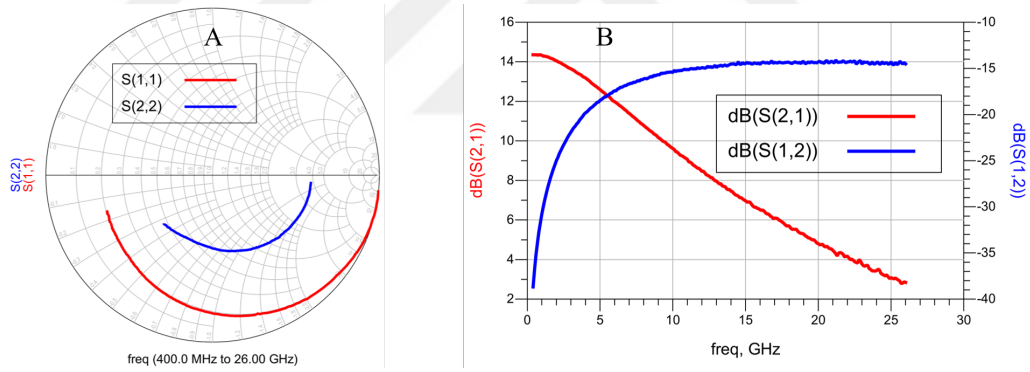

Figure 2.14: (A) IRC (S_{11}) and ORC (S_{22}), (B) Forward transmission (S_{21}) and reverse transmission (S_{12}) of a 4x75 µm CS HEMT at 12 V, 100 mA/mm.

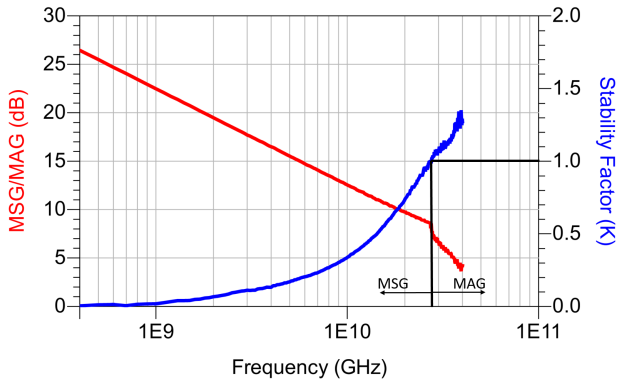

Figure 2.15: MSG/MAG and K-factor of a 4x75 µm CS HEMT.

f_T is defined as the frequency at which the current gain ($|h_{21}|$) becomes unity. It is approximtaed as

$$f_T \approx \frac{g_m}{2\pi C_{gs}}, \tag{2.11}$$

where g_m is the transconductance (Eq. 2.1) and C_{gs} is the gate-to-source capacitance. f_{max} is unity power gain frequency defined as the frequency where MAG becomes unity and given by

$$f_{max} \approx \frac{f_T}{2\sqrt{(R_s + R_g)g_{ds} + 2\pi f_T R_g C_{gd}}}, \tag{2.12}$$

where R_s, R_g, g_{ds}, and C_{gd} are source resistance, gate resistance, output conductance, and gate-to-drain capacitance, respectively.

Fig. 2.16 shows the f_T and f_{max} of 4x75 µm CS HEMT, determined using S-parameters. $|h_{21}|$ and MAG are extrapolated to achieve f_T and f_{max} as 46.5 GHz and 63.9 GHz, respectively.

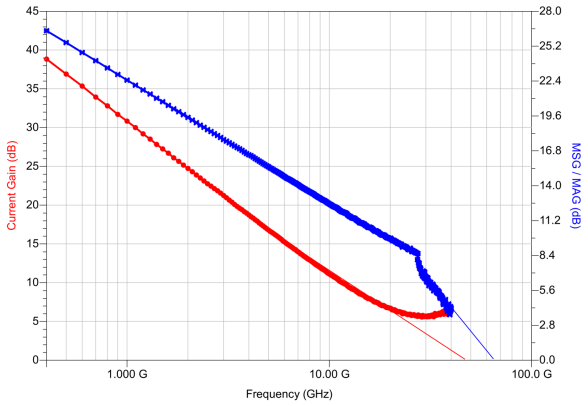

Figure 2.16: f_T and f_{max} of 4x75 µm CS HEMT showing fittings for current gain ($|h_{21}|$) and MAG.

2.2.3 Large-signal Characterization

Large-signal is defined as the input signal, which drives the device to operate in the non-linear region. Optimum load impedances for maximum gain and power are the same in the case of small-signal operations. On the other hand, for the large input powers, due to gain compression and power saturation, optimum

impedances for gain and power separate. Fig. 2.17 shows load-pull contours of gain (G_t) and output power (P_{out}) at 1-dB compression at 9 GHz for a 4x75 µm CS HEMT. The circles for G_t and P_{out} converge at different impedances.

Although it is the primary function of a PA to deliver high output powers, LNAs also have the requirements of P_{out} along with other performance parameters. These power and gain contours provide valuable information for designers while designing the matching networks for an LNA. In this thesis, load-pull measurements are utilized to extract the optimum impedances. Fig. 2.18 shows the block diagram of the vector-based load-pull measurement system.

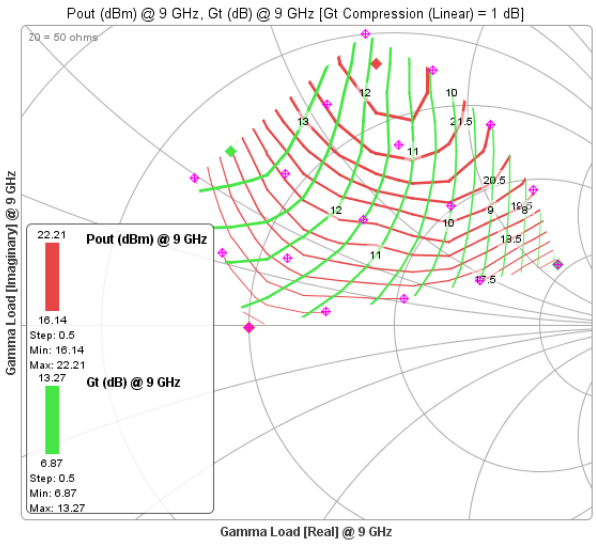

Figure 2.17: Load-pull contours of G_t and P_{out} of 4x75 µm CS HEMT at 9 GHz for 12 V, 100 mA/mm.

In the load-pull measurement system, low-loss couplers sample the incident and reflected waves at DUT's input and output. This leads to the direct calculation of available and delivered input and output powers via "a" and "b" waves, along with input, output, source, and load impedances at DUT reference planes.

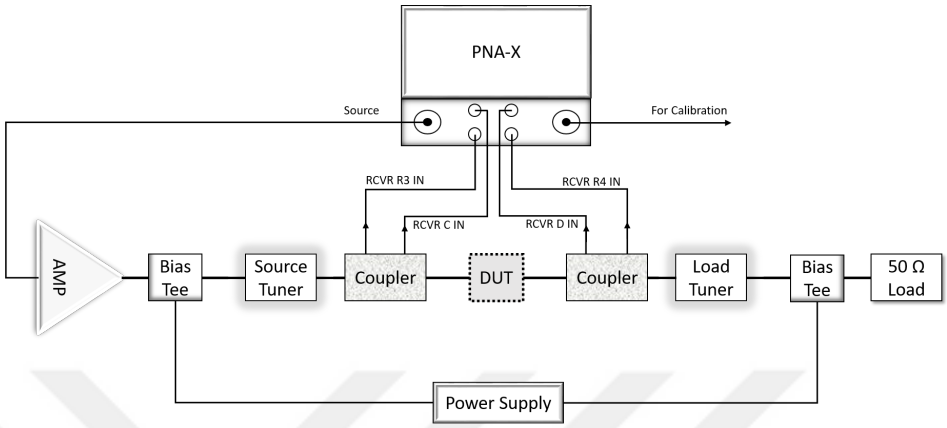

Figure 2.18: Schematic of VNA-based load-pull measurement system.

2.2.4 Noise Characterization

Fig. 2.19 shows a block diagram of a tuner-based automated noise characterization setup. The noise parameters (N-parameters) are represented and related by

$$NF = NF_{min} + 4\frac{R_n}{Z_o}\frac{|\Gamma_S - \Gamma_{opt}|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_S|^2)}, \tag{2.13}$$

where NF_{min} is the minimum noise figure, R_n is the equivalent noise resistance, Z_o is the matched load, Γ_S is the source reflection coefficient, Γ_{opt} is the optimum source reflection coefficient for minimum noise, and NF is the noise figure [64,65].

Proper calibration of the system is necessary to acquire accurate N-parameters. The conventional method to obtain the NF of the DUT is through the Friis formula given by Eq. 2.14, where F_{total} is the total measured NF, F_{DUT} is the NF of the DUT, F_{MS} is the NF of the measurement system, and $G_{A,DUT}$ is the available gain of the DUT.

$$F_{total} = F_{DUT} + \frac{F_{MS}-1}{G_{A,DUT}} \tag{2.14}$$

Eq. 2.14 shows that a low $G_{A,DUT}$ and a high F_{MS} result in erroneous measurements. Therefore, the automated N-parameters measurement system in Fig. 2.19 is based on the noise power method given by Eq. 2.15 [65], where NP is the total measured noise power, k is Boltzmann's constant, B is the measurement

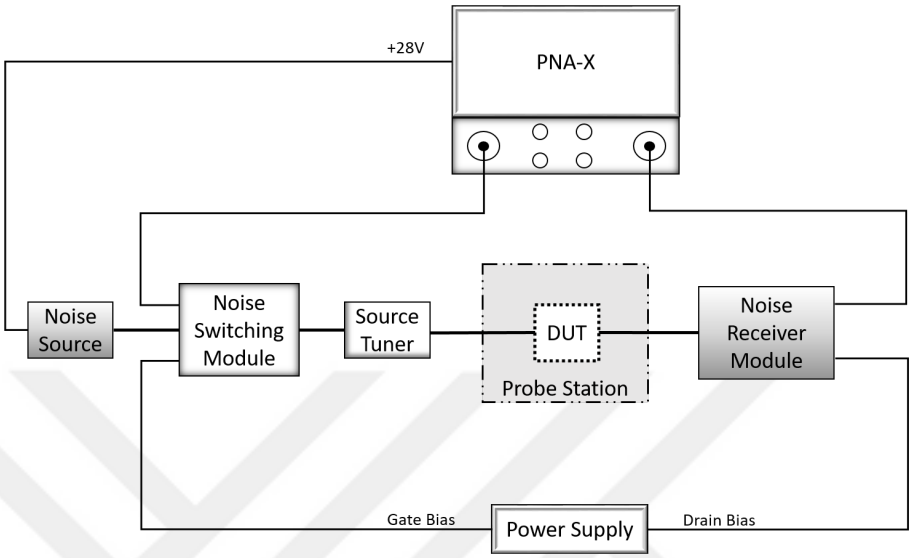

Figure 2.19: Block diagram of N-parameters measurement system.

bandwidth, T_{NS} is the noise temperature of the source, T_o is the reference temperature of 290 K, F_{DUT} is DUT's NF, $G_{A,DUT}$ is DUT's available gain, F_{MS} is the NF of the measurement system, and $G_{T,MS}$ is the transducer gain of measurement system.

$$NP = kB\{[T_{NS} + T_o(F_{DUT} - 1)] + G_{A,DUT} + T_o(F_{MS} - 1)\}G_{T,MS} \tag{2.15}$$

The measurement system first measures S-parameters of the DUT with respect to 50 Ω and then N-parameters. N-parameters (NF_{min}, magnitude, and phase of Γ_{opt}, and R_n) are measured for twenty-two source impedances at each frequency point.

Chapter 3

Design and Robustness Improvement of High-Performance LNA using 0.15 µm GaN technology for *X*-Band Applications

The contents of this chapter reflect the work reported in the following publication:

S. Zafar, B. Cankaya Akoglu, E. Aras *et al.*, "Design and robustness improvement of high-performance LNA using 0.15 µm GaN technology for X-band applications." *Int J Circ Theor Appl.*, 2022; 50(7): 2305- 2319.

3.1 Introduction

There have been recent reports for designing and fabricating GaAs-based LNAs [66–68], switches [69, 70], and multiphase clock generators [71] using 0.15 µm and

0.25 µm technology. LNAs based on other competitive technologies, CMOS [72–76] and SiGe BiCMOS [77, 78], have also recently been reported in the literature. CMOS technology has the advantage of high integration density, and low cost [24], whereas SiGe [25] and GaAs [26] have better noise performance. On the other hand, GaN's built-in power handling capability at the receive end without complex protection circuitry leads to robust GaN-based LNA designs. Although the initial focus of GaN technology was aiming toward high power performance, using the same technology for both transmit and receive chains was desirable for efficient and compact transceiver modules [27–29].

Small-signal gain, NF, reflection coefficients, output power at 1-dB gain compression (P_{1dB}), saturated power (P_{sat}), and output third-order intercept point (OIP3) are important parameters to consider for LNA's performance, and there are many recently reported designs targeting these parameters. The robustness of LNA is a critical factor in high-power applications, which is the central theme of GaN technology. Two important FoMs defining robustness are survivability and RRT. LNA in the receiver chain of radars is subject to high input drive levels due to transmitter leakage, close-range target reflections, and jamming signals. Transmitter leakage depends upon circulator isolation and is a strong function of transmitted power, while close-range reflection depends on the target radar cross-section (RCS). LNA should survive such high input drive levels and have a short recovery time. This means it should operate normally immediately after these signals are removed; otherwise, the system may miss useful return signals other than its blind range. For radar applications, the typical RRT requirement is in nanoseconds (200 – 300 ns) [79], while for some systems, it may go up to 1.5 µs [36]. Although robustness in terms of survivability has been addressed in the literature, few reports cover the RRT analysis and critical aspects related to it.

Oguz Kazan *et al.* [41] have presented an *X*-band GaN LNA with 34 dBm input survivability, and the same LNA is used to develop an *X*-band transceiver MMIC [80]. Çağdaş Yağbasan and Ahmet Aktuğ proposed two LNA designs in *X*-band, and the one with a passive limiter survived 37 dBm input power (P_{in}) [46]. Kim *et al.* [81] demonstrated robust current-shared LNA surviving 37 dBm RF

input stress level. A highly survivable (41 dBm P_{in}) X-band MMIC LNA has been demonstrated by Colangeli *et al.* [27] as suitable for synthetic aperture radar systems. The presented X-band LNA (XLNA) in this work survives P_{in} as high as 42 dBm.

Rudolph *et al.* [82] presented the idea of using a gate bias path resistor (R_{GB}) to enhance survivability. They claim that R_{GB} is required for the first stage only, while some designs [43, 49, 50, 83] have used it for all the stages in a multi-stage LNA. In this study, power measurements of two single-stage LNAs are performed to analyze the requirement of R_{GB} for subsequent stages in the context of forward gate turn-on. This analysis, significant in terms of MMIC LNA circuit design, has been performed for the first time to the best of our knowledge.

Previously [46], RRT is reported as 40 ms and 10 ms for gain compression levels of 33 dB and 3 dB, respectively. Liero *et al.* [36] reported the recovery time for LNA as low as 30 ns with a gain compression of around 8 dB. As explained by Meneghini *et al.* [84], buffer traps are introduced in Fe-doped AlGaN/GaN HEMTs, and their effect on the recovery time is explored by Olle Axelsson *et al.* [52]. They have shown an improvement in RRT in the order of 3 for LNA with undoped GaN buffer compared to LNAs with Fe-doped buffer. The proposed LNA in this work exhibits an RRT value of 20 ms for 34 dB gain compression and less than 27 ns for gain compression less than 12 dB.

When LNA is exposed to large input power, various key parameters determining the survivability and RRT are gain compression, forward gate current (I_{GF}), the RC time constant, and traps excitation. In this work, the survivability of the proposed XLNA is explored in terms of gain compression and I_{GF}. Moreover, the effect and dominance of either RC time constant or traps excitation for RRT is addressed in detail for the first time. Stage-wise analysis using two single-stage LNAs has also been performed to analyze the requirement of gate bias resistor for robustness. Two terminologies, "1-dB less recovery (1DLR)" and "2-dB less recovery" (2DLR), have been introduced in the context of RRT measurements.

The fabrication process is discussed in Chapter 2. LNA design, HEMT selection, and related techniques for matching and stability networks are in Section 3.2. Section 3.3 encompasses the results and measurements focusing on survivability, the requirement of R_{GB} in various stages, recovery time for different input stress levels, and the comparison with recently published data. The chapter is summarized in Section 3.4.

3.2 Proposed LNA Design

3.2.1 Choice of HEMTs

The choice of HEMTs for the stages is essential to meet the requirements for NF, gain, P_{1dB}, reflection coefficients, and survivability. 4x50 µm ISD HEMT is chosen for the first stage and 4x75 µm CS HEMT for the second stage, as shown in Fig. 3.1. Fig. 3.2 shows these transistors' small-signal and NF characterization, while load-pull contours are shown in Fig. 3.3.

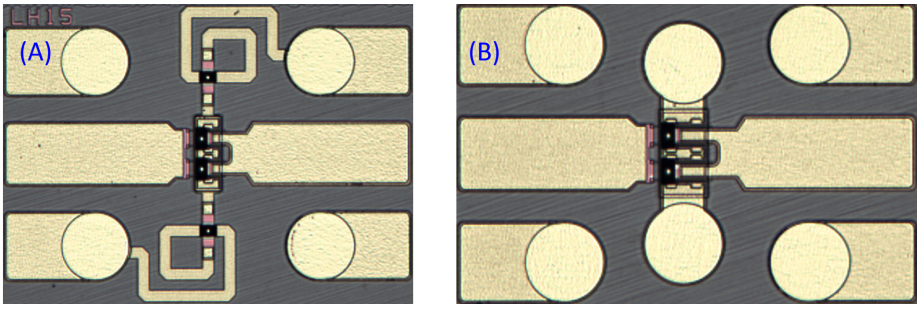

Figure 3.1: Microphotograph of (A) 4x50 µm ISD HEMT, (B) 4x75 µm CS HEMT.

Small-signal and noise characterization for HEMTs and MMICs are performed using ZVA40 from Rohde & Schwarz[1], PNA-X from Keysight Technologies[2], and RF and DC probes from GGB industries[3]. FormFactor's[4] probe station, Maury's

[1]Rohde & Schwarz GmbH & Co. KG., 81671 München, Germany
[2]Keysight Technologies, Inc., Santa Rosa, CA 95403, USA
[3]GGB Industries Inc., Naples, FL 34104, USA
[4]FormFactor Inc., Livermore, CA 94551, USA

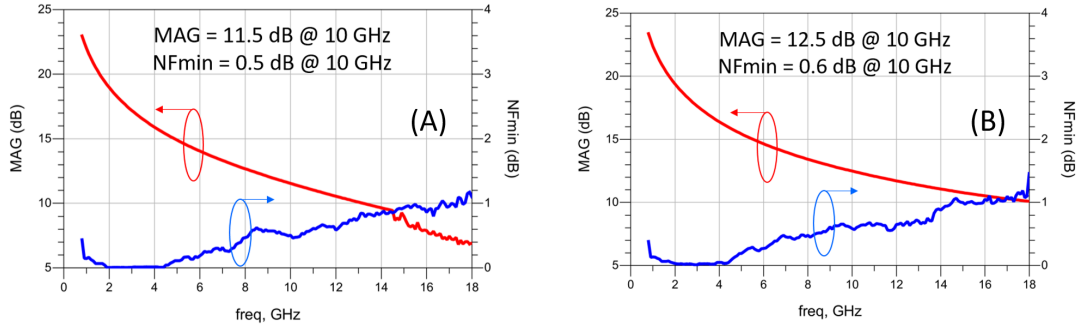

Figure 3.2: MAG and NF_{min} of (A) 4x50 µm ISD, (B) 4x75 µm CS HEMTs for 12 V, 100 mA/mm.

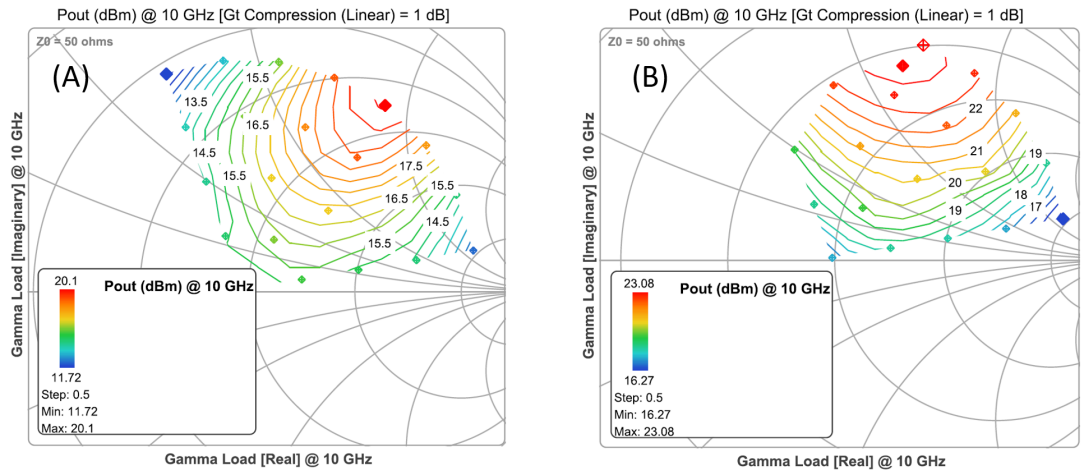

Figure 3.3: Load-pull contours for (A) 4x50 µm ISD, (B) 4x75 µm CS HEMTs at 10 GHz for 12 V, 100 mA/mm.

tuners[5], and Amcad Engineering's[6] IVCAD software are additionally used for large-signal characterization.

Major noise contribution in two-stage design is from the first stage, while the second stage adds very little to overall NF, as evident from the Friis formula

$$F = F_1 + \frac{F_2 - 1}{G_1}, \tag{3.1}$$

where F is the NF of the overall system, while F_1 and F_2 are NFs of the first and second stages, respectively, and G_1 is the gain of the first stage.

[5]Maury Microwave Technologies, Ontario, CA 91764, USA
[6]AMCAD Engineering, Limoges 87068, France

Stability networks containing resistive elements lead to an increase in the NF. HEMT with source degeneration is easy to stabilize because of the cancellation of the imaginary part of the impedance due to an inductor at the source and HEMT's input capacitance (C_{in}), thus moving the impedance closer to the resistive part of the Smith chart. After stabilization, it ensures a small increase in NF_{min}. This is the main reason for choosing ISD HEMT for the first stage, although this HEMT has a low MAG and is less survivable. A larger periphery HEMT at the second stage compensates for the required gain along with a high P_{out}. The survivability of a small-size ISD transistor at the first stage is enhanced by using a gate bias path resistor, R_{GB}, and will be discussed in detail in Section 3.3.2. Calculating the noise, gain, and power budget from the graphs in Fig. 3.2 and 3.3, the target was to achieve an NF less than 2 dB, a gain greater than 18 dB, and P_{1dB} more than 20 dBm.

3.2.2 MMIC Design

The schematic diagram and photograph of the proposed X-band LNA are shown in Fig. 3.4 and 3.5, respectively. The stability network for the first stage is designed at the output to minimize the effect of the resistive contribution at the input side to keep the NF_{min} value small. This stability network is designed to make the optimum noise reflection coefficient Γ_{opt} conjugate of input reflection coefficient Γ_{in} so that a simultaneous match may be achieved for better noise and gain performances. For the second stage, the stability network provides a simultaneous match between the output reflection coefficient Γ_{out} and the optimum load reflection coefficient for power Γ_L. This results in better power and gain performance at the same time. Input and output matching networks are designed for the 50 Ω noise and power match, respectively. Due to the conjugate match discussed hereinabove, the matchings for IRC and ORC are automatically achieved. The inter-stage matching network is designed for gain performance, and it also minimizes the gain ripple. Stability and matching networks also serve the purpose of the gate and drain bias for both stages to reduce the size.

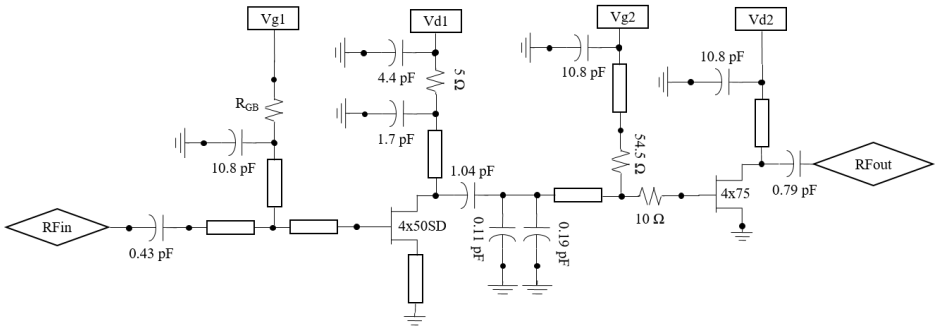

Figure 3.4: Schematic diagram of two-stage LNA.

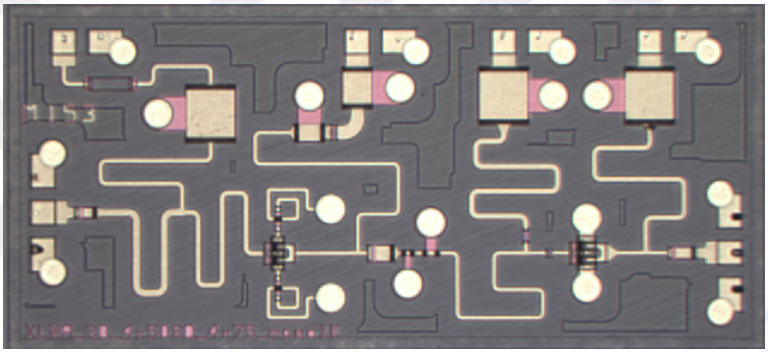

Figure 3.5: Microphotograph of two-stage LNA.

An important design aspect is to include a high-value resistance (R_{GB}) in the gate bias path. For multi-stage LNAs, an important design consideration is to incorporate this resistor only at the first or subsequent stages. R_{GB} is incorporated only for the first stage as a mesa-etched resistor in this work. The significance of this design aspect will be discussed in more detail in Section 3.3.2.

Fig. 3.6A shows electromagnetic (EM) simulation results for the small-signal and noise parameters of the proposed LNA, validating the choice of HEMTs and design approach. EM simulations are performed using PathWave Advanced Design System (ADS) from Keysight Technologies.

3.3 Results and Discussion

3.3.1 Small-signal, Noise, and Large-signal performance

The small-signal and noise performance of the fabricated LNA is shown in Fig. 3.6B. It provides a small-signal flat gain of more than 19 dB with a gain ripple of only 1 dB and NF of less than 2 dB. IRC and ORC are better than −9 dB and −10 dB, respectively. P_{1dB} of the proposed XLNA is greater than 19 dBm at 10 GHz for 12 V, 90 mA and increases with the increase in drain current, as shown in Fig. 3.7A. This P_{1dB} for in-band frequencies of 8 GHz, 10 GHz, and 11 GHz is shown in Fig. 3.7B. Fig. 3.8A shows P_{out} and gain versus P_{in} for a large input signal of 30 dBm. The value of P_{sat} is 27 dBm. OIP3 is an important FoM to indicate the linearity of the amplifier. Fig. 3.8B shows the values of OIP3 for in-band frequencies and is greater than 33 dBm at 11 GHz.

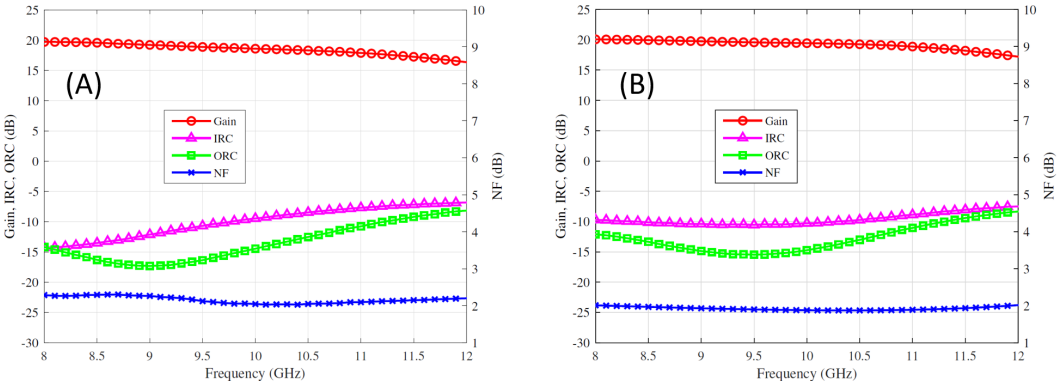

Figure 3.6: Small-signal and noise (A) EM simulation results, (B) Measurement results of fabricated MMIC.

3.3.2 Survivability

Survivability of the LNA is a crucial parameter, especially for radar applications, where the LNA in the receive chain is expected to handle high P_{in}. In this case, LNA should not undergo significant performance degradation after exposure to high power. A high P_{in} leads to a forward gate turn-on current, which may be

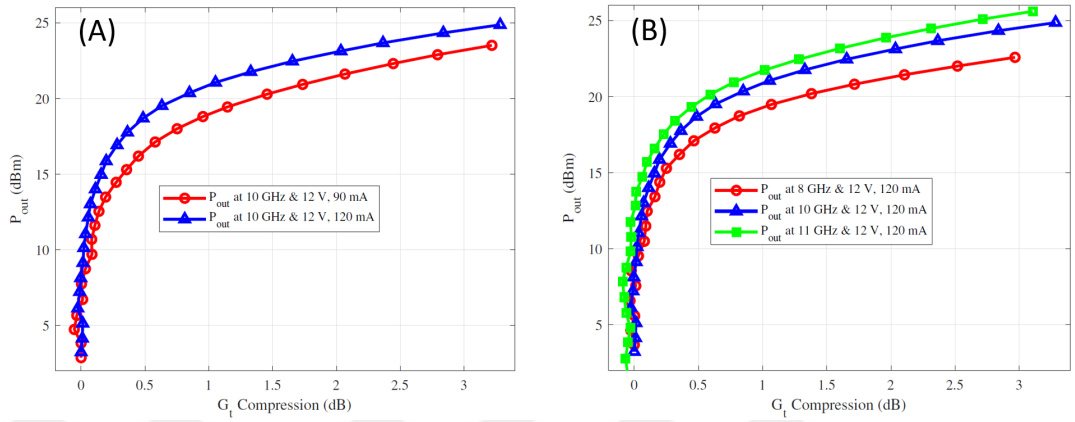

Figure 3.7: Measured P_{1dB} of fabricated MMIC at (A) 10 GHz for 12 V, 90 mA and 12 V, 120 mA, (B) 12 V, 120 mA for 8 GHz, 10 GHz, and 11 GHz.

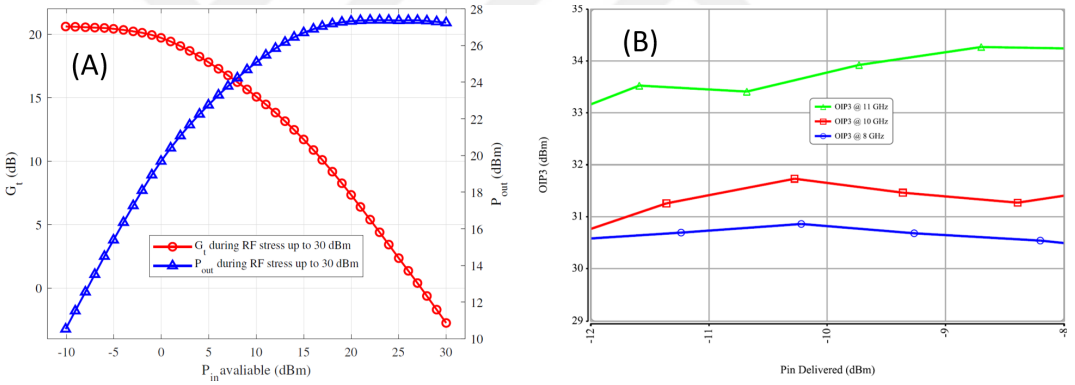

Figure 3.8: (A) Measured P_{out} and Gain vs. P_{in} for input stress level of 30 dBm, (B) Measured OIP3 for 8 GHz, 10 GHz, and 11 GHz.

limited by using passive and active limiters. Rudolph *et al.* demonstrated the idea of utilizing a gate bias path resistor, R_{GB}, reducing the gate current by feedback mechanism and, thus, enhancing the survivability [82]. In this study, the impact of the forward gate limitation is analyzed by subjecting the proposed LNA without and with R_{GB} (on-chip 1 kΩ and 5 kΩ).

Proposed LNA with R_{GB} = 1 kΩ is exposed to large P_{in} levels of 20 dBm, 24 dBm, 27 dBm, and 30 dBm in steps, and small-signal gain immediately after each step is measured to ensure the health of the device, as seen in Fig. 3.9. Fig. 3.10A shows the variation of gate current with increasing P_{in}. As soon as P_{in} is increased beyond 20 dBm, a large voltage swing turns the gate ON in the

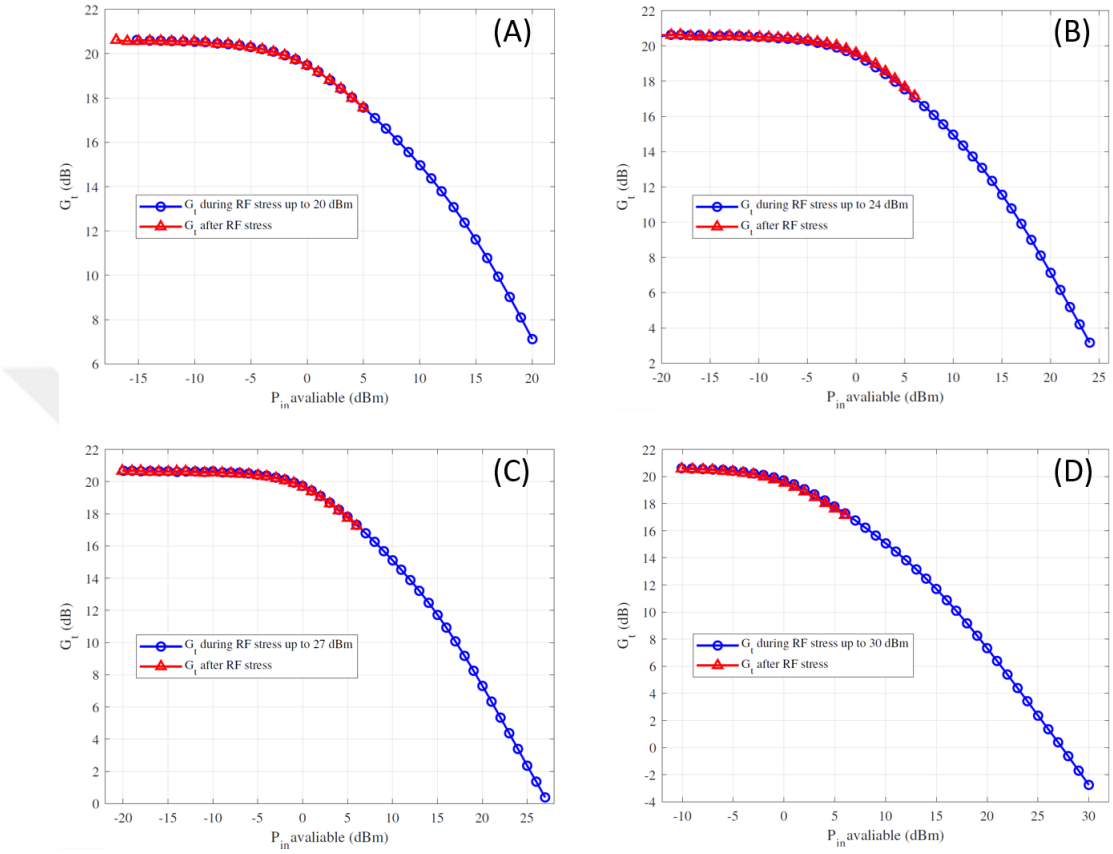

Figure 3.9: Gain before and after input stress levels of (A) 20 dBm, (B) 24 dBm, (C) 27 dBm, and (D) 30 dBm at 8 GHz.

forward direction. The forward gate turn-on is of significant importance in terms of survivability as well as RRT. R_{GB} serves the purpose of enhanced survivability by reducing I_{GF}. This effect is explained in more detail in Fig. 3.10B, where the same LNA is exposed to 25 dBm P_{in} without R_{GB}. The results show that the LNA without R_{GB} has I_{GF} of 3.3 mA for P_{in} = 25 dBm, while I_{GF} for the same power is 1 mA in the case of LNA with R_{GB} of 1 kΩ. I_{GF} is further reduced with R_{GB} of 5 kΩ. The slope of the curves in Fig. 3.10B indicates better power handling capability for LNA with R_{GB} by limiting I_{GF}. These survivability measurements correspond to 30 µs pulse width and 100 µs pulse period for RF at 8 GHz.

Fig. 3.11 shows the small-signal gain and NF results measured before and after exposing LNA to 42 dBm P_{in} with R_{GB} = 5 kΩ. Presented LNA survives up to 42 dBm P_{in} without any significant performance degradation. The NF

increases to a maximum of 2.1 dB while the gain is reduced by 0.3 dB only. The survivability limit may further be enhanced with an even higher value on-chip R_{GB}. The limiting factor for higher R_{GB} values is the level of negative voltage peak, which HEMT may withstand before the breakdown. Moreover, the gate leakage current variation results in the shift of gate bias voltage due to higher R_{GB}, which is not desirable.

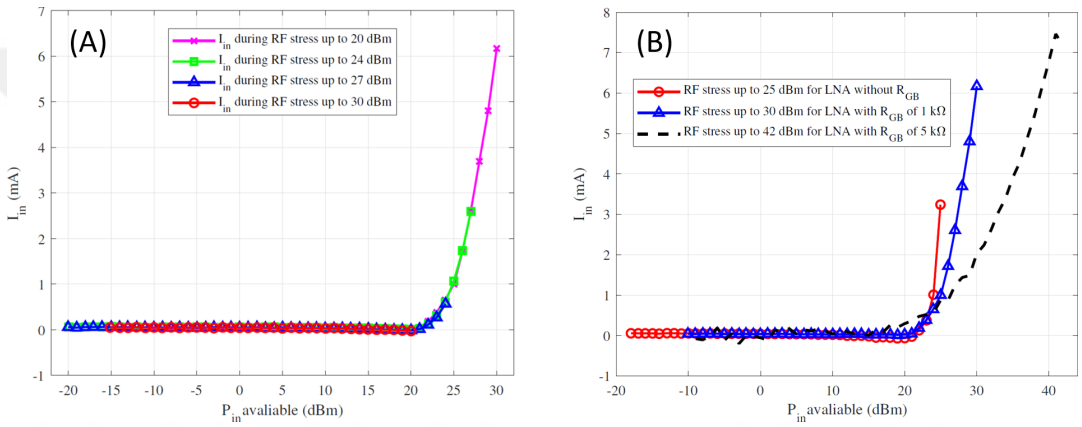

Figure 3.10: Variation in I_{GF} with increasing input stress for LNA (A) with R_{GB} = 1 kΩ, (B) with and without R_{GB}.

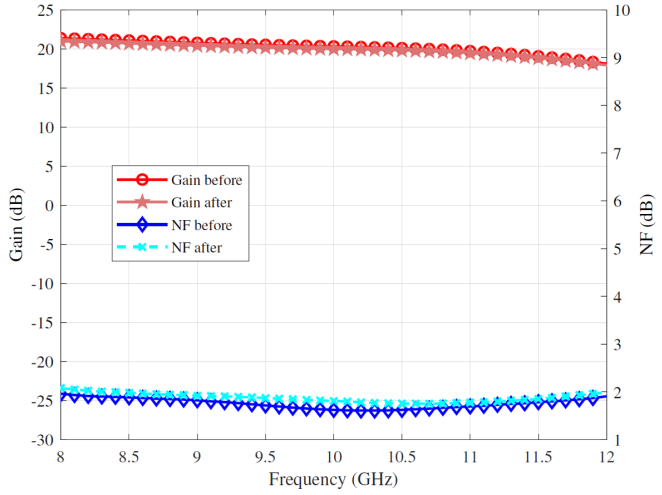

Figure 3.11: Small-signal gain and NF before and after RF stress of 42 dBm.

For multi-stage design, R_{GB} has been used for all the stages for some designs [43, 49, 50, 83], while others [82] claim that R_{GB} in the first stage is enough as only the first stage is subjected to stress. The requirement and choice of this DC gate feed resistor for the subsequent stages are addressed in this study, and it is

the first time to the best of our knowledge. For this purpose, single-stage LNA versions of 4x50 µm ISD and 4x75 µm ISD HEMTs (named LNA1SS and LNA2SS, respectively) without R_{GB} are designed, and measurements are performed by exposing to high P_{in}. The contribution of each stage toward gain compression and I_{GF} is investigated based on large-signal results from LNA1SS and LNA2SS. This study is valuable in addressing the necessity of R_{GB} at the second stage gate bias path. The value of P_{out} from the first stage is estimated to be around 24 dBm from Fig. 3.12A, where LNA1SS is exposed to a large signal of P_{in} = 25 dBm. The loss from inter-stage matching and second-stage stability network is 2.8 dB at 8 GHz, which implies that, for more than 22 dBm P_{in} at the input of XLNA, the second stage is exposed to 21.2 dBm. This power at the input of the second stage corresponds to approximately 6 dB compression with negligible I_{GF}, as evident from Fig. 3.12A and 3.12B. It shows that there was no need for R_{GB} at the second stage for the proposed XLNA. It is pertinent to mention that if the P_{out} of the first stage is large enough to drive the second stage into considerable gain compression and forward gate turn-on, the designer may consider including R_{GB} at the gate bias path of the second stage. A similar argument may be extended to designs with more than two stages.

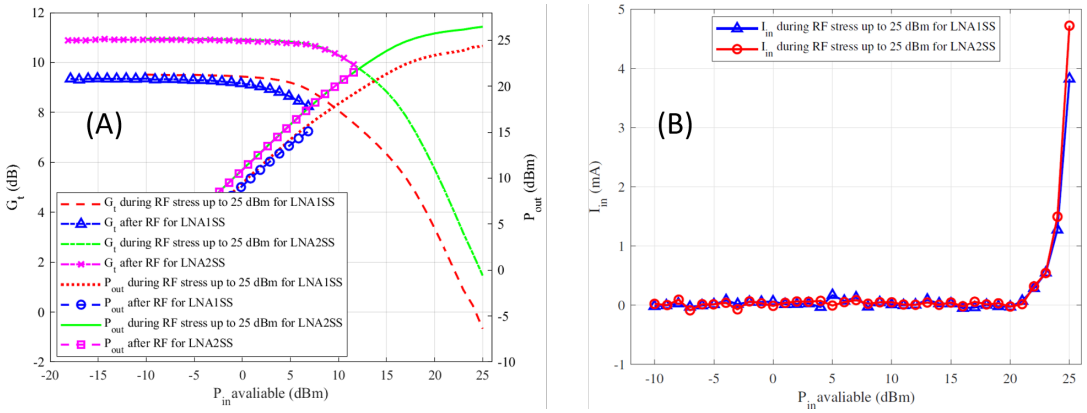

Figure 3.12: (A) Gain compression and P_{out} for LNA1SS and LNA2SS, (B) I_{GF} for LNA1SS and LNA2SS.

Proposed LNA with R_{GB} = 1 kΩ survives up to 30 dBm P_{in} with 4x50 µm ISD HEMT at the first stage. There are reported works with enhanced survivability, and they have used either a high-value R_{GB} (10 kΩ [27] and 8.2 kΩ [85]) or larger periphery HEMT (12 x 125 µm) [36] at the first stage. In the second run, the

proposed LNA is fabricated using on-chip $R_{GB} = 5$ kΩ at the first stage, thereby enhancing the survivability up to 42 dBm P_{in}. It is experimentally shown that, although second stage R_{GB} was not required for the proposed design, there may be a requirement for this resistor in other designs depending on the P_{out} from the first stage, which may drive the second stage into the compression and lead to forward gate turn-on.

3.3.3 Reverse Recovery Time

Reverse recovery time for an LNA is a crucial FoM to be considered for radar applications. It is time for the gate bias to return to its original value after lifting the high input stress. Neglecting the trap phenomenon, the RC time constant determines the time required to discharge input capacitances. RC time constant depends on series and parallel capacitances along the input signal line. The traps are activated as soon as the input stress level increases beyond a certain point and contribute toward RRT. In this study, these two cases are explored in detail, along with their significance in terms of dominance, for the first time to the best of our knowledge.

Fig. 3.13 shows the block diagram of the test setup used for the RRT measurements. In order to accurately measure RRT in general and in nanoseconds, particularly, a customized setup is implemented. Some of the critical factors considered for this setup to measure RRT as short as in tens of nanoseconds are the dynamic range of the signal generator (SG), bandwidth (BW) and the sampling rate of the oscilloscope, detector's dynamic range, and the capability of circulators to isolate reverse power at the input of SGs. In this setup, E8257D pulsed SG and DSOS204A oscilloscope from Keysight Technologies is used.

Fig. 3.14A and 3.14B show the RRT measurements for the proposed XLNA with $R_{GB} = 1$ kΩ. The signal level at 8 GHz is -11 dBm at the input of the DUT (small-signal region of LNA without any stress). A pulsed signal of 200 µs width and 90 ms duration is generated as the second tone, and its level at the input of the DUT is varied in the large-signal region. The fundamental signal at

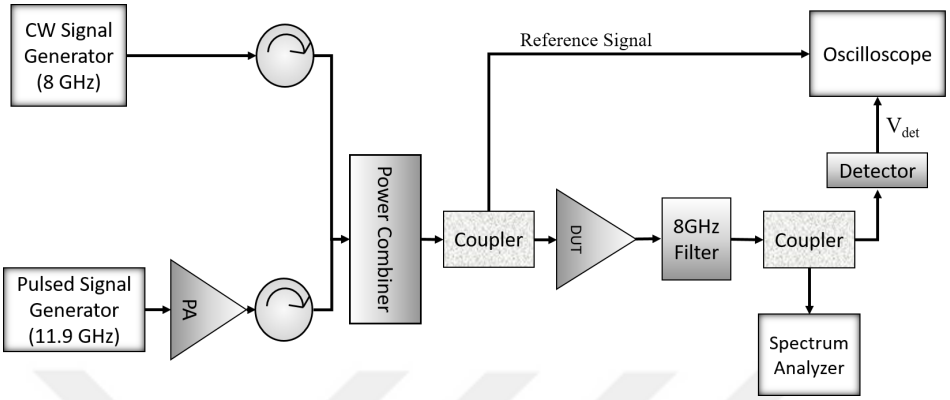

Figure 3.13: Reverse recovery time measurement setup.

8 GHz results in gain compression for 200 µs and is given a relaxation time of 90 ms, during which the recovery phenomenon happens. The LNA takes 20 ms to recover after being stressed by a high input pulse of 30 dBm with 200 µs width and 90 ms duration, as evident from Fig. 3.14A.

In the same context, another terminology, "1-dB less recovery" (1DLR), is introduced; defined as the time the LNA takes to recover its gain to 1 dB less than the level before the stress is applied. Depending on the application and output power requirements, 1DLR may be another critical FoM in terms of recovery. Defining RRT as 1DLR, its value reduces by hundreds of µs. In the proposed design, RRT for 1DLR is 20 µs for 30 dBm P_{in}, as shown in Fig. 3.14B, i.e., 1,000 times faster compared to full gain recovery. This definition may be extended to "2-dB less recovery" (2DLR) and further until a point where maximum power is recovered after stress, and it solely depends on the application and designer's choice. It also benefits using GaN LNAs for radar applications, where RRT is expected to be in the nanoseconds [79] or microseconds [36] range.

Fig. 3.15 shows the equivalent circuit model for the RC time delay of the proposed LNA, where R_{GB} is 1 kΩ, the DC block capacitor is 0.4 pF, the bypass capacitor is 10 pF, and C_{in} is 0.3 pF. I_1 is the forward gate current under high-stress levels, and V_1 is the external gate bias. Mathematical calculations for 10% to 90% result in an RC time constant of 23.5 ns. This RC time constant contribution toward RRT remains the same for all P_{in} levels, and the increase in

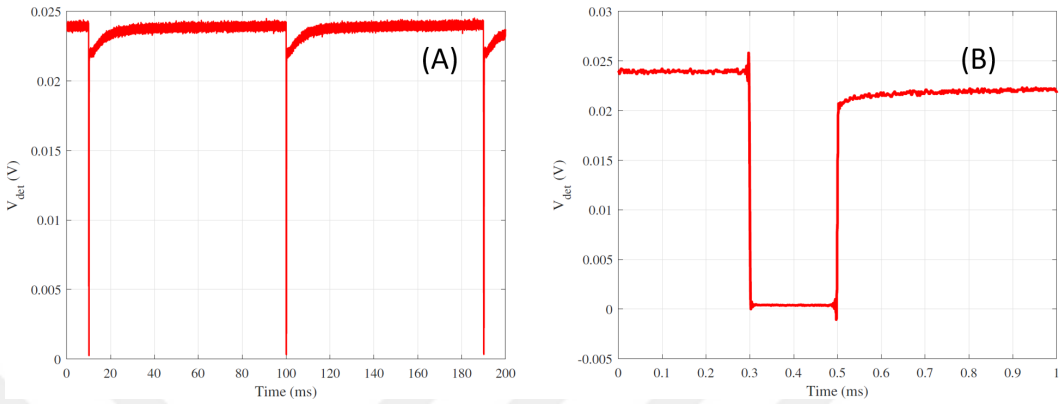

Figure 3.14: (A) Recovery time measurement results, (B) 1DLR for XLNA with 200 µs width and 90 ms duration.

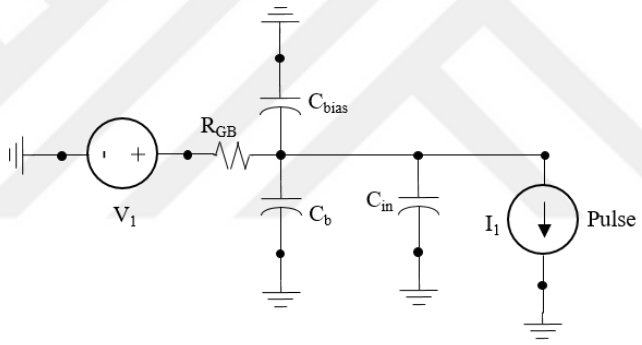

Figure 3.15: Equivalent circuit model to simulate RC time constant under input stress.

RRT beyond this time is due to the trap phenomenon.

Table 3.1 shows RRT and gain compression levels for corresponding pulsed P_{in} signals of 200 µs width and 90 ms duration. The LNA exhibits an RRT value in nanoseconds for P_{in} of 18 dBm; it is evident that the trap phenomenon starts to dominate for the P_{in} around 16 dBm (RRT > 23.5 ns). Changing the input level from 18 to 20 dBm, RRT elevates from 236 ns to 147 µs and further increases to 1 ms and 20 ms for P_{in} values of 25 dBm and 30 dBm, respectively. As discussed above, in terms of 1DLR or 2DLR, the recovery is much faster for the same input power. Notably, the gate turn-on occurs around 20 dBm P_{in} when there is a jump in RRT from the nanosecond regime to microseconds.

There are rather few reported works for RRT measurements. Çağdaş Yağbasan

Table 3.1: Gain compression and RRT for various P_{in} levels.

P_{in} (dBm)	Gain comp. (dB)	RRT (100%) (s)
30	34	20 m
25	25	1 m
20	18	147 µ
19	16	41 µ
18	14.5	236 n
17	13	52 n
16	12	27 n
15	10	7 n

and Ahmet Aktuğ [46] have reported RRT of 40 ms and 10 ms with gain compression of 33 dB and 3 dB, respectively, for the corresponding P_{in} being 36 dBm and 21 dBm. RRT of 30 ns for gain compression levels of around 8 dB is reported by Liero *et al.* [36]. The proposed LNA shows the RRT value of 20 ms and 27 ns with 34 dB and 12 dB gain compression, respectively. The corresponding P_{in} levels are shown in Table 3.1. It is worth mentioning that RRT depends on the LNA design (gate bias resistor and capacitor), HEMT characteristics (input capacitance), as well as device fabrication (traps). RRT from the gate bias resistor, gate bias capacitor, and the input capacitance of GaN-HEMT is always in the nanoseconds regime (23.5 ns in this case). Therefore, it is justifiable to conclude that the main contribution to RRT comes from the trap phenomenon in the proposed design and the earlier reported works mentioned above.

3.3.4 Comparison

Table 3.2 shows the comparative analysis of the proposed X-band LNA design with already published work. Survivability of 42 dBm is the highest reported for X-band LNAs with similar HEMT periphery and topology. The proposed LNA has the best combination of NF, gain, return losses, and OIP3 with respect to bandwidth and size. High OIP3 values for the whole band are an indication of good linearity. There have been a few X-band GaN-based LNAs using 0.15 µm L_g, and the presented work is one of these. This work shows promising results

for small-signal and large-signal performance compared with both 0.15 µm and 0.25 µm GaN technology nodes.

Table 3.2: A comparison of the designed MMIC with the recent works at the X-band.

Ref.	Freq. (GHz)	Gain (dB)	IRC (dB)	ORC (dB)	NF (dB)	OIP3 (dBm)	Surv. (dBm)	L_g (µm)
[27]	8.4–10.6	> 25	$< -10^{**}$	$< -12^{**}$	< 2.3	—	41	0.25
[32]	4–16	> 11	< -10	< -8	< 2.0	24	37.3	0.15
[80]	8–11	> 22	< -9	< -5	< 2.0	24–29	34	0.25
[81]	8–11	> 25	$< -8^{**}$	$< -10^{**}$	< 2.2	26	37	0.25
[85]	8–11**	> 16	—	—	< 2.3	—	41	0.25
[86]	8–11	> 17	$< -10^{**}$	$< -8.5^{**}$	< 2.5	—	39.5	—
[87]	7–12	> 14	$< -5^{**}$	$< -5^{**}$	< 2.5	28	—	0.25
[88]	9.7–12.9	> 20	$< -2^{**}$	$< -7^{**}$	< 2.1	32	—	0.25
[89]	8–11	> 16.8	< -8.8	< -10	< 1.7	—	—	0.15
[90]	9–11	> 13.5	< -11	< -5	< 2.2	29.5–34.5	—	0.15
This work	8–11	> 19	< -9	< -11	< 2.0	30.5–34.2	42	0.15

Surv. = Survivability, *Simulation based, **Estimated values from the figures

3.4 Summary

High-performance and robust X-band LNA has been realized using NANOTAM's 0.15 µm AlGaN/GaN fabrication technology. The proposed LNA has the best combination of NF, gain, return losses, and survivability with respect to bandwidth and size. LNA survives up to 42 dBm RF input stress, the best reported for X-band LNAs with similar HEMT periphery and topology. Survivability analysis in the context of gain compression and I_{GF} has been performed. The DC gate feed resistor requirement in the gate bias path to enhance survivability and its need for subsequent stages are addressed. By the stage-wise calculation of gain compression and forward gate current, the circumstances have experimentally been shown when the second stage R_{GB} needs to be used. The contribution and dominance of the RC time constant and trap phenomenon in RRT are critically analyzed. The recovery time due to the RC time constant is in the nanoseconds range, and the traps, excited after a particular P_{in}, become a major contributor to RRT. 1DLR and 2DLR (new terminologies introduced here in the context of RRT) make the choice of GaN-based LNAs more flexible for radar applications.

The proposed LNA provides a sub-2 dB NF, OIP3 up to 34.2 dBm, RRT in nanoseconds for 14.5 dB gain compression, and survivability as high as 42 dBm.

Chapter 4

Design of GaN-based *X*-Band LNAs to Achieve Sub-1.2 dB Noise Figure

The contents of this chapter reflect the work reported in the following publication:

S. Zafar, E. Aras, B. Cankaya Akoglu *et al.*, "Design of GaN-based X-band LNAs to achieve sub-1.2 dB noise figure." *Int J RF Microw Comput Aided Eng.* 2022; 32(11):e23379.

4.1 Introduction

GaAs technology takes an edge over GaN technology regarding noise performance [26,47,91–93]. There are recently reported works [25,73,77,78] with promising NF for other competitive technologies, i.e., SiGe BiCMOS and CMOS. A comparative noise investigation from DC – 60 GHz, using 70 nm GaAs and 60 nm GaN on Si processes, has shown superior noise performance of the GaAs process for most of the frequency range [94].

Various approaches have been adopted to improve the noise characteristics for LNA design at the transistor and circuit levels. Vignesh *et al.* [73] have proposed quasi-circulator LNA with the current reused technique to achieve optimized NF of less than 1.4 dB in the X-band using 0.065 µm CMOS technology. Colangeli *et al.* [95] proposed a three-stage LNA using 0.25 µm GaN on SiC technology by exploiting the same current-reuse architecture. The impedance between the base-collector terminals of common-emitter HBT is considered by Çalışkan *et al.* [77] to achieve sub-1 dB NF. Davulcu *et al.* [78] presented the first triple inductively degenerated cascode SiGe HBT in X-band. Kumar and Rebeiz [25] have proposed X- and K-band LNAs with a method of noise match optimization with respect to the base inductor in a 0.18 µm SiGe HBT technology. Cao *et al.* [72] have proposed a pole converging technique to improve the NF over a broad range from 8 to 12 GHz using 0.13 µm CMOS technology. Zailer *et al.* [96] have demonstrated a method based on transistor size selection, i.e., Cgs and simultaneous bias, to minimize the difference between NF and $\mathrm{NF_{min}}$ using 0.13 µm CMOS ISD cascode LNA. Sabzi *et al.* [97] have used a parallel design technique using 0.1 µm GaAs pHEMT technology to improve linearity and NF. Along with enhancing gain and linearity, they have achieved a low NF by optimizing the base inductor and placing an additional inductor between the second and third stages. Dai [24] proposed a novel modified complementary current-reused LNA using a forward body bias technique based on 0.18 µm RFSOI CMOS technology. Noise performance is improved by minimizing the body leakage by employing a diode-connected MOSFET forward bias. Sabzi *et al.* [98] demonstrated the reduction in overall NF in multi-stage LNAs by optimization of the first stage, along with improvement in gain and input matching.

Improving the NF for GaN-based LNAs and making it close to GaAs has always been challenging. Various efforts have been made to improve and address the performance parameters of GaN-based LNAs, including linearity, robustness, recovery time, and NF [26]. Although sub-1.5 dB NF has been reported [47–51] for K- and Ka-bands, GaAs comparative NF at X-band for GaN technology remained a challenge. Recently [42], sub-1.5 dB NF has been reported in X-band using 0.09 µm GaN on SiC technology. Yağbasan and Aktuğ [46] reported 1.6 dB

Table 4.1: A comparison of LNA-1 with the recently reported competitive technologies at X-band.

Ref.	Freq. (GHz)	NF (dB)	IRC (dB)	ORC (dB)	Gain (dB)	L_g (µm)	Tech.
[25]	6.4–11	< 1.3**	< -6**	< -2**	> 21	0.18	SiGe
[77]	8–12	< 1	< -9	< -24	> 10	0.13	SiGe
[78]	8–12	< 1.6**	< -10**	< -10**	> 18	0.13	SiGe
[66]	8–12	< 2.5	< -10	< -10	> 30	0.25/0.45	GaAs
[67]	8–10	< 1.4	< -8	< -8	> 25	0.15	GaAs
[68]	8–12	< 1.8	< -15**	—	> 24	—	GaAs
[105]	10.7–13.1	< 1.7**	< -8**	< -8**	> 17**	0.15	GaAs
[72]	8–12	< 3.6	< -9**	< -16**	> 13	0.13	CMOS
[73]	8–12	< 1.4	< -10**	< -10**	> 25**	0.065	CMOS
[106]	7.4–11.4	< 3.8	< -12	< -8**	> 23.5	—	CMOS
This work LNA-1	8–11	< 1.2	< -10.3	< -10.1	> 16.8	0.15	GaN

*Simulation based, **Estimated values from the figures

NF using 0.25 µm GaN on SiC technology for 8 – 11 GHz.

Two 2-stage X-band LNAs with two different topologies based on 0.15 µm GaN on SiC technology have been designed in this work. LNA-1 comprises ISD HEMTs at both stages, while LNA-2 is designed using ISD HEMT for the first stage only. ISD topology is used in LNA design to achieve a simultaneous match condition for source and optimum noise reflection coefficients, ensuring minimum NF and maximum gain [99–104]. In this study, a measurement model of CS HEMT is used to determine the value of the source degenerated (SD) inductor by measuring the input capacitance *(C_{in})*. The effect of using ISD topology for both stages (LNA-1) and first stage only (LNA-2) on the overall NF has been analyzed in detail. It is shown that LNA-1 having ISD HEMTs at both stages demonstrates better NF than LNA-2 having ISD HEMT at the first stage while CS HEMT at the second stage. In this work, the role of the stabilization techniques in improving the performance parameters has been demonstrated for the first time. Resistive stability networks lead to maximum available gain (MAG) drop and NF_{min} increase. Stability networks are designed in such a way as to minimize this effect for in-band frequencies. Moreover, the S-probe utility of PathWave Advanced Design System (ADS) from Keysight Technologies is used to ensure the stability of the device after the complete design.

To the best of our knowledge, for LNA-1, NF less than 1.2 dB is the best reported for X-band GaN-based designs to date. Moreover, this NF value is better than most state-of-the-art X-band LNAs reported using GaAs, SiGe BiCMOS, and CMOS technologies, as compared in Table 4.1. This study is a valuable contribution towards the efforts where GaN LNAs NF becomes even better than GaAs LNAs in X-band.

Another novel aspect of this study is demonstrating the simultaneous matching of power and gain for ISD HEMTs to achieve a higher P_{1dB} and OIP3. In this context, power and gain load-pull contours have been shown in Section 4.2.1, while LNA's P_{1dB} and OIP3 results are discussed in Section 4.3.

4.2 LNA MMICs Design

4.2.1 HEMTs' Characterization and Selection

Two HEMTs have been characterized for the proposed LNAs design, both 4 x 75 µm periphery, one with CS and the other with ISD topology. The layouts of both HEMTs are shown in Fig. 4.1. From the small-signal measurements of the CS HEMT, C_{in} is measured as 0.3 pF in X-band. Therefore, an SD inductor of 0.75 nH is designed and modeled in ADS to resonate with C_{in}, moving the input impedance closer to the resistive part of the smith chart.

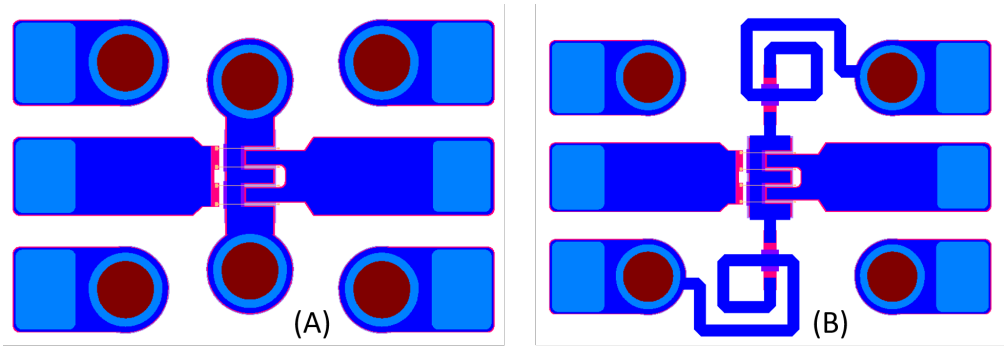

Figure 4.1: Layout of (A) 4x75 µm CS HEMT, (B) 4x75 µm ISD HEMT.

Fig. 4.2 shows the input reflection coefficient (Γ_{in}) and optimum noise reflection coefficient (Γ_{opt}), denoted by G_{in} and G_{opt}, respectively. An advantage of using ISD HEMTs for designing low noise amplifiers is that Γ_{in} becomes the conjugate of Γ_{opt}, as evident from Fig. 4.2. It allows the designer to match NF and IRC simultaneously. Another advantage of using ISD topology is the stabilization of HEMT with a minimum increase in NF, which is the main parameter of an LNA design. The stability in the high-frequency range is achieved with the help of a stability resistor at the output drain bias line, while the lower frequency band stabilization is done with the help of gate and drain bias line bypass capacitors. On the other hand, CS HEMTs are not easy to stabilize without introducing a resistive network at the input, which leads to increased NF. This is the main reason for choosing ISD HEMTs, particularly at the first stage in the presented designs. This design aspect will be discussed in further detail in Section 4.2.2.

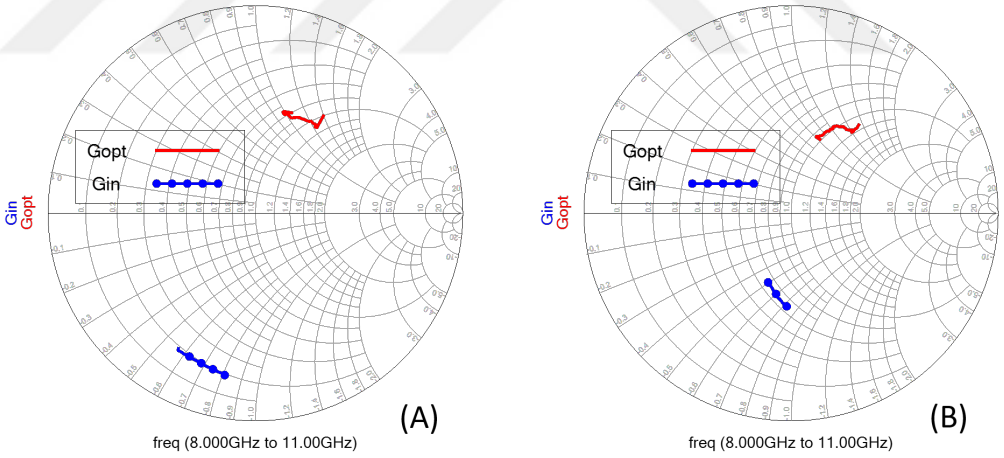

Figure 4.2: Γ_{opt} and Γ_{in} of (A) 4x75 µm CS HEMT, (B) 4x75 µm ISD HEMT.

Fig. 4.3 shows the MAG and NF_{min} curves for CS and ISD HEMTs. The gain for CS is more than ISD topology, while there is a slight variation in NF_{min}. Fig. 4.4 shows the large-signal characterization where the load circles and gain circles for maximum output are close to each other in the case of ISD HEMT. This gives another advantage of simultaneously matching the output for maximum gain and power performance. This way, an improved P_{1dB} value, and a better ORC are achieved. Higher P_{1dB} leads to better OIP3, leading to improved linearity of the LNA. Despite the lower gain, ISD HEMT is an obvious choice to achieve a

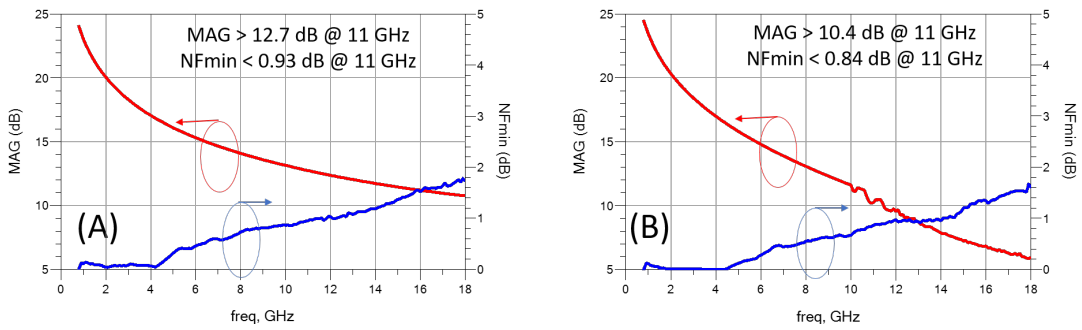

Figure 4.3: MAG and NF_{min} of (A) 4x75 µm CS HEMT, (B) 4x75 µm ISD HEMT for 12V, 200 mA/mm.

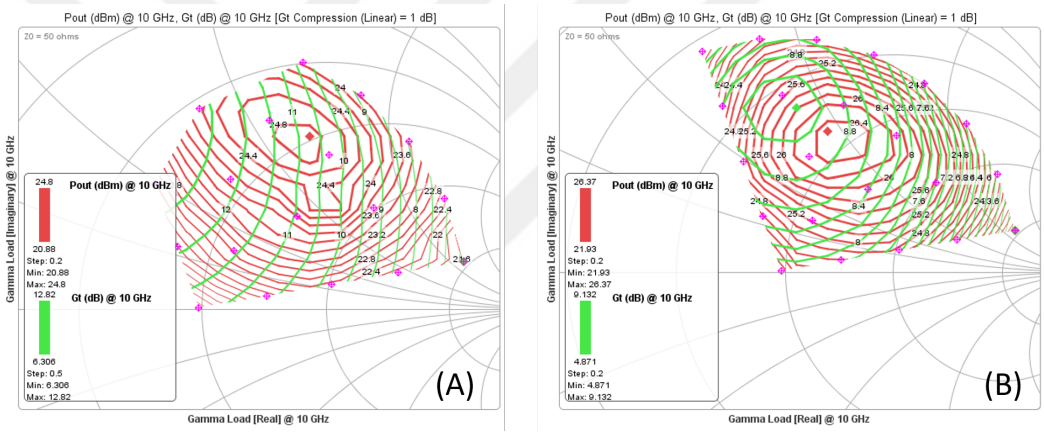

Figure 4.4: Load-pull contours for (A) 4x75 µm CS HEMT, (B) 4x75 µm ISD HEMTs at 10 GHz for 12V, 200 mA/mm.

low NF in an LNA design due to the abovementioned advantages. The reduction of NF in a multi-stage LNA design will be discussed in Section 4.2.2.

4.2.2 MMICs Design

Two 2-stage LNA MMICs are designed, namely LNA-1 and LNA-2. LNA-1 has 4x75 µm ISD HEMTs at both stages, while LNA-2 has the same HEMT at the first stage while 4x75 µm CS HEMT at the second stage. The contribution of each stage towards NF in both designs and its impact on overall NF is explored. Fig. 4.5A and 4.5B show schematic diagrams of the proposed LNA-1 and LNA-2, respectively.

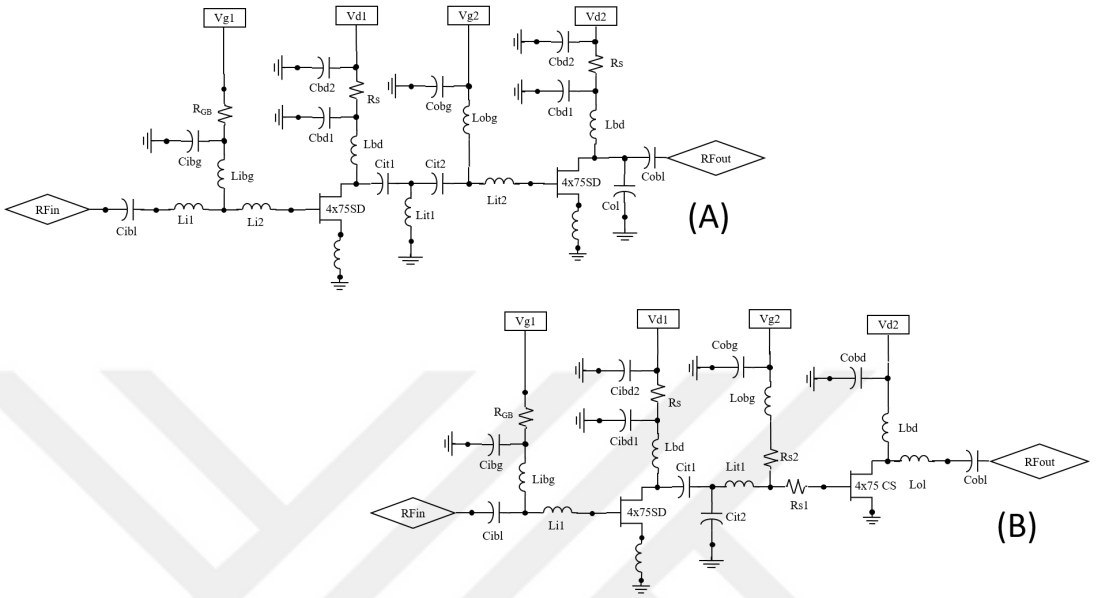

Figure 4.5: Schematic diagram of (A) LNA-1 having ISD HEMTs at both stages, (B) LNA-2 having ISD HEMT at the first stage and CS HEMT at the second stage.

4.2.2.1 HEMTs stabiltity, NF_{min}, and MAG

The stability of the HEMT is determined by three parameters, namely K-factor, μ, and $\mu^{'}$. The stability parameters of the ISD HEMT are shown in Fig. 4.6A. For the frequencies greater than 2 GHz, ISD HEMT at the first stage is stabilized using the network containing *Lbd*, *Rs*, *Cbd1*, and *Cbd2* (Fig. 4.5A) towards the drain side, as shown in Fig. 4.6B. Further stability for the lower frequencies is achieved using *Li2*, *Libg*, and *Cibg*. Fig. 4.6C shows that the condition for unconditional stability is fulfilled for lower frequencies. The increase in NF_{min} after stabilization is only 0.16 dB, while MAG is dropped by 0.8 dB only, as evident from Fig. 4.7. A similar procedure is adopted to stabilize the HEMT used for the second stage of LNA-1. R_{GB} is a high-value (1kΩ in this design) first-stage gate bias resistor used to enhance the survivability and does not affect the RF performance [82]. The significance of the R_{GB} in terms of survivability is discussed in Chapter 3.

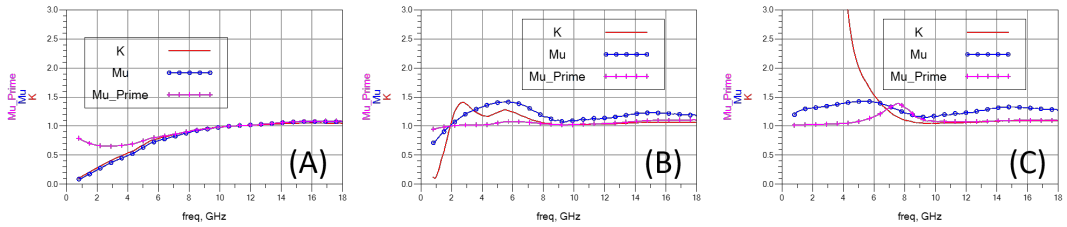

Figure 4.6: Stability parameters of the ISD HEMT (A) without any stabilization network, (B) with stability network at the drain side, (C) with overall input and output stability networks.

Fig. 4.8A shows the stability parameters of CS HEMT without any stabilization network. Referring to Fig. 4.5B, CS HEMT at the second stage is stabilized using a resistive network, *Rs1*, and *Rs2*, towards the gate side, along with bias capacitors and part of the matching networks containing *Logb*, *Cobg*, *Lbd*, *Cobd*, and *Lo1*. Fig. 4.8B shows the fulfillment of the condition for unconditional stability. NF_{min} is increased to 4.2 dB at 8 GHz, while MAG is dropped to 11.6 dB, as shown in Fig. 4.9. The increase in NF_{min} in the case of CS HEMT is more than ISD HEMT due to the resistive stability network towards the gate side. This is one of the reasons to use ISD HEMT at the first stage for both LNA-1 and LNA-2. Although the contribution in overall NF due to the second stage is less, as evident from Eq. 4.1, it still contributes around 0.3 dB to the overall NF for LNA-2.

$$F = F_1 + \frac{F_2 - 1}{G_1} \tag{4.1}$$

Here, F is the NF of the overall system, while F_1 and G_1 are NF and gain of the first stage, respectively, while F_2 is the NF of the second stage.

Fig. 4.6C and 4.8B show that the K-factor, μ, and μ' stability parameters are close to 1. In order to ensure that there are no even-mode oscillations after the completion of the whole design, another technique of the S-probe tool in ADS is used for both LNA-1 and LNA-2. This analysis is discussed in detail in Section 4.2.2.3.

A slight increase in NF_{min} after stabilization indicates a good choice of ISD HEMT for the first stage for both designs.

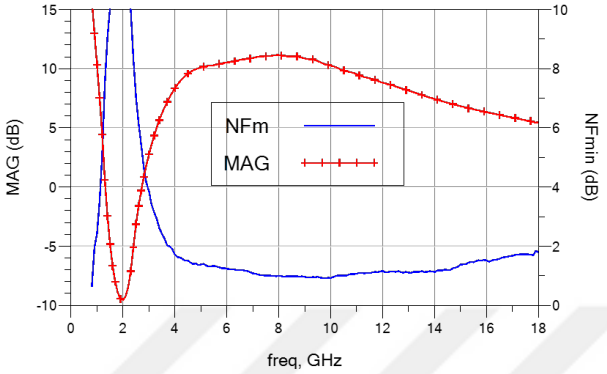

Figure 4.7: NF_{min} and MAG after stabilization of ISD HEMT.

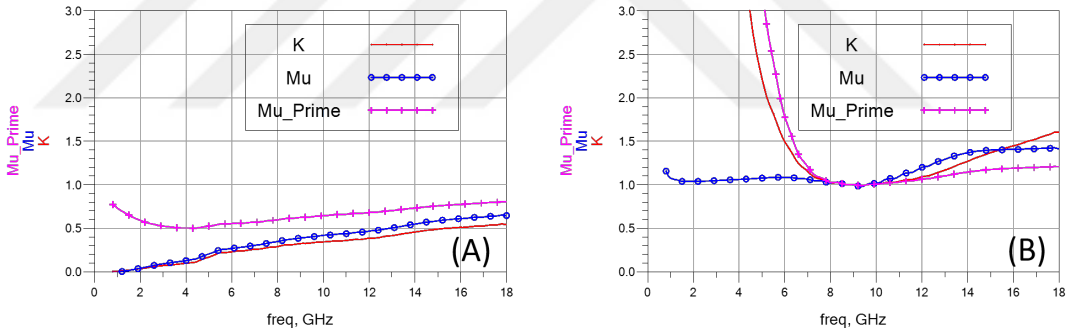

Figure 4.8: Stability parameters of the CS HEMT (A) without any stabilization network, (B) with overall input and output stability networks.

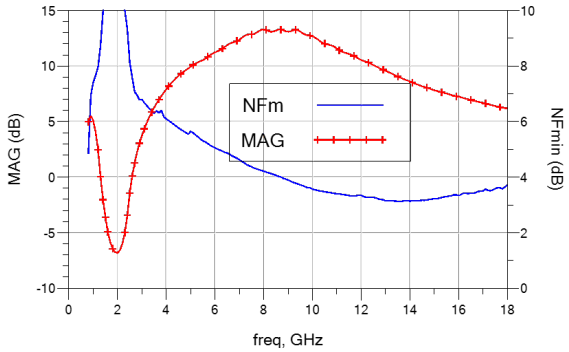

Figure 4.9: NF_{min} and MAG after stabilization of CS HEMT.

4.2.2.2 MMICs' simulation results

After achieving unconditional stability, matching networks are completed at the input, output, and inter-stage. The stability networks discussed in Section 4.2.2.1 are additionally serving the purpose of matching as well as gate and drain bias. This leads to a compact and efficient design. For LNA-1 and LNA-2, the components other than stability networks in Fig. 4.5 complete the input, output, and inter-stage matching networks.

Electromagnetic (EM) simulations are performed using ADS. Simulations for LNA-1 result in an overall IRC < -8.9 dB, ORC < -10.2 dB, NF < 1.4, and gain > 16.8 dB from 8 to 11 GHz, as evident from Fig. 4.10A. For LNA-2, as shown in Fig. 4.10B, simulated IRC < -11.4 dB, ORC < -12.6 dB, NF < 1.7, and gain > 17.7 dB are achieved in the desired frequency band. All the matching networks must be tuned and optimized simultaneously to achieve these results. The reason is that the matching networks affect each other due to smaller HEMT peripheries and thus having little reverse isolation.

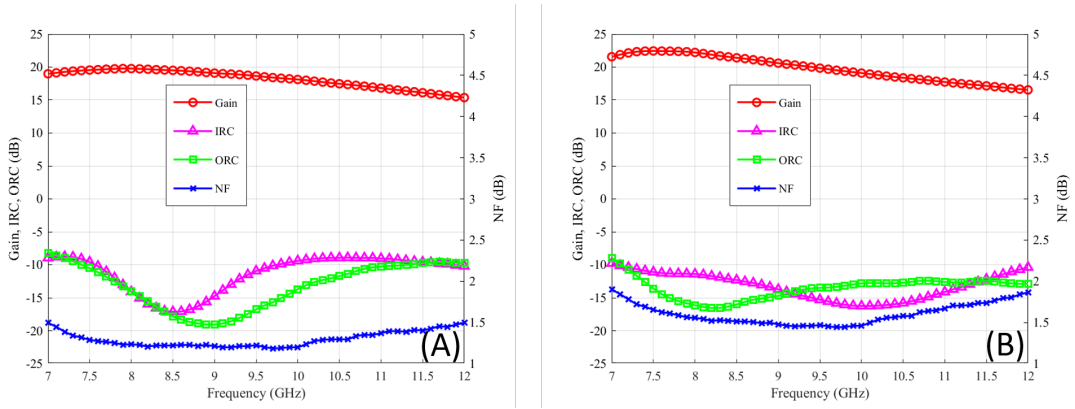

Figure 4.10: Small-signal simulated gain, IRC, ORC, and NF of (A) LNA-1, (B) LNA-2.

4.2.2.3 MMICs' stability consideration

The even-mode stability analysis of the complete layout of the MMIC is performed using the S-probe tool of ADS. Condition for any even-mode oscillation is checked

by calculating the impedances towards and away from the gate and drain side of the HEMTs at both stages, as shown in Fig. 4.11.

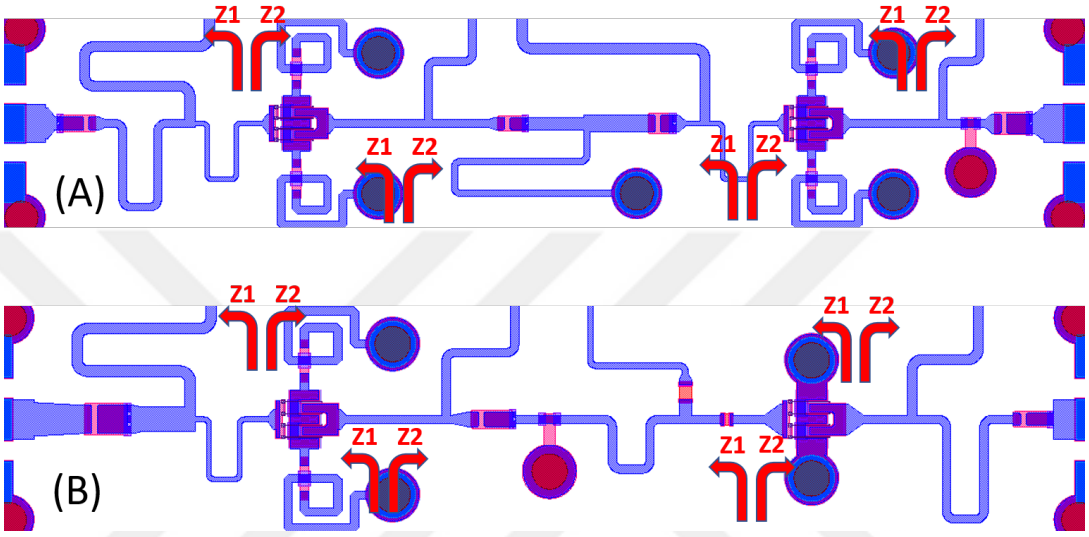

Figure 4.11: The impedances seen at the gate and drain side of the HEMTs using S-probe for (A) LNA-1, (B) LNA-2.

The condition for oscillations is defined by the following set of equations [107–109]:

$$z_1 = Re((Z_1 + Z_2), f) < 0 \tag{4.2}$$

$$z_2 = Im((Z_1 + Z_2), f) = 0 \tag{4.3}$$

$$\frac{\partial z_2}{\partial f} > 0. \tag{4.4}$$

Here, Z_1 and Z_2 are impedances seen towards and away from the gate and drain side of the HEMTs. In order for the oscillations to occur, the conditions in Eq. 4.2, 4.3, and 4.4 should simultaneously be satisfied at a particular frequency. For the oscillations to occur, if z_1 is negative at a particular frequency, there must be a zero-crossing for z_2 with a positive slope. Fig. 4.12 and 4.13 show that z_1 is always positive for all gates and drains of the designed LNAs. Hence, the condition for even-mode oscillation is not satisfied for any of the stages in LNA-1 and LNA-2, ensuring the stability of the devices. As discussed in Section 4.2.2.1, the stability parameters were kept close to 1 during the design process to have a minimum decrease in MAG and a minimum increase in NF_{min}. Therefore, the

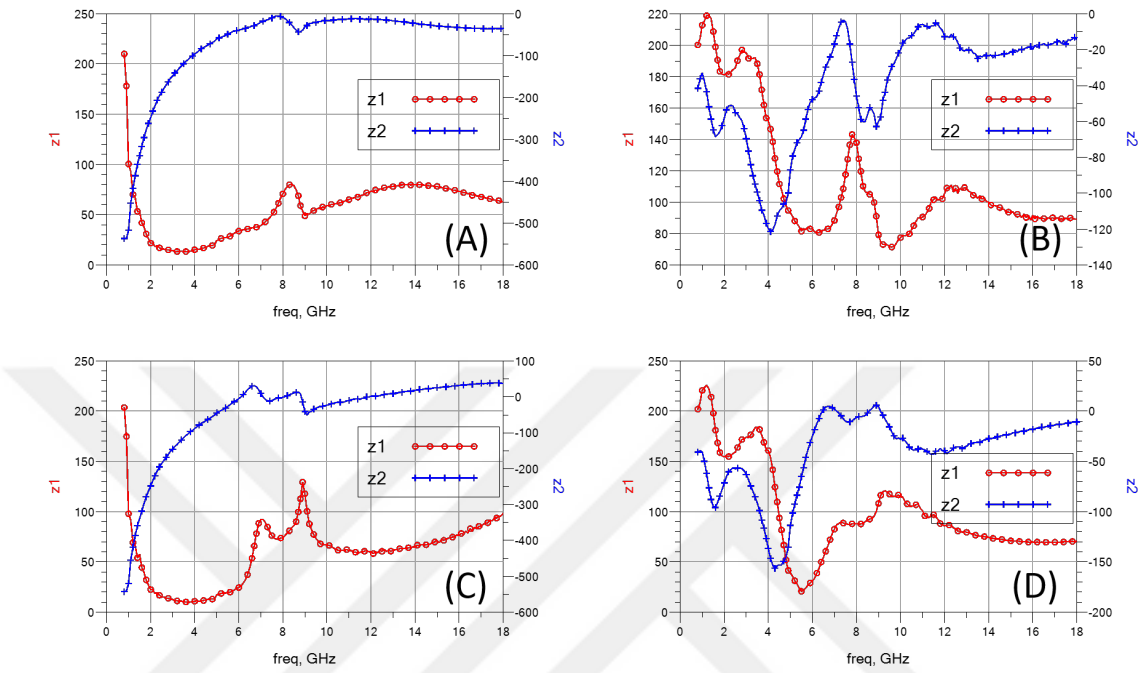

Figure 4.12: LNA-1 even-mode oscillations conditions check at the (A) Gate of the first stage HEMT, (B) Drain of the first stage HEMT, (C) Gate of the second stage HEMT, (D) Drain of the second stage HEMT.

S-probe analysis gives the designers an added advantage in solving any oscillation issue before fabrication.

4.3 Fabrication Results and Discussions

A microphotograph of the fabricated MMIC is shown in Fig. 4.14. Fig. 4.15A and 4.15B show the small-signal and noise measurement results of fabricated LNA-1 and LNA-2 MMICs, respectively. LNA-1 results in gain $>$ 16.8 dB, IRC $<$ -10.3 dB, ORC $<$ -10.1 dB, and NF $<$ 1.2 dB, while for LNA-2, NF $<$ 1.7 dB, IRC $<$ -11.6 dB, ORC $<$ -9.2 dB, and gain $>$ 17.2 dB is achieved. Transistors at both stages for LNA-1 after stabilization have only 1 dB $\mathrm{NF_{min}}$, resulting in an overall NF of 1.2 dB, the best-reported X-band design with two or more stages to the best of our knowledge. For LNA-2, as discussed in Section 4.2.2, $\mathrm{NF_{min}}$ for the second stage CS HEMT after stabilization is 4.2 dB, thus increasing the

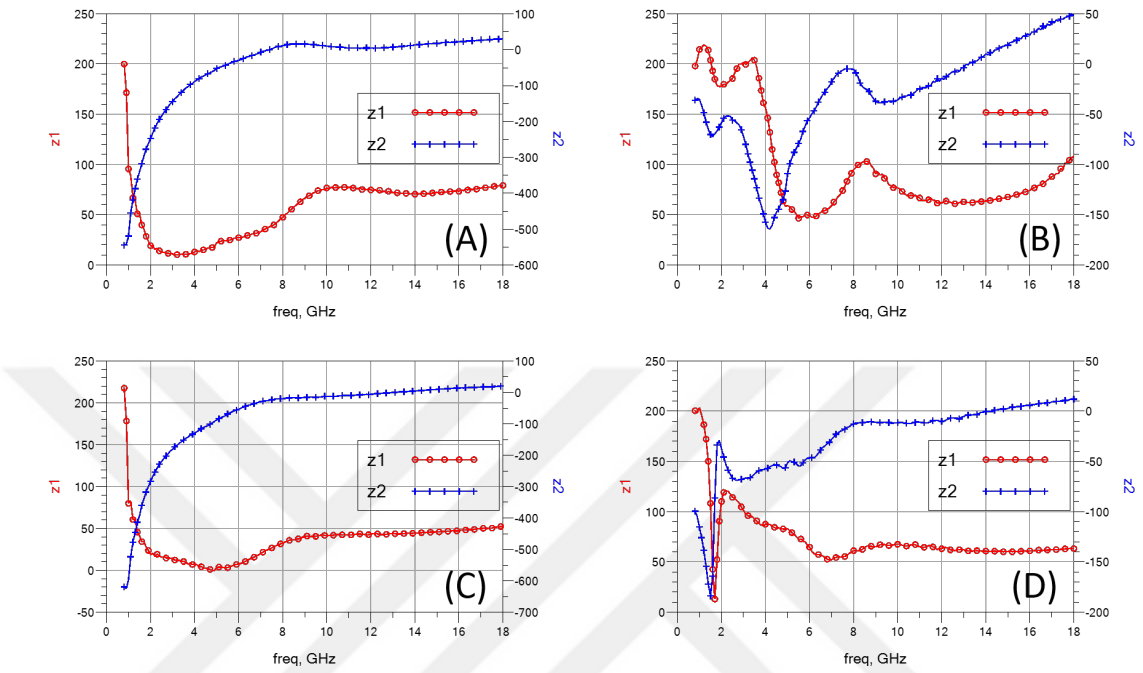

Figure 4.13: LNA-2 even-mode oscillations conditions check at the (A) Gate of the first stage HEMT, (B) Drain of the first stage HEMT, (C) Gate of the second stage HEMT, (D) Drain of the second stage HEMT.

overall NF to 1.7 dB. One advantage of using CS HEMT in LNA-2 is higher gain than LNA-1 but at the cost of higher NF. To conclude, the choice of ISD HEMT in subsequent stages of a multi-stage LNA design is desirable to achieve low NF values. Gain compensation may be achieved by increasing the number of stages, although at the cost of the size.

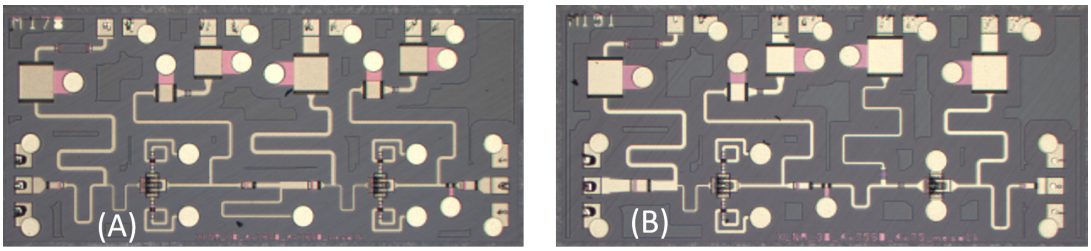

Figure 4.14: Microphotograph of (A) LNA-1 having ISD HEMTs at both stages, (B) LNA-2 having ISD HEMT at the first stage, and CS HEMT at the second stage.

P_{1dB} for LNA-1 and LNA-2 is shown in Fig. 4.16A and 4.16B, respectively. A noticeable difference of higher P_{1dB} for LNA-1 with ISD HEMT is evident

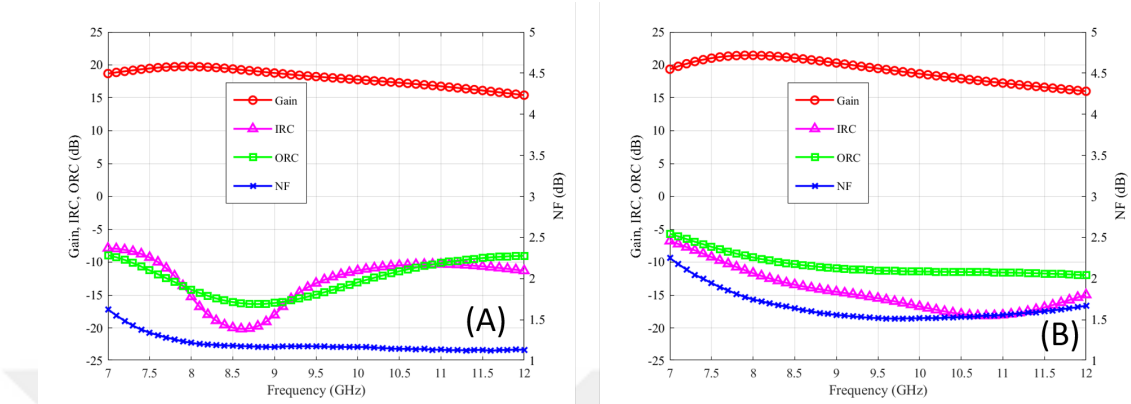

Figure 4.15: Measured gain, IRC, ORC, and NF of (A) LNA-1, (B) LNA-2.

compared to LNA-2 with CS HEMT at the second stage. Similar results for OIP3 measurements are achieved with LNA-1 having a higher OIP3 value, as shown in Fig. 4.17. Table 4.2 shows the comparative analysis of this work with recently published X-band LNAs. Both LNA-1 and LNA-2 have promising values of NF, gain, IRC, ORC, P_{1dB}, and OIP3. LNA-1 has the best reported NF in X-band compared with published designs using 0.25 µm, 0.15 µm, and 0.09 µm technologies.

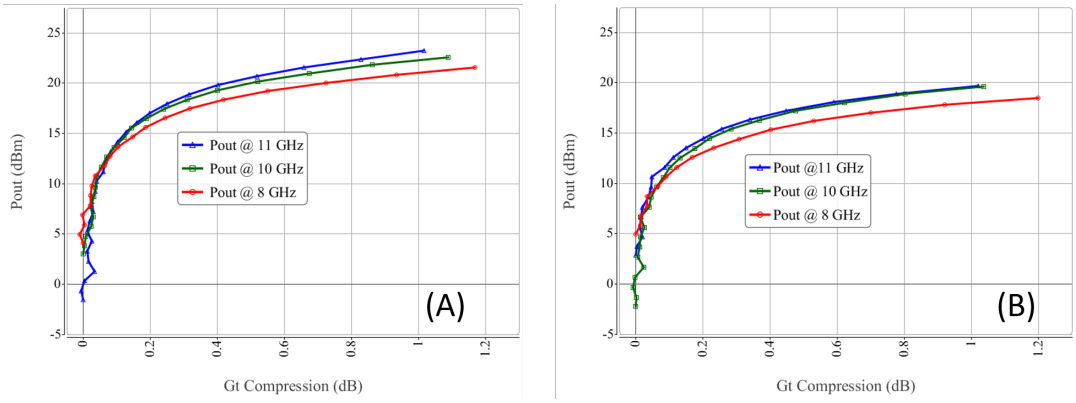

Figure 4.16: P_{1dB} of fabricated (A) LNA-1, (B) LNA-2 at 8 GHz, 10 GHz, and 11 GHz for 12 V, 200 mA/mm.

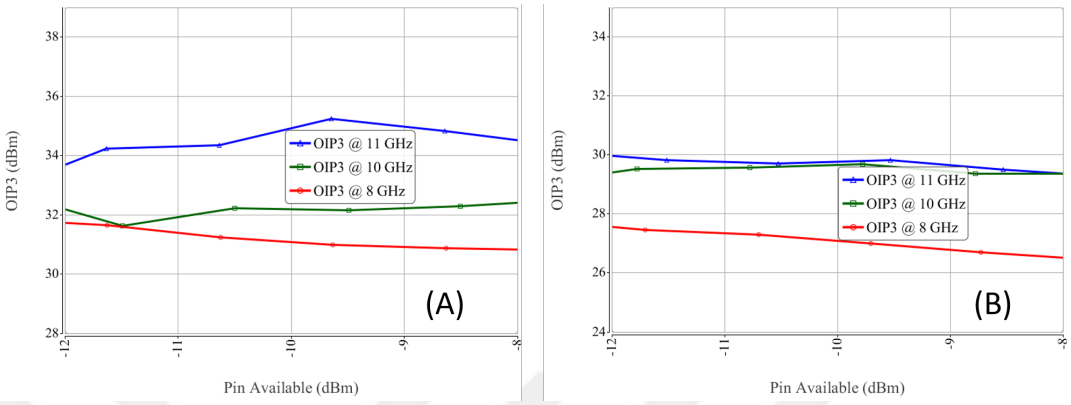

Figure 4.17: OIP3 of fabricated (A) LNA-1, (B) LNA-2 at 8 GHz, 10 GHz, and 11 GHz for 12 V, 200 mA/mm.

4.4 Summary

This study demonstrates two GaN-based X-band LNAs using 0.15 µm technology. ISD HEMTs, easy to stabilize and maintain a low NF_{min} after stabilization, are proven to be an optimum choice for all the stages in a multi-stage design to achieve overall low NF. Moreover, through simultaneous match conditions for ISD topology, minimum noise and a low IRC are achieved at the same time. Before fabrication, S-probe analysis is performed in ADS to check for any even-mode oscillation. LNA-1 achieves sub-1.2 dB NF and IRC better than -10.3 dB due to optimized stability networks and matching techniques. Small signal gain > 16.8 dB, ORC < -10.1 dB, $P_{1dB} > 21$ dBm, and OIP3 > 31 dBm for LNA-1 are achieved. LNA-2 having ISD HEMT at the first stage and CS at the second stage obtains NF < 1.7 dB and IRC < -11.6 dB. Moreover, gain > 17.2 dB, ORC < -9.2 dB, $P_{1dB} > 21$ dBm, and OIP3 > 27 dBm for LNA-2 are obtained. Sub-1.2 dB NF of LNA-1 is best for GaN-based X-band LNAs reported to date to the best of our knowledge. This NF value is comparable with other competitive GaAs and SiGe technologies known for best noise performance.

Table 4.2: A comparison of LNA-1 and LNA-2 with the recent GaN-based works at X-band.

Ref.	**Freq. (GHz)**	**NF (dB)**	**Gain (dB)**	**IRC (dB)**	**ORC (dB)**	**P_{1dB} (dBm)**	**OIP3 (dBm)**	**L_g (µm)**
[27]	8.4–10.6	< 2.3	> 25	< -10**	< -12**	—	—	0.25
[32]	4–16	< 2.0	> 11	< -10	< -8	—	24	0.15
[41]	8–11	< 2.0	> 22	< -9	< -5	—	24–29	0.25
[42]	9–11	< 1.5	> 13.5	< -10	< -8**	—	33–36	0.09
[43] (LNA A)	8–10	< 1.3	> 24	< -2	< -4	21**	33.8	0.25
[43] (LNA B)	10–12	< 1.75	> 24.4	< -10	< -12.5	20**	32.8	0.25
[44]	7.4–11.4	< 1.6	> 23	< -10	< -10	23	—	0.25
[45]	8–12	< 1.8	> 14	—	—	—	19.5	0.25
[46]	8–11	< 1.6	> 22.5	< -10	< -8	12	24	0.25
[81]	8–11	< 2.2	> 25	< -8**	< -10**	16	26	0.25
[85]	8–11**	< 2.3	> 16	—	—	—	—	0.25
[86]	8–11	< 2.5	> 17	< -10**	< -8.5**	> 17	—	—
[87]	7–12	< 2.5	> 14	< -5**	< -5**	20	28	0.25
[88]	9.7–12.9	< 2.1	> 20	< -2**	< -7**	—	32	0.25
[90]	9–11	< 2.2	> 13.5	< -11	< -5	—	29.5–34.5	0.15
[110]	8–11	< 2.0	> 19	< -9	< -11	> 19	30.5–34.2	0.15
[111]*	8–12	< 2.4	> 20	< -4	< -3	—	—	—
This work (LNA-1)	8–11	< 1.2	> 16.8	< -10.3	< -10.1	> 21	31–34	0.15
This work (LNA-2)	8–11	< 1.7	> 17.2	< -11.6	< -9.2	> 17	27–30	0.15

*Simulation based, **Estimated values from the figures

Chapter 5

Unveiling T_{max} Inside GaN HEMT based *X*-band Low-Noise Amplifier by Correlating Thermal Simulations and IR Thermographic Measurements

The contents of this chapter reflect the work reported in the following publication:

S. Zafar, Y. Durna, H. Kocer *et al.*, "Unveiling Tmax Inside GaN HEMT based X-band Low-Noise Amplifier by Correlating Thermal Simulations and IR Thermographic Measurements," *IEEE Transactions on Device and Materials Reliability*, doi: 10.1109/TDMR.2022.3230646.

5.1 Introduction

MMICs based on GaN HEMTs are designed as amplifiers (power and low-noise), mixers, and high-frequency switches. In MMICs based on GaN HEMTs, Joule heating causes a self-heating mechanism, leading to undesired hotspots in the device channel region. An increased channel temperature degrades the carrier mobility and saturated velocity, adversely affecting the device's electrical properties [112–117]. $MTTF$ is one of the crucial parameters in terms of the device's reliability [114, 118–121]. T_{max} happens inside the 2DEG region [122–125]. This temperature affects the $MTTF$ by the following relation [125, 126]:

$$MTTF \propto \exp(E_a/(k_b T_{max})), \tag{5.1}$$

where E_a is the activation energy, and k_b is Boltzmann's constant.

For an MMIC, T_{max} position is concealed in the 2DEG region of each HEMT used in the design. Electrical methods used for temperature measurements are simple, rapid, and noninvasive [115, 127, 128]. The drawback is that they underestimate peak channel temperature due to averaging over the active device region [129, 130]. Optical measurements such as micro-Raman and IR thermography [131–134] provide information on the surface temperature [122–124, 135], not the hotspots inside 2DEG buried below the gate of each HEMT. Moreover, spatial resolution limits optical measurements due to diffraction [136]. IR thermography is limited to a 3-10 µm wavelength range, while micro-Raman has a 0.5 µm resolution [131, 137]. All these constraints lead to inaccurate hotspot measurements in the 2DEG region, critical for $MTTF$ calculation. Although the measurements are essential, there is a need to couple these measurements with the 2D/3D FEA simulations through which the actual temperature profile inside the device is obtained [138–143]. In the case of an MMIC, critical factors in the simulations to be accurately modeled are device geometry, material parameters, thermal boundary resistance (TBR), boundary conditions, and dissipated power of each HEMT. In an MMIC, unlike an individual HEMT's temperature measurements, the spacing between the HEMTs is also important. It provides

valuable information to the circuit designer regarding the minimum distance between the active devices in an MMIC to avoid thermal coupling. In this study, the surface temperature profile of a two-stage X-band LNA MMIC is measured through IR thermography. This data is then correlated with 3D FEA simulations to accurately reveal the T_{max} of stage-1 and stage-2 HEMTs. The correlation is performed simultaneously for both HEMTs in the MMIC, thereby revealing the real hotspots inside the 2DEG.

In this chapter, Section 5.2 discusses the matching technique to unfold the actual 2DEG temperature profile. Section 5.3 presents 3D FEA simulations and IR thermographic measurements, while the correlation method is described in Section 5.4. The summary of the chapter is in Section 5.5.

5.2 Matching Technique to Reveal the Actual 2DEG Temperature Profile

A two-stage X-band LNA MMIC is shown in Fig. 5.1 with a 4x50 µm transistor (HEMT1) at the first stage and a 4x75 µm transistor (HEMT2) at the second stage. The design and performance of this LNA have already been discussed in Chapter 3. This study focuses on the thermal profiling of the HEMTs integrated into the MMIC using 3D FEA thermal analysis and IR thermography. 3D FEA analysis is performed in COMSOL Multiphysics environment, and IR thermographic measurements are carried out using a thermal microscope, from Quantum Focus Instruments [1] (QFI), with 12x magnification. The MMIC's geometry, along with the package in COMSOL, is shown in the bottom-right area of Fig. 5.1 with the zoomed version of one of the HEMTs. The hotspots (gate fingers) between the source and drain are visible in red color. The input for 3D FEA analysis includes 3D geometry of the MMIC, material parameters, thermal boundary resistance (TBR), and dissipated power (P_{diss}). As an output of this analysis, the surface temperature profile $T_{surf.}$ is achieved across the MMIC,

[1] Quantum Focus Instruments, 2385 La Mirada Dr, Vista, CA 92081, USA

revealing the hotspots.

For the measurements of the MMIC, the electrical bias V_d/I_d of 13 V / 58 mA and 13 V / 72 mA are applied for HEMT1 and HEMT2, respectively. An IR image of MMIC revealing the surface temperature profile T_{QFI} of the whole MMIC is shown in the top-left section of Fig. 5.1. Before applying the electrical signals, emissivity calibration is performed. QFI measurements are not depicting the actual surface temperature profile of the MMIC due to distortions in IR transmission media and the diffraction effect on the MMIC surface. 3D FEA analysis, on the other hand, reveals the actual surface temperature, including the hottest points in the MMIC. For that matter, there is a need to harmonize the IR thermographic measurements with 3D FEA results. To achieve this goal, two filters, one "Gaussian" and the other "Moving Average (MA)," have been employed to represent the distortions and diffraction effects. The parameters for the Gaussian filter are given as follows [122]:

$$Filter(x) = g_o + (A/(w\sqrt{(}\pi/2)))exp[(-2(x - x_c)^2)/w^2] \tag{5.2}$$

$$w = 2\sigma = \{FWHM\}/\sqrt{(}2In2). \tag{5.3}$$

Here, g_o is the offset of the Gauss function, x_c is the center of the Gauss function in µm, A is the area under the Gauss function, FWHM is full width at half maximum in µm, and σ is the standard deviation in µm.

In this study, g_o and x_c are fixed to zero, while A is taken as 0.1. Here, g_o and x_c are spatial quantities, and defining values other than zero for these does not change the output waveform shape of Eq. 5.4 and 5.5, where spatial convolution is performed. Similarly, the spatial "window" parameter of the MA filter is employed as in Fig. 5.1. Spatial convolution of $T_{surf.}(x)$ with $Filter(x)$ is performed, shown by blue arrows in Fig. 5.1, and FWHM is adjusted to achieve the following conditions:

$$T_{QFI}(x)@HEMT1 = T_{surf.}(x)@HEMT1 * Filter(x) \tag{5.4}$$

$$T_{QFI}(x)@HEMT2 = T_{surf.}(x)@HEMT2 * Filter(x). \tag{5.5}$$

These conditions guarantee the validity of the temperature profile achieved from 3D FEA thermal simulations. After matching the surface temperature profiles of

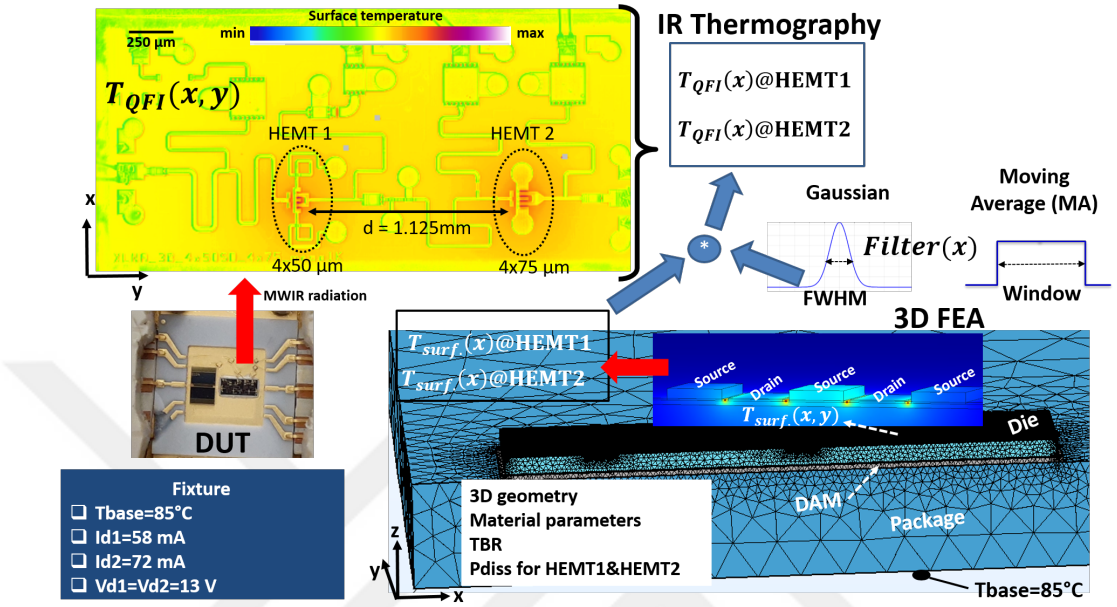

Figure 5.1: Flow chart for the estimation of 2DEG temperature profile of X-band LNA using the correlation between 3D FEA and IR thermography.

3D FEA and QFI, it is justified to claim that the 2DEG temperature of both the HEMTs in the MMIC revealed by 3D FEA is the most realistic. A critical aspect considered in this study is achieving the above-mentioned matching conditions for both HEMTs simultaneously. Moreover, both Gaussian and MA filters converge to satisfy the matching conditions.

5.3 3D FEA Thermal Modeling and IR Thermographic Measurements

5.3.1 LNA Design and 3D FEA Simulation Setup

Fig. 5.2 shows the schematic circuit representation and layout of the two-stage X-band LNA used in this study. The first stage consists of 4x50 µm ISD HEMT1, while the second stage has 4x75 µm CS HEMT2. The choice of HEMTs and their small and large signal performance has already been discussed in Chapter

3. In Fig. 5.2A, *R2*, *L5*, *C3*, and *C4* towards the drain side, while *L2*, *L3*, and *C2* towards the gate side of the HEMT1 constitute the stability network. The stability network additionally serves the purpose of the gate and drain bias. *L1* and *C1* are part of the input matching network. *C1* and *C2* additionally serve the purpose of blocking and bypass capacitors, respectively. *R1* is the high-value resistor for enhancing the survivability of the LNA and not affecting its RF performance [82]. *L4* is the inductor used for the source degeneration of the HEMT1. *R3*, *R4*, *L7*, and *C8* towards the gate side of HEMT2 are part of the stability and gate bias network. *L8*, *C9*, and *C10* towards the drain of HEMT2 complete the stability and output matching network and further serve the drain bias purpose. The rest of the components in Fig. 5.2A constitute the inter-stage matching network.

The geometric structure used for 3D FEA thermal simulations in COMSOL is shown in Fig. 5.3. The 3D half-symmetric structure of the LNA MMIC and the package used in the simulations is shown in Fig. 5.3A. As evident from Fig. 5.3B, the MMIC die is attached to Copper Molybdenum Copper (CMC) package using a die-attach material (DAM). Half-symmetric boundary conditions, defined as isothermal ($T_{base} = 85$ °C) at the bottom and adiabatic on all other surfaces, are selected [144, 145]. The effect of the radiative and the convective heat transfer mechanisms is negligible compared to conductive heat transfer; therefore, the radiative and the convective heat transfer mechanisms are not utilized [145]. The thermal conductivities of the materials used in the simulations are tabulated in Table 5.1 [122], while the geometry of the device and its components and layers are mentioned in Table 5.2. All metallizations in the MMICs, shown in yellow in Fig. 5.3, are defined as Au in the FEA.

The distance *"d"* between two HEMTs is 1.125 mm. The zoomed view of one of the HEMTs is shown in Fig. 5.3C. The length from source to drain (L_{SD}), gate foot length (L_g), and gate-gate spacing (pitch) are the same for HEMT1 and HEMT2. The thermal boundary resistance (TBR) is defined between GaN and SiC interface [17, 151], and its value is optimized in the simulations as 30 K.m^2/GW. Fig. 5.3D shows the T-gate head and foot with the regions where surface and

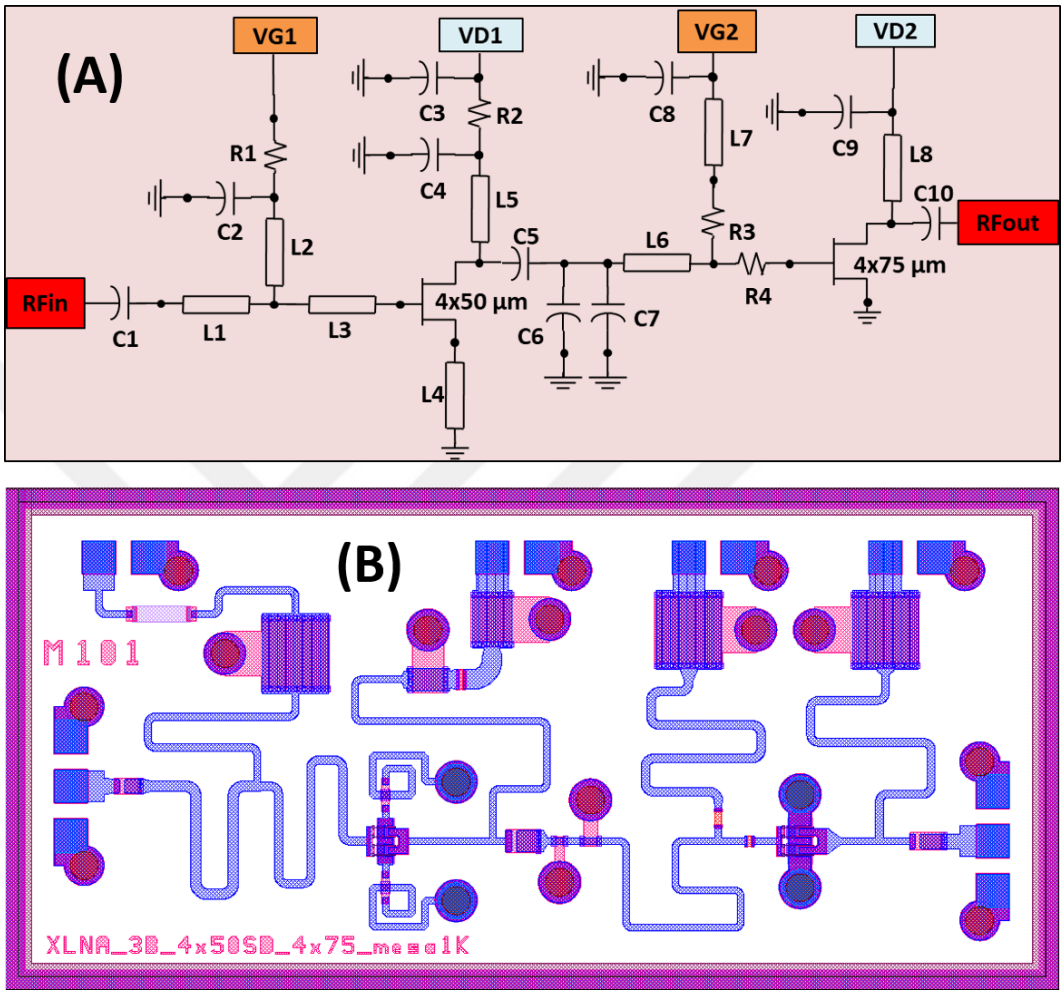

Figure 5.2: (A) Schematic circuit diagram, (B) Layout of two-stage X-band LNA.

Table 5.1: Thermal Conductivities Utilized in the FEA Thermal Simulations.

Material	**Temp. (K)**	**Thermal conductivity (W/mK)**
GaN [145], [146]	T	$130\text{x}(300/\text{T})^{1.4}$
SiC [145], [146]	T	$430\text{x}(300/\text{T})^{1.49}$
Si_3N_4 [147]	T	33
CMC [148]	T	180
DAM [149]	T	200
Au [150]	100	327
	200	323
	400	311
	600	298
	800	284
	1000	270

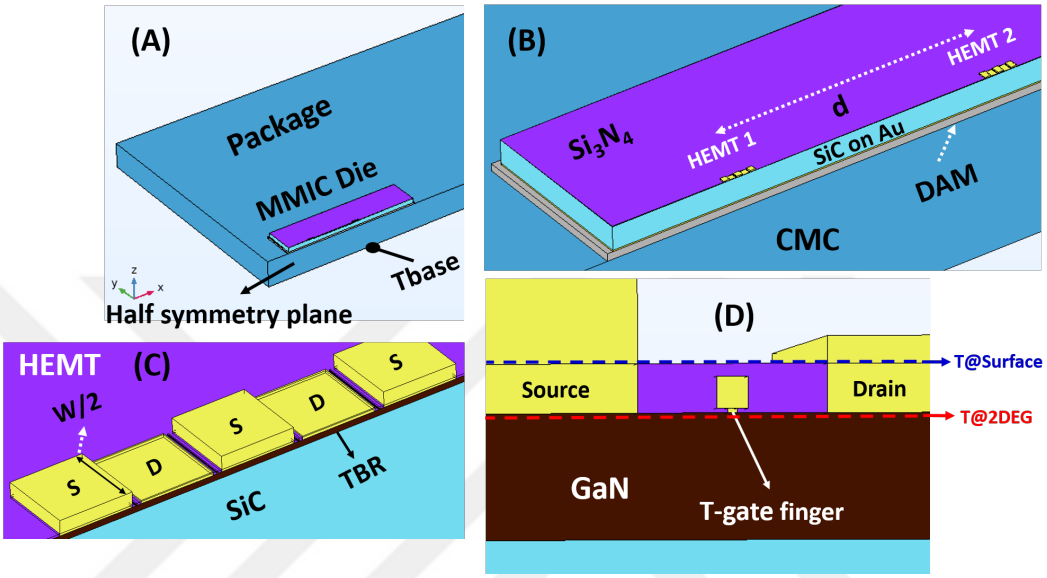

Figure 5.3: (A) 3D half-symmetric structure of the LNA MMIC along with the package, (B) MMIC die attached to CMC package using DAM, (C) The zoomed version of one of the HEMTs, along with TBR, is defined between GaN and SiC interface, (D) Close-up view of the T-gate, surface temperature, and 2DEG regions.

Table 5.2: Dimensions.

Dimension	Name	Value (µm)
L_{Die}	Length of MMIC Die	3100
W_{Die}	Width of MMIC Die	1410
t_{CMC}	Thickness of CMC package	600
t_{DAM}	Thickness of die-attach material	30
t_{Au}	Thickness of bottom gold layer	5
t_{SiC}	Thickness of SiC layer	98
t_{GaN}	Thickness of GaN layer	2
$t_{Si_3N_4}$	Thickness of nitride layer	0.775
L_{SD}	Length from source to drain of HEMT1&2	3
$L_{GateFoot}$ or L_g	Gate foot length of HEMT1&2	0.15
$L_{GateHead}$	Gate head length of HEMT1&2	0.50
$Pitch$	Gate-gate spacing HEMT1&2	28
W_{s,d_HEMT1}	Width of ohmic layer in source and drain of HEMT1	50
W_{s,d_HEMT2}	Width of ohmic layer in source and drain of HEMT2	75
$t_{s_HEMT1,2}$	Thickness of ohmic layer in source of HEMT1&2	5.22
$t_{d_HEMT1,2}$	Thickness of ohmic layer in drain of HEMT1&2	1.22

Table 5.3: Electrical Parameters.

Parameter	Description	Value
P_1	P_{diss} in HEMT1	3.69 W/mm
P_2	P_{diss} in HEMT2	3.12 W/mm
V_d	Drain voltage across both HEMTs	13 V
I_1	Drain current through HEMT1	58 mA
I_2	Drain current through HEMT2	72 mA
S_1	Total periphery of 4x50 µm HEMT1	0.2 mm
S_2	Total periphery of 4x75 µm HEMT1	0.3 mm
R_2	Resistance in drain bias line of HEMT1	5 Ω

2DEG temperature profiles are obtained. Although 2DEG is formed at AlGaN/GaN interface, the 20 nm AlGaN layer is not included in FEA analysis due to its thermal insignificance and effect on computational speed [145, 152]. Constant P_{diss} of 3.69 W/mm and 3.12 W/mm are applied through a constant heat source for HEMT1 and HEMT2, respectively. There is another hotspot in the MMIC, represented as R_2 in Fig. 5.2A, which is also seen in the thermographic MMIC image in Fig. 5.1. The value of this R_2 in the drain bias line and the calculations for P_{diss}, including R_2 in the drain bias line are given in Eq. 5.6 and 5.7, and the description of the parameters and their values are given in Table 5.3.

$$P_1 = (((V_{\mathrm{d}} - I_1 * R_2) * I_1)/S_1) \tag{5.6}$$

$$P_2 = ((V_{\mathrm{d}} * I_2)/S_2) \tag{5.7}$$

LNA is packaged and mounted on a fixture for IR thermographic measurements using QFI thermal microscope. Fig. 5.4A shows packaged LNA MMIC on the fixture, while Fig. 5.4B is the zoomed view of the package, where RF input/output, drain/source bias, and 50 Ω transmission line are visible. MMIC is made further visible in Fig. 5.4C, showing MMIC die, DAM, and square capacitors in the bias lines. SEM image of the MMIC in Fig. 5.4D gives another clear picture with wire bonds used in RF and DC paths. SEM images of stage-1 and stage-2 HEMTs are shown in Fig. 5.4E and 5.4F, respectively, with gate fingers having dimensions in the nanometer range.

IR thermographic measurement setup is shown in Fig. 5.5. Packaged MMIC

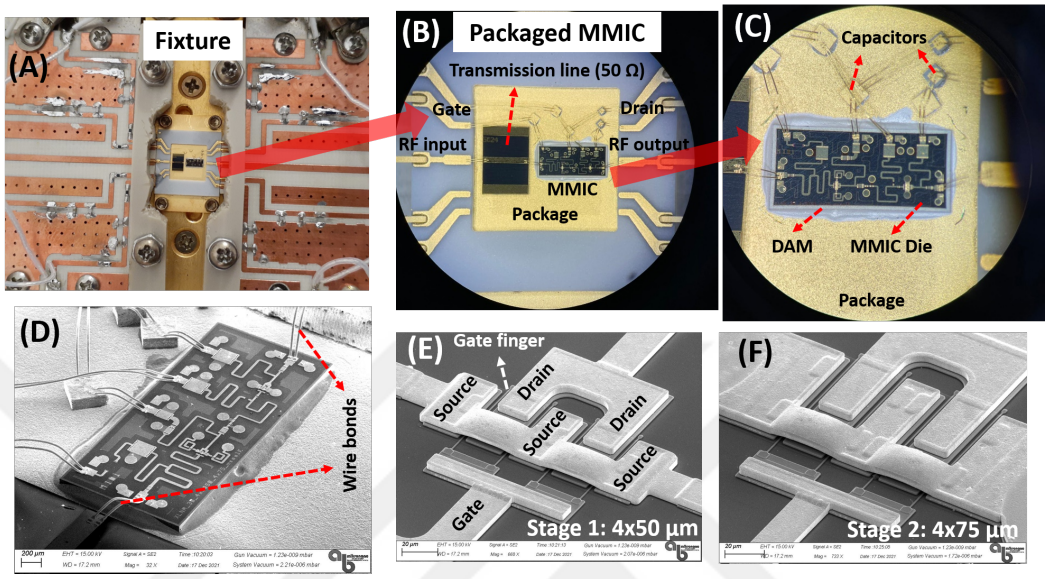

Figure 5.4: (A) Packaged LNA MMIC on the fixture, (B) Zoomed version of the package with RF input/output, drain/source bias, and 50 Ω transmission line, (C) Further close-up shows MMIC die, DAM, and square capacitors in the bias lines, (D) SEM image of the MMIC with wire bonds used in RF and DC paths, (E) SEM image of HEMT1, (F) SEM image of HEMT2.

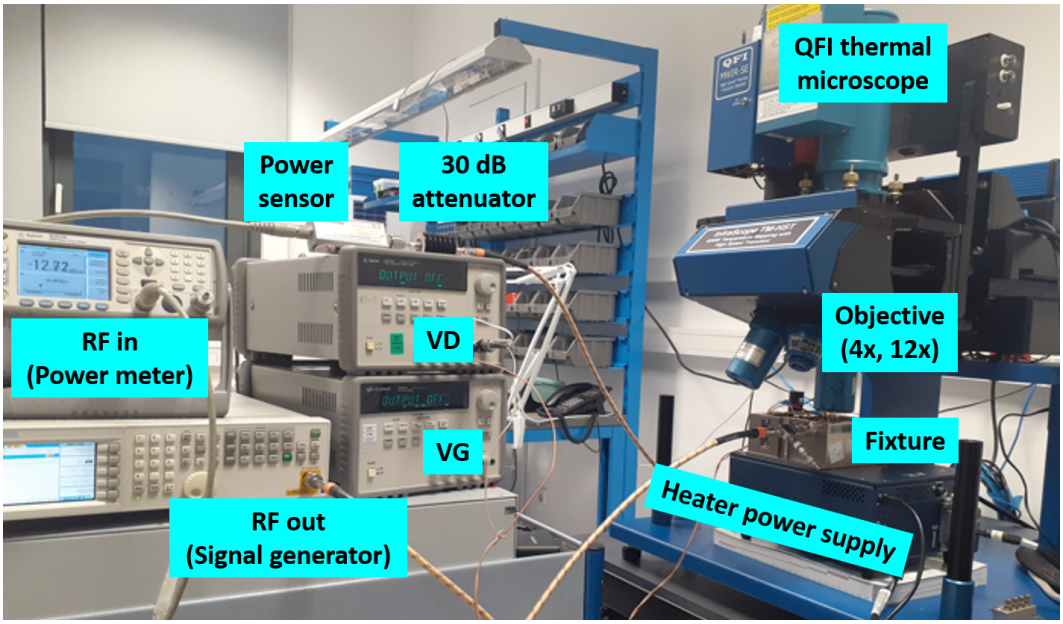

Figure 5.5: IR measurement setup showing packaged MMIC mounted in the fixture, QFI thermal microscope, heater, supply voltages V_G and V_D for gate and drain, respectively, signal generator, power meter, power sensor, and attenuator.

mounted in the fixture is placed beneath the QFI thermal microscope. The heater is used to adjust the base temperature (T_{base}). MMIC is biased using two supply voltages named V_G and V_D for the gate and drain, respectively. Before turning on the electrical signals, T_{base} is set to 85 °C, and the emissivity calibration of the QFI microscope is performed. In the next step, LNA is electrically turned ON by applying a continuous DC voltage of 13 V and P_{diss} of 3.69 W/mm for the first stage and 3.12 W/mm for the second stage, respectively. After stabilizing the T_{base} and P_{diss} to the desired values, the surface temperature is measured using a 12x objective lens of the QFI thermal microscope. Although this study does not include an RF signal generator, power meter, power sensor, and attenuator, they are shown in Fig. 5.5 as a complete setup for DC and RF thermal measurements of the MMIC.

5.4 Results and Discussions

Fig. 5.6 shows the 3D FEA simulated surface and 2DEG temperature profiles along with QFI surface temperature measurements under electrical and thermal conditions mentioned in previous sections. Fig. 5.6A shows simulated and measured temperature profiles of overall MMIC. The red and grey curves are FEA simulations of surface and 2DEG levels, respectively. Blue and green curves are LNA's stage-1 and stage-2 QFI temperature profiles, respectively. Measurements are taken along the middle of the HEMTs using the cut line at the hotspots of HEMT1 and HEMT2, shown as insets in Fig. 5.6A. To get a clearer picture, Fig. 5.6B and 5.6C show the zoomed versions of the HEMT1 and HEMT2 hotspots, respectively. The peaks and dips of the simulated and measured profiles appear at the exact locations for both stages, showing a good agreement. The highest 2DEG FEA simulated temperature profile is of the third gate finger of HEMT1 and HEMT2, which is further zoomed and shown in Fig. 5.6D and 5.6E, respectively. The exact location of the peaks and dips in the profiles for both stages simultaneously proves the simulation's validity.

The methodology explained in Section 5.2 using the simulated and measured

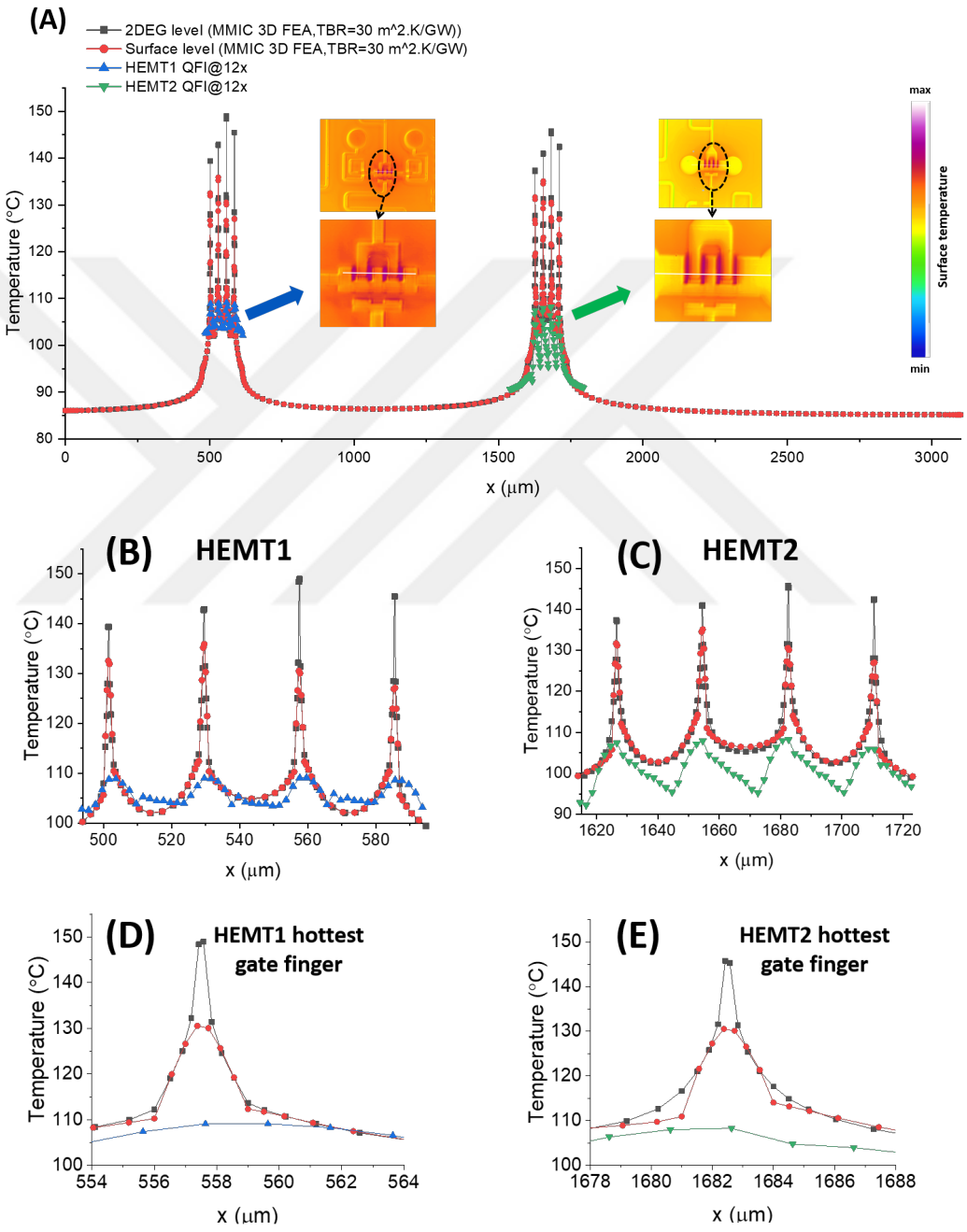

Figure 5.6: (A) Measured (QFI@12x) and 3D FEA simulated (surface and 2DEG) temperature profiles of overall MMIC, (B) Zoomed version of the HEMT1 hotspots, (C) Zoomed version of the HEMT2 hotspots, (D) HEMT1 hottest gate finger, (E) HEMT2 hottest gate finger.

thermal profiles is implemented. The correlation method explained earlier is applied to simulated and measurement data in Fig. 5.6. With 12x magnification, the spatial resolution of the QFI microscope is 2 µm, which is too large for the minimum feature size of the MMIC. In order to address the diffraction-limited resolution, spatial convolution is performed with simulated surface temperature and two filters (Gaussian and MA). FWHM is given a sweep from 5 µm to 15 µm in discrete steps. For lower spatial frequency regions, FWHM's effect is not significant because there are no spatial fluctuations in the locations other than hot fingers. Over these diffraction-free and optically large areas, IR imaging losses are negligible. In areas other than non-peak regions with high spatial fluctuations, the filter expands spatially with an increase in FWHM, thereby becoming less sensitive to spatial fluctuations.

The best match between the measurements and filter is for FWHM = window = 10 µm, shown in Fig. 5.7. The simulation temperature and Gaussian/MA filter data overlap in the non-peak areas guaranteeing the proper functioning of both filters. The data and the pictures of the whole MMIC with zoomed hotspot areas of both the HEMTs are shown with better visualization in Fig. 5.7. The maximum surface temperatures realized from FEA simulations are 136.4 ℃ and 135.5 ℃ for HEMT1 and HEMT2, respectively. Thermal profiles measured from QFI result in maximum temperature peaks of 109 ℃ for HEMT1 and 108.3 ℃ for HEMT2. The successful correlation method reveals the actual FEA 2DEG temperature with maximum peaks at 149 ℃ and 145.8 ℃ for HEMT1 and HEMT2, respectively.

Table 5.4 summarizes the peak temperature points achieved from FEA simulations and QFI measurements. Corresponding $MTTF$ calculations are made according to Eq. 5.1. The activation energy E_a value is taken as 1.5 eV and k_b as 8.6x10^{-5} eV/K [125]. In order to compare the $MTTF$ values calculated from FEA analysis and measurements, the ratios of $MTTF$ parameters 'A,' 'B,' and 'C' are taken into account. A smaller value of these ratios indicates a big difference between the actual $MTTF$ (by FEA analysis) and incorrect $MTTF$ (by QFI measurements). This shows the importance of finding the actual T_{max} inside the device.

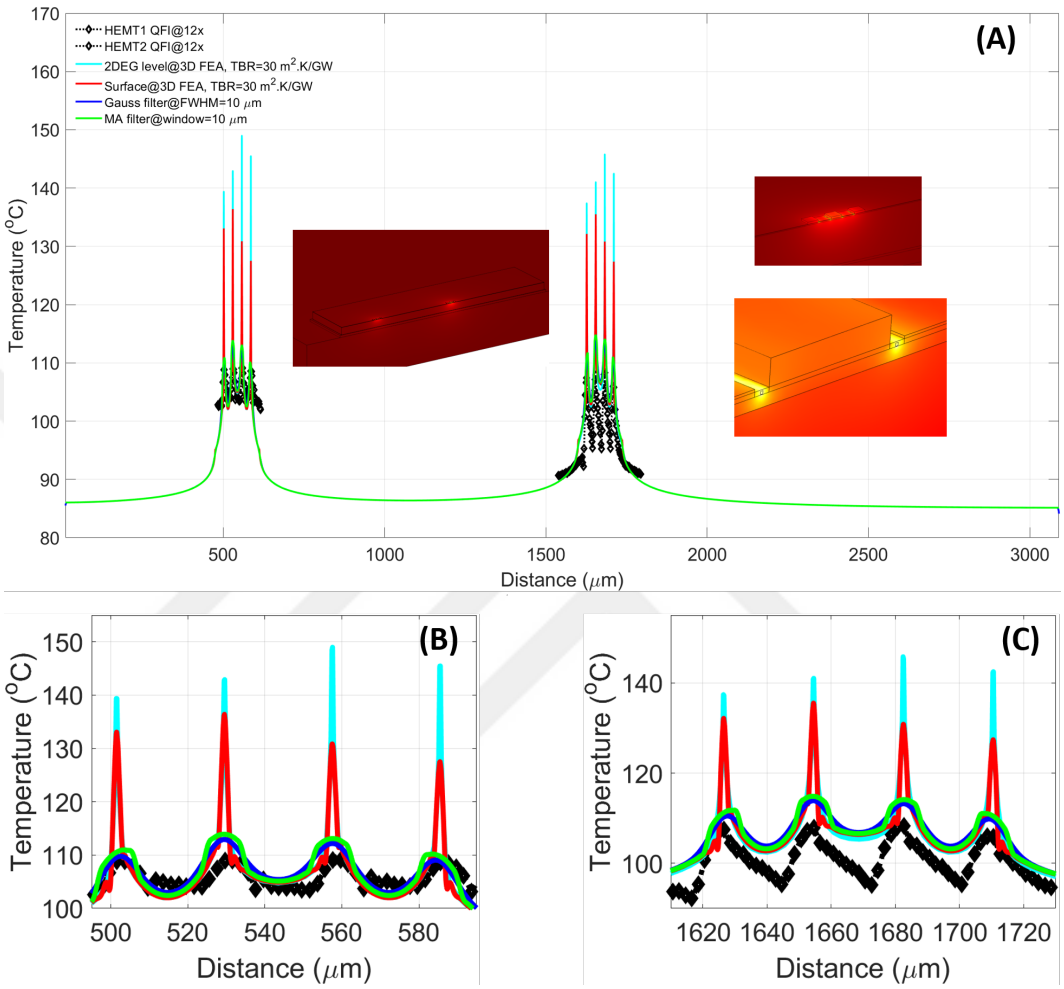

Figure 5.7: (A) Measured (QFI@12x) temperature, 3D FEA simulated (surface and 2DEG) temperature at TBR=30 K.m^2/GW, and convolution results with Gaussian and MA filter at FWHM and window of 10 µm, (B) Zoomed hotspot areas of HEMT1. (C) Zoomed hotspot areas of HEMT2.

Table 5.4: *MTTF* Ratios from Simulated and Measured Thermal Profiles.

Parameter	**HEMT1**	**HEMT2**
T_{max} 2DEG FEA '*T1*'	422.15 K (149 °C)	418.95 K (145.8 °C)
T_{max} surf. FEA '*T2*'	409.55 K (136.4 °C)	408.65 K (135.5 °C)
T_{max} QFI '*T3*'	382.15 K (109 °C)	381.45 K (108.3 °C)
MTTF 2DEG FEA '*M1*'	8.8 x 10^{17}	1.2 x 10^{18}
MTTF surf. FEA '*M2*'	3.1 x 10^{18}	3.5 x 10^{18}
MTTF QFI '*M3*'	6.6 x 10^{19}	7.3 x 10^{19}
A = *M1/M2*	0.280	0.35
B = *M2/M3*	0.047	0.048
C = *M1/M3*	0.013	0.016

The difference in the T_{max} value from FEA simulations and QFI measurements for HEMT1 is 40 K, leading to a substantial change in corresponding $MTTF$ values. This results in a minimal value of the $M1/M3$ ratio, i.e., 0.013. Similarly, for HEMT2, this ratio is 0.016. It also shows that this is HEMT1 that decides the overall MMIC's reliability. The method proposed in this study to unveil the actual hotspots in an MMIC proves critical for the device's reliability.

5.5 Summary

The reliability of a device is much dependent on accurate temperature profile measurement. Optical techniques (micro Raman and IR thermography) measure the surface temperature only and are also limited in spatial resolution. On the other hand, FEA thermal simulations reveal the actual sub-surface hotspots inside the device. In order to realistically reveal the actual T_{max} inside the device, 3D FEA thermal simulations are correlated with IR thermographic measurements performed on a two-stage X-band LNA MMIC. FEA thermal simulations are performed using COMSOL Multiphysics software by careful device modeling, and IR thermographic measurements are carried out using a QFI thermal microscope with 12x magnification for better resolution. The correlation method is implemented using two filters (Gaussian and moving average) to simultaneously unveil the hotspots inside 2DEG of LNA's stage-1 and stage-2 HEMTs. The ratios of $MTTF$ values achieved from FEA simulations and QFI measurements in this study indicate the importance of finding the actual peak temperature point inside the device. Moreover, in the LNA MMIC used in this study, it is HEMT1 that decides the overall MMIC's reliability. This work is a valuable contribution toward a reliability study where MMICs have multiple hotspots inside two or more active devices.

Chapter 6

Conclusion

LNA is an integral and critical component in an RF transceiver system. LNAs based on GaN HEMT technology offer promising small and large signal performance parameters. Three LNAs have been designed using NANOTAM's 0.15 µm GaN on SiC HEMT process.

One of the designed LNAs discussed in Chapter 3 has the best combination of gain, return losses, NF, and survivability with respect to size and bandwidth. Owing to the optimum choice of HEMT topologies and simultaneous matching technique, LNA achieves an NF better than 2 dB, P_{1dB} higher than 19 dB, and IRC and ORC better than -9 dB and -11 dB, respectively. The small-signal gain of LNA is more than 19 dB for the whole band, and NF has a minimum of 1.74 dB at 10.2 GHz. LNA obtains an OIP3 up to 34.2 dBm and survives input power as high as 42 dBm. Survivability is investigated in terms of gain compression and forward gate current. RRT, a crucial parameter for radar front-ends, is explored with respect to the RC time constant and trap phenomenon. The analysis shows that the significant contribution in RRT is due to traps while the RC time constant is in the nanoseconds range. Moreover, this study also addresses the requirement and choice of a DC gate feed resistor for the subsequent stages in a multi-stage design.

In the second part of the study, discussed in Chapter 4, HEMT topologies and design techniques have been presented to achieve a sub-1.2 dB NF for one of the designed LNAs. This NF is comparable with state-of-the-art reported works in competitive GaAs and SiGe technologies. Moreover, this is the best reported NF in X-band using GaN technology to date. Two LNAs are fabricated using in-house 0.15 µm AlGaN/GaN on the SiC HEMT process, one with ISD HEMTs at both stages, while the other having ISD HEMT at the first and CS HEMT at the second stage. The significance of ISD HEMT towards NF improvement for the first or subsequent stages in a multi-stage design is addressed. The criticality of stability networks towards NF contribution and its design is discussed in detail. Furthermore, even-mode stability of each HEMT after complete LNA design is assured using the S-probe method in Pathwave Advanced Design Systems.

The reliability of a device is greatly dependent on accurate temperature profiling, especially where MMICs have multiple hotspots inside two or more active devices. Chapter 5 is based on this study using a two-stage X-band low-noise amplifier with 4x50 µm and 4x75 µm HEMTs at the first and the second stage, respectively. The surface temperature measured through IR thermography has a diffraction-limited resolution. Moreover, it is impossible to measure sub-surface T_{max} residing inside the 2DEG of HEMT using IR thermographic measurements. FEA thermal simulations are performed in this study to acquire the surface and sub-surface temperature profiles of the whole MMIC. IR measurements and FEA simulations are integrated through a correlation-based method verifying the accuracy of the FEA-based temperature profiles. This method leads to accurately finding the hotspots in the MMIC, thus revealing the T_{max} of both stages. The correlation method using two filters approach to match the measurements and simulated temperature profiles of all the stages finds its application in MMICs' high-temperature operating lifetime reliability tests.

In future works, different design techniques used in this thesis will be combined to fabricate a single LNA MMIC to achieve robustness and low NF simultaneously. The designed LNAs will be integrated in the X-band transceiver modules using NANOTAM's fabrication process. RRT measurements for various duty cycles and multiple R_{GB} values will be performed. Moreover, IR thermographic

measurements will be extended to DC and RF to analyze the effect of RF signals on multiple hotspots in an MMIC.

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