PROCESS DEVELOPMENT FOR MICROFABRICATION OF PHASE REVERSAL CMUT DEVICES FOR STRUCTURAL HEALTH MONITORING AND DEVELOPMENT OF DYNAMIC CHARACTERIZATION PROCESSES FOR MEMS APPLICATIONS

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Merve Mintaş Küçük

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Process Development for Microfabrication of Phase Reversal CMUT Devices for Structural Health Monitoring and Development of Dynamic Characterization Processes for MEMS Applications
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Abdullah Atalar(Advisor)

Mehmet Yılmaz(Co-Advisor)

Barbaros Çetin

Ayhan Bozkurt

Approved for the Graduate School of Engineering and Science:

Orhan Arıkan
Director of the Graduate School

ABSTRACT

PROCESS DEVELOPMENT FOR MICROFABRICATION OF PHASE REVERSAL CMUT DEVICES FOR STRUCTURAL HEALTH MONITORING AND DEVELOPMENT OF DYNAMIC CHARACTERIZATION PROCESSES FOR MEMS APPLICATIONS

Merve Mintaş Küçük
M.S. in Materials Science and Nanotechnology
Advisor: Abdullah Atalar
Co-Advisor: Mehmet Yılmaz
August 2024

If appropriately designed, Capacitive Micromachined Ultrasonic Transducers (CMUTs) offer advantageous properties such as low cost, small size, low impedance, and environmental friendliness, over piezoelectric transducers. These advantageous properties of CMUTs enable the CMUT devices to be employed in a large area of applications, such as medical applications and non-destructive testing (NDT) applications. CMUT devices and technologies that are heavily developed for medical applications also shed light on the development of CMUT devices to be used in Structural Health Monitoring (SHM) applications for civil infrastructures. Continuous monitoring of the signals produced by the sudden changes happening within civil infrastructures such as bridges or railways may give crucial information about the health of these structures. The rapid release of localized strain energy, which generates Acoustic Emission (AE) waves, is an important indicator of the state of the health of a structure. Detecting AE wave signals may give significant clues about damage formation such as impact, crack initiation, or crack growth. Because AE waves are scattered among a broad range of frequencies, sensing of such AE waves should also be done in broadband, and sensors are preferred to be highly sensitive among such band. For real-life applicable developments, it should be also considered that the environment of the real-life application may be very noisy due to many unrelated reasons, which makes employment of the CMUTs developed in a tightly controlled laboratory environment unpractical for the real-life applications. The noise may often be induced by the noise interferences that are produced by a variety of events that

are not needed to be detected. To prevent misjudgments, it is important to differentiate between noise interferences and relevant AE signals, as the presence of significant noise can hinder the detectability of AE waves associated with structural damage.

In this process development for CMUT prototype microfabrication study, we collaborated with a group of researchers who have introduced a new approach to designing broadband CMUTs, as well as a unique type of CMUT combination that uses phase-reversal (PR) of generated electrical current for detecting a wide range of mechanical vibration wave frequencies and reducing unwanted noise. By considering the simplest combination of two CMUT cells, the theoretical study, supported by FEM simulations, demonstrated that reversing the electrical current phase of one cell can create low-frequency and high-frequency stopbands for noise rejection, which is applicable for CMUTs operating in air damping.

The primary objective of this thesis study is to develop microfabrication processes to microfabricate PR-CMUT devices to bridge the gap between theoretical design and real-world application of PR-CMUT devices. These PR-CMUT arrays that are designed for wafer-scale batch-compatible manufacturability have a flat passband in the 200-250 kHz and 200-300 kHz frequency ranges and two improved stopbands on both sides of the relevant frequency ranges. The photolithography masks, compatible material selections, and microfabrication process flows (integration processes) required for the microfabrication of these PR-CMUT devices were designed considering the capabilities of our cleanroom facility. Microfabrication of the devices was tried multiple times, and in line with the problems encountered in these processes, the microfabrication process flows were updated and the PR-CMUT devices were tried to be produced in multiple iterations. Unit processes, and multiple integration processes were developed and completed. Possible solutions to be implemented in the future microfabrication studies were determined. Additionally, dynamic characterization of individual circular geometry CMUT membranes were explored using a ZYGO Optical Profilometer. With this measurement tool (ZYGO), it is possible to measure CMUT device membrane displacements precisely when the membrane of the CMUT device is moving (vibrating) dynamically. Results obtained from ZYGO Optical Profilometer tool were compared with the impedance analyzer results. It was shown that the resonance frequency of a circular membrane CMUT device can be observed with the ZYGO Optical Profilometer. Furthermore, based on the conclusions from

the studies in this thesis, future studies are suggested for further development towards realization and characterization of these PR-CMUT MEMS (MicroElectroMechanical System) devices.

Keywords: Process Development, Wafer-scale Batch-compatible Microfabrication, Capacitive Micromachined Ultrasonic Transducers, CMUT, Structural Health Monitoring, SHM, MEMS, Dynamic Measurements with Optical Profilometer.

ÖZET

YAPISAL SAĞLIK İZLEME İÇİN FAZI TERSİNE ÇEVİREN CMUT CİHAZLARININ MİKROÜRETİMİ İÇİN SÜREÇ GELİŞTİRİLMESİ VE MEMS UYGULAMALARI İÇİN DİNAMİK KARAKTERİZASYON SÜREÇLERİNİN GELİŞTİRİLMESİ

Merve Mintaş Küçük
Malzeme Bilimi ve Nanoteknoloji, Yüksek Lisans
Tez Danışmanı: Abdullah Atalar
İkinci Tez Danışmanı: Mehmet Yılmaz
Ağustos 2024

Eğer uygun bir şekilde tasarlanırsa, Kapasitif Mikroişlemeli Ultrasonik Transdüserler (CMUT'lar), piezoelektrik transdüserlere kıyasla düşük maliyet, küçük boyut, düşük empedans ve çevre dostu olma gibi avantajlı özellikler sunar. Bu avantajlı özellikler, CMUT cihazlarının tıbbi uygulamalar ve tahribatsız test (NDT) uygulamaları gibi geniş ve oldukça çaşitli alanlarda kullanılmasını sağlar. Tıbbi uygulamalar için yoğun bir şekilde geliştirilen CMUT cihazları ve teknolojileri, aynı zamanda CMUT cihazlarının büyük altyapılar için Yapısal Sağlık İzleme (SHM) uygulamalarında kullanılmasının önünü açmıştır. Köprüler veya demiryolları gibi altyapılarda meydana gelen ani değişimlerin ürettiği sinyallerin sürekli izlenmesi, bu yapıların sağlığı hakkında önemli bilgiler verebilir. Yerel (lokal) gerinim enerjisinin hızlı bir şekilde serbest bırakılması, Akustik Emisyon (AE) dalgaları oluşturur ve bu durum, bir yapının sağlık durumu hakkında önemli bir göstergedir. AE dalga sinyallerinin tespit edilmesi, darbe, çatlak oluşumu veya çatlak büyümesi gibi hasar oluşumu hakkında önemli ipuçları verebilir. AE dalgaları geniş bir frekans aralığına yayıldığından, bu tür AE dalgalarının algılanması da geniş bantta yapılmalıdır ve sensörlerin bu bant içerisinde oldukça hassas olması tercih edilir. Gerçek hayatta uygulanabilir gelişmeler için, gerçek hayat uygulamasının ortamının asıl konu ile ilgisi olmayabilecek birçok nedenden dolayı çok gürültülü olabileceği de göz önünde bulundurulmalıdır, bu da sıkı bir şekilde kontrol edilen laboratuvar ortamında geliştirilen CMUT'ların gerçek hayat uygulamaları için pratik olmamasına neden olabilir. Gürültü genellikle tespit edilmesi

gerekmeyen çeşitli olaylar tarafından üretilen parazit gürültülerden kaynaklanabilir. Yanlış değerlendirmeleri önlemek için, gürültü parazitleri ile ilgili akustik emisyon (AE) sinyalleri arasında ayrım yapmak önemlidir, çünkü önemli miktarda gürültünün varlığı, yapısal hasarla ilişkili AE dalgalarının tespit edilebilirliğini engelleyebilir.

Bu CMUT prototipi mikroüretim çalışması için süreç geliştirme aşamasında, geniş bant CMUT tasarımında yeni bir yaklaşım ve mekanik titreşim dalga frekanslarının geniş bir yelpazesini tespit etmek ve istenmeyen gürültüyü azaltmak için faz terslemesi (PR) kullanan benzersiz bir CMUT kombinasyonu tanıtan bir araştırma ekibi ile iş birliği yaptık. İki CMUT hücresinin en basit kombinasyonu dikkate alınarak yapılan teorik çalışma ve FEM simülasyonları, bir hücrenin elektrik akımı fazını tersine çevirmenin, hava sönümlemesi altında çalışan CMUT'lar için gürültü reddi açısından düşük frekans ve yüksek frekans durma bantları oluşturabileceğini gösterdi.

Bu tez çalışmasının temel amacı, PR-CMUT cihazlarının teorik tasarım ile gerçek dünya uygulaması arasındaki boşluğu doldurmak için mikrofabrikasyon süreçlerini geliştirmektir. Yonga ölçeğinde seri üretimle uyumlu üretilebilirlik için tasarlanan bu PR-CMUT dizileri, 200-250 kHz ve 200-300 kHz frekans aralıklarında düz bir geçiş bandına ve ilgili frekans aralıklarının her iki tarafında iki geliştirilmiş durma bandına sahiptir. Bu PR-CMUT cihazlarının mikrofabrikasyon için gerekli fotolitografi maskeleri, uyumlu malzeme seçimleri ve mikrofabrikasyon süreç akışları (entegrasyon süreçleri), kullandığımız temioda yeterlilikleri dikkate alınarak tasarlandı. Cihazların mikrofabrikasyonu birçok kez denendi ve bu süreçlerde karşılaşılan sorunlara paralel olarak mikrofabrikasyon süreç akışları güncellendi ve PR-CMUT cihazları birçok kez üretilmeye çalışıldı. Birim süreçler ve birçok entegrasyon süreci geliştirildi ve tamamlandı. Gelecek mikrofabrikasyon çalışmalarında uygulanacak olası çözümler belirlendi. Ayrıca, dairesel geometrili CMUT tekli membranlarının dinamik karakterizasyonu ZYGO Optik Profilometre kullanılarak araştırıldı. Bu ölçüm aracı (ZYGO) ile CMUT cihazının dairesel membranı dinamik olarak hareket ederken (titreşim yaparken) CMUT cihazı membran hareketlerini kesin olarak ölçmek mümkündür. ZYGO Optik Profilometre ile elde edilen sonuçlar, empedans analizörü sonuçları ile karşılaştırıldı. Dairesel membran CMUT cihazının rezonans frekansının ZYGO Optik Profilometre ile gözlemlenebileceği gösterildi. Ayrıca, bu tez çalışmasındaki

sonuçlara dayanarak, bu PR-CMUT MEMS (MikroElektrikMekanik Sistem) cihazlarının gerçekleştirilmesi ve karakterizasyonu için daha fazla gelişim sağlanması adına gelecekteki çalışmalar önerildi.

Bu tez çalışmasının temel amacı, PR-CMUT cihazlarının teorik tasarımı ile gerçek dünya uygulaması arasındaki boşluğu doldurmak için PR-CMUT cihazlarını mikroyapım süreçleri geliştirerek üretmektir. Yonga ölçekli seri uyumlu üretilebilirlik için tasarlanan bu PR-CMUT dizileri, 200-250 kHz ve 200-300 kHz frekans aralıklarında düz bir geçiş bandına ve her iki tarafta da geliştirilmiş iki durdurma bandına sahiptir. Bu PR-CMUT cihazlarının mikrofabrikasyonu için gerekli fotolitografi maskeleri, malzeme seçimleri ve mikrofabrickasyon işlem akışı, UNAM temiz oda tesisinin yetenekleri göz önünde bulundurularak tasarlandı. Cihazların mikrofabrikasyonu birçok kez denendi ve bu süreçte karşılaşılan sorunlar doğrultusunda mikrofabrikasyon işlem akışı değiştirildi ve PR-CMUT cihazları farklı iterasyonlarla üretilmeye çalışıldı. Zaman kısıtlamaları nedeniyle, çalışan bir PR-CMUT üretimi tamamlanamadı, ancak birim süreçler tamamlandı ve bir sonraki üretimde uygulanacak çözümler belirlendi. Ek olarak, CMUT cihazlarının dinamik karakterizasyonu ZYGO Optik Profilometre kullanılarak incelendi. Bu ölçüm aracıyla, CMUT cihazın zarı dinamik olarak hareket ederken CMUT cihaz zarı yer değiştirmeleri hassas bir şekilde ölçülebilir. Elde edilen sonuçlar empedans analizörü sonuçlarıyla karşılaştırıldığında, CMUT cihazının rezonans frekansının ZYGO Optik Profilometre ile elde edilebileceği gösterildi. Ayrıca, bu ölçümlerden elde edilen diğer sonuçların anlamlı bilgi elde etmek için daha fazla incelenmesi gerektiği sonucuna varıldı.

Anahtar sözcükler: Süreç Geliştirme, Toplu Üretim Uyumlu Mikrofabrikasyon, Kapasitif Mikro İşlenmiş Ultrasonik Dönüştürücüler, CMUT, Yapısal Sağlık İzleme, SHM, MEMS, Optik Profilometre ile Dinamik Ölçümler.

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whenever I faced challenges played a crucial role in the completion of my research.

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Chapter 1

Introduction

Capacitive micromachined ultrasonic transducers (CMUTs) are an innovative technology that was initially developed to overcome the limitations of traditional piezoelectric transducers in the field of ultrasonic transducers, especially in the MHz frequency range [1]. The beginning of CMUT technology can be traced back to the innovative work of Haller and Khuri-Yakub at Stanford University in 1996 [1]. They created the basis for CMUT technology and inspired researchers around the world to explore new ways to use CMUT devices. One of the early milestones of CMUTs was an underwater experiment that demonstrated the significant advantages of CMUTs over traditional piezoelectric transducers such as broad bandwidth, wide temperature tolerance, and fabrication at low cost [2]. This crucial discovery demonstrated the versatility and potential of CMUT technology with the development of sealed CMUTs designed for immersion (i.e. in water, in vegetable oil) applications.

When comparing traditional piezoelectric ultrasonic transducers with CMUT, CMUT devices have numerous advantages in many areas where they contribute, especially in high-frequency applications. These advantages include broad bandwidth, easy integration with electronic systems, increased sensitivity, and a wide operating temperature range [2–4]. These characteristics are important in applications such as medical imaging, underwater sonar applications, and SHM that

require precise and reliable performance in broadband frequency ranges, making CMUTs an alternative to piezoelectric transducers.

CMUT is a type of MEMS-based device used for both transmitting and receiving ultrasonic waves. The structure typically consists of a thin, flexible membrane suspended over a cavity, with a fixed electrode beneath it [3]. When acting as a transmitter, an alternating voltage is applied between the membrane and the fixed electrode, causing the membrane to vibrate and produce ultrasonic waves. When functioning as a receiver, incoming ultrasonic waves cause the membrane to vibrate, generating a corresponding electrical signal. The fact that CMUT structure can be varied and changed according to the application area offers the potential for enhanced sensitivity at a wide range of frequencies and makes it suitable for working at broadband frequencies compared to traditional piezoelectric transducers. Additionally, CMUT fabrication processes are compatible with integrated circuits (ICs), miniaturization, and complex array configurations, allowing them to be easily used in a variety of electronic systems [4].

CMUTs are well suited for a variety of medical applications, where high resolution and precise measurements are critical. For accurate diagnosis and treatment planning, it is crucial to have high-resolution image, due to the CMUTs having broad bandwidth and high sensitivity allowing them to be used in ultrasound imaging [5–7]. Additionally, CMUTs have found applications in intravascular imaging, where their small size and ability to operate at high frequencies make them ideal for imaging within the blood vessels [6–9]. Additionally, the low cost, small size, and environmental friendliness of CMUTs compared to traditional piezoelectric transducers make them a promising alternative for tumor treatments [10, 11]. These applications show the versatility of CMUT technology in addressing the specific needs of various biomedical applications.

After CMUT technology matured, researchers began to explore the potential of CMUTs in fields other than biomedical applications. For instance, CMUTs have been considered as humidity [12], and gas sensors [13,14]. The ability to fine-tune the frequency response and sensitivity of CMUTs through precise control of their fabrication processes makes them suitable for emerging applications.

One of the promising new applications of CMUT technology is SHM. SHM involves the continuous monitoring of large-scale civil infrastructures such as bridges, tunnels, pipelines, and railways to detect early signs of structural damage and prevent catastrophic failures [15]. Over time, infrastructures are subject to environmental stress, and other factors that can lead to structural damage. Early detection of such damage is crucial for ensuring the long-term integrity and safety of these structures. The importance of SHM cannot be overlooked, as these infrastructures are critical to public safety and economic stability [16].

One of the key methods used in SHM is the monitoring of Acoustic Emission (AE) signals. During events such as crack initiation, or material failure, any impact can cause the rapid release of localized strain energy within the structure, and this released energy generates AE signals [15–18]. AE signals can occur in a broad frequency range; to accurately detect and analyze the AE signal it is necessary to use sensors with high sensitivity and broad frequency capability. CMUTs are ideally suited for AE signal detection in SHM applications with their broad bandwidth and high sensitivity [19].

Despite the significant potential of CMUTs in SHM, their adoption in this field has been relatively recent, compared to their more established use in medical applications. One of the first CMUTs specifically designed for SHM was developed around 2003 [20].The success of these initial designs to detect AE signals led to further research and development of CMUTs in SHM. Over the past decade, significant advancements have been made in CMUT design, fabrication, and electronic integration to improve their performance as AE sensors [20]. In 2006, Ozevin et al. [21] demonstrated the potential of capacitive-type vibration transducers for AE signal detection. When the results were compared to the commercially available piezoelectric transducers, signal-to-noise ratios were lower [21]. Additionally, Saboonchi et al. developed CMUTs with improved signal-to-noise ratios and these results make CMUTs more competitive with traditional AE sensors [22].

While CMUTs have shown significant promise in detecting AE signals for SHM, there are notable challenges when applying these devices in real-world

environments. Most of the previous studies on CMUTs have been conducted under well-controlled experimental conditions. CMUTs have demonstrated good performance in detecting AE signals in ideal settings. However, in practical applications, the environment is often far from controlled, with various external noise sources. This external noise can interfere with the detection process. The challenge, therefore, lies in effectively separating the relevant AE signals from the background noise to ensure accurate and reliable monitoring of structural integrity. To address these challenges, Lu et al. [23] introduced an innovative solution in the form of Phase-Reversal CMUT (PR-CMUT) devices. PR-CMUT design targets the issue of noise interference by using a phase-reversal technique. In this PR-CMUT method, the phase of the current in one CMUT device is reversed relative to another CMUT device, creating a stopband that effectively suppresses the noise while maintaining a flat passband for broadband sensing.

The primary objective of this thesis study is to develop microfabrication processes (both unit processes and integration processes) to microfabricate PR-CMUT devices using microfabrication techniques available at our cleanroom facilities at Bilkent University UNAM. We aimed to make significant process development advancements towards bridging the gap between theoretical design and practical implementation for real-world applications of PR-CMUT devices.

The design and modeling part of the PR-CMUT devices presented in this thesis study are strongly based on the studies presented by Lu et al [23]. Furthermore, in this thesis study, which is focused on the development of processes for the microfabrication of PR-CMUT devices, the theoretical design and modeling efforts are performed by our collaborators from Institute of Ultrasonic Testing at Jiangsu University and State Key Laboratory of Dynamic Testing Technology at North University of China. During the modeling of the PR-CMUT devices for manufacturability, we collaboratively worked to set the geometrical dimensions of the PR-CMUT devices that we can microfabricate at our cleanroom facilities at Bilkent University UNAM. Other than the selection of the geometrical dimensions for manufacturability, the rest of the PR-CMUT device modeling studies are performed by our collaborators, and are "given" to our microfabrication studies in this thesis.

In addition to the development of microfabrication processes (both unit processes and integration processes) to fabricate PR-CMUT devices, this thesis also explores the dynamic characterization of CMUT devices using the ZYGO Optical Profilometer that is available at our cleanroom facility. This advanced characterization technique allows for precise measurement of the displacements of CMUT devices, while the membrane of the CMUT device is in dynamic motion. With this ability especially the resonance frequency of the CMUT devices can be observed.

This thesis is structured as follows: Chapter 2 very briefly explains the modeling approach behind PR-CMUT devices. Furthermore, Chapter 2, in detail discusses the selection of appropriate materials, layout mask design, and the precautions taken during the design process. Chapter 3 focuses heavily on the experimental aspects of the study, detailing the microfabrication of PR-CMUT devices in our cleanroom. Chapter 4 presents the dynamic characterization of other, already microfabricated, circular membrane CMUT devices using the ZYGO Optical Profilometer, including measurements of resonance frequency and membrane displacement. Finally, Chapter 5 concludes the thesis by summarizing the findings and discussing potential directions for future research related to both PR-CMUT realization and dynamic characterization using ZYGO Optical Profilometer.

Chapter 2

Theory

SHM is a critical area of research aimed at ensuring the safety and longevity of civil infrastructures, such as bridges, pipelines, and railways [15]. Real-time structural damage detection and assessment is essential to prevent catastrophic failures and minimize maintenance costs [24, 25]. Capacitive Micromachined Ultrasonic Transducers (CMUTs) have become highly promising devices in this field, due to their broad frequency range AE signal detection capability, which makes them ideal for SHM applications [26, 27].

Traditional CMUT designs often face challenges related to noise interference and limited bandwidth, which can negatively affect their effectiveness in real-world monitoring scenarios [15]. Recent work has focused on creating broadband CMUTs with improved noise rejection capabilities to address these issues shown in Figure 2.1 [23].

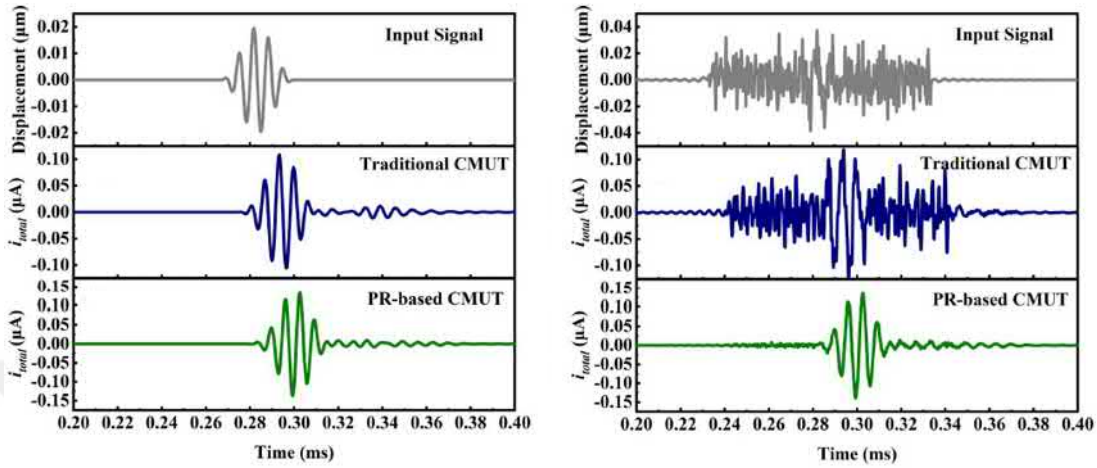


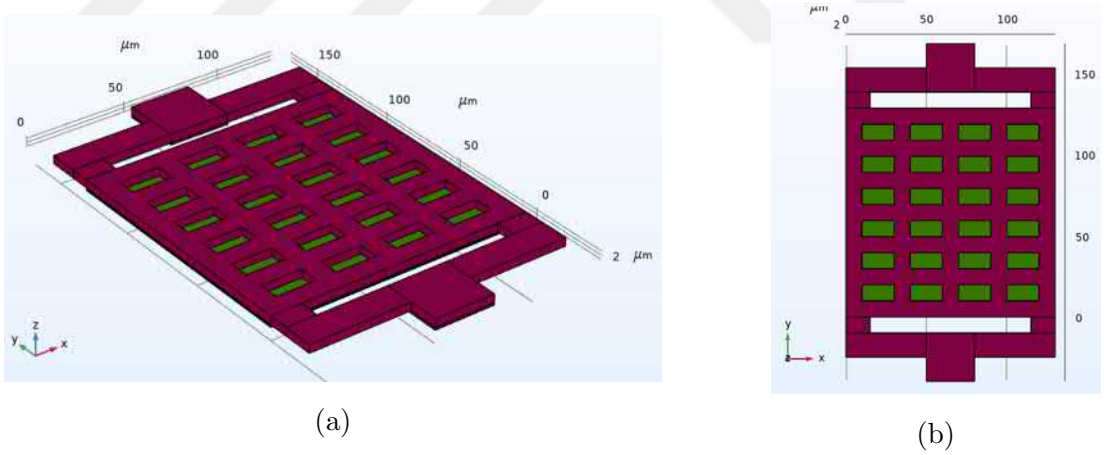
Figure 2.1: Comparison between traditional CMUT and PR-CMUT: (a) without noise in the input signal and (b) with noise in the input signal (will be asked for use permission from the publisher before the thesis is finalized.)

This thesis builds upon the innovative work of Lu et al. [23], who introduced a PR-CMUT designed specifically to improve noise rejection while maintaining a flat passband for effective broadband sensing. The phase-reversal technique reverses the phase of the current in one CMUT device with respect to the other, thus creating a stopband and filtering out unwanted noise. With this method, the accuracy and clarity of the signal to be detected are enhanced [23].

In the following sections of this chapter, theoretical foundations, detailed design considerations and simulation results about PR-CMUT will be discussed. Then, microfabrication steps planned for production, material selection and mask design will be included.

2.1 Simulation and Mask Design

Previously published work presented by the team we collaborated with, a PR-CMUT was developed and optimized for broadband sensitivity in the 40.8 kHz to 50 kHz frequency range using a genetic algorithm. That study demonstrated the effectiveness of the phase-reversal mechanism in enhancing noise rejection while maintaining consistent sensitivity [23]. Building on these findings, our current work aims to apply this technique to higher frequency ranges, specifically 200-250 kHz and 200-300 kHz. The goal is to design and microfabricate PR-CMUT devices that operate effectively within these frequency bands. Simulation techniques and optimization processes were adapted to target our specific frequency range by our collaborators. Figure 2.2 shows the overview of the PR-CMUT structure planned for microfabrication.



(a) (b)

Figure 2.2: Overview of PR-CMUT devices: (a) side view and (b) top view[1].

[1]This image is obtained from the efforts of the research group of Assoc. Prof. Sai Zhang who is affiliated with Institute of Ultrasonic Testing, Jiangsu University, Zhenjiang, 212013, China, and State Key Laboratory of Dynamic Testing Technology, North University of China, Taiyuan, 030051, China. The image is used with permission from Assoc. Prof. Sai Zhang.

At this stage, progress was performed by being in continuous communication with the collaborating computational and theoretical design team and exchanging feedback with each other especially about geometrical dimensions of PR CMUT MEMS devices that may be manufacturable with the capabilities in our cleanroom facilities at Bilkent University UNAM. First of all, the selection of the materials to be used and the limit of material thicknesses within the available possibilities of our cleanroom were decided.

In this section, general information will be given about simulation (briefly) and mask design (in detail). Details about material selection will be given in the next sections, but for better understanding, the materials that are used are mentioned within this section.

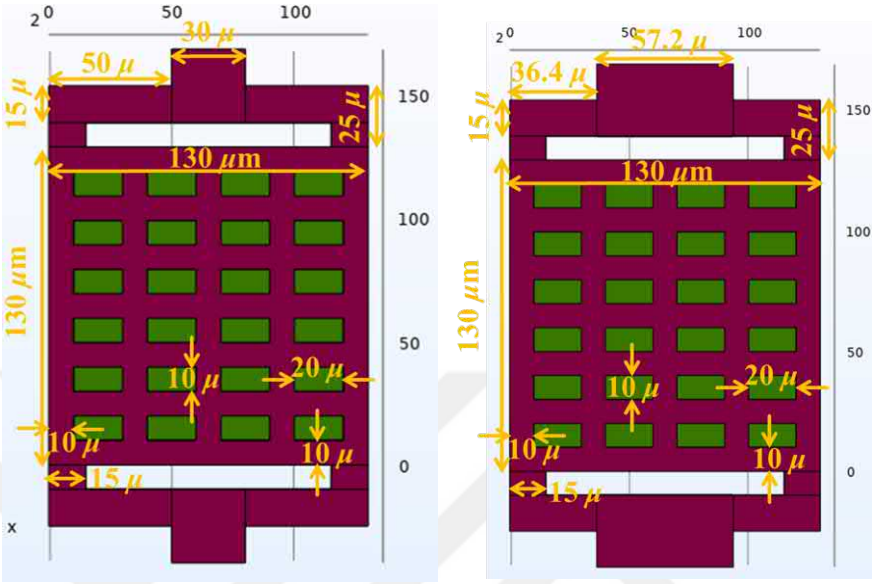
It was decided to use chromium (Cr) as an adhesion layer for the bottom electrode and to deposit gold (Au) on top of the Cr layer. It was decided that the total bottom electrode thickness would be 500nm to able to do good quality wire bonding. It was aimed to use HfO_2 as a dielectric layer on top of bottom electrode to avoid any short. Since the HfO_2 deposition study has never been tried before by our group with e-beam evaporation technique, this experiment was conducted, in order to understand our limitations. While determining the thickness, this study was done and previously a low-rate deposition was made with e-beam up to 150nm and after it was verified that this was possible. This range was presented to the team we collaborated with, with a minimum thickness of 50nm and a maximum thickness of 150nm. The reason for the lowest thickness being 50nm is that there is a pinhole effect at low thicknesses and the breakdown voltage may decrease due to these pinholes. As a result of the simulations made by the team we collaborated with, it was decided that 150nm would be suitable.

It was decided to use Poly-Si as the sacrificial layer to form the gap between the top and bottom electrodes. Here again, since it was not tested how much Poly-Si could be deposited with the e-beam evaporation technique, this study was also carried out by us. It was reported to the team we collaborated that we could deposit up to a maximum of 1 μm. It was stated that our preference here was for the lowest possible thicknesses. The reason for requesting a low

thickness here is that the capacitance will increase with the decrease in the gap height and thus the device area can be reduced. As a result of simulation studies conducted by our collaboration team, although a larger cell capacitance can be obtained by reducing the gap height, air damping would increase sharply as the gap height decreases due to the incompressibility of air at the microscopic level. A PR-CMUT cell with a gap height of less than 400 nm was attempted to be designed by our collaborators; however, the obtained quality factor was very poor (about 2-3). Due to these concerns, the gap height was increased to 600 nm, and the quality factor was improved to 5. It was decided that this quality factor was sufficient for the preliminary design. After the first fabrication was completed, it was decided that the deficiencies would be eliminated, and simulations would be done to increase the quality factor as future studies.

Finally, the material selection, thickness and design of the top membrane were studied. It was decided to use copper (Cu) as the material for top membrane. As a result of the simulations, it was concluded that a thick Cu membrane was required. Since the Cu membrane is planned to be patterned with the lift-off method, the most important factor in determining the Cu thickness is the thickness of the photoresist to be used. As a result of our studies, it has been concluded that we can deposit Cu up to 4 μm.

Simulations were performed by our collaborators in the light of this information. It was decided that there would be 4 different regions planned for microfabrication. The first region consisted of devices that were expected to resonate only at a certain frequency of 200 kHz. The second region, similar to the first region, consists of devices that will only resonate at 250 kHz. The purpose of these two areas here is to try to understand our manufacturing process and to produce CMUT devices with a specific resonance. It is also aimed to characterize these devices to investigate the behavior of CMUT chips with a specific resonance frequency. The structure and dimensions of the devices belonging to the first and second regions are given in Figure 2.3a and 2.3b.



(a) (b)

Figure 2.3: Structure and dimensions of the PR-CMUT cells: (a) for the first region and (b) for the second region[2].

In the third region, there are two different CMUT cells with different resonance frequencies to achieve broadband frequency range of 200-250 kHz. The resonance frequency of one of these different PR-CMUT cells is 200 kHz and the other is 250 kHz. The CMUT structures to be used in region 3 consist of combinations of the devices in region 1 and region 2 in Figure 2.3.

The targeted frequency range for region 4 is 200-300 kHz. There are 4 different PR-CMUT structures to be used to obtain broadband frequency in this range. The resonance frequencies of the devices to be used in this region are 200 kHz, 276.3 kHz, 226.5 kHz, and 300 kHz, respectively. Region 4 consists of the combination of these structures. Figure 2.4 show the dimensions of these different PR-CMUT cells.

[2]This image is obtained from the efforts of the research group of Assoc. Prof. Sai Zhang who is affiliated with Institute of Ultrasonic Testing, Jiangsu University, Zhenjiang, 212013, China, and State Key Laboratory of Dynamic Testing Technology, North University of China, Taiyuan, 030051, China. The image is used with permission from Assoc. Prof. Sai Zhang.

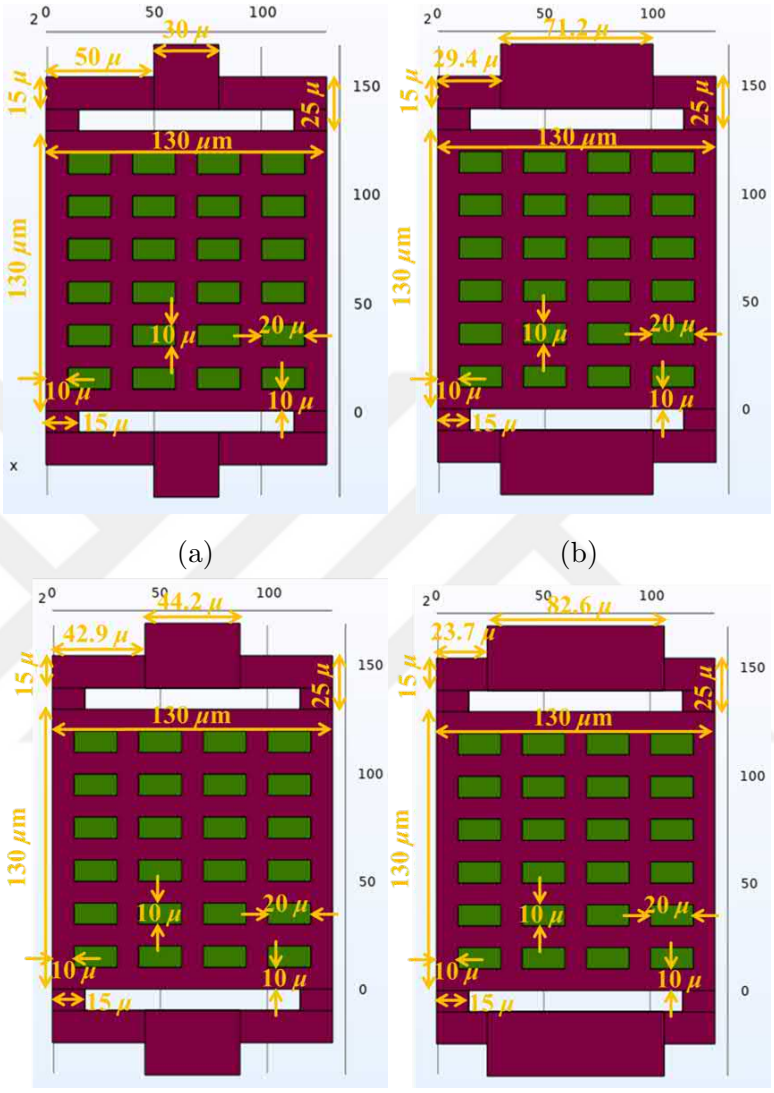
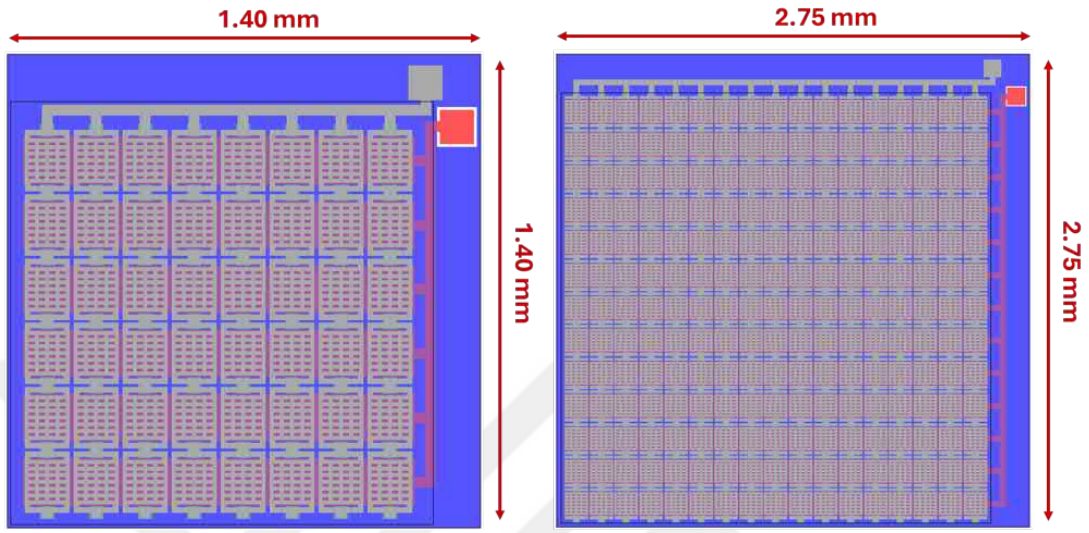


Figure 2.4: Illustration of the dimensions of the four different CMUT structures designed to achieve a broadband frequency range of 200-300 kHz in Region 4. The resonance frequencies of these devices are (a) 200 kHz, (b) 276.3 kHz, (c) 226.5 kHz, and (d) 300 kHz, respectively[3]

[3]This image is obtained from the efforts of the research group of Assoc. Prof. Sai Zhang who is affiliated with Institute of Ultrasonic Testing, Jiangsu University, Zhenjiang, 212013, China, and State Key Laboratory of Dynamic Testing Technology, North University of China, Taiyuan, 030051, China. The image is used with permission from Assoc. Prof. Sai Zhang.

After the devices in each region were designed, the dimensions of these regions were determined. Our collaborators provided crucial insights for detecting ultrasonic-guided waves, emphasizing the importance of considering the wavelength (λ) of the waves. For example, they highlighted that in an aluminum plate with a thickness of 3 mm, the A0 and S0 Lamb waves at a frequency of 200 kHz have wavelengths of 10 mm and 26.7 mm, respectively. According to their theoretical analysis, the overall dimensions of the detection area should not exceed $\lambda/8$. Therefore, for detecting A0 waves at 200 kHz, they recommend that the total dimensions of Region I be less than 1.25 mm $\times$ 1.25 mm. If this area is considered too small, a maximum area of 2.5 mm $\times$ 2.5 mm could also be acceptable. They further provided evaluations for other regions, suggesting dimensions of 1 mm $\times$ 1 mm for Region II (with a maximum allowable area of 2.1 mm $\times$ 2.1 mm), 1 mm $\times$ 1 mm for Region III (with a maximum allowable area of 2.1 mm $\times$ 2.1 mm), and 0.9 mm $\times$ 0.9 mm for Region IV (with a maximum allowable area of 1.88 mm $\times$ 1.88 mm). Our collaborators emphasized that CMUT cells should be densely arranged within each of these regions to enhance sensitivity. To enable phase-reversal formation in the upper membranes, a voltage of -18 VDC and 18 VDC will be applied, while the bottom electrodes will be grounded at 0 V.

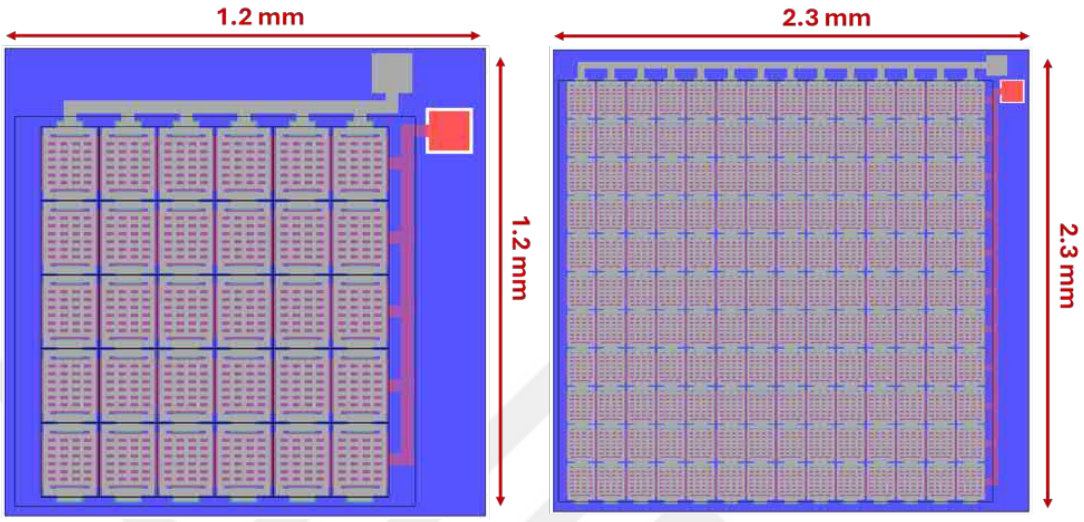
With the help of genetic algorithm, our collaboration team calculated the ratios of different structures in the regions in a way that optimizes sensitivity and shared this with us. According to the genetic algorithm result, the ratio between the 200 kHz and 250 kHz CMUT structures in the 3rd region is 13 to 11. The cell number can be increased by the relation of $N_1/N_2 = 13/11$. In the 4th region, the CMUT cells with resonance frequencies of 200 kHz (N_1), 276.3 kHz (N_2), 226.5 kHz (N_3), and 300 kHz (N_4) have corresponding ratios of $N_1 = 9$, $N_2 = 3$, $N_3 = 3$, and $N_4 = 6$, respectively. Considering the information provided to us by our collaborators, individual chip designs were first made for each region. While designing masks, 2 different designs were made for the minimum and maximum field sizes for each region. In all regions, the areas where the devices are located are designed to comply with the given conditions. Figure 2.5 includes the individual chip design of the minimum and maximum areas of the first region.



(a) (b)

Figure 2.5: Individual chip design of the minimum and maximum areas of the first region: (a) minimum area and (b) maximum area

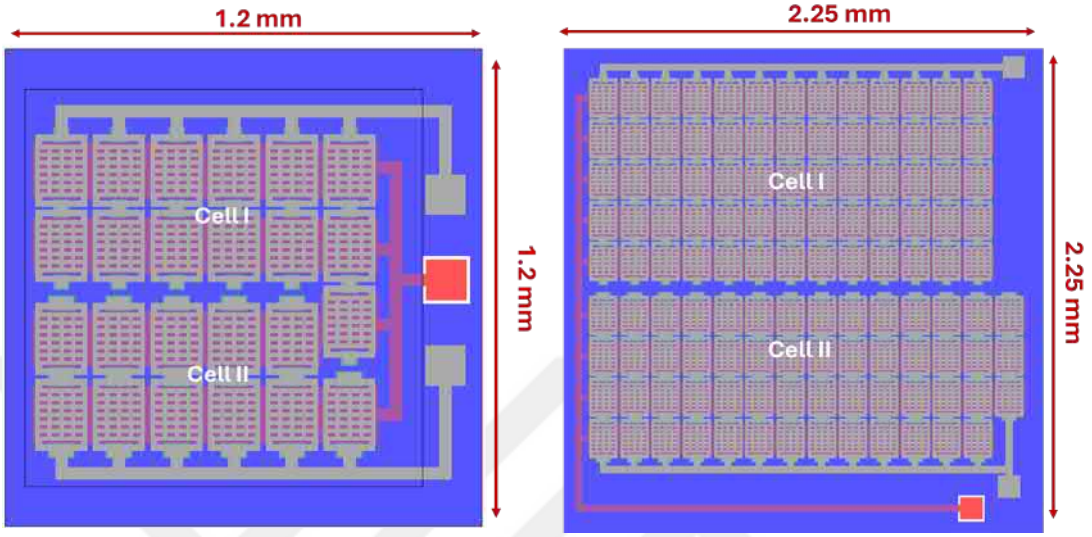
While making these designs, an attempt was made to create a structure as dense as possible. The minimum area chip design (primary design area) for the first region contains 48 cells, and the chip design for the maximum area (secondary design area) contains 221 cells. Primary and secondary design areas of the 2nd region are included in Figure 2.6. The primary design area consists of 30 cells and the secondary design area consists of 154 cells.



(a) (b)

Figure 2.6: Individual chip design of the minimum and maximum areas of the second region: (a) minimum area and (b) maximum area

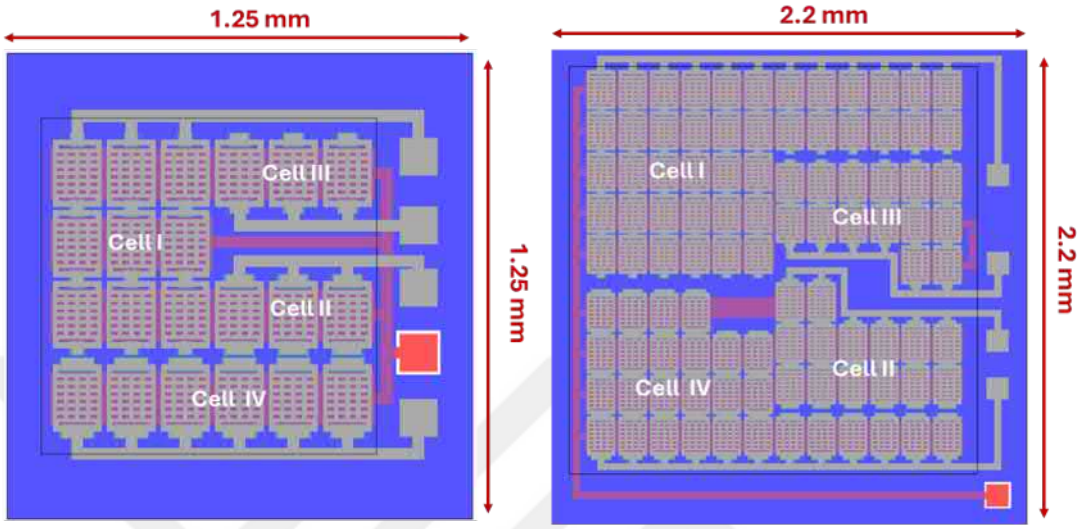
2.7 presents the primary and secondary area designs formed by the configurations of two different CMUT cells in the 3rd region. The primary design area includes 13 of Cell 1 and 11 of Cell 2, while the secondary area consists of 65 of Cell 1 and 55 of Cell 2.



(a) (b)

Figure 2.7: Individual chip design of the minimum and maximum areas of the third region: (a) minimum area and (b) maximum area

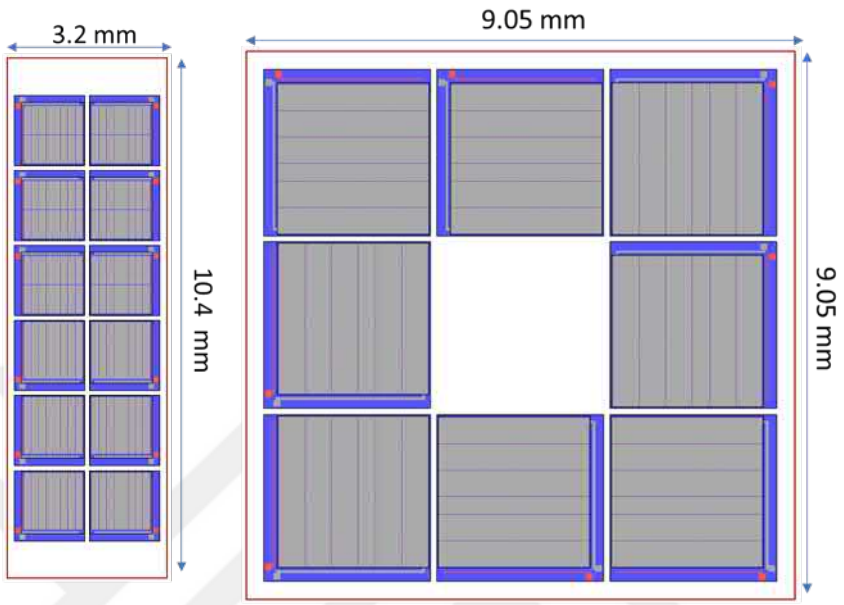
Finally, the designs for the 4th region primary and secondary areas are included in the Figure 2.8. Figure 2.8 presents the primary and secondary area designs formed by the configurations of four different CMUT cells in the 4th region. The primary design area includes 9 of Cell 1, 3 of Cell 2, 3 of Cell 3 and 6 of Cell 4, while the secondary area consists of 52 of Cell 1, 14 of Cell 2, 14 of Cell 3 and 28 of Cell 4.



(a) (b)

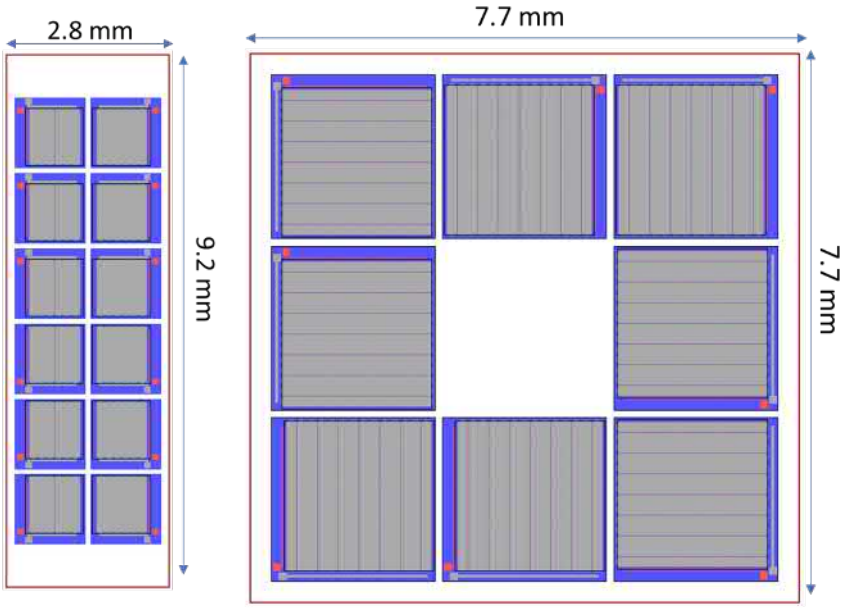
Figure 2.8: Individual chip design of the minimum and maximum areas of the fourth region: (a) minimum area and (b) maximum area

After the individual chip designs of different regions were completed, the wafer scale design was started. Here, in order to avoid difficulties in handling and problems during the dicing, these individual chips were brought together and grouped. The Figures 2.9-2.12 below show the dimensions of individual chips belonging to these groups. The layout of these chips on the wafer is shown in Figure 2.13 and 2.14.



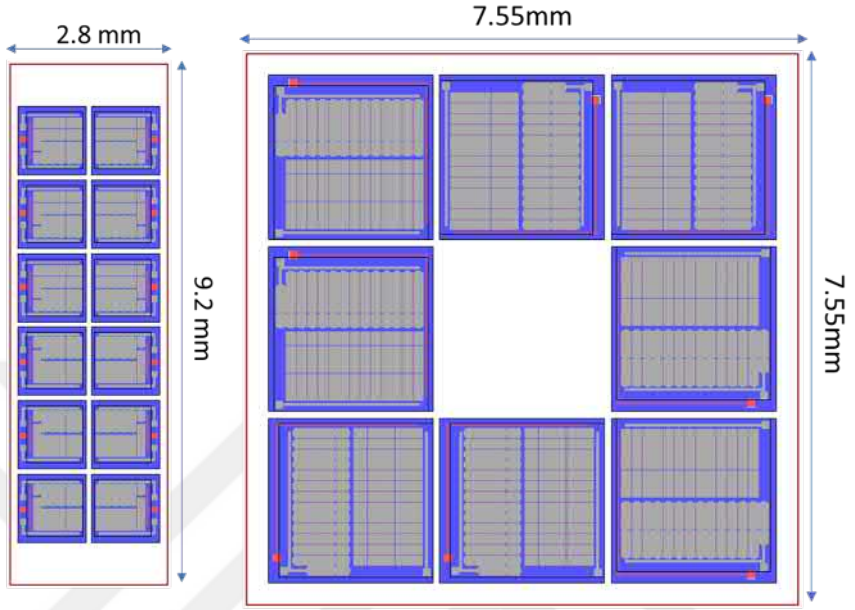
(a) (b)

Figure 2.9: Arrangements and dimensions of individual chips for primary and secondary design of first region groups



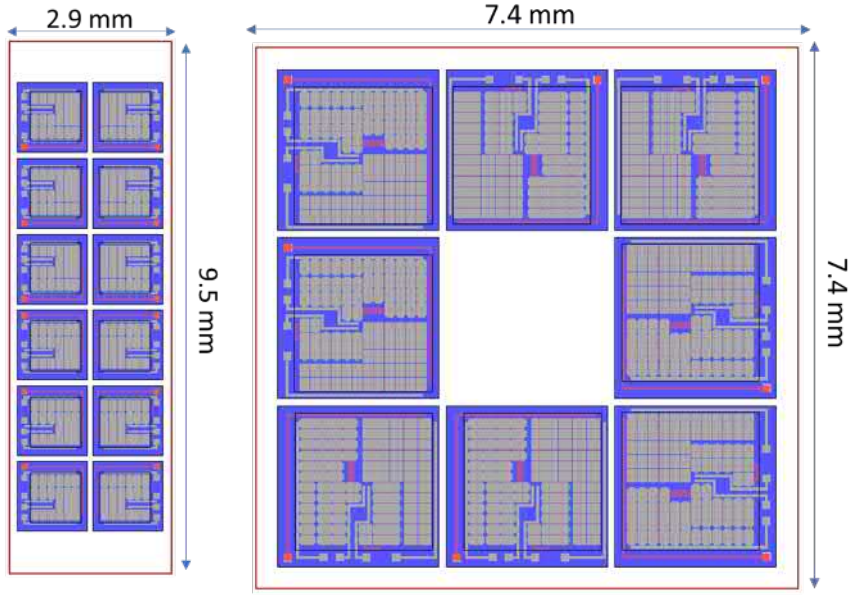
(a) (b)

Figure 2.10: Arrangements and dimensions of individual chips for primary and secondary design of second region groups



(a) (b)

Figure 2.11: Arrangements and dimensions of individual chips for primary and secondary design of third region groups



(a) (b)

Figure 2.12: Arrangements and dimensions of individual chips for primary and secondary design of fourth region groups

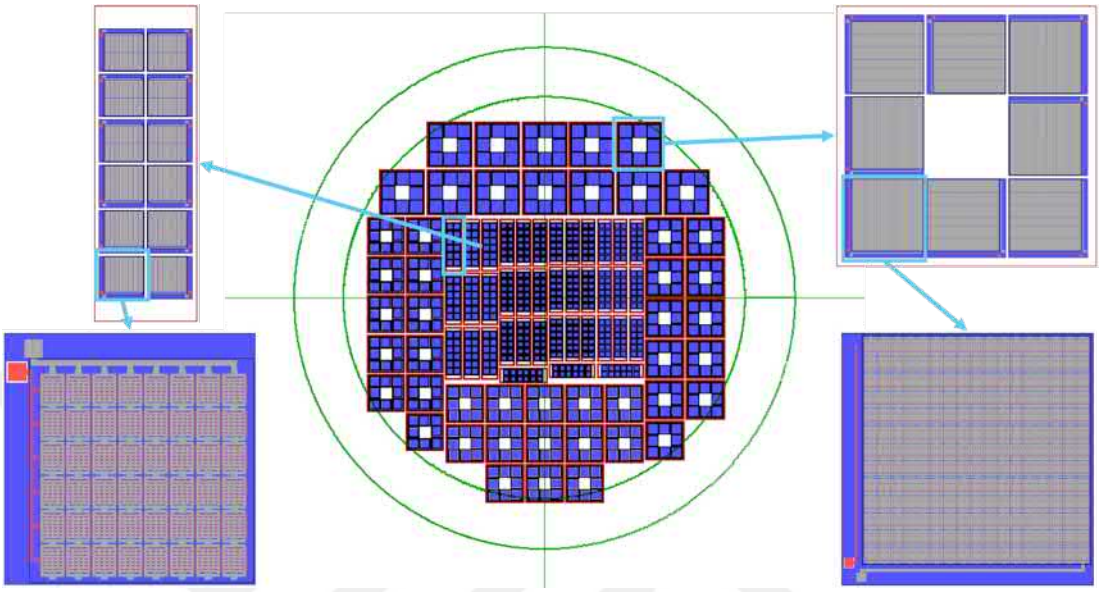


Figure 2.13: Layout of the chips

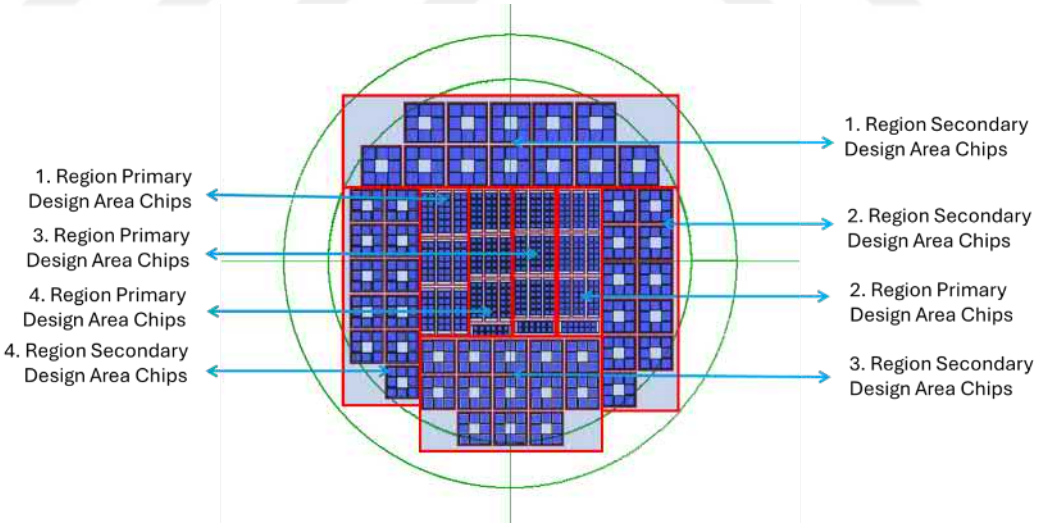


Figure 2.14: Layout of different areas on the wafer

2.2 Material Selection, Mask and Microfabrication Process Design

The materials to be used for the fabrication of PR-CMUT devices, as well as the mask design and process steps, were carefully considered with multiple factors in mind. This section will cover the details regarding these aspects. The proposed microfabrication flowchart is shown schematically below in Figure 2.15. This representation is a rough schematic, created solely for understanding the steps and materials involved.

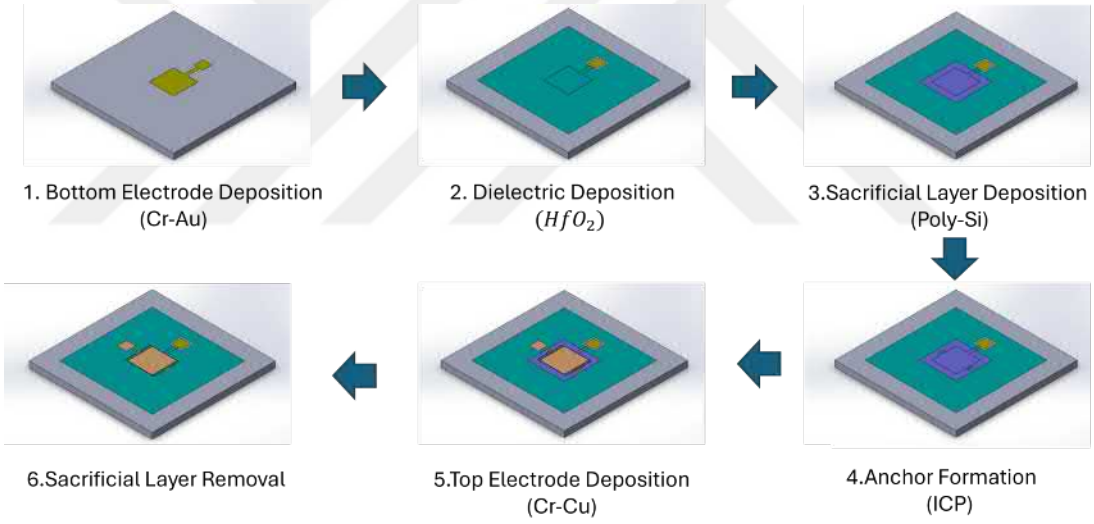


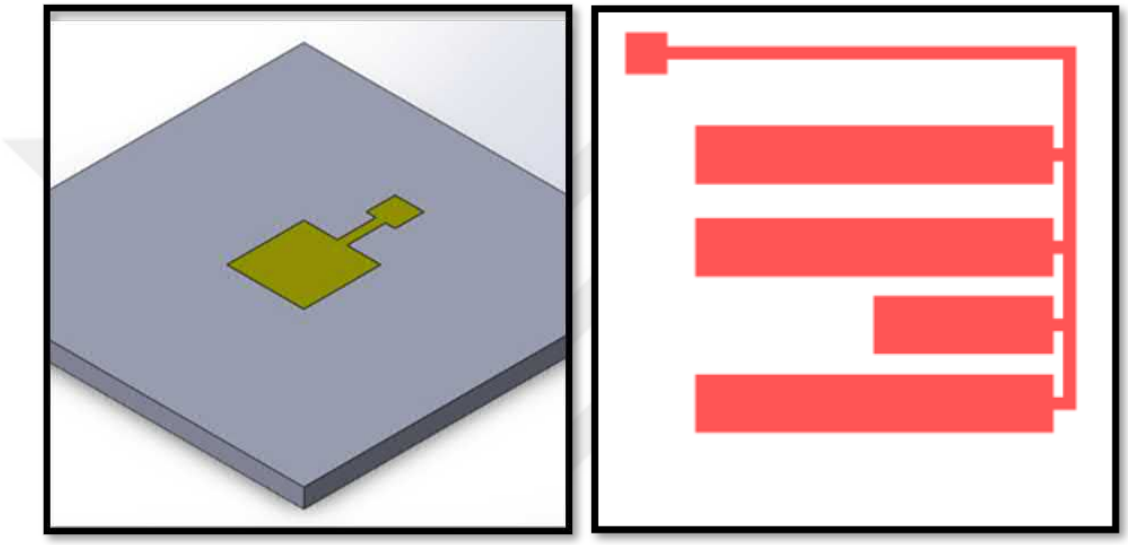
Figure 2.15: Proposed microfabrication flowchart

For the bottom electrode of the CMUT, a combination of Chromium (Cr) and Gold (Au) has been selected, with a thickness of 50 nm for Cr and 450 nm for Au. Chromium is deposited here as an adhesion layer between Pyrex and gold. Cr provides excellent adhesion properties, which is critical for the stability and reliability of the bottom electrode. It will also ensure stability during the fabrication of the device in other steps [28,29]. The main reasons for choosing gold are its high electrical conductivity and chemical stability. Gold minimizes resistive losses and ensures efficient signal transduction. These features are particularly important in this study to maintain the sensitivity.

Based on the requirements for successful wire bonding, the precise thicknesses of 50 nm for Cr and 450 nm for Au were chosen. Previous work has shown that a minimum 400-500 nm thickness of the gold layer is necessary for successful wire bonding, which is the process of connecting the CMUT to external pads. This ensures a reliable and robust connection, which is necessary for the device to operate correctly.

It was decided to use e-beam evaporation technique for the deposition of these materials. With this technique, Cr and Au thickness and uniformity can be controlled. Thus, high-quality deposition required in CMUT production can be obtained. It is planned to use an image-reversal photoresist to create patterns related to the bottom electrode, then to deposit the bottom electrode with e-beam, and then to apply the lift-off technique with the help of acetone. This method is particularly effective when working with the thin layers and high-resolution features needed in the microfabrication of CMUTs.

For this purpose, schematic representation of bottom electrode and the drawing of the pattern in a particular area of the mask prepared for the bottom electrode is shown in Figure 2.16. All of the bottom electrodes are connected to each other as they will be ground.

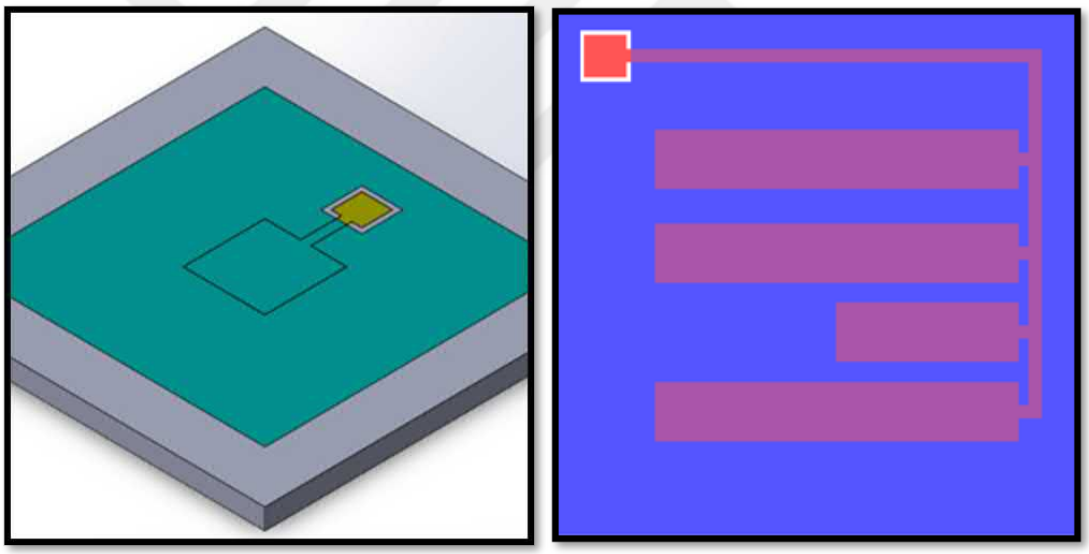


(a) (b)

Figure 2.16: Bottom electrode formation: (a) schematic representation (b) mask design

For the dielectric layer, hafnium dioxide (HfO_2) has been selected due to its high dielectric constant, which is crucial for achieving significant capacitance in a compact CMUT design. Typically, HfO_2 is deposited using Atomic Layer Deposition (ALD) due to its ability to produce highly conformable and uniform films with precise thickness control [30]. However, in this project, e-beam evaporation was chosen for HfO_2 deposition. This decision was made because e-beam evaporation offers cheaper, simpler, and faster alternative to ALD, resulting in a more cost-effective and faster fabrication process [31]. In this way, we use HfO_2 deposited via e-beam evaporation as a platform to explore and understand the behavior of the material in this application. This approach allows us to evaluate the suitability of e-beam deposited HfO_2 for future CMUT designs while maintaining the performance characteristics required for our current device.

By choosing HfO_2 and experimenting with e-beam deposition, we aim to strike a balance between performance and fabrication efficiency, while also gaining valuable insights into alternative deposition techniques for dielectric layers in CMUTs. The thickness of the HfO_2 layer is planned to be 150 nm. The patterning of the HfO_2 layer will be achieved using the lift-off technique. Similar to the bottom electrode, first the pattern parts will be determined with an image reversal photoresist, then e-beam deposition will be made and after deposition, unnecessary materials will be removed from the surface with lift-off. The schematic representation of the dielectric layer and the photomask designed for creating the patterns to be deposited are also included in Figure 2.17.



(a) (b)

Figure 2.17: Dielectric layer formation : (a) schematic representation (b) mask design

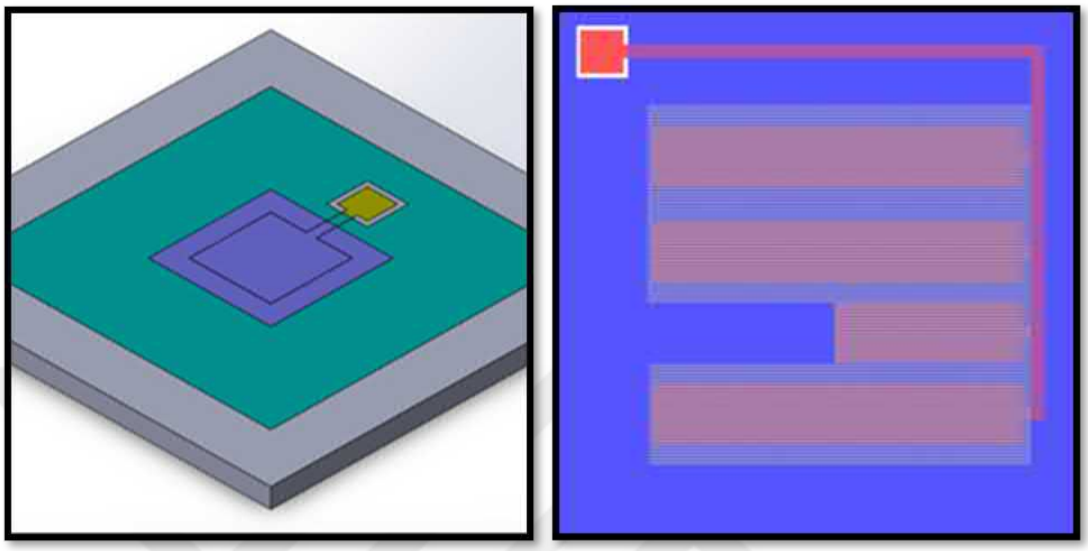
As can be seen from the mask design, the pad area of the bottom electrode is designed not to be covered with dielectric. The pad part is covered with photoresist to prevent it from being deposited. The reason for this is that an electrical connection will be made from these pads during the characterization of these devices.

Polycrystalline silicon (Poly-Si) has been selected as the sacrificial layer in the CMUT fabrication process. The main purpose of using the sacrificial layer method is to create the necessary gap between the membrane and the bottom electrode. First, Poly-Si will be patterned and deposited and then removed by the gas phase dry etching method in the final stages of device production.

Xenon Difluoride (XeF_2) gas phase dry etching process will be used to remove Poly-Si used as a sacrificial layer [32]. There are several reasons why gas phase dry etch is chosen instead of wet etch as the sacrificial layer release method. During and after wet etching, there is a significant risk of stiction, where the CMUT membranes might adhere to the substrate after the etching process. Due to this stiction, the devices cannot operate and the yield decreases [33]. When the etch process is done as gas phase dry etch with XeF_2, the possibility of stiction is greatly reduced and the overall yield of CMUT fabrication can be increased. Another advantage of preferring sacrificial layer release with XeF_2 is that XeF_2 is highly selective and suitable for isotropic etching for Pols-Si. Thus, after microfabrication, after all layers are deposited, it will be possible to etch Poly-Si without damaging previously deposited layers.

Poly-Si will be deposited as 600nm with e-beam evaporation. Following deposition, the lift-off technique will be used to pattern the Poly-Si layer. This method allows for accurate and clean patterning of the sacrificial layer, which is essential for the subsequent etching process to correctly form the gaps without damaging the surrounding structures.

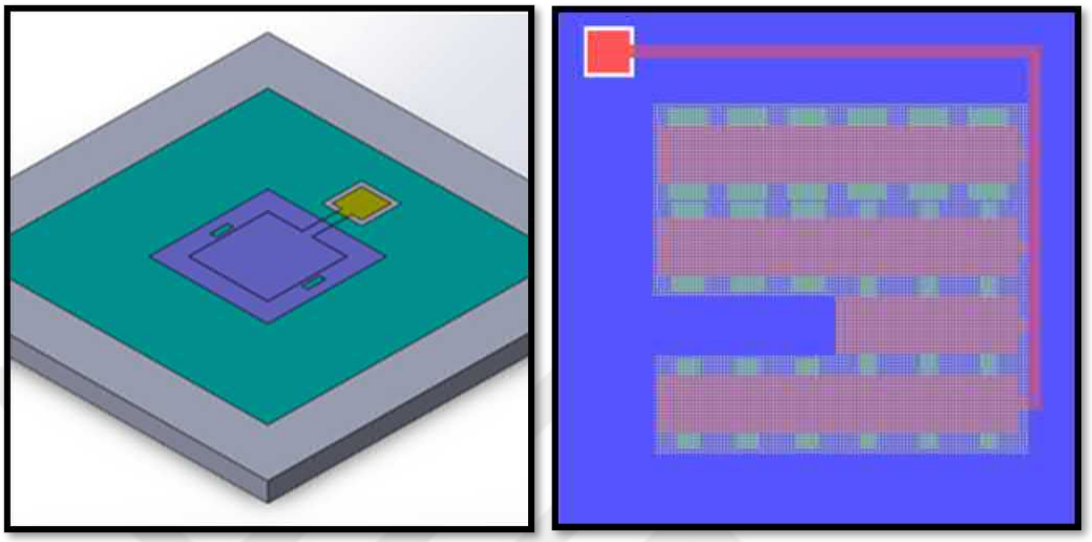
The schematic representation and mask design of the relevant Poly-Si coating is also included in Figure 2.18. One of the important points to consider when designing this mask is to keep the area to be coated with Poly-Si as small as possible, to reduce the amount of material to be used in the subsequent XeF_2 process and the etch time.



(a) (b)

Figure 2.18: Sacrificial layer formation : (a) schematic representation (b) mask design

The next step after this process is the formation of the anchors that will provide contact between the top membrane and the surface after Poly-Si etch. In this step, certain areas on the Poly-Si will be anisotropically etched with ICP tool etching to reach the dielectric layer underneath. In order to perform this process, the surface will be covered with a thick photoresist and after the photoresist process is completed, only the photoresist in the anchor areas to be etched will be removed and Poly-Si access will be provided. The schematic representation and mask design of the relevant anchor formation process included in Figure 2.19.

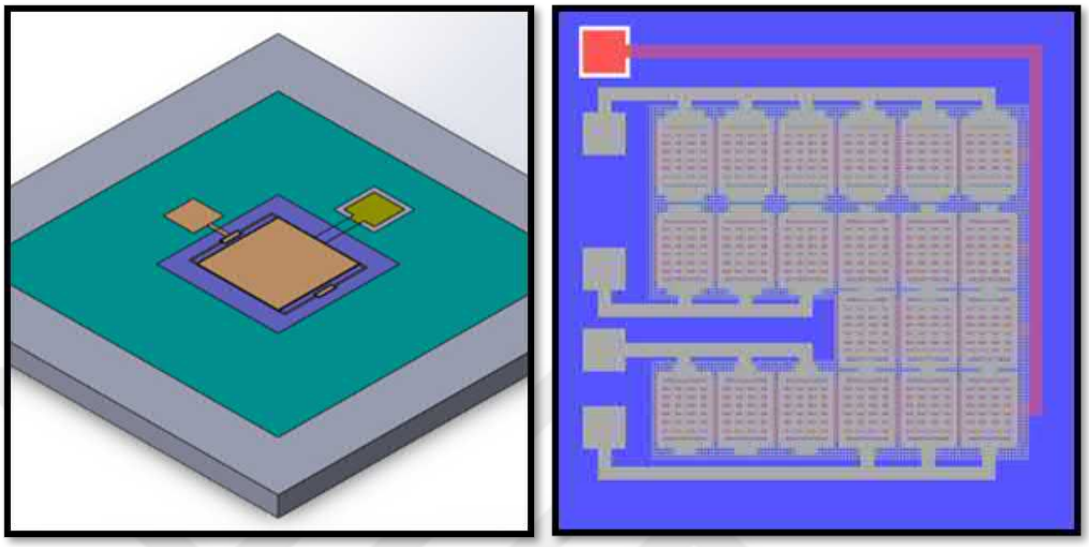


(a) (b)

Figure 2.19: Anchor formation : (a) schematic representation (b) mask design

For the top membrane of the CMUT, Copper (Cu) has been chosen as the material. The selection of Cu is primarily driven by its cost-effectiveness, excellent electrical conductivity, and high etch resistance to XeF_2. Copper is significantly less expensive than other conductive materials like gold or platinum, making it a practical choice for large-scale fabrication without compromising performance. In CMUT devices, the membrane is usually made with a non-conductive material and then a conductive material is deposited to form the upper electrode. Here, copper acts as both the membrane and the top electrode.

In addition to its electrical properties, Cu is also relatively easy to deposit using various techniques, making it a versatile choice for the top membrane. The deposition of the Cu membrane will be carried out using e-beam evaporation and the total thickness of the membrane will be 4 μm. E-beam evaporation was chosen as a deposition method against electroplating due to precise control over the thickness and uniformity of the deposited layer. While designing the top membrane mask, gaps were created on the membrane with a through hole to allow air to escape easily while the CMUT device is operating. The schematic and mask design of the upper membrane are shown in Figure 2.20.



(a) (b)

Figure 2.20: Top membrane and top electrode formation : (a) schematic representation (b) mask design

2.3 Fabrication Limitations and Design Considerations

During the design stages of the mask design and fabrication process, some limitations and considerations were taken into account for the successful fabrication and production of PR-CMUT. First of all, the placement of the devices on the wafer was taken into consideration. At this stage, during the mask design, all devices were placed in the mask, leaving approximately 1 cm of space from the edges of the wafer. The first reason for giving this margin here is to ensure that the edge beads that will be formed during the photoresist spin coating stage do not encounter the areas where the devices are located. These edge beads can lead to pattern distortion or loss if they extend into the active area of the wafer. Secondly, the 1cm gap leaves us space for handling during fabrication. This area allows for safe handling with tweezers or other tools during the fabrication process, without the risk of contaminating or damaging the active regions of the wafer. Wafer size and mask design for device designs are also included in Figure 2.21.

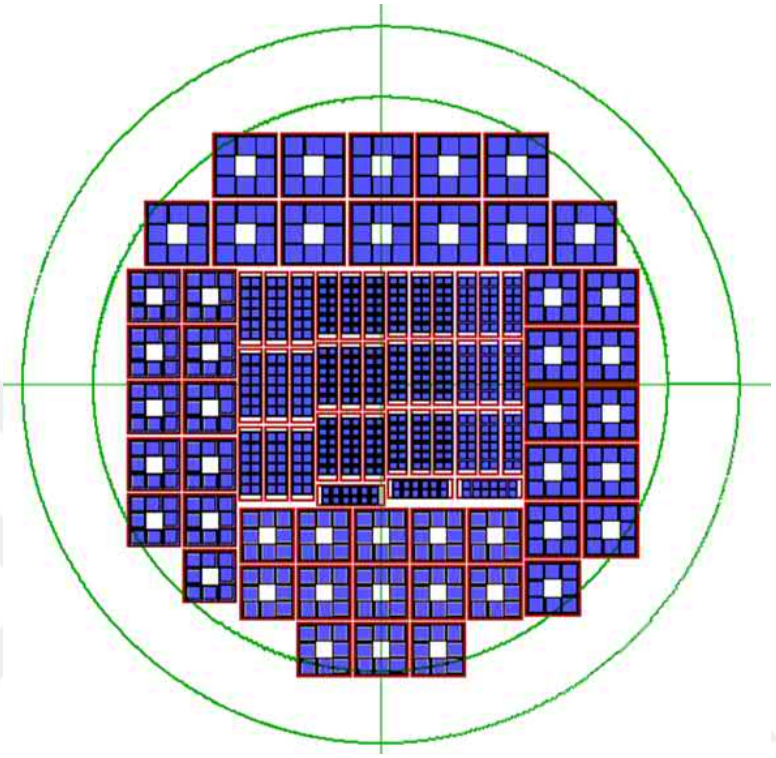


Figure 2.21: Mask desgin in wafer scale

Furthermore, the chips of 8 different design regions mentioned in the previous sections are not placed individually. The chips were grouped together during the design process. Although these chips will be individually evaluated after dicing, grouping them helps protect them from damage during the dicing process. Grouping also makes it easier to handle the chips with tweezers after dicing. Individual PR-CMUT chips have an area of only a few millimeters, making them very difficult to handle. By grouping the chips, not only is the risk of damage during dicing reduced but handling and characterization post-dicing also become more manageable. Figure 2.22 shows the grouping of the 4th region primary design area. As can be seen here, individual chips are too small to handle and there is a possibility that they may break off due to the water pressure during dicing. Therefore, it was decided that grouping them in this way would be easier to handle by dicing from the red lines. Additionally, at least 1 mm space left between each group for dicing.

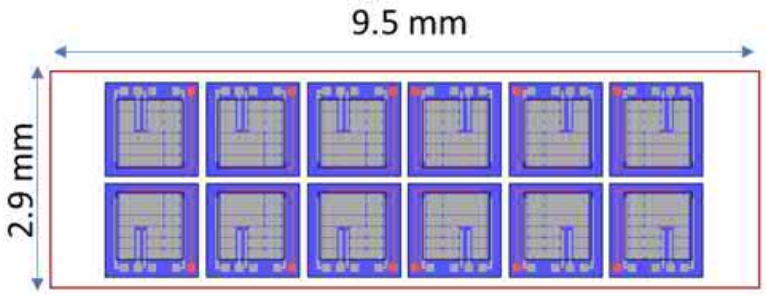


Figure 2.22: Grouping of the 4th region primary design area

Here, after the devices are grouped, the groups belonging to the primary design are positioned in a way that they are in the middle of the wafer. The reason for this is that this area will be coated more uniformly during deposition, that it will have a more reliable photoresist thickness during spin coating, and finally, to reduce the possibility of a possible damage and protect the primary designs as much as possible. Figure 2.23 shows the groupings of different regions.

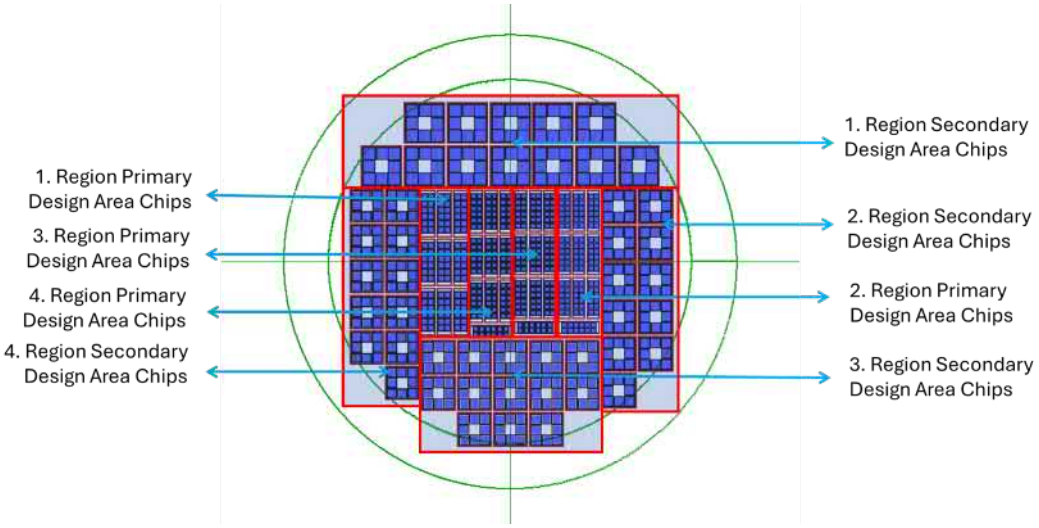
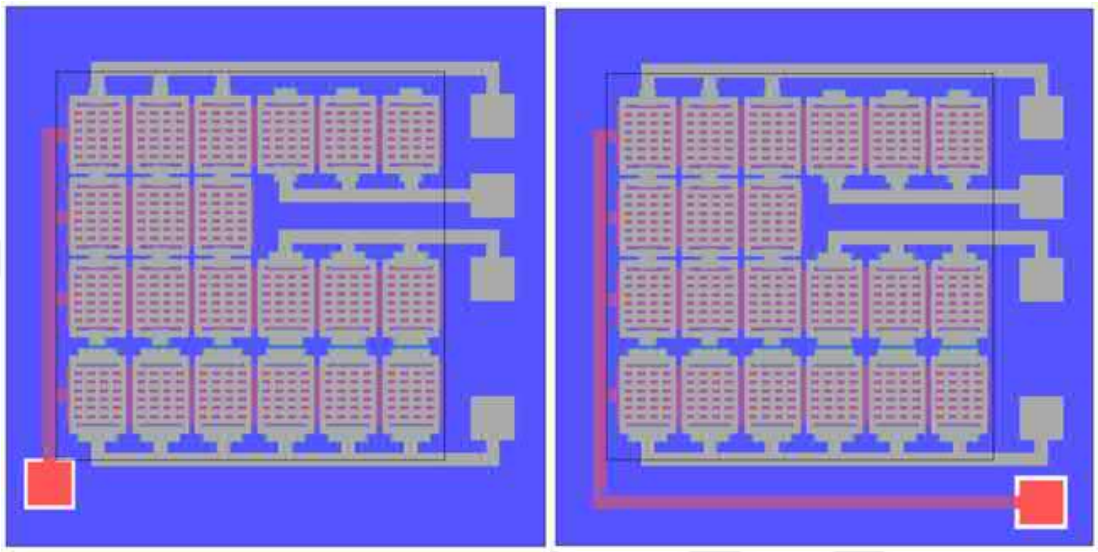


Figure 2.23: Overview of wafer scale mask design and different regions

In addition, when designing individual chips, care was taken to ensure that the pad sections were on the same edge. The reason for this was to make the connections to the PCB easier during the wire bonding process. Figure 2.24 show the old and new versions of 4th region primary design. In the old design in Figure

2.24a, it can be seen that the pads were placed on different edges, while in Figure 2.24b, they were changed so that they were all on the same edge.



(a) (b)

Figure 2.24: Mask design for 4th region primary design area : (a)old version (b)new version

Furthermore, when organizing the groupings, all chips were arranged in a way that their wire bonding pad areas were oriented toward the edges. This layout was specifically chosen to facilitate easier wire bonding during the later stages of fabrication. As can be seen in the mask design of the 4th region secondary design area in Figure 2.25, the pad parts of all the grouped individual chips are designed to be on the edges.

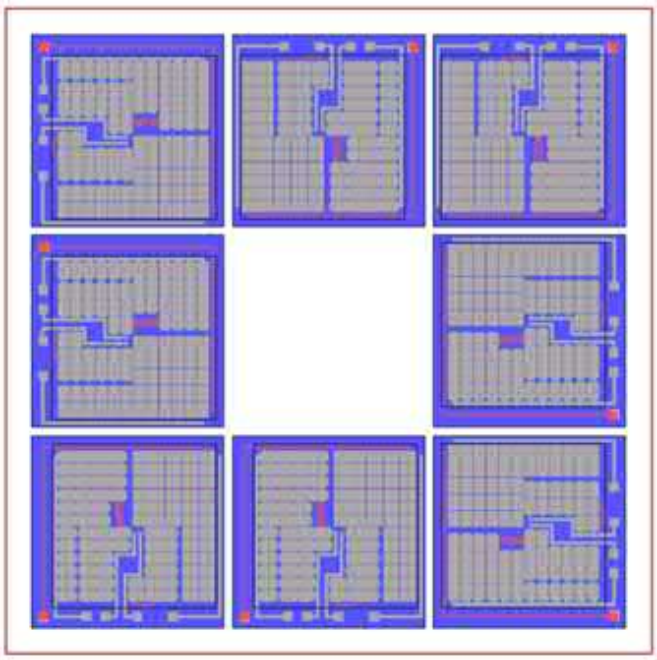
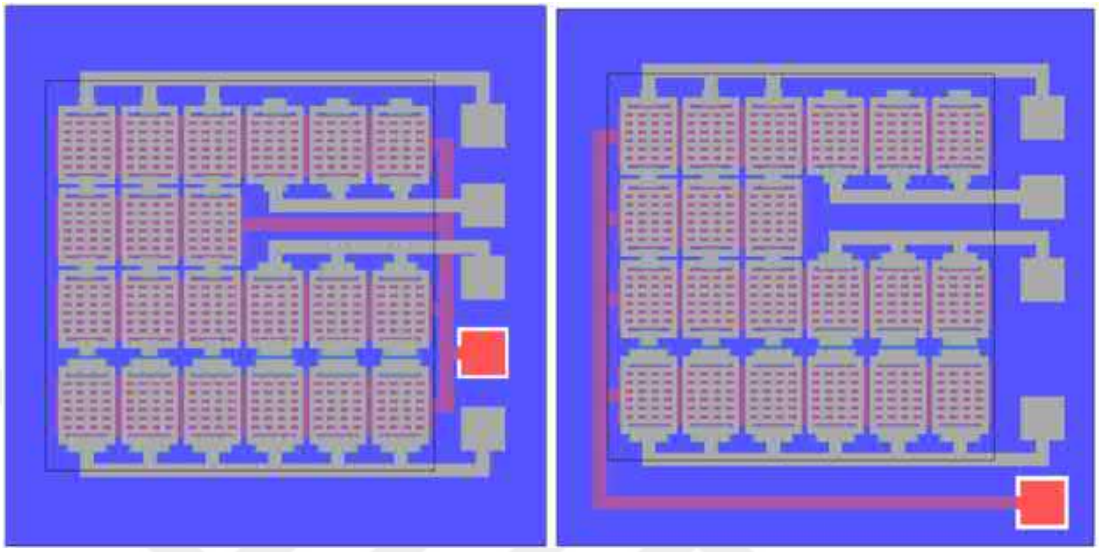


Figure 2.25: Mask design of the 4th region secondary design area grouping

When designing the chip, attention was paid to avoid overlapping the top and bottom electrode connections as much as possible. The primary goal of this design choice was to minimize parasitic effects, which can significantly impact the performance of the CMUT. By minimizing the overlap of electrode connections, the design reduces these parasitic interactions, thereby enhancing the overall performance and reliability of the CMUT. Figure 2.26a shows the old mask design made without considering the parasitic effects of the 4th region primary design, and Figure 2.26b shows the new mask design for the same region.



(a) (b)

Figure 2.26: 4th region primary design : (a) the old mask design, created without considering parasitic effects, and (b) the new mask design, incorporating parasitic effect considerations

Another critical consideration in the chip design was misalignment between different process masks. Due to the nature of microfabrication techniques that involve multiple process masks, some degree of misalignment between these masks is inevitable. Typically, while photolithography, misalignment inevitably occurs, with some areas experiencing up to 5 μm of misalignment, while other areas may have misalignment reduced to as low as 1 μm. Taking misalignment into account, margins were left in the masks. By designing with these margins, it was aimed to ensure that the critical features of the CMUT devices remain within acceptable tolerance levels, even if slight misalignments occur during fabrication. This precaution helps maintain the overall functionality and performance of the devices, despite the inevitable variations that can arise during the complex fabrication process. In Figure 2.27, representative images of possible misalignments are given in Figures 2.27a and 2.27b. In Figure 2.27c, a schematic representation of perfect alignment is given.

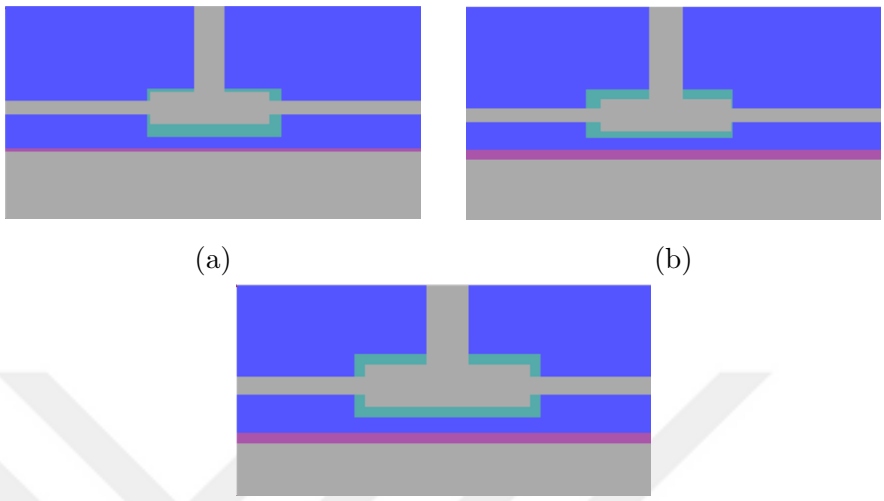


Figure 2.27: (a) and (b) possible misalignments; (c) perfect alignment

Another issue to be considered is that the 4 μm-thick copper during the deposition of the top membrane cannot be deposited with 90-degree vertical side walls due to the nature of lift-off process. As a result of measurements and calculations made from different areas of the 4 μm-thick copper deposited during the trial studies, it was observed that this angle had a slope of around $70^\circ - 75^\circ$ shown in Figure 2.28.

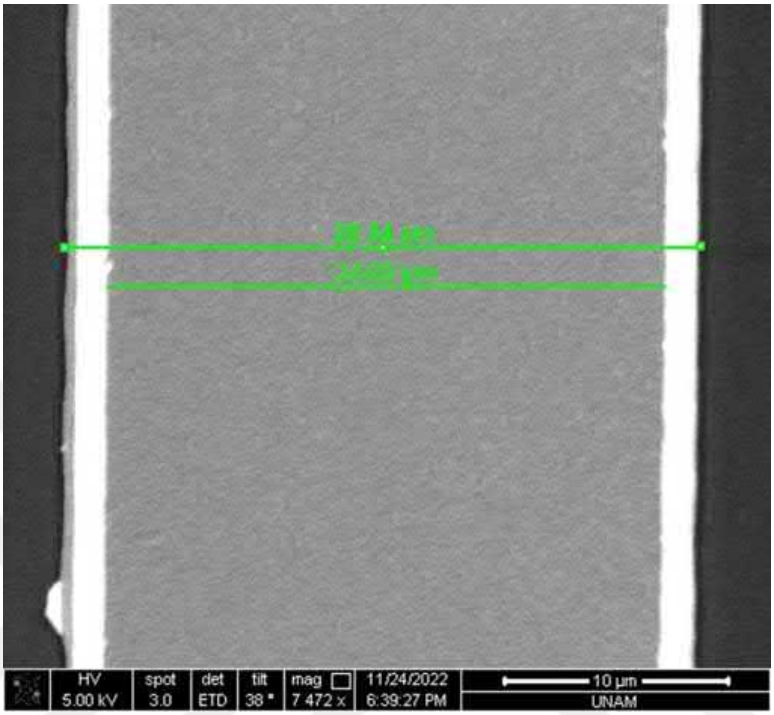


Figure 2.28: SEM image of 4μm Cu from top view

Since this inevitable angle will affect the structure of the CMUT device and indirectly its operating parameters, this information obtained was shared with the team we are in collaboration with in order to evaluate this angle in simulation studies. When the simulations were repeated taking this angle into account, it was concluded that this difference would not cause a significant change and was negligible.

Chapter 3

Experimentation

The fabrication of PR-CMUT devices designed for use in SHM involves precise and iterative trials in a cleanroom environment. This chapter describes the experimental process, such as photolithography, deposition, etching, and lift-off, and the modifications we developed to solve the specific problems we encountered. Considering batch compatibility and scalability, an appropriate production flow was designed and carried out on a wafer scale. The goal was to fabricate high-quality CMUT devices with good performance and well-designed structural features suitable for large-scale production.

The real PR-CMUT fabrication stages are designed to be performed on Pyrex wafers. However, the first productions were carried out on Si wafers to provide better visual inspection reduce the charging during SEM imaging, and obtain better-quality images. Since the production steps have not been tried before and the steps need to be optimized, a Si wafer was used as it will be easier to understand directly with naked eyes, especially optical microscope and SEM imaging techniques, at each step. The use of Si wafers provides several advantages, especially in visual tracking and making necessary improvements in the photolithography, deposition, and lift-off steps. After the steps were established, all fabrication was carried out on Pyrex wafers in the final trials.

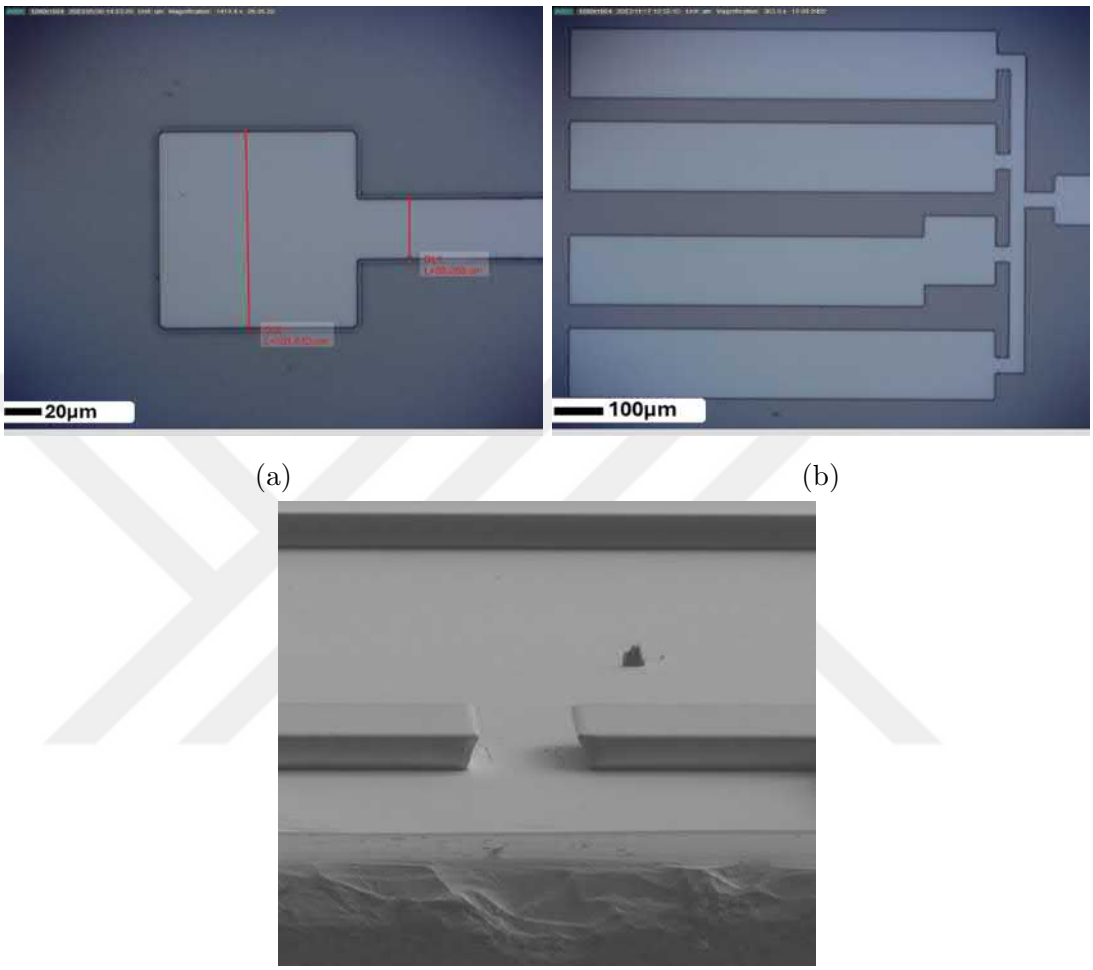
3.1 Initial Microfabrication Process for PR-CMUT

PR-CMUT device fabrication begins with cleaning the wafer to get rid of any foreign materials that could be present and have a negative impact on the process afterwards. In order to ensure excellent adhesion and patterning in subsequent steps, cleaning is a crucial step [34, 35]. First, the Si wafer was immersed in acetone for 3 min and waited for the organic contaminates on the surface to dissolve. Afterward, the wafer was kept in isopropyl alcohol (IPA) for another 3 min. This step was done to allow IPA to clean the organic residues and traces of acetone remaining on the wafer surface. After IPA, the wafer was placed in DI water for 3 min. In all of these cleaning processes, a faster and better cleaning was tried to be achieved with the help of a sonicator. The surface was dried with Nitrogen (N_2) gun blow which effectively dried the wafer without leaving any watermarks or stains. Finally, the wafer was left to dry on the hot plate at 120°C for 10 min. This thermal treatment aims to evaporate all possible moisture from the surface and prepare the surface for the photolithography process by promoting better adhesion of subsequent layers such as photoresists (PR) during photolithography.

Our first step after the cleaning was patterning the bottom electrode using photolithography and Mask 1. A promoter coating called Hexamethyldisilazane (HMDS) is applied to ensure good adhesion between the Si wafer surface and the photoresist to be used [35]. With the help of a spin coater, the wafer is spun for 1 min with a coating speed of 2000 rpm and an acceleration of 1000 rpm/s. Then, before proceeding to the photoresist stage with the real wafer, the photoresist is poured onto the dummy wafer surface in the spin coater for conditioning purposes, and the entire spin coater is spun to ensure it is covered with photoresist.

Since the features are desired to be created with the lift-off process in the following steps. We do not want the side walls of the photoresist to be coated during Electron Beam (E-Beam) evaporation. If the side walls of the PR are covered, it will be very difficult to reach the photoresist with acetone and this

will negatively affect both the lift-off time and the quality of the pattern. For this reason, AZ 5214E Image Reversal photoresist was chosen, with which we can create a negative side wall angle and prevent the side walls of the PR from being covered during the e-beam evaporation deposition stage [36]. After the spinner conditioning process, the AZ 5214E Image Reversal photoresist is spun onto the real Si wafer for 1 min at 1000 rpm speed and 500 rpm/s acceleration. The photoresist thickness after spin coating is estimated to be approximately 2 μm [36]. The wafer is then soft-baked on a hotplate at 110°C for 1 min to evaporate the solvent from the photoresist. After this process, the wafer was exposed to ultraviolet (UV) light using Mask 1 with an exposure dose of 40mJ/cm^2 using the EVG 620 Mask Alignment System. At this stage, the parts that are closed on the mask and not exposed on the wafer during UV light exposure will be the patterns on which the photoresist will be developed later. After the first exposure, the wafer was kept on the hotplate for image reversal bake at 120°C for 1 min. Afterwards, flood exposure was performed without a mask (i.e. flood exposure) at 250mJ/cm^2 dose. This step ensures that the exposed areas become insoluble in the developer, while the unexposed areas remain soluble. The final step in the photolithography is developing the photoresist. At this stage, the wafer was immersed in 1:4 dilutedAZ 400K (1 unit AZ 400K : 4 units DI water) developer and agitated gently for 1 min. This process removes the soluble photoresist from the surface of the wafer and reveals the patterns we are trying to get with Mask 1. The optical microscope and SEM images were examined in order to verify the accuracy and quality of the patterning. The dark colors visible at the edges in Figure 3.1a are due to undercut. From here we can understand that we can achieve a negative wall angle. SEM images in Figure 3.1b also confirm this result



(a) (b)

(c)

Figure 3.1: (a) Optical image of the undercut, (b) optical image of the pattern after development, (c) SEM image of the undercut

The next step after completion of the photolithography steps is to use oxygen plasma with the Inductively Coupled Plasma (ICP) etching. This step, called the descum process, removes any photoresist residues that are remaining on the patterned areas. This helps to make sure that the surface is clean and well-defined for the deposition of the next layers of materials. The wafer is first taped to a thick glass substrate in order to keep the wafer stable and avoid gas leaks from occurring from the back of the wafer. If you clamp Si inside the ICP chamber, the wafer can be bent because the wafer is a thin substrate. The extra support from

the thick glass substrate helps the wafer to stay strong while it is being etched with oxygen plasma. After preparation of the wafer, the ICP etching system undergoes a 15 min warm-up process in order to make sure the plasma conditions remain stable, and the etching occurs consistently. The brief 10-second oxygen plasma etching step is the actual descum process. This short duration is sufficient to remove any thin photoresist residues that may remain on the substrate after PR development.

After descum process with oxygen plasma, the wafer is ready for bottom electrode deposition with the e-beam evaporation technique. The bottom electrode consists of 50nm Titanium (Ti) and 450nm Copper (Cu). Initially, it was decided to use Chromium and Gold as the bottom electrode materials while designing the masks, but for the first prototype, using Ti and Cu decided to be more affordable. Before starting the actual coating, coating is done with 3 small Si wafer pieces to calculate the tooling factor of the device. This step is important to ensure that the coating thickness we apply on the actual wafer is closer to the desired one. Initially, 50nm of titanium is deposited on all three samples. After the titanium deposition, two of the samples are removed from the e-beam deposition chamber. The remaining titanium-coated sample undergoes a deposition of 100nm of copper. One of the removed titanium-coated samples is then placed back into the chamber, and an additional 150nm of copper is deposited under the same conditions. This results in one sample with 50nm of Ti and 150nm of Cu, another with 50nm of Ti and 250nm of Cu, and one with only 50nm of Ti. The thicknesses of the samples are measured using Atomic Force Microscopy (AFM) to calibrate the tooling factor of the e-beam evaporator.

After the tooling factor was calculated, deposition started on the Si wafer. 50 nm Ti was deposited as the adhesion layer. After titanium deposition, 450nm copper deposition was performed without breaking the vacuum to completely form the bottom electrode. During the deposition, the first 10nm was deposited at a rate of 0.3 Å/sec, and the following thicknesses were deposited at a rate of 0.5-0.8Å/sec. The aim here is to deposit the first layers at low speed to ensure good adhesion to the surface and uniform layer formation.

Several important precautions are taken during the deposition process to ensure high-quality results. The life of the crystal monitor is checked to ensure accurate thickness measurements, before starting the e-beam deposition. Additionally, the material inside the crucible is inspected to ensure that it has melted sufficiently to prevent surface roughness caused by splashed particles. To avoid sudden temperature changes that could compromise the integrity of the deposited layers, the chamber is allowed to cool for at least 30 min before the chamber vacuum is interrupted. Figure 3.2 shows the optical microscope image immediately after deposition.

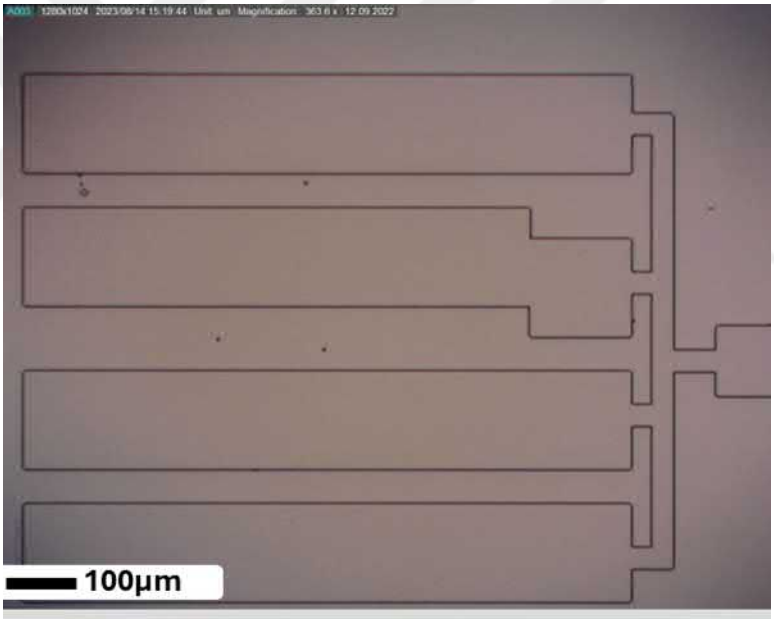
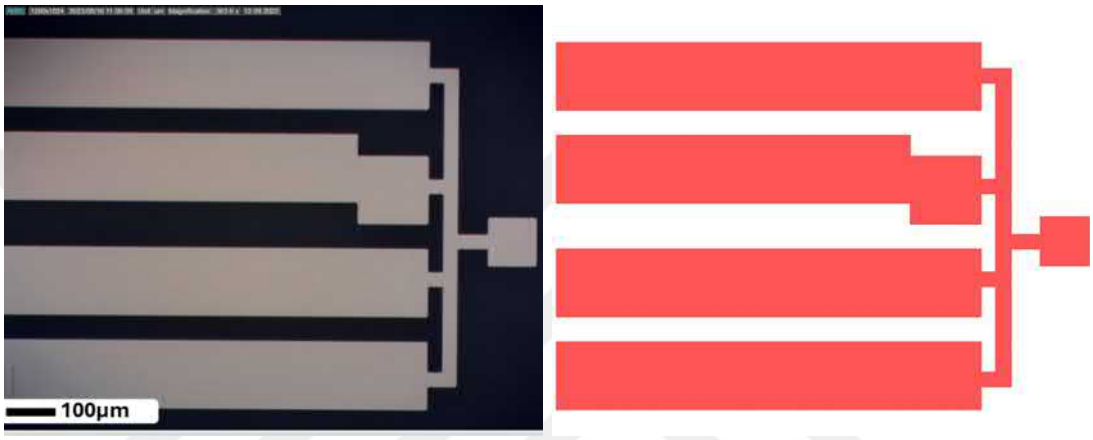


Figure 3.2: Optical microscope image of wafer part right after Ti-Cu deposition with e-beam

After e-beam evaporation, the next process step is lift-off, which aims to get rid of photoresist and unwanted metals. After this process, only the metals in the patterned area are expected to remain. The wafer was placed in a container filled with acetone. A sonicator was not used in this process in order not to damage the metals in the areas that we wanted it to be patterned. After waiting in acetone long enough to completely get rid of the photoresist and the metal on it, the wafer was placed in the DI wafer. The purpose of this step is to get rid of acetone and

dissolved material residues remaining on the surface of the substrate. Finally, the surface was dried with N_2 gun blow. As can be seen in Figure 3.3a, the metals in the patterned parts on the surface after lift-off are shown. The image of the same area in the mask design is also included in figure 3.3b.

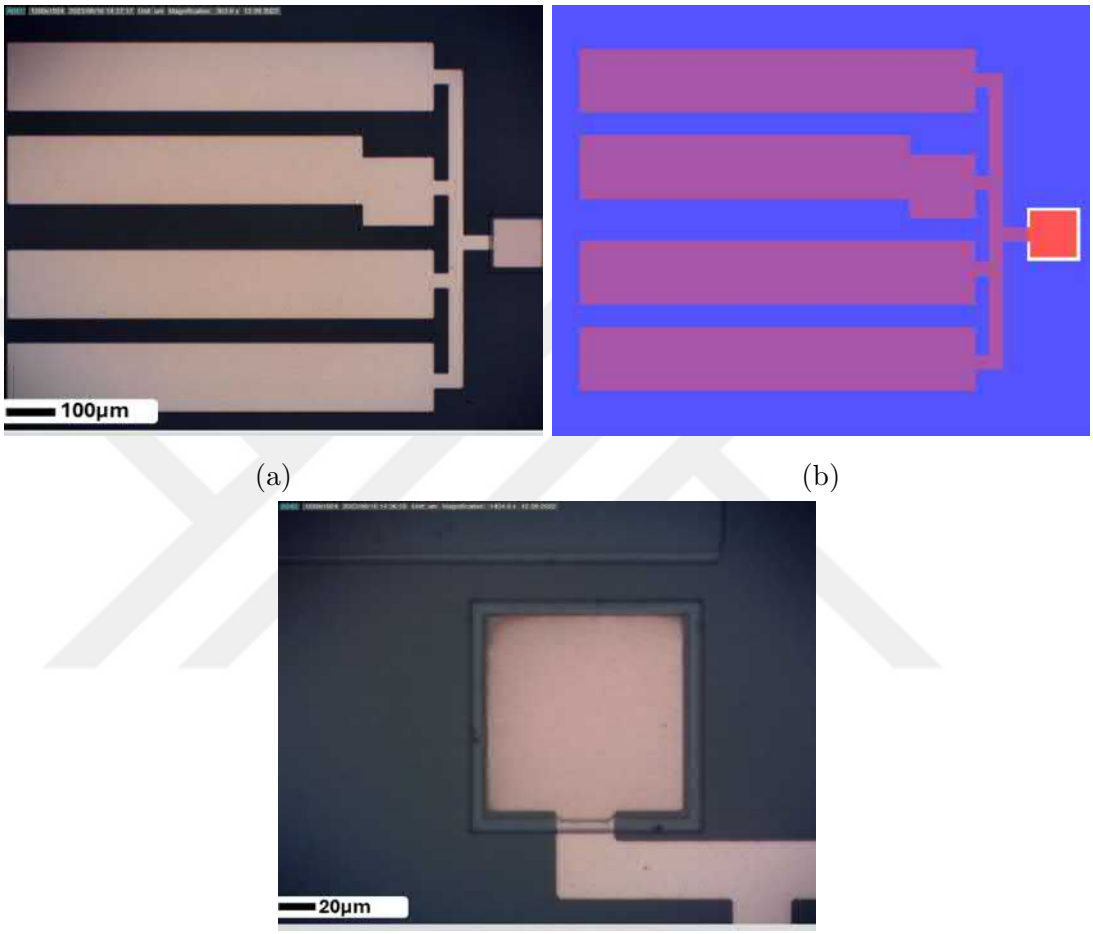


(a) (b)

Figure 3.3: (a) Optical microscope image of the wafer after lift-off process, (b) mask design of the same area

The next step after lift-off is the next photolithography step, where the patterns will be transferred to the wafer for dielectric layer deposition using Mask 2. This step is crucial to determine the area where the dielectric material will be deposited and to obtain good electrical insulation in PR-CMUT devices. The fundamental steps in this photolithography process are the same as those previously mentioned. These steps are HMDS coating, AZ 5214E image reversal coating, UV exposure, flood exposure, and development. This involves careful alignment and patterning to create precise openings and ensure that the dielectric layer covers the correct areas without any overlap or gaps. Following the photolithography step, descum process was performed, which was the same as the previous descum step, in order to get rid of photoresist residues in the patterned areas. The parts where the pads are located are covered with photoresist to prevent dielectric coating. When production is completed, these pads will be used to electrically characterize the device. Figure 3.4a shows the optical microscope image obtained after photolithography steps. Figure 3.4b shows a closer

optical microscope image of the pad part covered with photoresist.



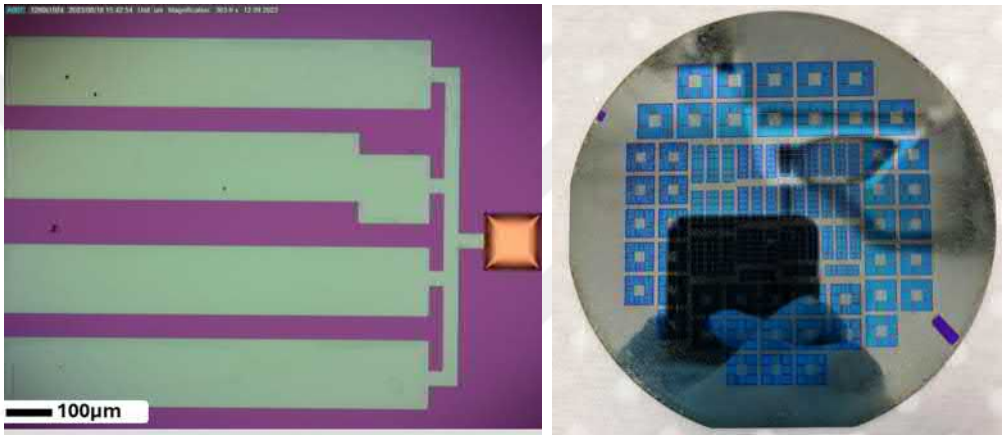
(a) (b)

(c)

Figure 3.4: (a)Wafer after photolithography with Mask2, (b) mask design of the same area, and (c) higher magnification of the pad area

Photolithography step and descum step have been completed successfully. The next step involves dielectric layer deposition with e-beam evaporation. A 150nm layer of HfO_2 is deposited onto the wafer. Before coating on the real wafer, 3 small silicon wafer pieces were coated with HfO_2 at different thicknesses, as in the previous e-beam step, and their thicknesses were measured with AFM, to calculate the tooling factor for HfO_2. The tooling factor was calculated by comparing the results obtained with AFM with the targeted coating thicknesses. The real Si-wafer is deposited in a controlled manner. In this process, the first

10nm of HfO_2 was deposited at a speed of 0.3 Å/sec and the remaining 140nm at a speed of 0.5 Å/sec. After the deposition, the chamber is allowed to cool down for at least 30 min before breaking the vacuum to prevent sudden temperature changes that could stress the newly deposited HfO_2 layer. The optical microscope image after coating and just before lift-off is in Figure 3.5a and the wafer image is in Figure 3.5b.



(a) (b)

Figure 3.5: (a) Optical microscope image of wafer part right after HfO_2 deposition with e-beam, (b) wafer image after deposition

Following the e-beam evaporation of the HfO_2 layer, the lift-off process is performed in the same manner as the previous lift-off steps. The wafer is soaked in acetone, then rinsed with deionized (DI) water, and dried using a nitrogen (N_2) blow. Figure 3.6 shows the optical image after lift-off.

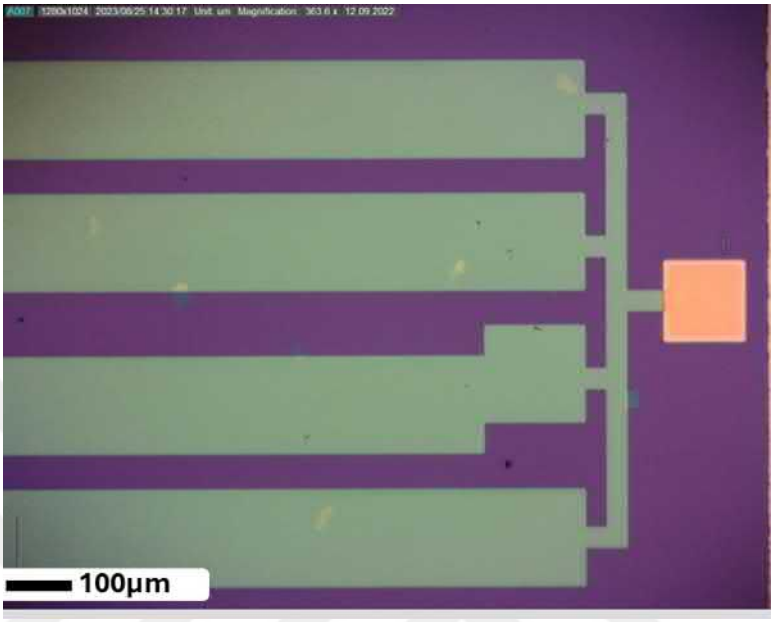
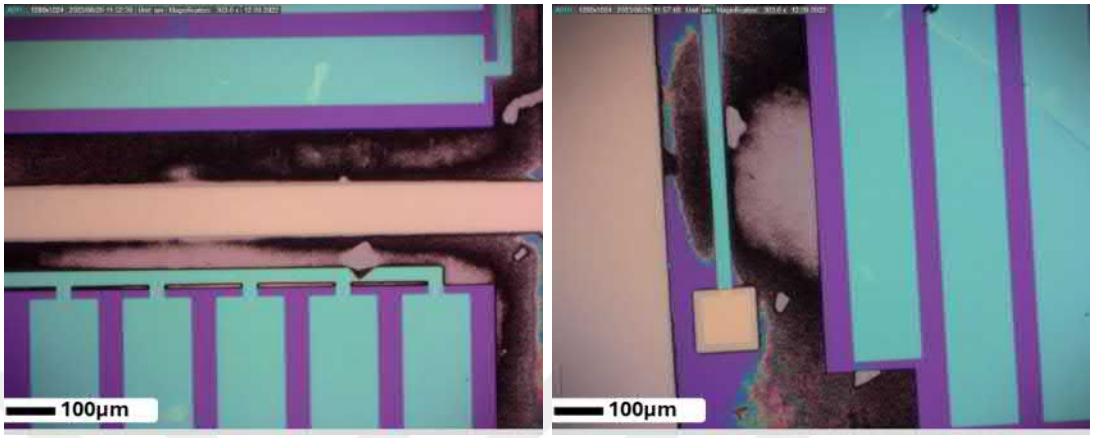


Figure 3.6: Optical microscope image of the wafer after lift-off process

After the successful dielectric layer patterning and deposition steps, the photolithography step was performed with Mask 3 for the next layer, Poly-Si layer, patterning. The photolithography process follows the same basic steps as previously described: HMDS coating, AZ 5214E image reversal coating, UV exposure, flood exposure, and development. However, after this photolithography step, we encountered issues with the photoresist development. The photoresist did not adhere properly and did not develop correctly. This step was repeated on an empty Si-wafer, considering that it might be caused by the photoresist condition, exposure time, or the device conditions used at that time. While the photolithography study performed with the same parameters developed properly on an empty Si-wafer, it always gave poor results on the real wafer. As a result of these studies, it was concluded that a suitable adhesion between HfO_2 and the photoresist surface could not be achieved. Figure 3.7a and 3.7b show optical microscope images of photoresist that were not developed properly.



(a) (b)

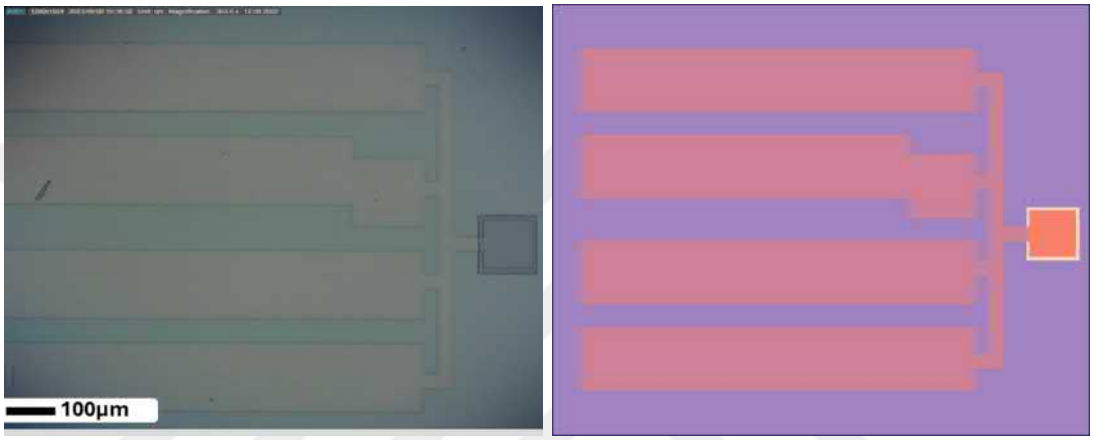
Figure 3.7: (a) and (b) Optical microscope images of photoresist that is not properly developed in different regions

3.2 First Revision of PR-CMUT Microfabrication Process

If the process proceeds as anticipated, the next course of action will involve continuing with the procedures outlined in Appendix-A.1. However, since this problem prevented further progress, it was planned to obtain a better adhesion by coating the entire wafer surface with Cr as a solution to this problem. However, this step introduces additional steps that will need to be addressed in the future and has led to the development of the planned fabrication stages outlined in Appendix-A.2. The next steps will be continued as stated in Appendix-A.2 unless any additional issues arise.

As a solution to the adhesion problem we encountered, the entire wafer surface was uniformly coated with 50nm Cr with e-beam deposition without any mask. Chromium was chosen not only for its excellent adhesion properties but also for its ease of removal using a chromium wet etchant. Chromium etchant is a chemical that is commonly found in multi-use cleanrooms. In addition, when we use Chromium etchant later to remove Cr, it does not harm the HfO_2 we

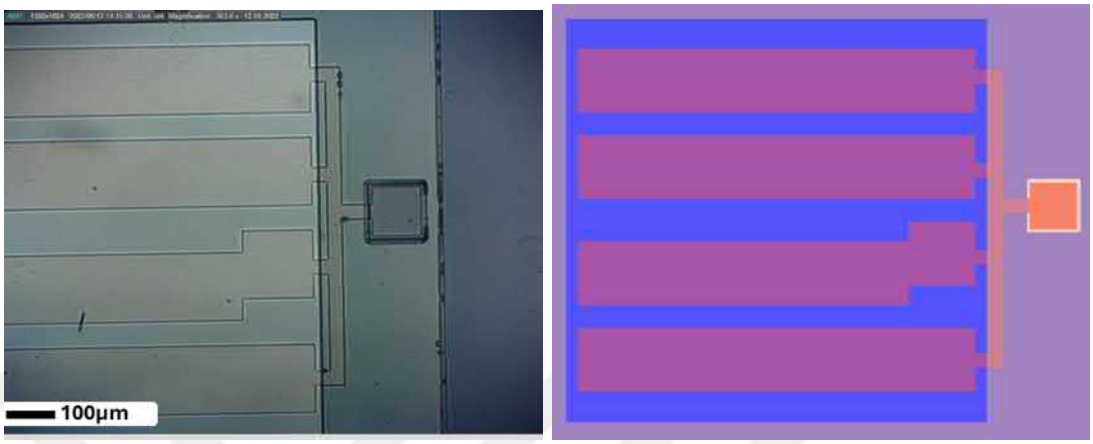
deposited before. These characteristics made chromium an ideal choice, as it could be easily etched away from unwanted surfaces later in the process. Figure 3.8a shows the optical microscope image after 50nm thick Cr deposition with e-beam without using a mask. Figure 3.8b shows the mask design for this region.



(a) (b)

Figure 3.8: (a) Optical microscope image after 50nm thick Cr deposition with e-beam without using a mask, (b) mask design for the same region

After the chromium deposition, the photoresist was applied again following the standard photolithography procedure using Mask 3. This included HMDS coating, AZ 5214E image reversal coating, UV exposure, flood exposure, and development. The Cr layer used here provided a better adhesion and enabled successful photoresist development. Following photolithography, another descum process was performed to clean the patterned areas. The optical microscope image of the pattern obtained as a result of photolithography with Mask 3 is shown in Figure 3.9a. The mask design is also included in Figure 3.9b.

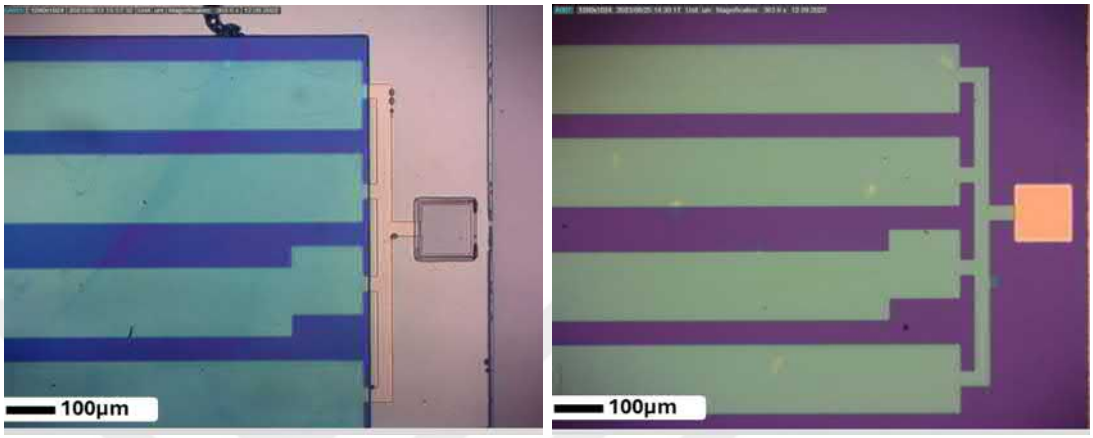


(a) (b)

Figure 3.9: (a) Optical microscope image of the pattern obtained through photolithography using Mask 3, (b) corresponding mask design

Before proceeding with the poly-silicon (Poly-Si) deposition, it was necessary to remove the chromium layer from the device areas. If the Cr layer here is not removed, a conductive layer that is called "floating electrode" will remain on the dielectric layer. Our PR-CMUT MEMS device is not designed for "floating electrode" configuration. For this reason, the Cr layer in the device area should be completely etched. This was accomplished using a chromium etchant diluted 1:3 with deionized (DI) water. The reason for diluting the Cr etchant is to create a controlled etch environment. The etch rate of the Cr etchant for Cr is 170nm/sec. The wafer was immersed in the etchant, and the etch rate was monitored every 10 seconds using an optical microscope. The etching process continued until the exposed areas reverted to the original color of HfO_2, indicating that the chromium layer had been fully removed from the device areas. It took 40 seconds (i.e. 4 repetitions of 10 seconds etching) to remove all Cr layer. Figure 3.10a shows the optical microscope of the wafer after Cr etch. Figure 3.10b shows the optical microscope before Cr coating for color comparison. Although it is observed that there is a color difference in the device area in these two images, it is thought that this is actually due to the current light balance difference of the optical microscope. After Cr etchant EDX analysis has been done to verify that the entire Cr layer has been etched from the surface. As a result of EDX, no Cr peak

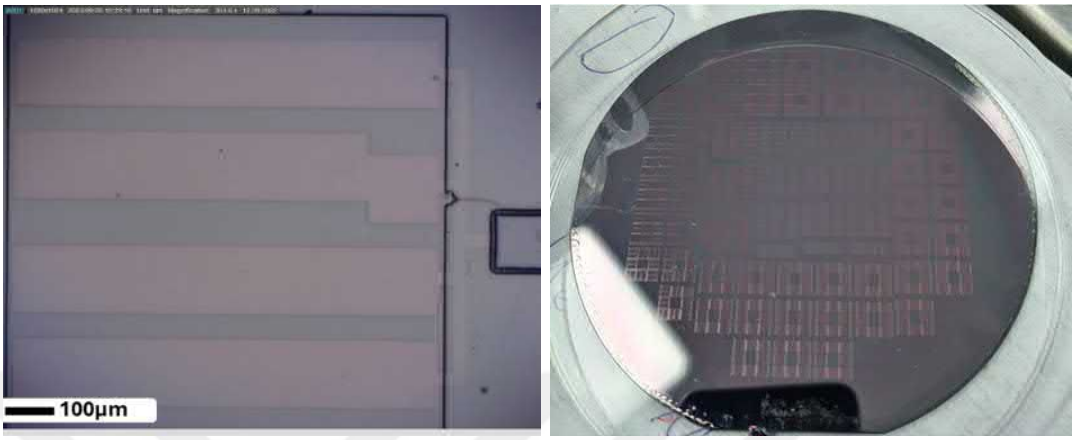
was detected from the surface.



(a) (b)

Figure 3.10: (a) Optical microscope image of the wafer after Cr etch, (b) optical microscope image before Cr coating

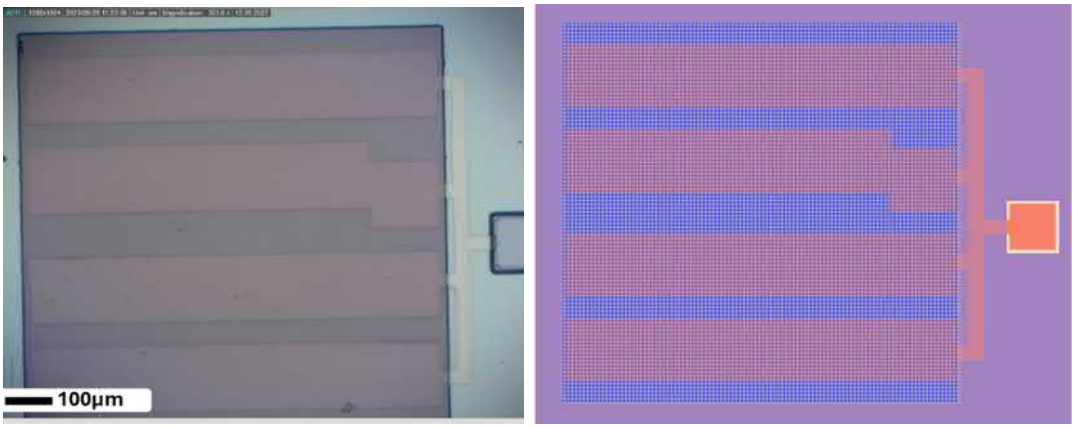
After removing the Cr layer from the device area, the next step is Poly-Si deposition, which is the sacrificial layer to be used in the gap formation required for PR-CMUT. A 600nm layer of Poly-Si is deposited onto the wafer. As in previous e-beam depositions, the tooling factor was calculated, low deposition rates were used, and a 30 min cool-down period was waited before breaking the vacuum after deposition. Figure 3.11a shows the optical microscope image pre-lift-off, and post-deposition. Figure 3.11b exhibits the entire wafer image post-deposition.



(a) (b)

Figure 3.11: (a) Optical microscope image after Poly-Si deposition with e-beam, (b) wafer image after deposition

Following the deposition of Poly-Si, the lift-off process is carried out to remove excess poly-silicon and photoresist. The lift-off process is executed in the same manner as the previous steps. Figure 3.12a shows the final state of the wafer after lift-off. The pinkish-colored areas are the Poly-Si deposited parts. These Poly-Si coated parts are shown in Figure 3.12b as a white mesh on the mask design.

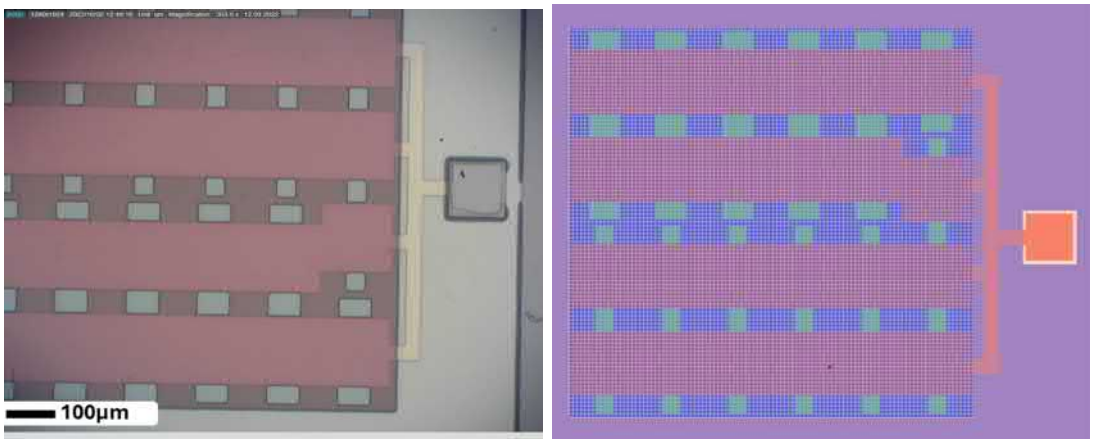


(a) (b)

Figure 3.12: (a) Optical microscope image of the wafer after lift-off process, (b) mask design of the same area

The next step will be to etch Pol-Si in the anchor parts with the BOSCH Process. Photolithography will be performed with Mask 4 to ensure that only the Poly-Si in the anchor parts is etched and the Poly-Si in the other parts remains undamaged. With this method, the photoresist will be used as a mask. Since it is planned to etch a Poly-Si thickness of 600nm at this stage, it is necessary to use a thick photoresist mask that can last during this etch period.

As in the previous photoresist steps, promoter HMDS was used first. In this step, AZ 4562 positive photoresist was used, which unlike the previous ones, offers a thicker photoresist thickness [37]. After applying AZ 4562, it was spun for 1 min with a spin speed of 4000 RPM and an acceleration of 500 rpm/s. At the end of this process, a photoresist thickness of approximately 6 μm is expected with this spin rate [37]. After spinning, the wafer was soft-baked at 110°C for 1 min to allow the solvents in the photoresist to evaporate. The wafer is then exposed to ultraviolet (UV) light through Mask 4 with an exposure dose of 140 mJ/cm^2. As the last step, the photoresist was developed by slowly moving it in 1:4AZ 400K developer and DI Water for 1-2 min. Figure 3.13a shows the result after the photolithography development of Mask 4. Figure 3.13b shows the mask design corresponding to this part.



(a) (b)

Figure 3.13: (a) Optical microscope image after photolithography with Mask 4, (b) mask design of the same area

A 15 min warm-up is required before starting the ICP etching process in order to stabilize the plasma conditions and ensure reliable etching performance. The wafer is subsequently placed into the ICP etching chamber, where the wafer undergoes a 10-second descum process to ensure a clean surface for accurate etching by removing any remaining particles of photoresist that may have remained in the patterned areas after development. The Bosch process, an anisotropic etching method that alternates between etching and passivation cycles, is used for the actual silicon etching. While the passivation cycles deposit a protective layer on the trench sidewalls to ensure vertical sidewalls and prevent lateral etching, the etching cycles remove the exposed poly-silicon areas. To achieve the required depth and profile, the etching process is continuously observed. The endpoint of the etching is determined by observing a change in the color of the underlying layer (HfO_2). It took 63 cycles to remove all Poly-Si from the anchors. In Figure 3.14, the color changes at the end of each etch process can be followed step by step. In fact, as can be seen in Figure 3.14, there is no change in color between the 53rd and 63nd cycles, but it was deemed appropriate to do 10 more cycles to ensure that it is completely etched. After Poly-Si etch EDX analysis have been done to make sure there is no Poly-Si in the anchor areas.

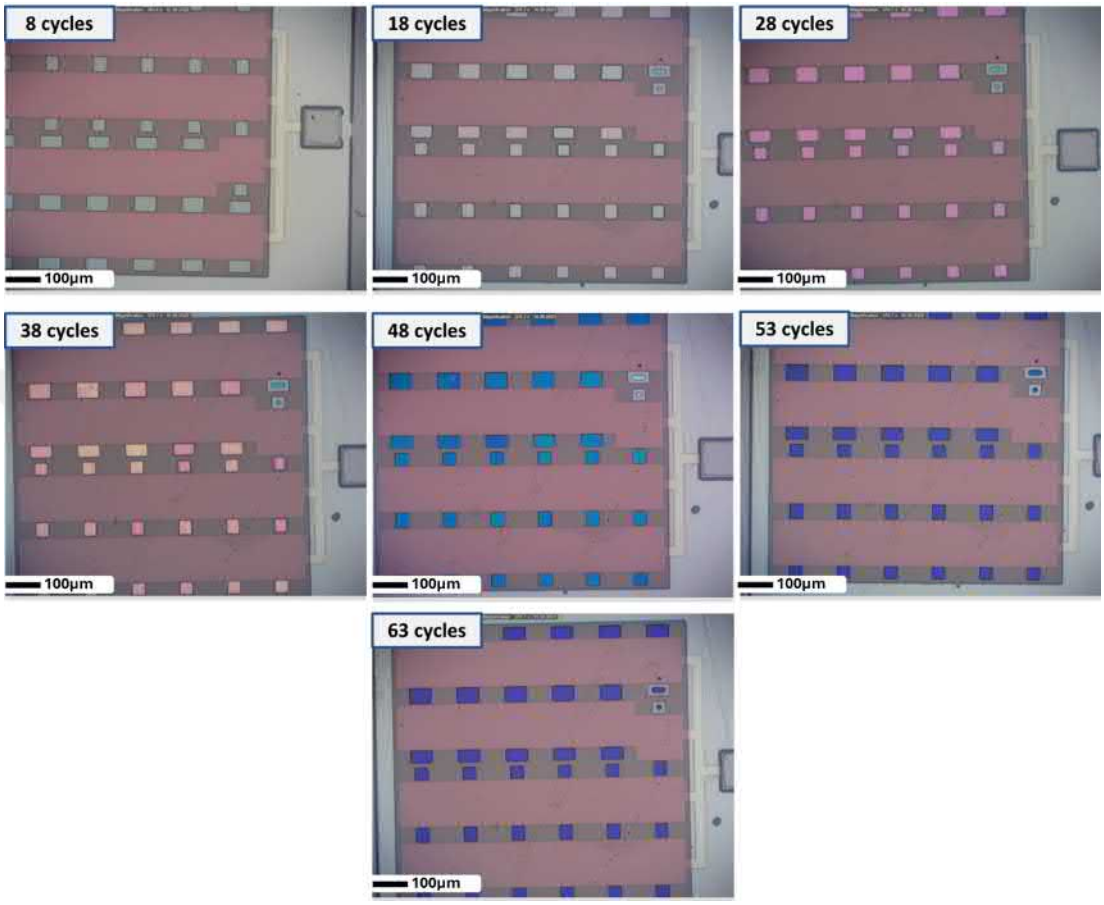


Figure 3.14: Optical microscope images of the wafer after each etch cycle

The photolithography step, which is one of the last steps, will be applied to create the top membrane. For this, HMDS will be coated as in the previous photolithography steps. To lift-off a 4 μm thick deposition, a thick photoresist layer must be obtained. For this purpose, a thick photoresist was obtained by coating AZ 5214E image reversal photoresist, which was also used in the previous steps, with a low spin rate. This is achieved by spinning the wafer at 500 RPM with an acceleration of 250 rpm/s for 1 min, resulting in an initial thickness of around 5 μm. The wafer is then soft-baked at 110°C for 1 min to ensure complete solvent evaporation. The parameters used in the subsequent steps for photolithography were applied to be the same as the previous AZ 5214E processes.

The final step in this photolithography process is the development of the photoresist. The wafer is immersed in a 4:1 solution ofAZ 400K developer and DI water for 1 min. Although higher photoresist thickness was obtained by spin coating at low spin rates, this caused significant edge bead formation. Since these edge beads are not only on the edges of the wafer and move too far into the wafer, they have also prevented the production of some desired devices. Since the parts with edge beads are higher than the normal photoresist thickness, it creates an elevation difference during the mask alignment stage and prevents proper alignment. In addition, since the solvents do not fully evaporate in the part with edge beads during the baking period, it causes the wafer to stick to the mask. Figure 3.15 shows the edge bead formation that occurs as a result of the 500 RPM spin rate. Despite attempts to remove these edge beads, the thickness variation across the wafer creates alignment issues during the mask alignment step and these variations lead to non-uniform exposure and development, causing certain areas of the wafer to be adequately developed while others are overdeveloped. This problem creates difficulties for the next steps in the fabrication process and reduces the overall quality and accuracy of the patterning process.

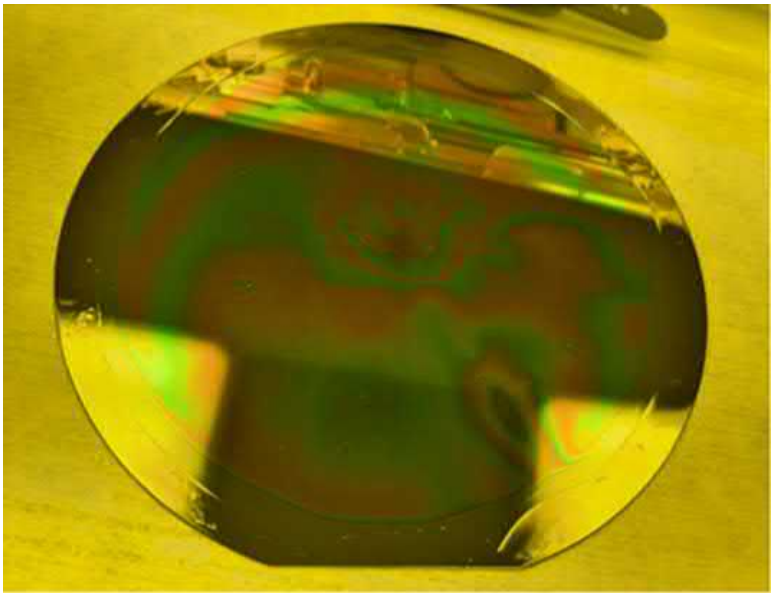
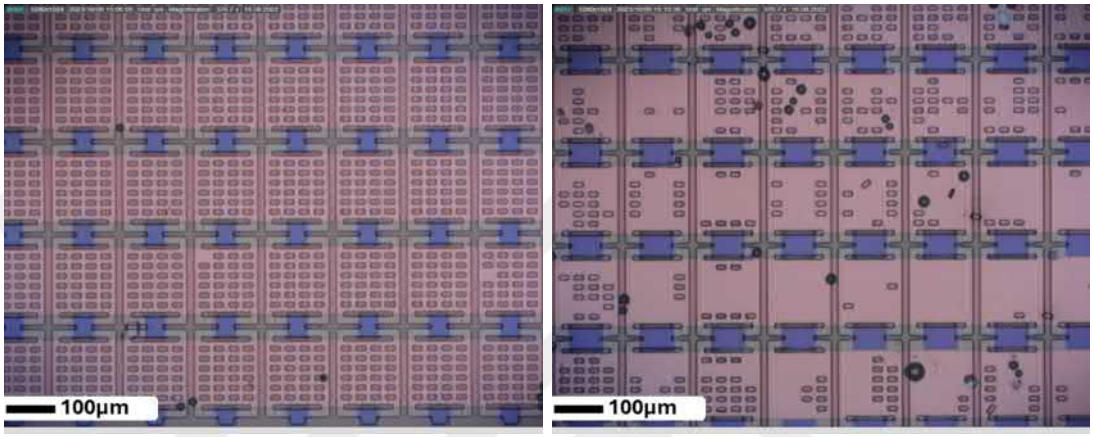
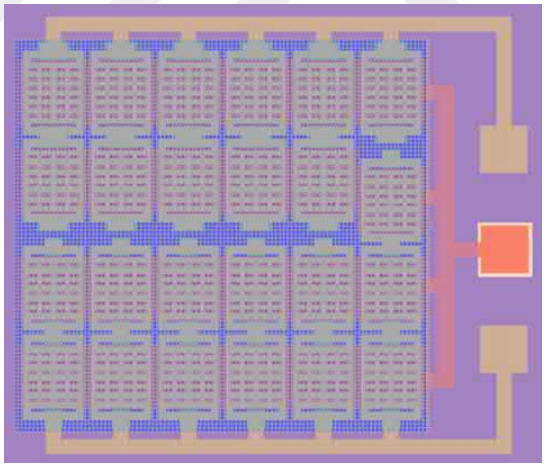


Figure 3.15: The edge bead formation due to 500 rpm spin rate

While one part of the wafer was properly developed, as in Figure 3.16a, another part was overdeveloped, causing poor quality patterning as a result of the separation of photoresists that could not adhere to the surface, as in Figure 3.16b.



(a) (b)

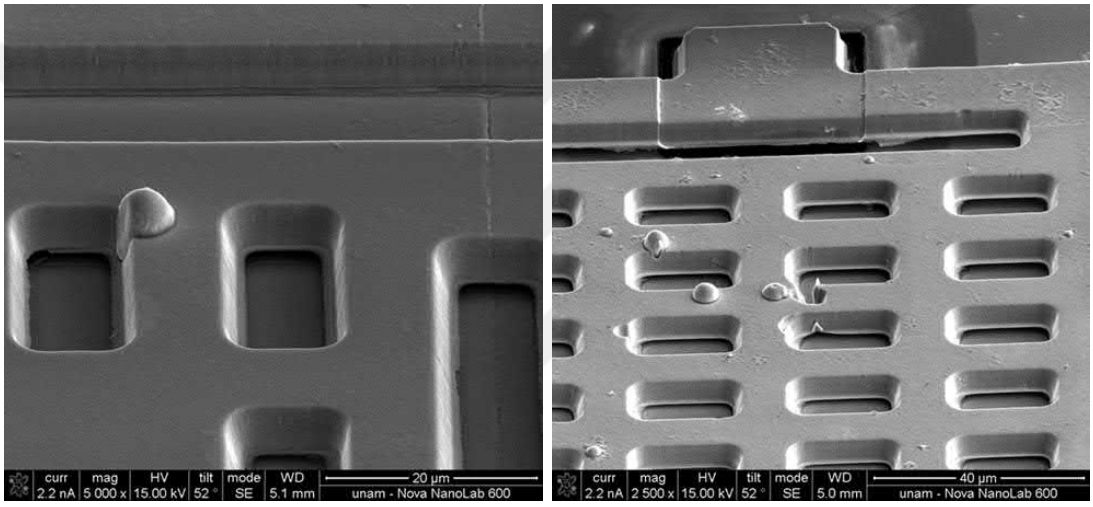


(c)

Figure 3.16: (a) and (b) Optical microscope images taken at different points on the wafer, (c) corresponding mask design

Although photolithography on the wafer surface is not uniform, two main steps following this step—thick copper deposition and subsequent XeF_2 etching process—were attempted. The wafer was broken into pieces, and the next steps were continued with the areas where photolithography was successful. This part was coated with 50nm Ti and 4 μm e-beam evaporated Cu. After the copper

lift-off, XeF_2 etching steps were performed. It was known that since the wafer was silicon, the wafer itself would also be etched in this step during the XeF_2 process. However, preliminary testing was intended in these experiments. As can be seen from the SEM images in Figure 3.17, partial etching of the Poly-Si layer was successfully achieved. After 10 cycles of XeF_2 treatment at 3.5 Torr pressure for 600 seconds, all surfaces emerged in high quality and without damage.



(a) (b)

Figure 3.17: SEM images of Wafer surface after XeF_2 treatment at 3.5 Torr pressure for 600 seconds

As can be seen from the optical microscope images, photolithography was not fully optimized for the thick photoresist step. This resulted in varying development times in different regions of the wafer. The observed inconsistencies and defects indicate that this process is not suitable for wafer fabrication. As a result, it was decided to develop a new method with the resources we have to solve these problems and obtain more uniform and reliable patterning results. This innovative approach aims to obtain a photoresist thickness that allows us to lift off a 4 μm thick coating. A negative slope profile for the side walls is also required to ensure successful lifting.

Given that the cleanroom infrastructure in which we worked did not support commercially available thick image reversal photoresists, existing photoresists were used to develop a new approach. The following experimental section will detail the development and application of this new photolithography technique, along with the information and additional details provided so far.

3.3 Development of Multi-layer AZ 5214E Photoresist for High-Thickness Material Lift-off

Successful methods have been proposed in the literature for the lift-off of thick films with different techniques. To enable the fabrication of PR-CMUT thick membrane, a suitable lift-off method was developed by obtaining a thick photoresist with AZ 5214E image reversal photoresist. For a successful lift-off, the side wall angles of the photoresist must be negatively inclined. This way, the side walls will not be coated during deposition and will be accessible with acetone during lift-off. This "negative slope," which is generated by carefully adjusting the photoresist spinning, baking, exposure, and development processes, is also known as a "retrograde profile" or a "reverse taper". As stated in the literature, the maximum lift-off material thickness depends on the photoresist thickness, and this thickness is required to be at least 1.2 to 1.3 times greater than the thickness of the material to be deposited [38].

At least three well-known methods exist to achieve the photoresist required for the lift-off process. These mainly consist of single-layer photoresist, bi-layer photoresist, and photoresist surface modification methods. The single-layer photoresist method is obtained using negative photoresist or image reversal photoresist. The negative-tone MaN 1440 photoresist with a single layer exhibits excellent properties for lift-off processes [38]. These properties include adjustable sidewall profiles, the ability to vary in thickness, and easy removal. There are also special lift-off resists such as TI XLiftX that can be applied to obtain single-layer thick image reversal photoresist [39]. Image reversal photoresist, like AZ 5214E, is a

commonly used single-layer photoresist to use for thin film lift-off method known for its high reproducibility [40–42]. In bi-layer methods, two different photoresists are spun on top of each other to obtain the negative slope. Since the bottom one of these photoresists develops faster than the upper one, the negative slope is obtained with the same development time.

According to the literature, the image reversal feature is achieved through a special crosslinking agent in the resist formulation, which activates at temperatures above 110°C, and crucially, only in areas exposed to UV light. This agent, together with the photoactive compound (PAC), becomes insoluble and insensitive to light. After flood exposure, the areas that were not exposed to light in the first lithography step are dissolved in the developer solution during development [36]. Image reversal photoresist steps are included in Figure 3.18.

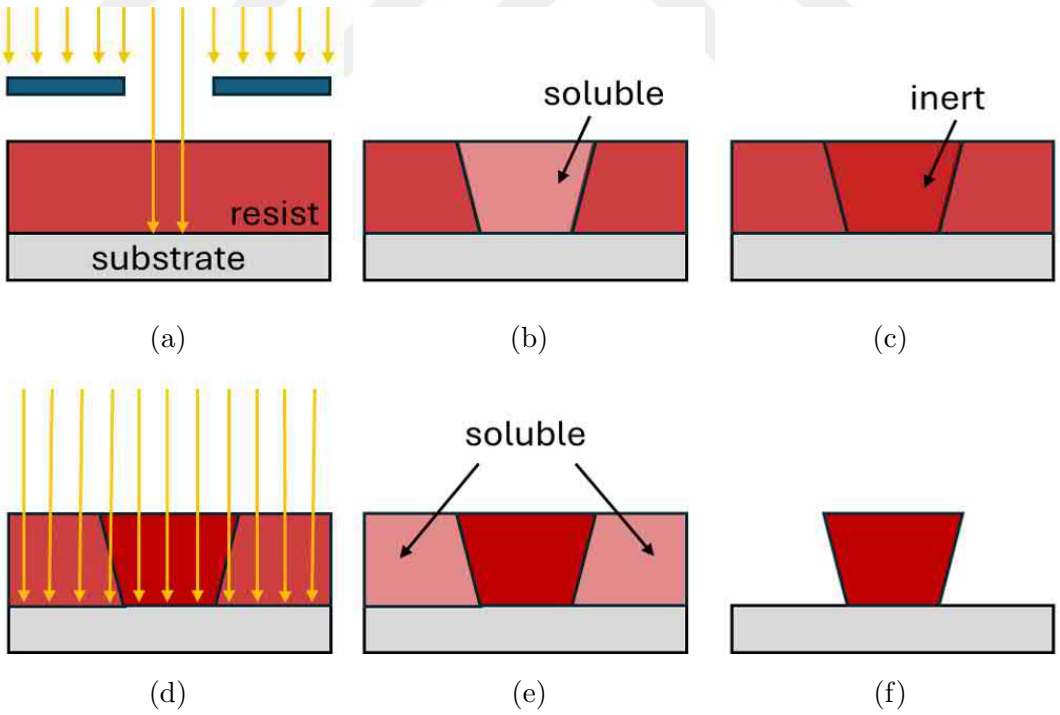


Figure 3.18: (a)First exposure with mask, (b) soluble photoresist after exposure, (c) reversal bake, (d) flood exposure without mask, (e) soluble photoresist after flood exposure, (f) photoreisst after development

The new production process, developed using AZ 5214E image reversal photoresist, begins with wafer cleaning. The wafer is cleaned with acetone, IPA, and DI water, and then dried at 120°C for 10 min on a hot plate to get rid of moisture. Before the wafer is coated with HMDS, the spin coater is thoroughly cleaned with acetone and IPA. HMDS is applied to the wafer by spinning it at 2000 RPM with an acceleration of 1000 RPM/s for one min, followed by placing the wafer on a hot plate at 150°C for 5 min to evaporate any excess solvent. Due to the limited resources in the cleanroom, both HMDS and photoresist spin coating is done with the same spin coater. Following the application of HMDS on the real wafer, a dummy wafer is coated with photoresist and spun to cover the walls of the spin coater, a process that we named as "spinner chamber conditioning." The primary reason for this procedure's necessity is the possibility of HMDS vapor penetrating the subsequent resist films. This might cause the photoresist film to partially crosslink during the soft bake, degrading the resist profile and resolution and slowing down the development process [35].

The first layer AZ 5214E photoresist is spun at a speed of 1000 RPM with acceleration of 250 RPM/s, for one min, then soft-baked on the hot plate at 110°C for 15 seconds. A second layer of AZ 5214E is then spun at the same speed and acceleration, soft baking at the same temperature on top of the first layer for 15 seconds. Finally, a third layer is applied at the same speed and acceleration, with a soft bake on top of the second layer for one min at 110°C.

After spin coating, it is essential to soft-bake each photoresist layer to make sure that the solvent evaporates sufficiently and the spun photoresist film stays stable on the wafer. A thicker overall photoresist coating on the wafers is possible with this layer-by-layer method. Without soft baking after each layer, the solvent in the photoresist does not evaporate entirely and this leads to a thinner photoresist height. Moreover, applying several layers of photoresist without first soft baking may result in the formation of bubbles between layers, which may cause problems with UV exposure and soft baking. Additionally, if the solvent does not evaporate enough during the soft bake process, it can affect the uniformity of the next photoresist layer. Residual solvent from the previous layer can interfere with achieving an even thickness in the subsequent layer.

After preparing the tri-layer AZ 5214E photoresist, the wafer is exposed to 40 mJ/cm^2 of UV light using a mask, then reversal-baked for one min at 120°C on a hot plate. Subsequently, it undergoes a flood exposure at 250 mJ/cm^2 of UV light without a mask, followed by developing the photoresist for 60 seconds in a 1:4 diluted AZ 400K developer. The process flow of this developed method is shown in Figure 3.19.

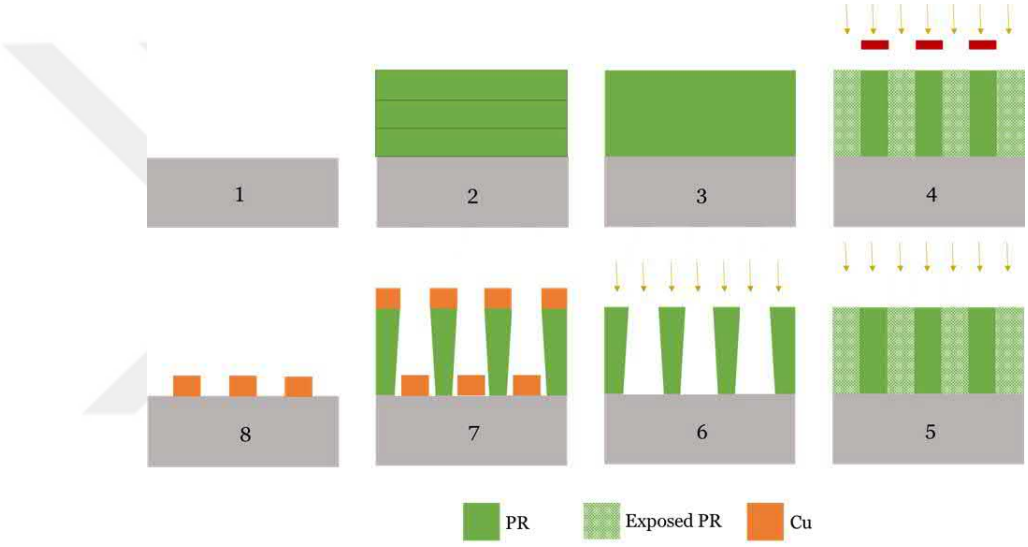
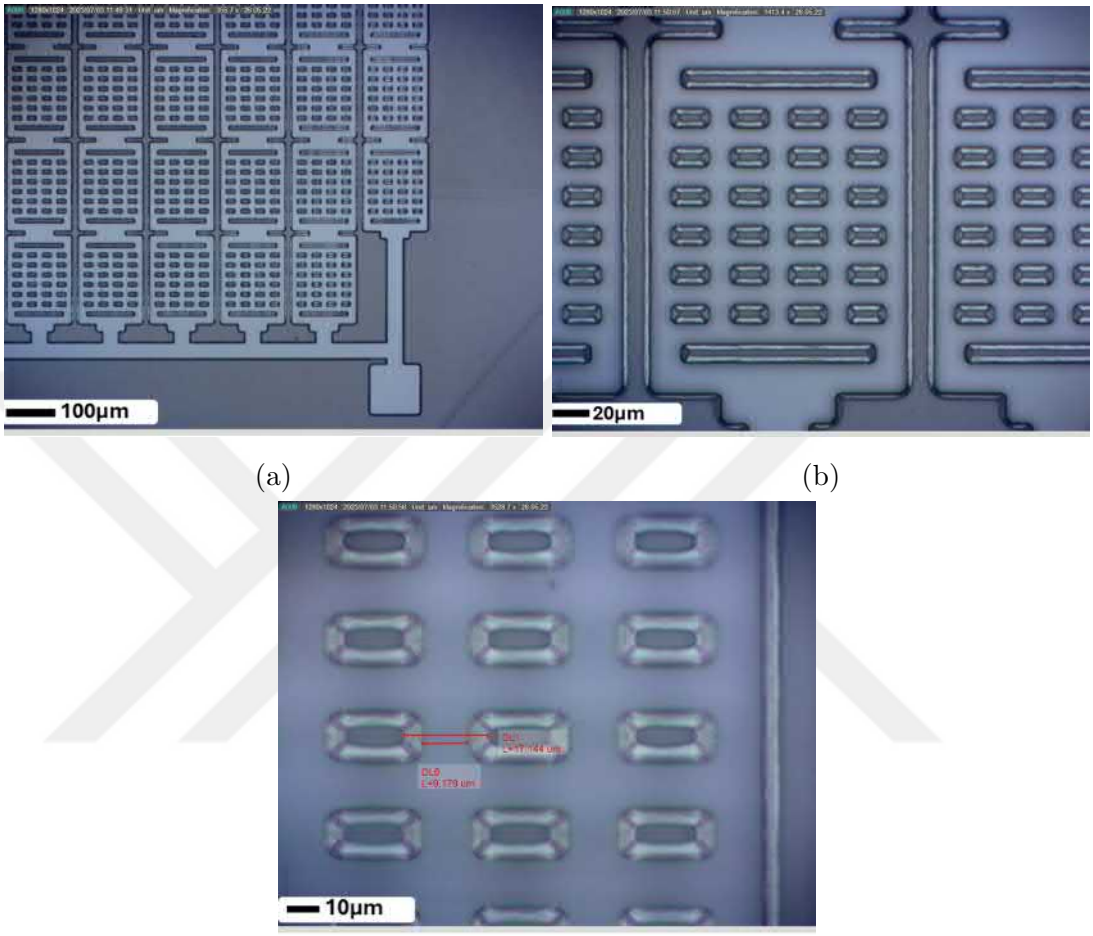


Figure 3.19: Schematic for new developed multi-layer AZ 5214E thick photoresist method

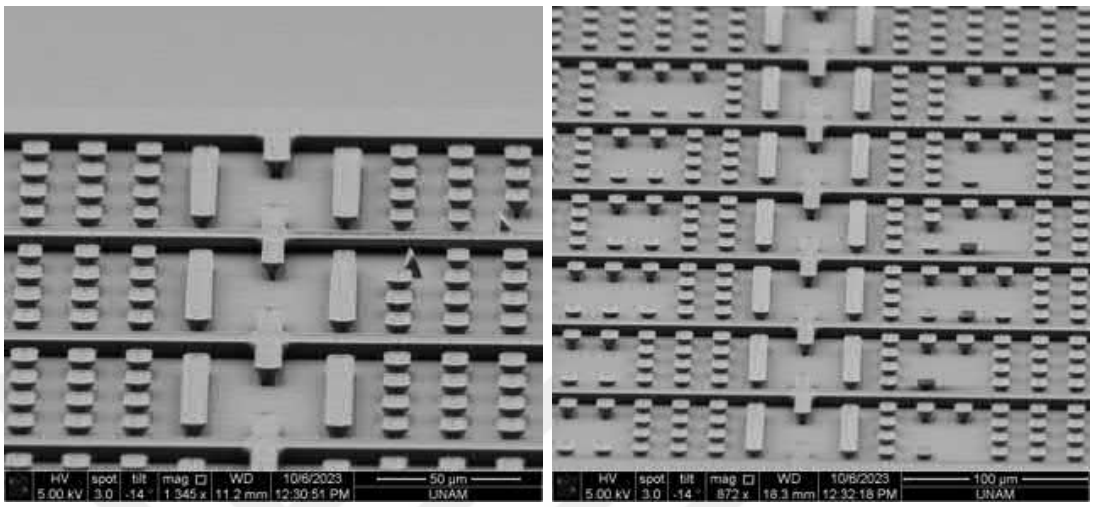
The optical microscope image in Figure 3.20 shows photoresist after development. The thick lines seen at the edges of the photoresist appear this way due to the negative wall angle. Without taking the SEM image, only an optical microscope can determine whether the negative angle is formed and how deep it is. These white stripes seen in Figure 3.20c are the parts where the negative angle is captured, and the gray-colored parts are the parts where the photoresist adheres to the surface. When the same sample was examined with SEM, it was understood that the angle was more than desired. As can be seen in Figure 3.21, the part of the photoresist adhering to the ground has decreased significantly and for this reason, some of the photoresists could not stand firmly upright and lay on their side.



(a) (b)

(c)

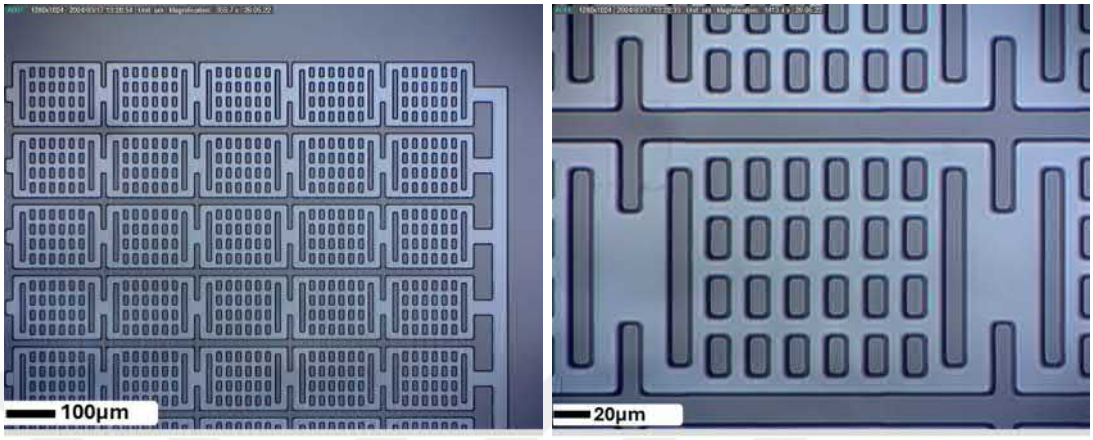
Figure 3.20: (a) Optical microscope image of the photoresist after development, (b) closer optical image, (c) closer optical image showing the negative side wall angle



(a) (b)

Figure 3.21: (a) SEM image of the photoresist after development showing uneven features, and (b) SEM image of the photoresist after development showing missing features due to inefficient process parameters

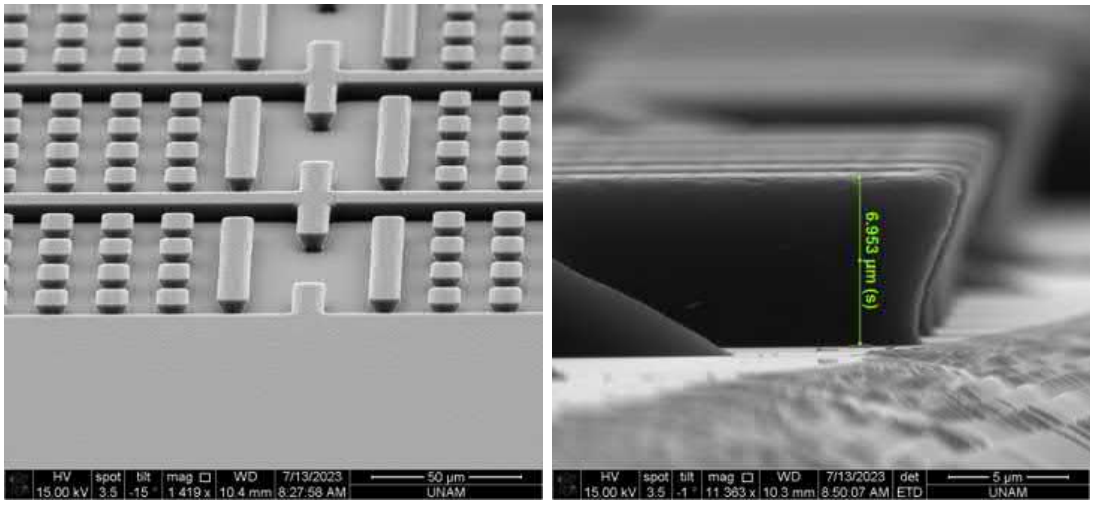
To solve this problem, which was encountered due to the process not being fully optimized, both soft-bake and development times were changed, and all other parameters were kept the same. In the new experiment, the soft-bake times applied after the first and second layering were increased from 10 seconds to 15 seconds and the development time was reduced to 60 seconds from 90 seconds. As a result of these changes in the process, the side wall angles obtained were improved and these angles were found sufficient to continue. Optical microscope images obtained after new improvements are shown in Figure 3.22.



(a) (b)

Figure 3.22: (a) Optical microscope image after optimization of the photoresist process, (b) closer optical image showing sufficient negative side wall angles

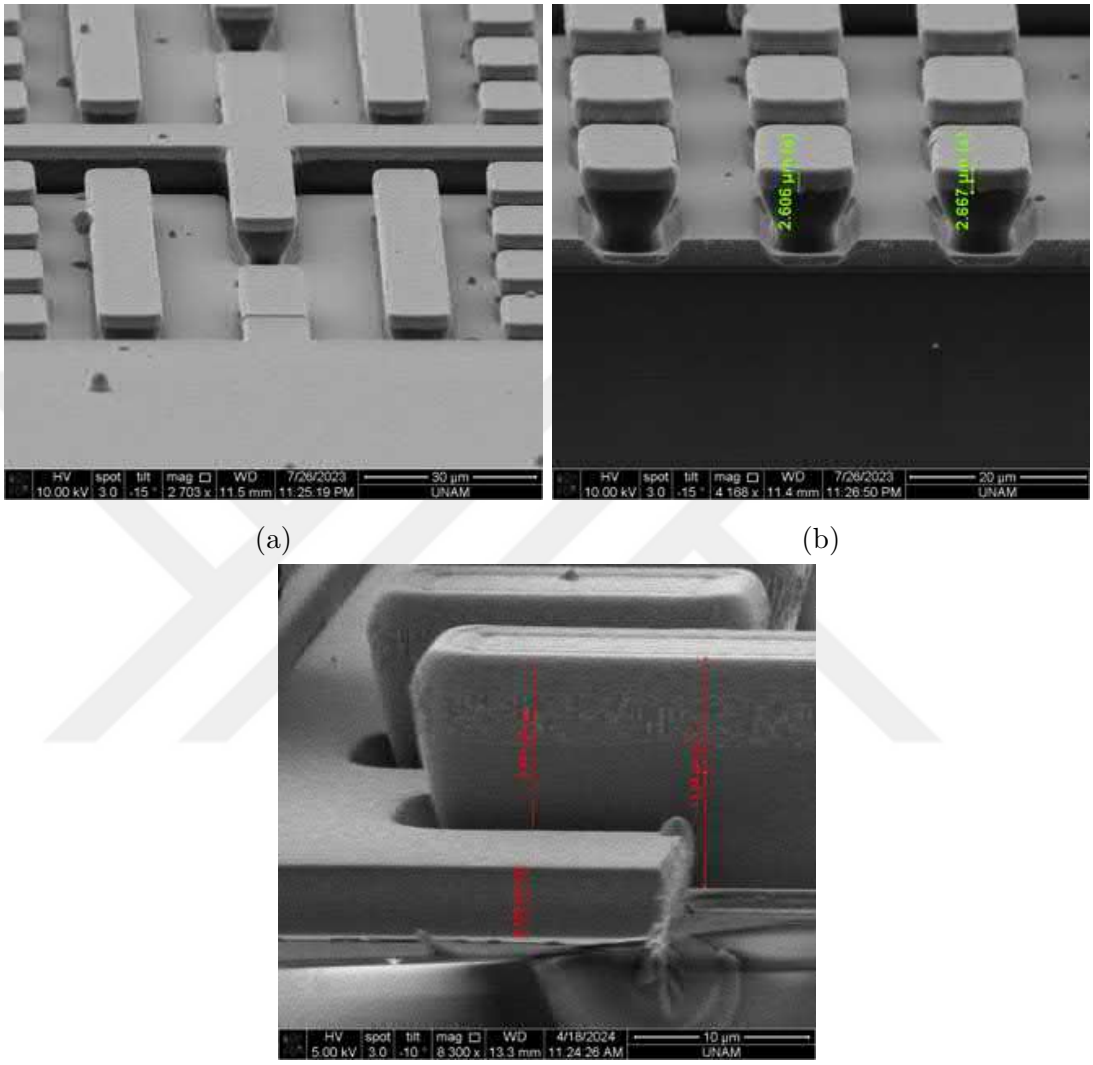
The wide edges that seen in the optical microscope images in Figure 3.20c in our previous experiment were narrower in this experiment. This increased the part of the photoresist that adheres to the substrate. As can be seen from the SEM images of this process in Figure 3.23, a proper negative wall angle has been obtained and sufficient contact with the surface has been achieved.



(a) (b)

Figure 3.23: SEM image of (a) optimized photoresist process after development, and (b) negative side wall angle

After the optimizations in the photoresist process are completed, the next step is the 4 μm thick upper membrane deposition. Before starting the actual wafer deposition, to follow the metal and photoresist profile coated at different thicknesses during e-beam deposition, a dummy wafer was coated step by step, and SEM images were taken. With e-beam deposition, first 50nm Ti and then 4 μm Cu were deposited step by step. Figures 3.24a and 3.24b show an SEM image of the wafer after depositing approximately 2 μm of copper, which is half of the target thickness, and full deposition which is approximately 4 μm shown in Figure 3.24c.



(a) (b)

(c)

Figure 3.24: (a)SEM image after 2 μm of copper deposition, (b)SEM cross-section image after 2 μm of copper deposition, (c)SEM image after 4 μm deposition

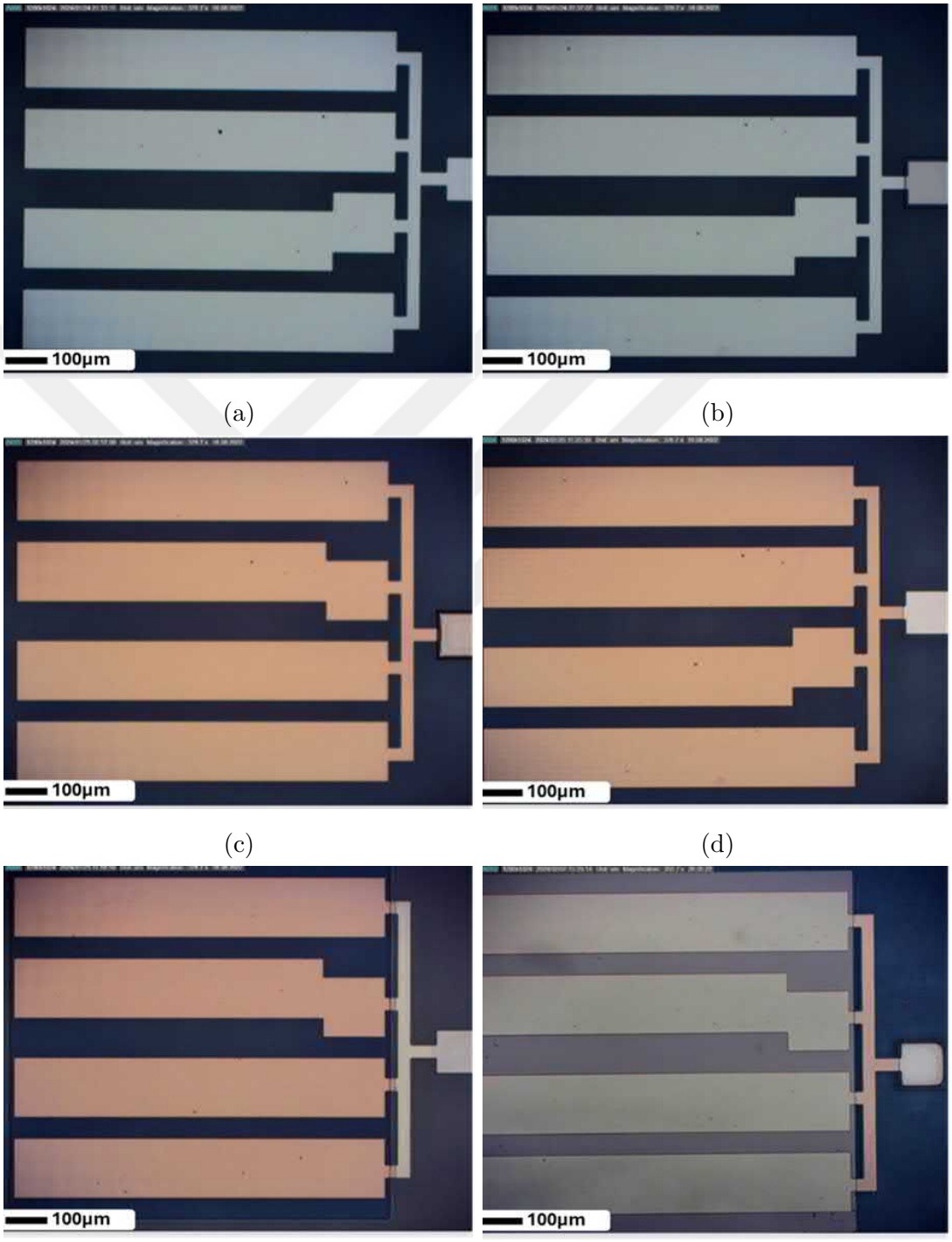
3.4 Second and Final Revision of PR-CMUT Microfabrication Process

As a result of the studies, a new photoresist method has been developed with which we can make 4 μm coating and lift-off it. After this stage, the production of PR-CMUT devices with the actual wafer will continue.

The work completed so far has consisted of experimental sets for both the development of unit processes and the identification of problems that may be encountered. Up to this stage, fabrication has progressed on Si-Wafer. The advantages and disadvantages of using Si-wafer are explained in detail in the previous sections. However, the actual fabrication of PR-CMUT can not be on Si-Wafer. The reason for this is that the wafer will be etched in XeF_2. As previously planned, future fabrication will continue with a clean Pyrex wafer. The problem of photoresist not adhering to HfO_2, which we encountered in the previous fabrication, will be tried to be eliminated by using SiO_2 layer deposited on HfO_2 layer in this fabrication instead of depositing Cr. This change will allow us to complete the fabrication with fewer steps and will prevent us from endangering the wafer by eliminating wet etching steps.

All steps in this trial are made exactly the same as the recipes in the previous steps, unless stated otherwise. In order not to repeat ourselves, recipes for the same steps are not given separately. However, process flow charts for all fabrications are included in Appendix-A.3. Visuals of this production flow are included in Figure 3.25. The bottom electrode was deposited in the same way as the previous fabrication. The image of this step is shown in Figure 3.25a. The next step for the fabrication is the formation of insulation layer. After the patterns were created with Mask 2 for dielectric deposition, the ICP descum process was completed. First 150nm HfO_2 was coated with e-beam evaporation and then 50nm SiO_2 was coated on HfO_2 without breaking the vacuum shown in Figure 3.25b, and 3.25c, respectively. After this step, the lift-off step was completed, the same as in previous fabrications shown in Figure 3.25d. Since it was no longer necessary to deposit the Cr layer, which was used as an adhesive layer, lithography was

performed with Mask 3, and the necessary features for sacrificial layer deposition were determined with photoresist. Following the completion of the ICP descum process, 600nm Poly-Si deposition was completed with e-beam evaporation and lift-off was performed as in the previous steps shown in Figure 3.25e, and 3.25f. The next step is to obtain the necessary patterning by photolithography shown in Figure 3.25a to etch the anchor parts with the ICP Bosch process. In this step, the ICP process continued until the SiO_2 color was reached as shown in Figure 3.26b. It was analyzed with EDX for a second checkpoint. Afterwards, newly developed multilayer thick photolithography with AZ 5214E image reversal photoresist was performed using Mask 5 with the multi-layer photoresist process developed for membrane deposition shown in Figure 3.26c.

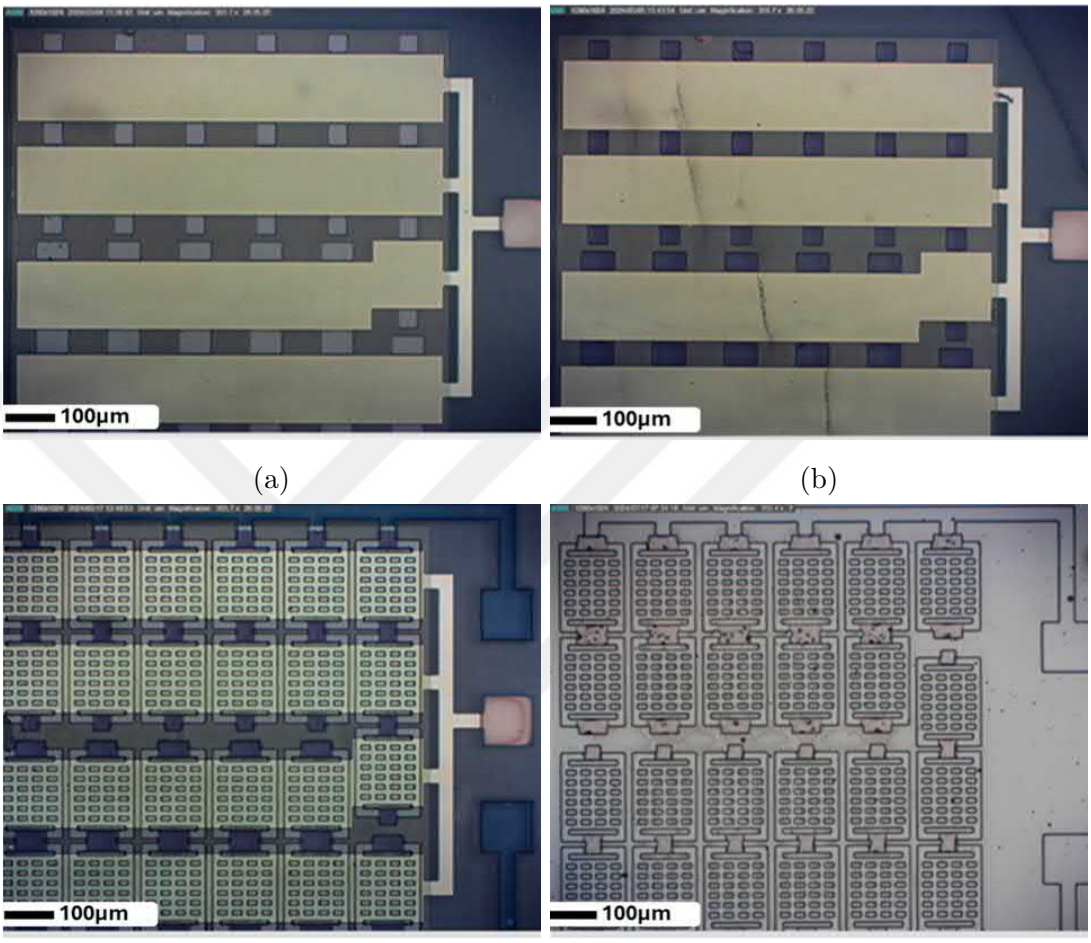


(a) (b)

(c) (d)

(e) (f)

Figure 3.25: (a) Bottom electrode deposition, (b) dielectric layer photoresist development, (c) after HfO_2 +SiO_2 deposition, (d) after lift-off, (e) sacrificial layer photoresist development, (f) Poly-Si deposition



(a) (b)

(c) (d)

Figure 3.26: (a)Anchor formation photoresist development, (b) after ICP bosch process, (c) top electrode photoresist development, (d) after 4 μm thick Cu deposition

Since everything was going smoothly up to this stage, experiments were carried out on a clean wafer to see any problems that may occur during the deposition of thick membrane or in the following steps before moving on to the next step with the real wafer. However, the optical microscope image was obtained after a single shot of 4 μm deposition on the actual wafer given in Figure 3.26d in order not to disrupt the flow. Additionally, Figure 3.27 includes images of the Pyrex wafer after the bottom electrode deposition and lift-off, dielectric deposition, and sacrificial layer deposition steps, respectively.

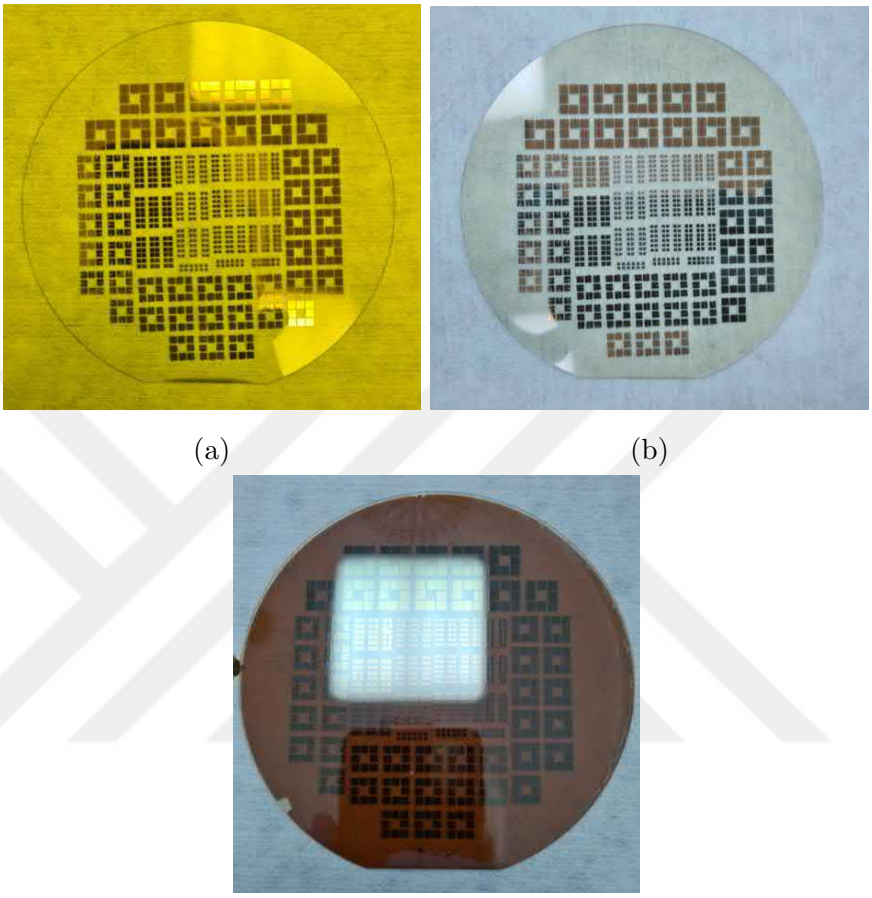
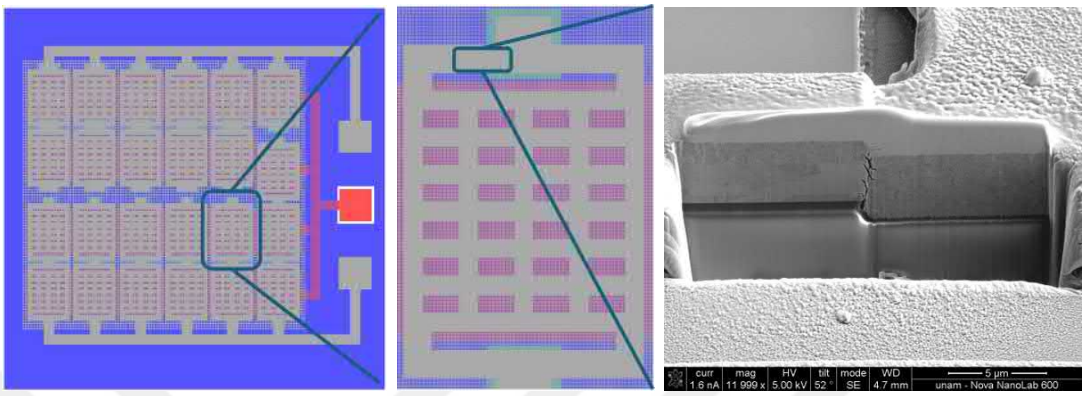


Figure 3.27: (a)After Bottom electrode deposition and lift-off, (b) after Dielectric layer deposition (HfO_2 and SiO_2), (c) after scrificial layer deposition (Poly-Si)

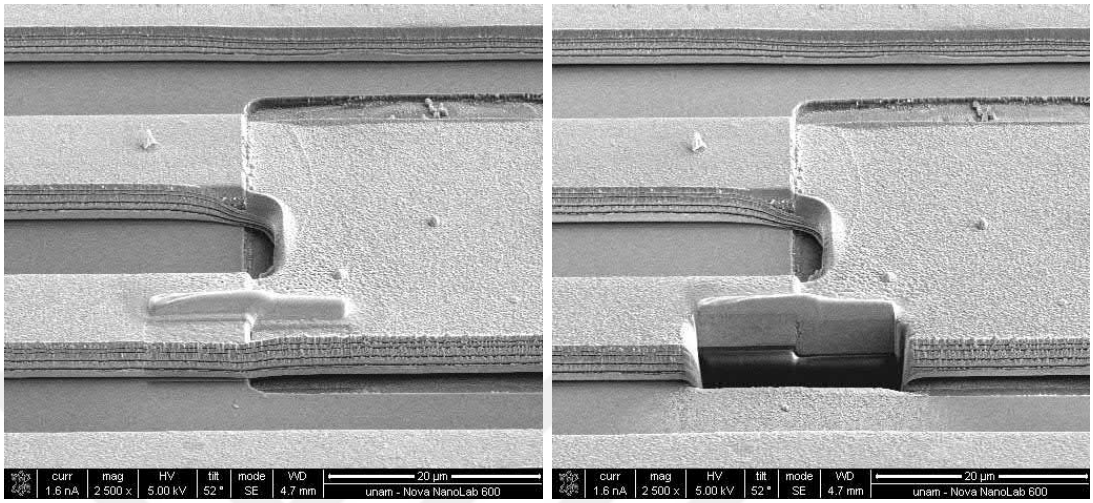
To optimize the process and outputs of thick membrane deposition, firstly a dummy wafer was used to develop this step. This new wafer was first coated with Poly-Si without using a mask. Afterward, the ICP Bosch process was carried out to form the anchors. After the photoresist coating process was completed with Mask 5, 50nm Ti and 4 μm Cu coating was carried out step by step as in the previous fabrication.



(a) (b) (c)

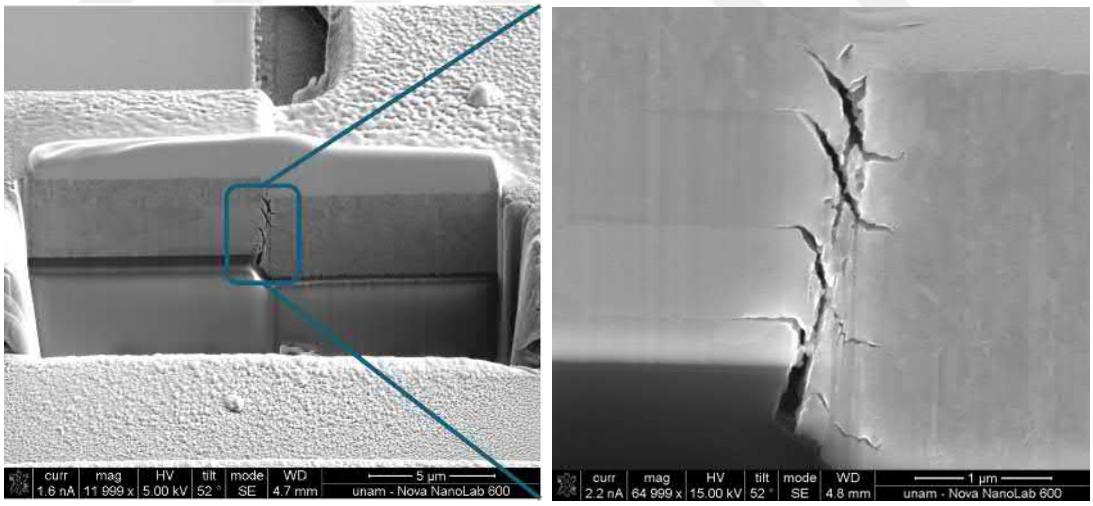
Figure 3.28: (a) Mask design to show the place of FIB cross-section, (b) closer image for this specific area, (c) FIB cross-section image

After deposition, FIB images were taken in the section we call "spring", which is the membrane transition in the anchor section shown in Figure 3.28. As can be seen in Figure 3.29b, crack formation was observed due to the vertical walls formed after the ICP Bosch process. While the main reason for these cracks is thought to be due to the vertical wall structure, another main reason is that the deposition was done in more than one step. Each deposition step and the cracks caused by these steps can also be seen in the FIB image shown in Figure 3.30.



(a) (b)

Figure 3.29: (a) Before FIB etching process image, (b) FIB cross-section image

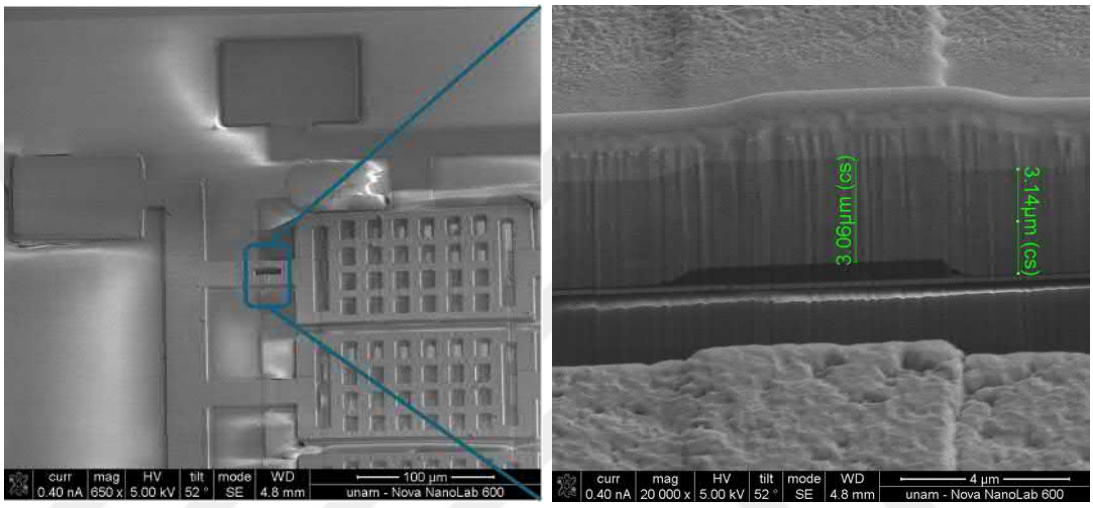


(a) (b)

Figure 3.30: (a) FIB cross section image, (b) closer FIB image

To minimize the crack formation, deposition was done in one shot 3 μm and the FIB cross-sectional images were taken and examined again for the deposition. As can be seen in Figure 3.31, crack formation has been greatly reduced, but step coverage has not been improved enough to completely eliminate these defects. To completely remove this crack formation, it was decided that the solution was

to reduce the wall angle. However, since it was not feasible to uniformly reduce this angle with the silicon etch tool (Si ICP) in our cleanroom, other solutions have been focused on. As we can see from the FIB images, we can obtain the necessary angle after lift-off to ensure a smoother transition.



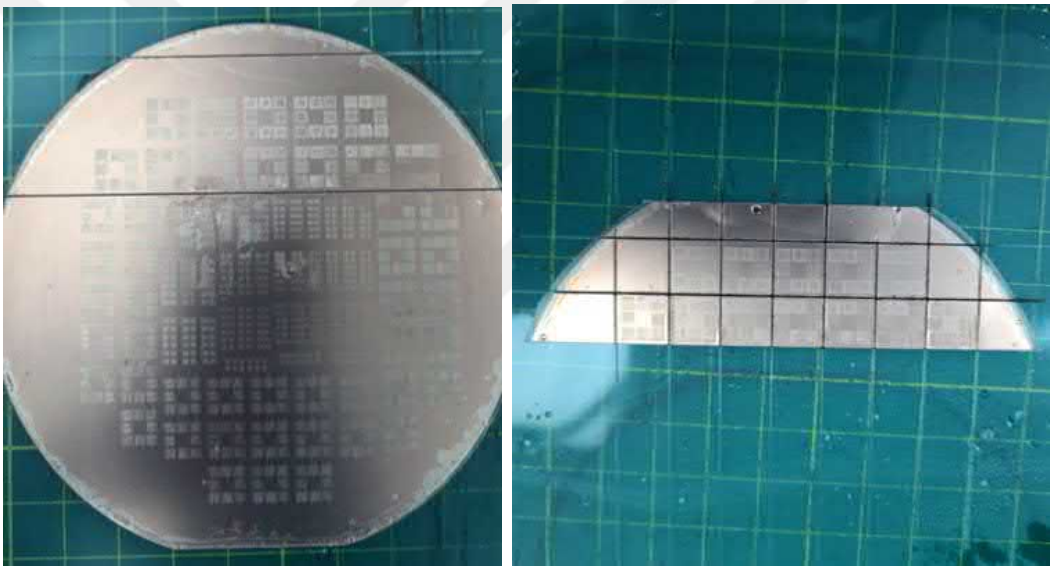
(a) (b)

Figure 3.31: (a)FIB cross section image, (b) closer FIB image

To achieve such a smooth transition in the anchors, the masks were modified, and the 3rd and 4th masks were combined into a single mask. In this way, it is aimed to keep the anchor parts empty during the Poly-Si lift-off step of the process. The new process flow created with this change is explained in detail in the 4th flow chart. Although it will be a smoother step transition, it was thought that taking a break while evaporating the Cu would cause stress and negatively affect the mechanical properties of the membrane, so it was deemed appropriate to deposit the membrane in one shot in the new fabrication process flow. This flow could not be realized yet due to time constraints. Since it would not be possible to work with new masks due to lack of time, it was decided to continue with the wafer we had. After this step was developed on the dummy wafer, it was thought that it was ready to be applied to the real wafer. Since these vertical walls were formed during silicon etch on the real wafer and since it was not feasible to uniformly reduce this angle with the silicon etch tool (Si ICP)

in our cleanroom, it was decided to continue by doing this deposition in a single shot.

After deposition shown in Figure 3.26d, the dicing step was started without continuing the lift-off step. In this step, dicing tape was adhered both on the wafer and under the wafer to protect the devices on the surface. Individual chips were obtained by separating the wafer into larger pieces and then into smaller chips with the help of a Dicing Saw equipment as shown in Figure 3.32.



(a) (b)

Figure 3.32: (a)Wafer with dicing tape after first dicing, (b) individual chips after dicing

After this process, the next step is to get rid of the dicing saw tape pieces that were stuck to the chips of the wafer. For this purpose, the dicing tape was first tried to be removed by reducing the adhesive strength of the dicing tape by UV exposure. The dicing saw tape attached to the bottom of the wafer (the side where there were no devices) came off easily after UV exposure. However, the tape on the PR-CMUT side (device side) where the devices are located did not come off even though the UV exposure dose was increased. As a solution to this dicing tape removal difficulty problem, the diced chips were kept in acetone and

sonicated for 1.30 hours. This way, the dicing tape was completely separated from the surface of the chips. While the chips were kept in acetone and interacted faster with the help of the sonicator, the tape was separated and the lift-off process was carried out simultaneously. After the individual chips are separated from the dicing tape on the surface as shown in Figure 3.33, we can continue with the XeF_2 etch part and the preparations before XeF_2.

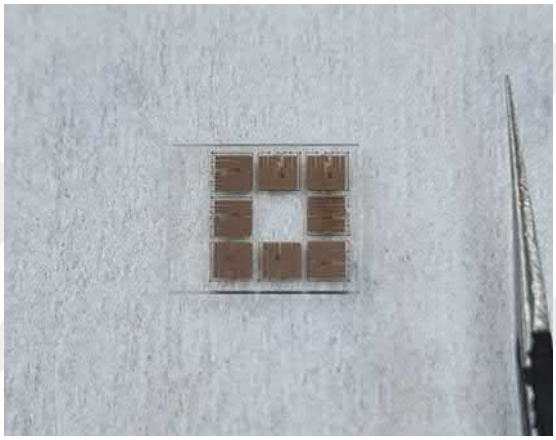


Figure 3.33: Individual chip after removal of dicing tape and lift-off

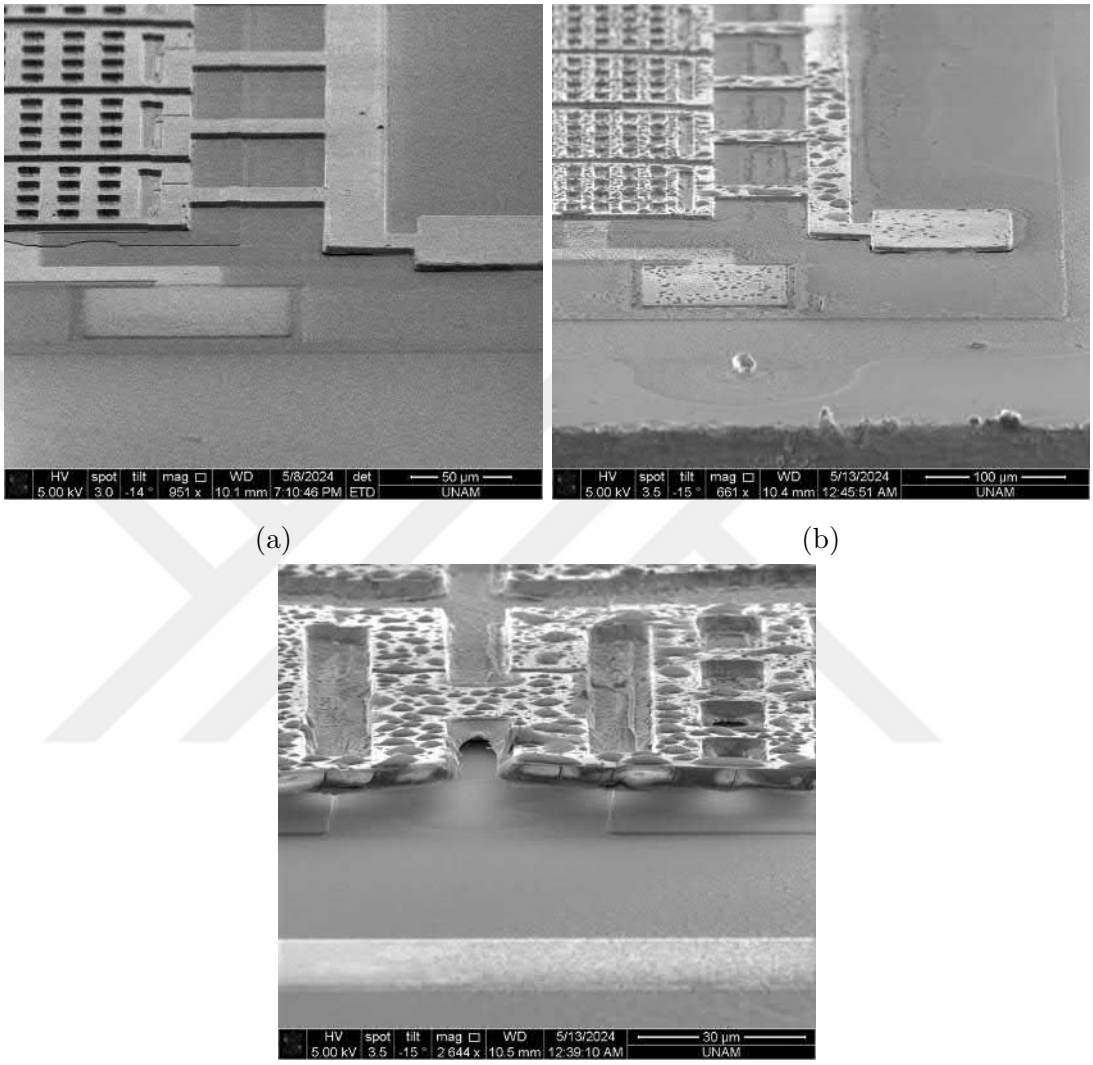
3.5 Sacrificial Layer Release with XeF_2

This part details the experimental procedures employed to investigate the effects of various etching parameters on the surface quality of copper, dielectric, and Pyrex surfaces and the etch rate of XeF_2 on Poly-Si. The experiments mainly focus on the effects of XeF_2 cycles, Piranha etch times, baking times and temperatures, and BOE etch times. The objective is to identify optimal conditions for achieving a smooth surface at the same time with a fully complete Poly-Si etch. The parameters of each experiment are presented in Table 3.1.

Experiment Number	Xenon Difluoride Cycles	Piranha Etch Time	Bake Time	BOE Etch Time
1	25	-	5 min 110°	-
2	25	-	30 min 120°	20sec
3	45	-	30 min 120°	20 sec
4	150	-	30 min 120°	20 sec
5	45	5 sec	30 min 120°	20 sec
6	70	5 sec	30 min 120°	20 sec
7	20+50	-	30 min 120°	20 sec

Table 3.1: XeF_2 Etching Process Parameters

Different combinations of parameters have been applied to find the optimum process. For the experiments, XeF_2 cycle parameters were set as follows: XeF_2 pressure:3.5 Torr, cycle time:600 seconds, and pump-out pressure: 400 mTorr. The first experiment involves baking the chips for 5 min at 110°C to remove moisture not to affect the XeF_2 etching. After baking the chip, 25 cycles of XeF_2 etching have been applied. SEM images before and after the XeF_2 process are shown in Figure 3.34.



(a) (b)

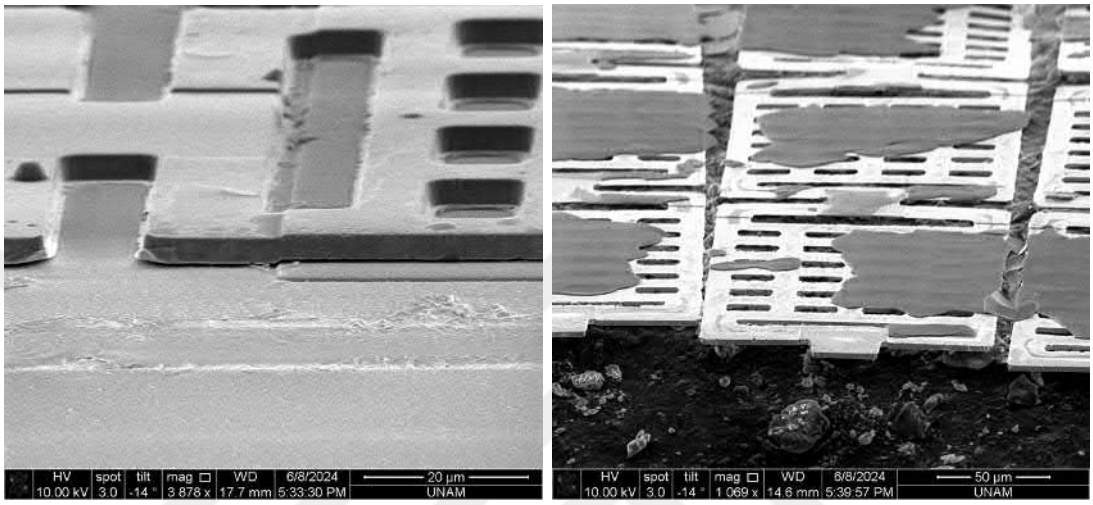
(c)

Figure 3.34: (a)SEM image before XeF_2 Etch, (b) SEM image after XeF_2, (c) closer SEM image after XeF_2 etching

After XeF_2 etching, different formations were observed on the copper surface. It is thought that the main reason for these changes may be due to not baking the chip for sufficient time and temperature.

For the second experiment, another sample was carefully put into BOE solution for 20 seconds to get rid of any native oxide on the Poly-Si layer. After BOE, the wafer was rinsed with DI water and followed by a baking process for 30 min

at 120°C to stabilize the surface and remove any moisture from the surface. The sample was subjected to 25 cycles of XeF_2 etching after baking.



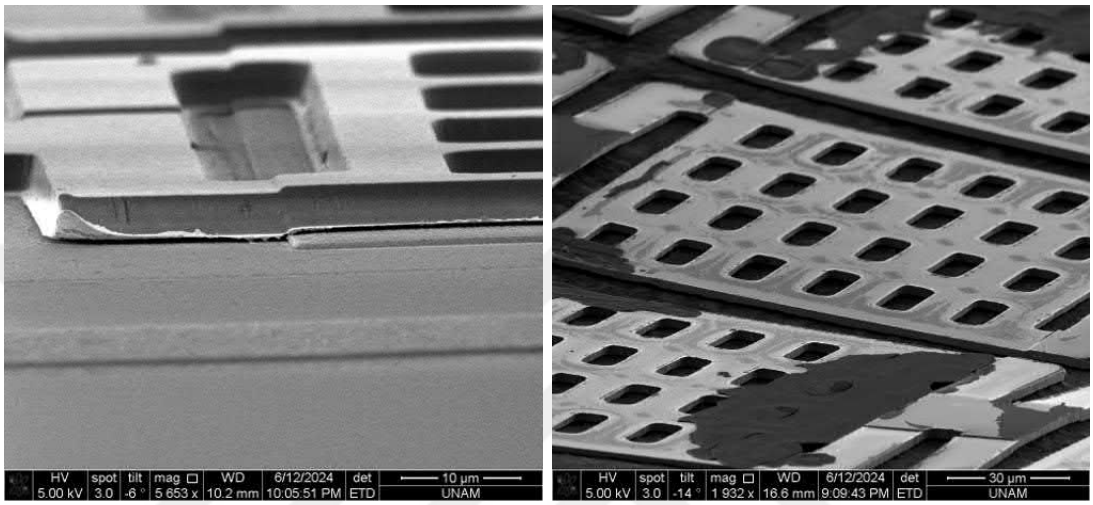
(a) (b)

Figure 3.35: (a)SEM image after Experiment 2 XeF_2 Etching, (b) SEM image of back side of the membrane

As can be seen from the SEM image in Figure 3.35a, increasing the baking time results positively. The formations we encountered before were not seen this time. However, XeF_2 etching was not sufficient, and the entire Poly-Si layer could not be removed. To understand this better, carbon tape was placed onto the membranes in a part of the sample and peeled off. Figure 3.35b shows the SEM image of the back sides of the CMUT membranes. The dark-colored parts seen on the membrane are the dielectric layers separated from the device. The reason why these layers are removed along with the membrane is that the Poly-Si layer in between is not completely etched, so Poly-Si clings to the dielectric and the membrane together. When the membrane is removed, the dielectric layer also comes along. Additionally, no negative effects of BOE implementation were encountered.

For the third experiment, XeF_2 etch time increased, and it was expected to see better etching for the sacrificial layer. BOE etching was done for 20 seconds, and the sample was then rinsed with DI water. After 30 min of baking the chip

at 120°C, there were 45 cycles of XeF_2 etching. When comparing this experiment with Experiment 2, the only difference is the XeF_2 etch time.

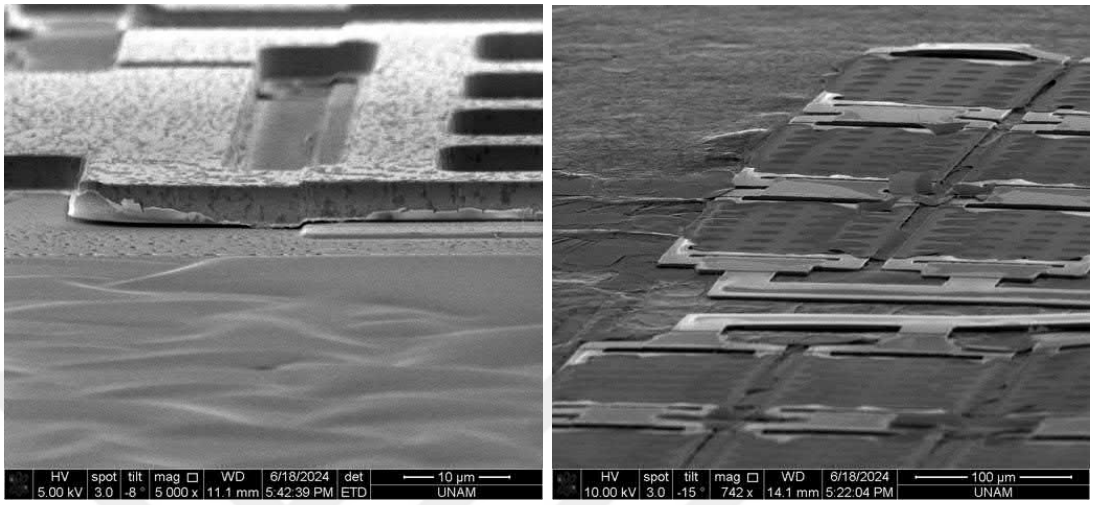


(a) (b)

Figure 3.36: (a) SEM image after Experiment 3 XeF_2 Etching, (b) SEM image of back side of the membrane

The results showed in Figure 3.36, both the copper and dielectric surfaces achieved good surface quality. Also, XeF_2 etch rate was higher than the Experiment 2. It can be concluded from this experiment that increasing the etch time of XeF_2 affects positively but still the etching was not enough to remove sacrificial layer completely.

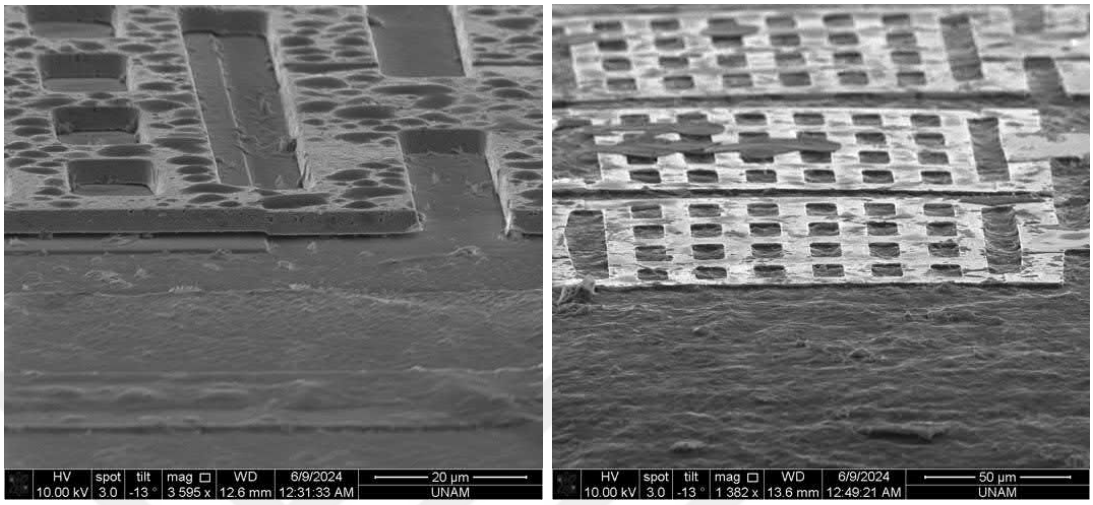
For the fourth experiment same as the second and the third experiment BOE and baking have been done with same parameters. Again, XeF_2 etch time increased from 45 cycles to 150 cycles to get rid of the sacrificial layer. Contrary to expectations, the Poly-Si etch rate of XeF_2 was very low, as can be seen from the large amount of dielectric part adhered behind the membrane in Figure 3.37b. Even the etch rate obtained in Experiments 2 and 3 could not be achieved in this experiment. In addition, the dielectric surface also lost its uniformity, as shown in Figure 3.37a. It was observed that the copper surface quality also decreased.



(a) (b)

Figure 3.37: (a) SEM image after Experiment 4 XeF_2 Etching, (b) SEM image of back side of the membrane

In the fifth experiment, a different approach was followed to get rid of the lift-off flags. These lift-off flags are unintended deposits of copper and titanium in areas where deposition was not intended. The excessive lateral width caused by the high negative slope undercut is one of the causes of these lift-off flags. It was important to remove these lift-off flags because they could cause a short circuit if they move with the membrane and come into contact with the surface when voltage is applied to the device. To address this issue, Piranha Solution, which can etch both copper and titanium, was used. A brief 5-second 1:20 DI water diluted Piranha etching, sample was applied to get rid of lift-off flags. Following the Piranha etching sample rinsed with DI water, and BOE etch was performed for 20 seconds to remove native oxide. The sample was baked for 30 min at 120°C, and 45 cycles of XeF_2 etching was done.

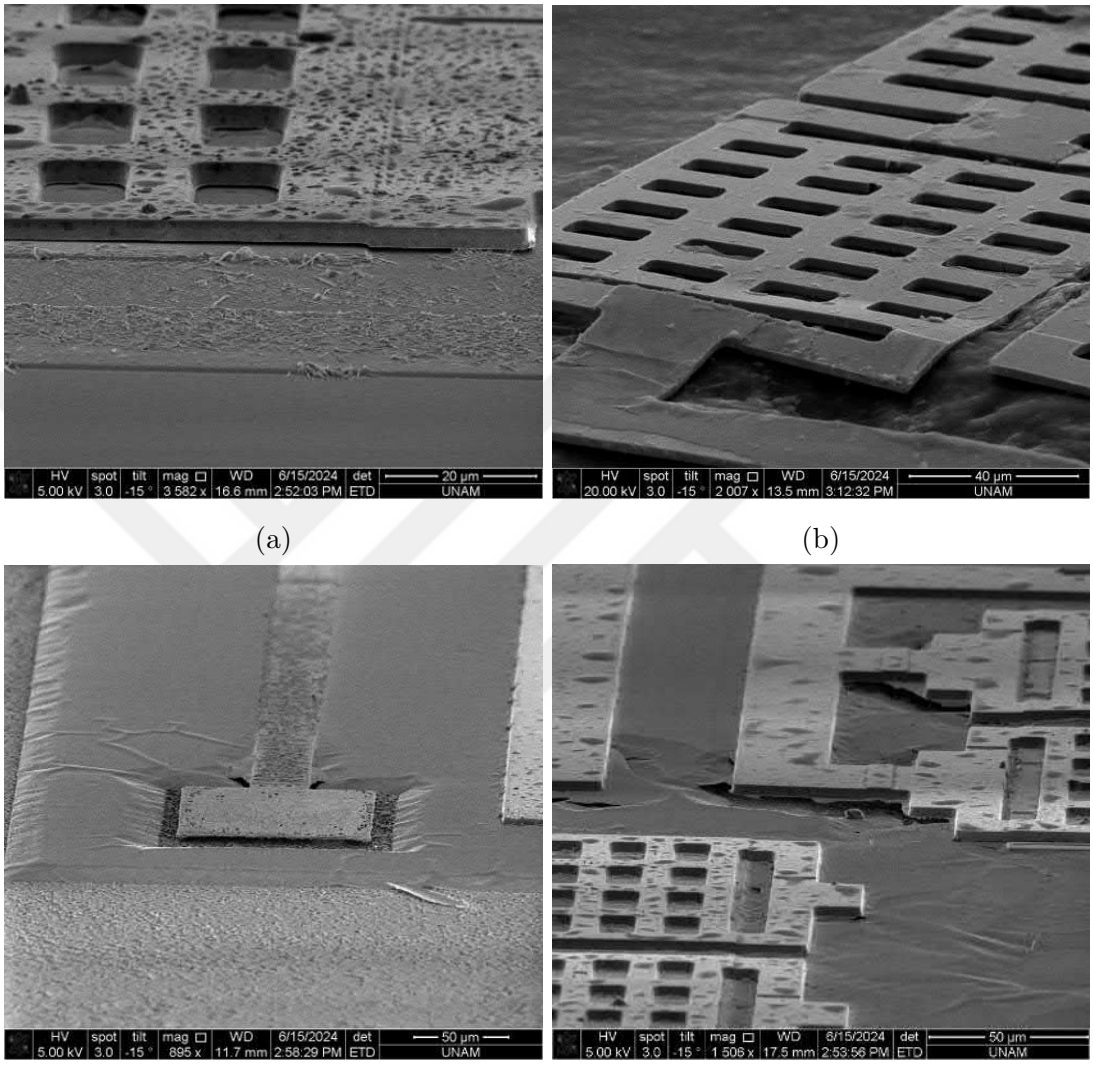


(a) (b)

Figure 3.38: (a) SEM image after Experiment 5 XeF_2 Etching, (b) SEM image of back side of the membrane

At this stage, different formations were observed. It is thought that the reason for these formations is Piranha etching. By looking at the range marked etch rate, it is observed that etching occurs. When the back surface of the membrane in Figure 3.38b is examined, it is seen that less dielectric layer is removed with the membrane compared to Experiment 2 and 4. It is concluded from these images that a better etch is obtained.

Although the surface quality obtained with Piranha was insufficient, it was aimed to etch at least completely the Poly-Si layer by increasing the XeF_2 time and the sixth experiment was arranged accordingly. By keeping the other parameters, the same as in experiment 5, only the XeF_2 etch cycles were increased from 45 to 70, to aim better etch result. Figure 3.39 shows the results after XeF_2 etch.



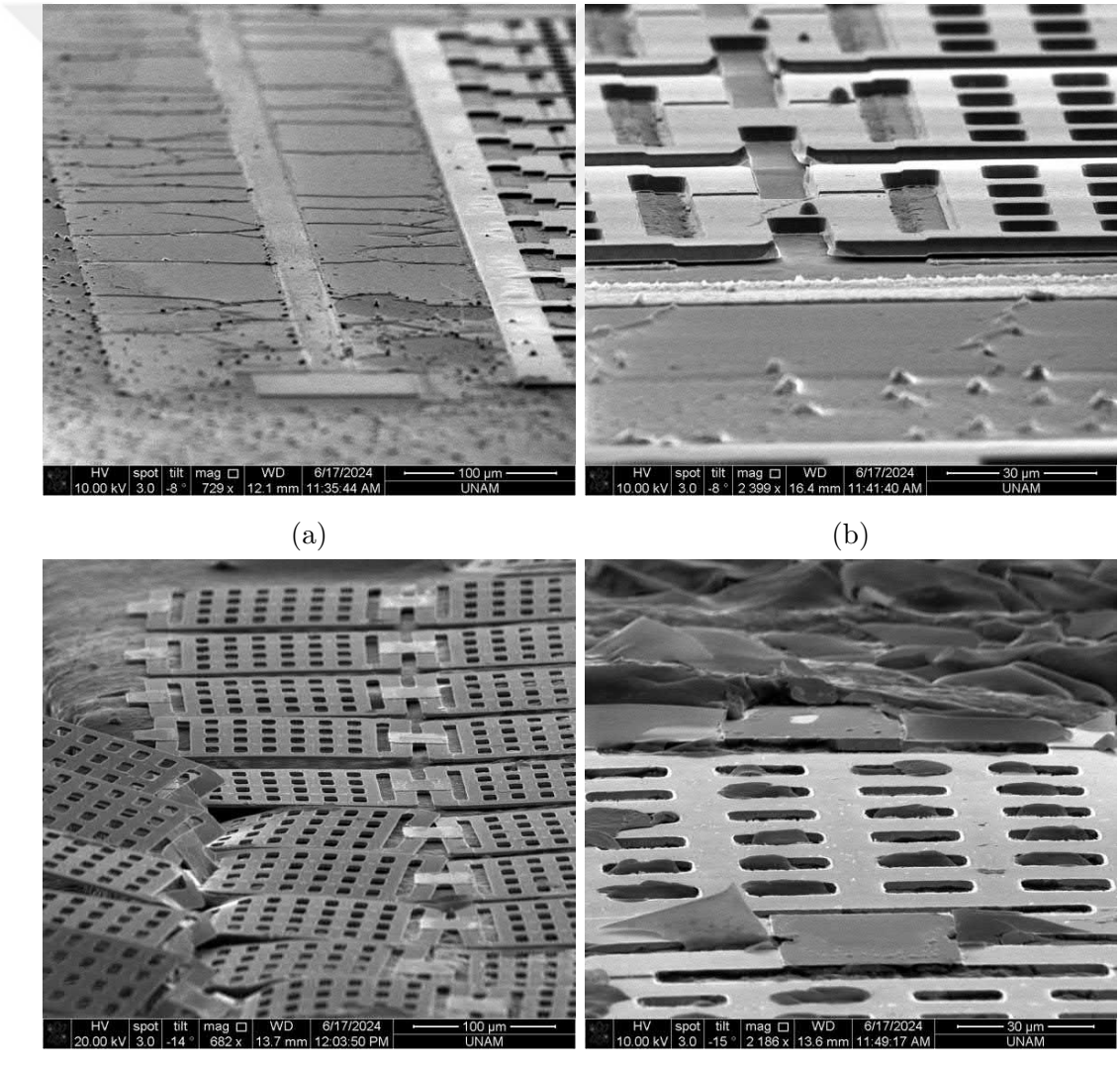
(a) (b)

(c) (d)

Figure 3.39: (a) SEM image after Experiment 6 XeF_2 Etching, (b) SEM image of the back side of the membrane, (c) SEM image of pad area of the device, (d) SEM image of the dielectric layer

As shown in Figure 3.39a, although the surface quality is still poor as expected, it is concluded that there is almost no adhered material on the back side of the membrane in Figure 3.39b and the etch rate was good. However, as can be seen in Figures 3.39c and 3.39d, it was observed that the dielectric layer was negatively affected after this process.

In experiment 7, the aim was to get rid of the lift-off flags again. For this purpose, the sample was first kept in BOE for 20 seconds to etch the native oxide. Then, it was rinsed with DI water and kept at 120°C on the hot plate for 30 min. Afterward, 20 cycles of XeF_2 etching were performed, and the sample was placed in a container filled with acetone and kept in the sonicator for just 1 second. The sample was then rinsed again and applied for another 50 cycles of XeF_2.



(a) (b)

(c) (d)

Figure 3.40: (a) SEM image of dielectric cracks after Experiment 7 XeF_2 etching, (b) SEM image of partial gap formation, (c) and (d) SEM image of back side of membrane

The aim here was to disconnect the lift-off flags from the surface after the first 20-cycle etch and allow them to quickly break off from the surface with the help of a sonicator in acetone. However, cracks occurred on the dielectric surface during the sonicator as shown in Figure 3.40a. Cracks were not observed in the device part, only the dielectric parts coated on the Pyrex substrate were observed to crack. Additionally, even though the entire Poly-Si layer has still not been completely etched, the gap formation is higher than in previous attempts as seen in Figure 3.40b. Due to time constraints, experiments to fully release the sacrificial layer could not be continued from here on.

Chapter 4

Characterization

4.1 Principles and Operation of Optical Profilometry

An optical profilometer is a non-contact measurement tool that provides highly accurate surface topography characterization. Without actually touching the sample, it uses optical methods like laser triangulation or white light interferometry to capture surface details [43–47]. The optical profilometer directs the light from a wide-spectrum light source, usually white light, to the surface [43–45]. This light is split into two separate beams with the help of a beamsplitter. One of the beams (the reference beam) is directed to the reference mirror, and the other beam (the measurement beam) is directed to the sample surface. The measurement beam reflects from the sample surface and recombines with the reference beam. The difference in the path lengths of the two beams results in an interference pattern when they recombine. The interference pattern is a result of constructive and destructive interference between the two beams. The surface topography of the sample can be identified by this pattern [46]. The interference pattern is captured by a detector, usually a CCD camera. After that, the pattern is examined through advanced algorithms to precisely reconstruct the

sample's surface profile down to the nanometer scale [46–48]. This makes it possible to characterize step heights, surface roughness, and overall topography in high levels of detail. The design of the profilometer is also included in Figure 4.1. This system includes complicated elements such as an LED light source, camera, beamsplitter, and mirror objective.

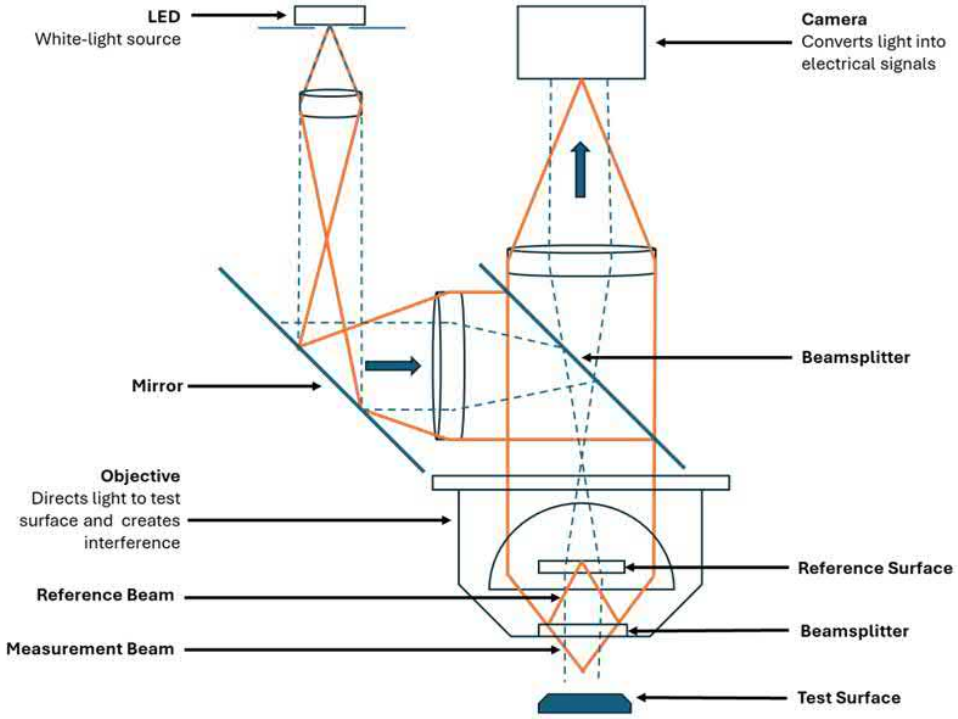


Figure 4.1: Optical Profilometer working principle

The white light interferometry (WLI) system can be adapted for use in measuring periodic oscillations of MEMS devices or sensors [49, 50]. This adaptation includes a two-channel signal generator that drives the sample to create harmonic motion and stroboscopic connections that synchronize the profilometer with the signal generator. The sample is illuminated with short light pulses, and the sample is made to "appear static (frozen)", and the sample can be captured in different motion states by adjusting the phase between the illumination and the driving signal.

The measurement starts with the harmonic motion of the sample with the help of a two-channel signal generator [51]. While one channel drives the sample, the other channel controls the timing of the stroboscopic illumination. Synchronization plays a crucial role at this stage because it is important to be able to freeze the motion instantly and to obtain images in the same phase in every place of the sample. By carefully adjusting the phase relationship between the illumination and the driving signal, the motion behavior of the sample at different points of the oscillation cycle can be examined. The information obtained as a result of this measurement provides valuable insights into the dynamic behavior and structural character of the sample. As seen in Figure 4.2, where the stroboscopic relationship is shown, an image is taken at a certain phase by sending a short light pulse and this is taken repeatedly at the same phase.

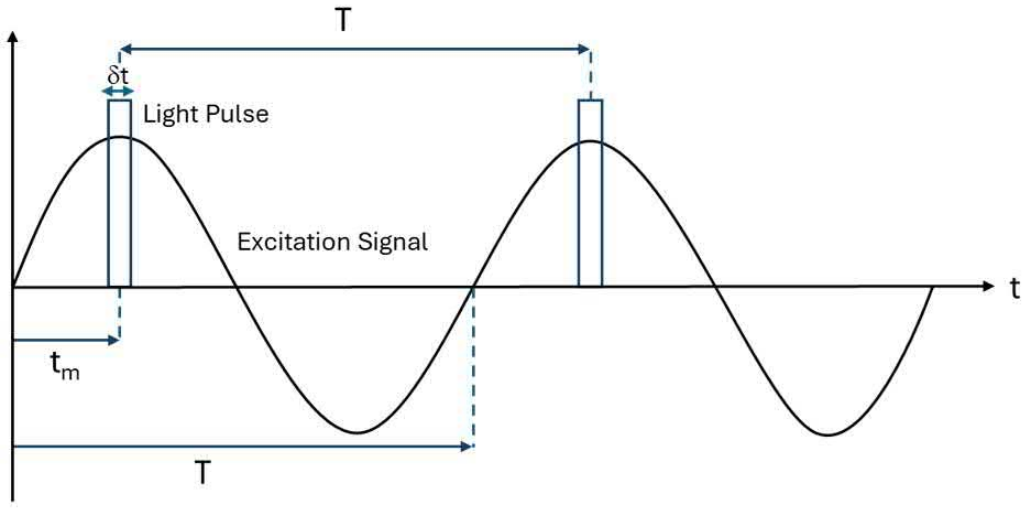


Figure 4.2: Illustration of signal in stroboscopic interferometry

These systems can measure vibrations from a few Hz to several MHz, and with advanced supercontinuum sources, even up to tens of MHz. Stroboscopic pulses can have a duration of up to 50 ns, and they can even be shorter with certain picosecond sources, which could allow vibrations at frequencies of hundreds of MHz to be measured [52, 53].

4.2 ZYGO Optical Profilometer Dynamic Metrology Module

The ZYGO Profilometer is an advanced optical metrology instrument used for precise surface measurements. It operates based on interferometry principles, specifically utilizing white light interferometry (WLI) to generate high-resolution surface topography maps. ZYGO Profilometer is a device that contains sophisticated hardware and software capable of measuring different surfaces and structures, including microelectromechanical systems (MEMS).

The ZYGO Dynamic Metrology Module (DMM) expands the capabilities of the profilometer in dynamic applications by allowing measurements of moving MEMS devices.

The Dynamic Metrology Module (DMM) includes several key components designed for advanced measurement applications. To begin with, it includes the MetroPro Dynamic application (Dynamic.app), which is necessary for examining dynamic behaviors of samples. A TEGAM Arbitrary Waveform Generator (AWG) that offers flexible signal generation capabilities is also incorporated into the module. The TEGAM 2350 Dual Channel High Voltage Amplifier, which is essential for amplifying signals to the required levels for accurate measurements, is the last component of the DMM. When combined, these elements allow for accurate and precise dynamic metrology. The actual image of the entire system is in Figure 4.3 and its schematic representation is in Figure 4.4.

Figure 4.3: Complete setup of the ZYGO Optical Profilometer dynamic measurement

The dynamic application freeze-frames the MEMS device's motion by synchronizing the strobe light source in the NewView interferometer with a driving signal from an Arbitrary Waveform Generator. Using the stroboscopic light source, the motion of MEMS device can be efficiently frozen. MetroPro generates several data files when the device is moving, provided the software controls and LED strobing are appropriately configured.

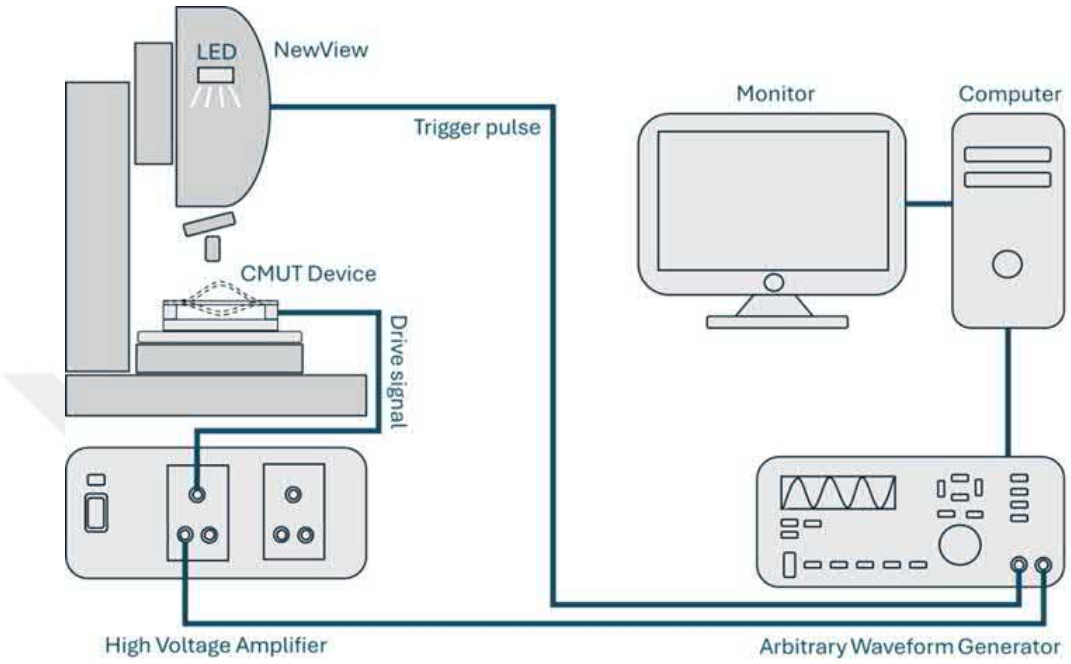


Figure 4.4: Schematic of dynamic measurement setup

Several measurement modes are available on the Dynamic Metrology Module (DMM) to accommodate diverse dynamic analysis requirements. In Single Measurement Mode, DMM captures a single measurement for CMUT devices using a specific drive signal and phase delay. Frequency Sweep Mode allows the device to be measured while the frequency is varied across a desired range with a fixed phase delay. In Phase Sweep Mode, the frequency remains constant while the phase delay is varied. Lastly, Phase and Frequency Sweep Mode simultaneously adjusts both phase and frequency to drive the device, providing a comprehensive analysis of its dynamic behavior.

The electrical characteristics of the same samples were measured using an impedance analyzer in addition to the optical measurements made with the ZYGO profilometer. Important information about capacitance, impedance, and other electrical properties of MEMS devices can be found with the Impedance Analyzer [54]. By comparing the results from both the ZYGO profilometer and the Impedance Analyzer, a comprehensive understanding of the device performance can be achieved.

The ZYGO Dynamic Metrology Module has been used in our experiments to conduct phase sweep, frequency sweep, and combined phase and frequency sweep measurements. These measurements were essential for examining the dynamic responses of MEMS devices to varied excitation conditions. To verify the optical measurements and acquire a better understanding of the behavior of the device, the outcomes were then contrasted with those derived from the Impedance Analyzer.

4.3 Characterization Measurements

Experiments with the ZYGO Optical Profilometer Dynamic Module were initiated in parallel with the microfabrication of the PR-CMUT devices. Since the PR-CMUT devices were not ready for measurement during the ZYGO Dynamic Module experiments, another CMUT device that was previously fabricated was used in these experiments. The aim here is to understand the operating principles of the ZYGO Optical Profilometer Dynamic Module equipment and to create an infrastructure that can accurately and reliably characterize PR-CMUT devices as soon as they are fabricated.

The first measurement (Measurement 1) is a static measurement. This measurement was conducted by increasing the DC voltage alone, without the application of any AC voltage. The aim here is to understand the breakdown voltage or collapse voltage value of the circular CMUT device (CMUT device #1) under test. After this information is obtained, it is aimed to determine the voltage range in which we can work. At the end of the measurements, the circular CMUT device (CMUT device #1) became unusable because the breakdown voltage value of the circular CMUT device (CMUT device #1) was exceeded, and measurements were continued with another circular CMUT device (CMUT device #2).

In the next measurement (Measurement 2), measurements were taken between 1-1000kHz with the Impedance Analyzer to determine the resonance frequency of the CMUT device (CMUT device #2). To understand whether the results were

compatible with the Impedance Analyzer result, the resonance frequency was measured with the ZYGO Optical Profilometer (Measurement 3). The issue that should be taken into consideration here is that the same excitation parameters could not be used on the same CMUT device (CMUT device #2) due to the limitations of both of the characterization devices (ZYGO Optical Profilometer and Impedance Analyzer). The highest DC voltage value can be applied with the Impedance Analyzer is 40 V and AC can be applied at most as 1 V. Such low AC and DC voltage values cannot be applied simultaneously with the ZYGO Optical Profilometer setup.

The resonance frequency was measured at various voltage levels using the Impedance Analyzer (Measurement 4). Additionally, another measurement (Measurement 5) was conducted by ZYGO applying a phase shift to observe the membrane movement of the CMUT device at resonance frequency.

4.4 Explanation of Data Analysis Software

After the measurements were performed using ZYGO Optical Profilometer, the results should be analyzed. Analysis of even one measurement manually is impractical, since a sweep in frequency or phase (or both) is performed with each measurement. Each sweep may produce hundreds or thousands of data points. To mitigate this, an algorithmic approach was developed.

Each data point was obtained in ".dat" format. To load each data point in the correct form for processing, a software called "Gwyddion" was used. Gwyddion is a free and open-source software that is primarily used for scanning probe microscopy (SPM) data analysis like Atomic Force Microscopy (AFM), Scanning Tunneling Microscopy (STM), Magnetic Force Microscopy (MFM), and Near-field Scanning Optical Microscopy (NSOM) [55]. It supports multiple data formats and offers functionalities for data manipulation, such as leveling, filtering, and statistical analysis. Additionally, Gwyddion is extendable through plugins and

modules, allowing for custom analysis methods and processing routines. Gwyddion can be controlled using its Python API. Each data point was loaded by controlling Gwyddion software. Here's an example of such data point:

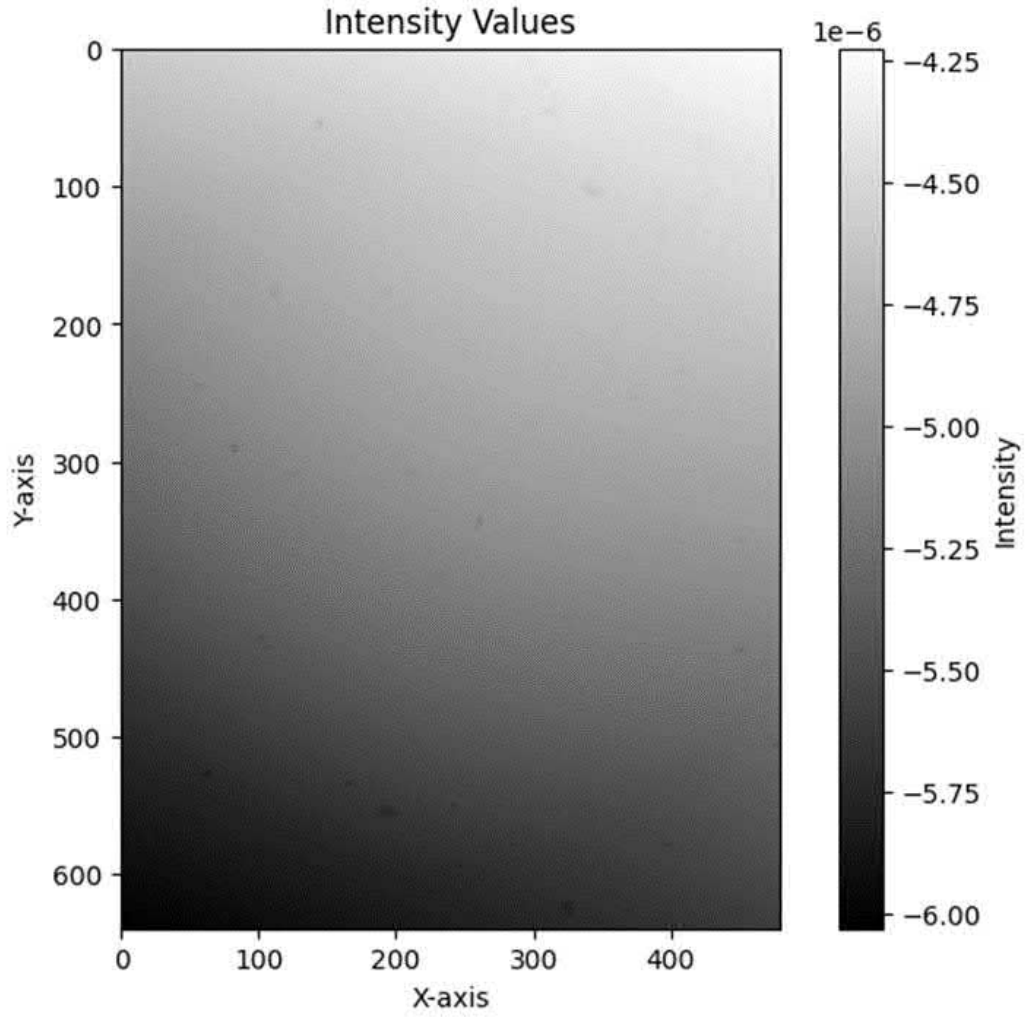


Figure 4.5: Example data point loaded using Gwyddion

The collection process often experiences significant tilting due to the alignment of the setup. This severe tilt greatly affects the accuracy of the displacement calculation, as it dominates the actual data being measured. The severity of the issue is evident when observing Figure 4.5. In Figure 4.5, a clear tilt can be seen along the axis which can be denoted by "X=Y" line equation (from the bottom-left corner to top-right corner). Also, it is evident that no clear observations can

be seen, due to the dominant tilt.

To make the observations clear and comparable to other experiments, one needs to address the tilt issue first, before conducting any kind of data analysis study.

A certain transformation should be applied to the data. Two simple transformations that can handle such issues are rotation and elevation adjustment (z-axis transformation). One may want to find the "plane underneath" of the device, observe the parameters of the rotation and elevation parameters of the plane, and find the inverse transformations to level the data.

A plane is a two-dimensional surface that extends indefinitely. A plane can be defined using the following mathematical expression:

$$ax + by + d = z \tag{4.1}$$

Where a,b and d are constants that define the rotation and bias (position) of the plane in 3D space. The (x, y, z) tuple denotes the coordinates of any point on the plane.

Three non-collinear points define a unique well-defined plane within the 3D space. The non-collinearity ensures the defined plane is not degenerate (not collapsing into a line or a single point).

Given the points $P_1(x_1, y_1, z_1)$, $P_2(x_2, y_2, z_2)$, and $P_3(x_3, y_3, z_3)$, it is aimed to find the plane equation $ax + by + d = z$.

So, the found a, b and d parameters should satisfy the following system of equations:

$$\begin{cases} ax_1 + by_1 + d = z_1 \\ ax_2 + by_2 + d = z_2 \\ ax_3 + by_3 + d = z_3 \end{cases} \tag{4.2}$$

This system can be expressed as the following matrix form:

$$Ac = z \tag{4.3}$$

Where

$$A = \begin{bmatrix} x_1 & y_1 & 1 \\ x_2 & y_2 & 1 \\ x_3 & y_3 & 1 \end{bmatrix}, c = \begin{bmatrix} a \\ b \\ d \end{bmatrix}, z = \begin{bmatrix} z_1 \\ z_2 \\ z_3 \end{bmatrix} \tag{4.4}$$

This system can be solved using the least squares method.

The residual sum of squares can be calculated as the following:

$$RSS = ||Ac - z||^2 \tag{4.5}$$

The optimization procedure is the minimization of the RSS, in terms of c.

$$min_c||Ac - z||^2 \tag{4.6}$$

This is to be found by finding the gradients of the RSS, and finding where the gradient is zero.

$$\nabla RSS = 2A^T(Ac - z) = 0 \tag{4.7}$$

where

$$2A^T Ac - 2A^T z = 0 \tag{4.8}$$

So, this can be reduced to the following expression:

$$c = (A^T A)^{-1} A^T z \tag{4.9}$$

Found plane that is obtained from the data that is shown in Figure 4.5 is shown in Figure 4.6.

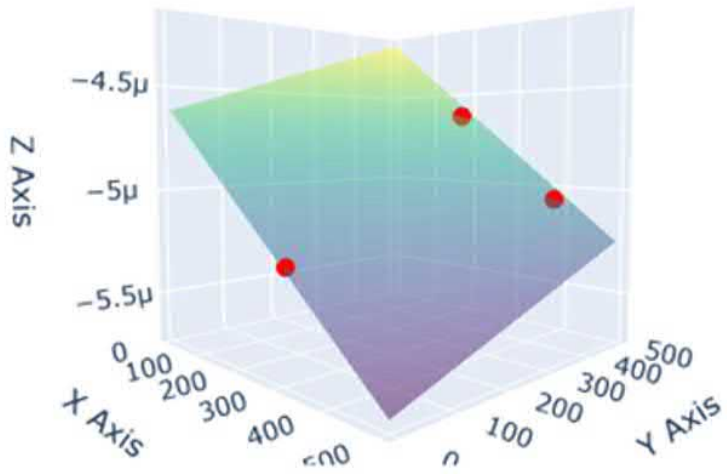


Figure 4.6: Plane obtained from the data

When a rotation matrix is multiplied with a vector, it rotates the vector about the origin, while preserving its magnitude. It is necessary to align the rotation matrix of this plane with the vertical direction (z-axis).

To obtain this rotation matrix, first, it is needed the cross-product vector, to obtain determining the components of the rotation matrix.

$$\vec{v} = \vec{n} \times \vec{k} \tag{4.10}$$

where $\vec{n}$ is the normal vector of the plane $(a, b, -1)$ and $\vec{k}$ is the unit vector of the z-axis $(0, 0, 1)$.

And $\vec{c}$ is the dot product.

$$\vec{c} = \vec{n} \cdot \vec{k} \tag{4.11}$$

The skew-symmetric cross-product matrix is like:

$$[v]_x = \begin{bmatrix} 0 & -v_z & v_y \\ v_z & 0 & -v_x \\ -v_y & v_x & 0 \end{bmatrix} \tag{4.12}$$

So, the final rotation matrix is:

$$R = I + [v]_x + \frac{[v]_x^2}{1 + c} \tag{4.13}$$

where I is the identity matrix.

Once the rotation matrix is obtained, the rotation matrix can be applied to the data matrix.

$$\begin{bmatrix} x' \\ y' \\ z' \end{bmatrix} = R \begin{bmatrix} x \\ y \\ z \end{bmatrix} \tag{4.14}$$

where, (x, y, z) is the original data point, and (x', y', z') is the rotated data point.

Once the data is transformed to "not to be tinted", one needs to level it to the zero point in the y-axis to eliminate the elevation. One can simply adjust the elevation of the data by applying the following:

$$\bar{z} = \frac{z_1 + z_2 + z_3}{3} \tag{4.15}$$

$$z'' = z' - \bar{z} \tag{4.16}$$

where z_1, z_2, and z_3 are the z values of the picked data points, and z'' is the latest values of the data matrix.

The data points should be selected at the places which are known to reside on the 'underlying surface'. However, this might not be enough, as the measurements can be noisy. These noisy data points can be observed in Figure 4.7. To mitigate this issue, the points are sampled by picking the median value from a region, instead of the exact point. Here is the sampling process:

$$Region(x_i, y_i) = data[x, y] | x_i - 5 \leq x \leq x_i + 5, y_i - 5 \leq y \leq y_i + 5 \tag{4.17}$$

$$Median(x_i, y_i) = median(Region(x_i, y_i)) \tag{4.18}$$

Processed version of the data in Figure 4.5 can be seen in Figure 4.7.

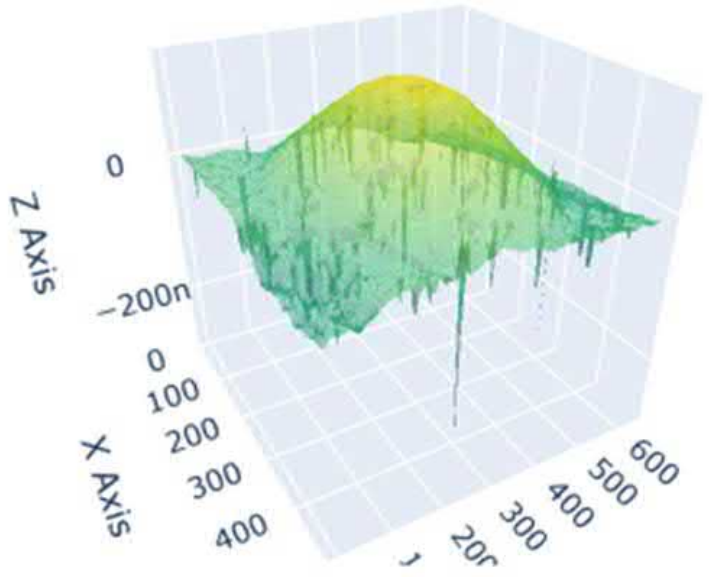


Figure 4.7: Processed data

One can also observe the unwanted peaks and dips in Figure 4.7. The modified data point picking approach resolves this issue.

The contour data of the processed data can be seen in Figure 4.8.

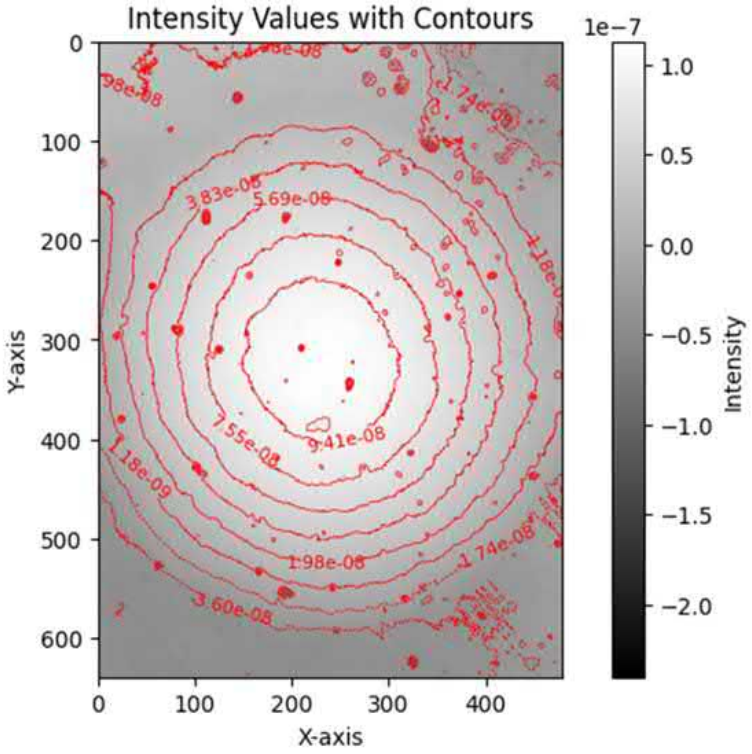


Figure 4.8: Contour of the processed data

As it can be seen, the algorithmic approach is useful, and enables user to use the data, despite the severe issue introduced by the dominant tilt. After the data pre-processing part, one can obtain any value from the processed data points. These sampled data points can be plotted against the sweeping variable(s), in order to demonstrate the effect of the variable change.

4.5 Results for Characterization Measurements

After the data for each measurement were obtained as mentioned above, the height data for the midpoint of the membrane were taken.

Measurement 1 contains data obtained by increasing the DC Voltage from 0V to 315V. The displacement results of the membrane midpoint obtained with Measurement 1 are given in Figure 4.9. While the membrane moved downward until the voltage reached 315 V, the device membrane suddenly ruptured at 315 V.

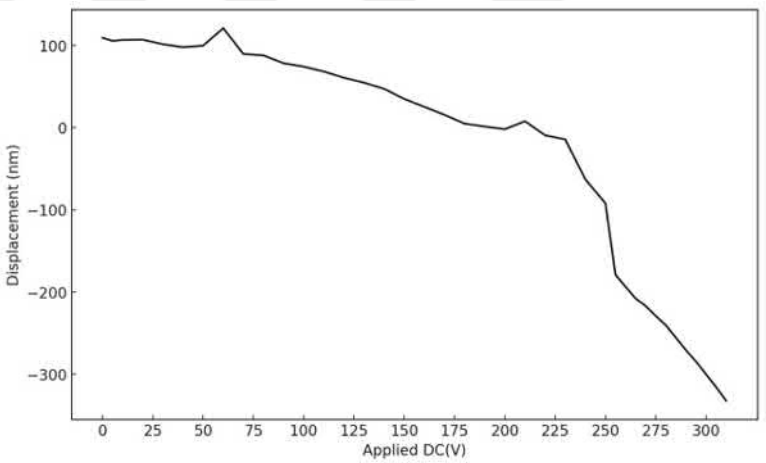


Figure 4.9: DC voltage sweep to determine maximum applicable voltage

Since the gap height of the device (CMUT device #1) we were testing is 4 μm, it can be seen in Figure 4.9 that the static displacement of the membrane was not enough to consider the applied voltage as collapse voltage because the membrane displacement was only about 400 nm, and the membrane did not reach the bottom electrode surface (∼4 micrometers of downward displacement). At 315 V , there was a sudden spark coming from the CMUT under test that may be implying that the CMUT device failed due to dielectric breakdown of the insulating SiO_2. After this measurement, since this CMUT device was no longer operational, measurements were continued with another CMUT device (CMUT device #2) on the same wafer.

In Measurement 2 (CMUT device #2), the conductance versus frequency results obtained by applying 40V DC and 1V AC to the Impedance analyzer are given in Figure 4.10.

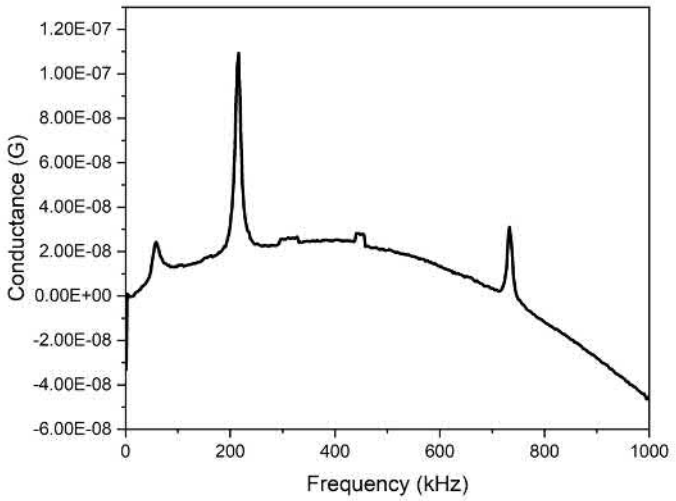


Figure 4.10: Frequency sweep to identify resonance frequency using an Impedance Analyzer

As shown in Figure 4.10, a resonance frequency of approximately 200 kHz is observed. Upon closer examination, as depicted in Figure 4.11, this resonance frequency is more precisely identified as 215-216 kHz.

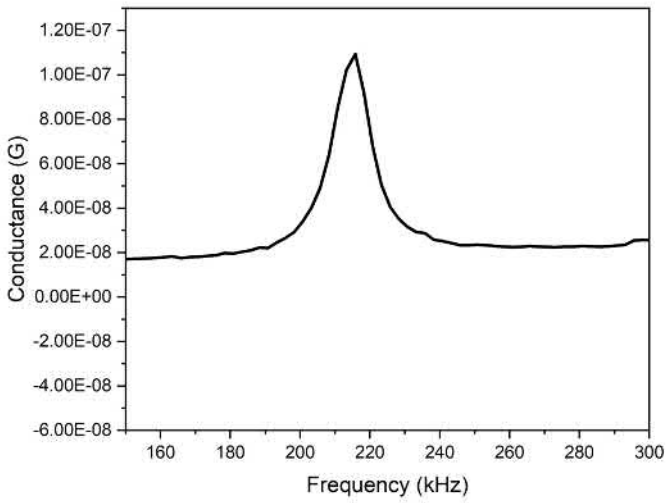


Figure 4.11: Close-up of Frequency Sweep to Identify Resonance Frequency Using an Impedance Analyzer

In Measurement 3, ZYGO Optical Measurement setup was used, and 150V AC + 0V DC was applied to the same CMUT device (CMUT device #2). While constant AC voltage is applied, the frequency is swept between 150-300 kHz in 1 kHz steps. The relevant results of this measurement are given in Figure 4.12.

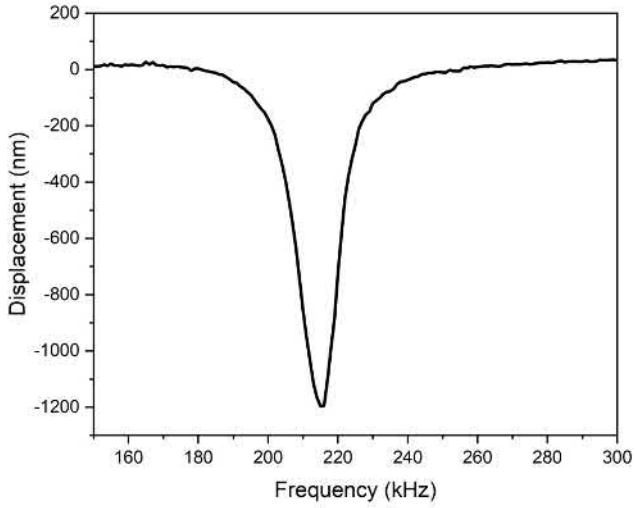


Figure 4.12: Frequency Sweep to Identify Resonance Frequency Using ZYGO Optical Profilometer DMM

When the 200-230kHz range is examined more closely in Figure 4.13, it is seen that there is a resonance frequency at 215-216kHz.

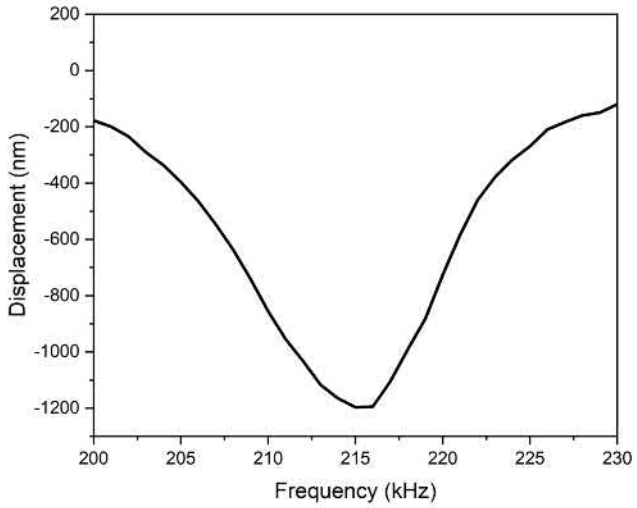


Figure 4.13: Close-up of Frequency Sweep to Identify Resonance Frequency Using ZYGO Optical Profilometer DMM

For the same CMUT device, the results obtained with both the impedance analyzer and the ZYGO Optical Profilometer Dynamic Metrology Module show that the resonance frequency of this CMUT device is between 215-216 kHz.

The next measurement was obtained by applying a constant 1V AC while changing the DC voltage with the Impedance Analyzer. The change in the resonance frequency of the CMUT device was examined under different DC voltages of 0, 10, 20, 30, and 40 V as shown in Figure 4.14.

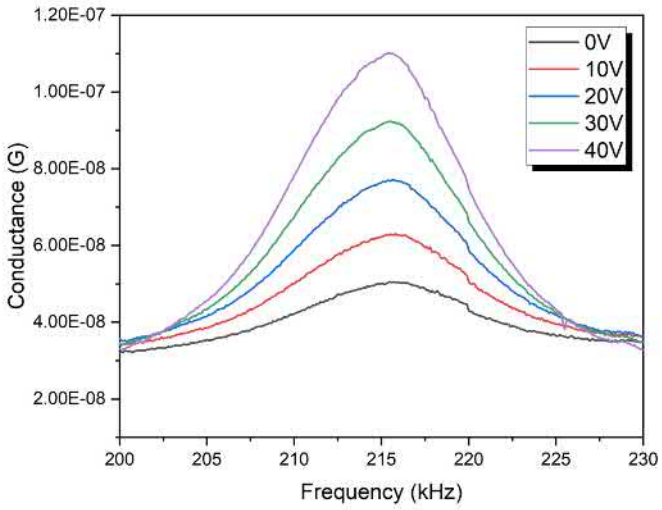


Figure 4.14: Effect of Different DC Voltages on Resonance Frequency Using Frequency Sweep

When examining the peak points of the resonance frequencies obtained from this measurement, a slight shift is observed shown in Figure 4.15.

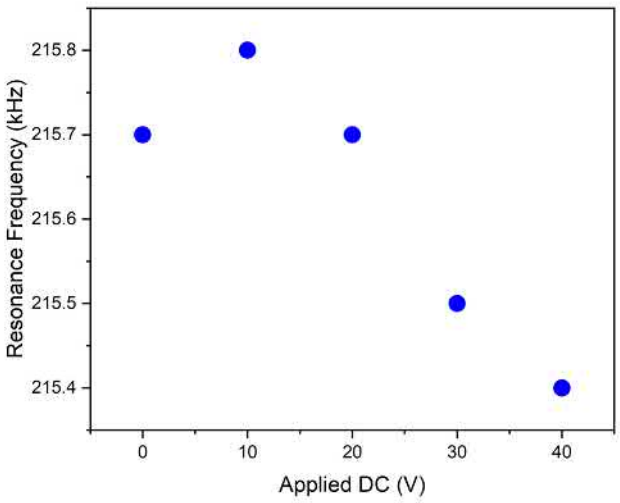


Figure 4.15: Analysis of Peak Points

Finally, to observe the movement of the CMUT membrane (CMUT device #2), the phase angle was shifted between 0–360 degree increments at 215 kHz constant frequency. The membrane displacement graph depending on the phase angle obtained as a result of this measurement is shown in Figure 4.16. Images of membrane movement taken from these measurements are provided below from Figures from 4.16 to 4.24.

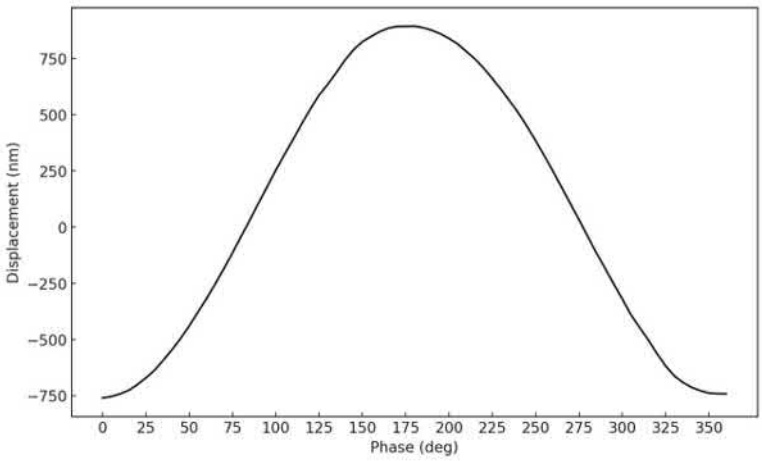


Figure 4.16: Phase Sweep to Observe Membrane Movement at Resonance Frequency

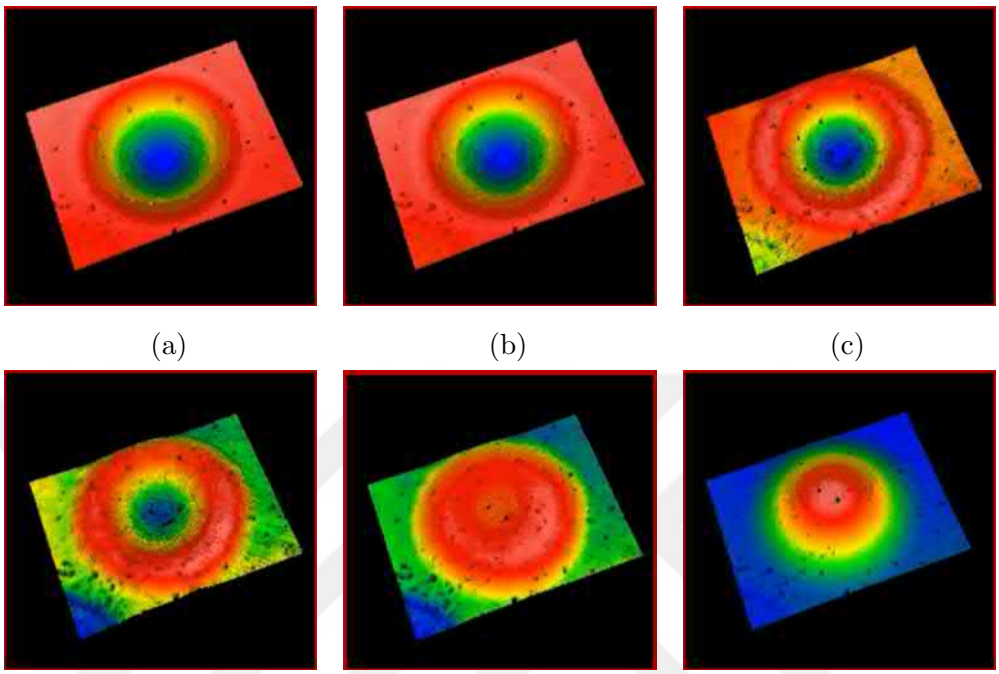
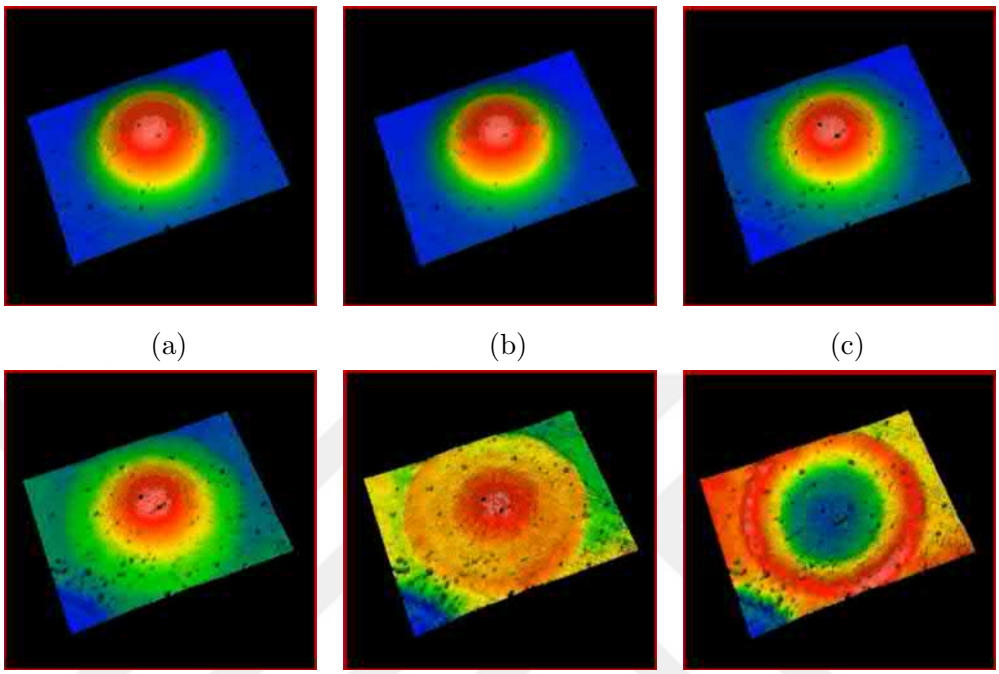


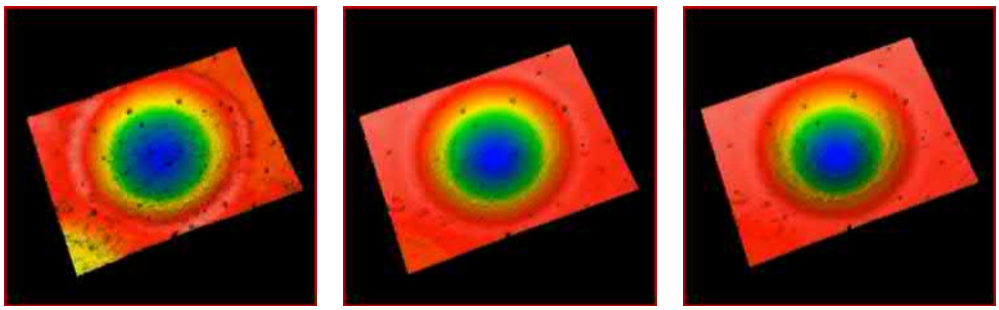
Figure 4.17: 3D Visualizations of the CMUT Membrane at Different Phase Angles at 215 kHz Frequency (a)0° (b)45° (c)75° (d)90° (e)95° (f)120°



(a) (b) (c)

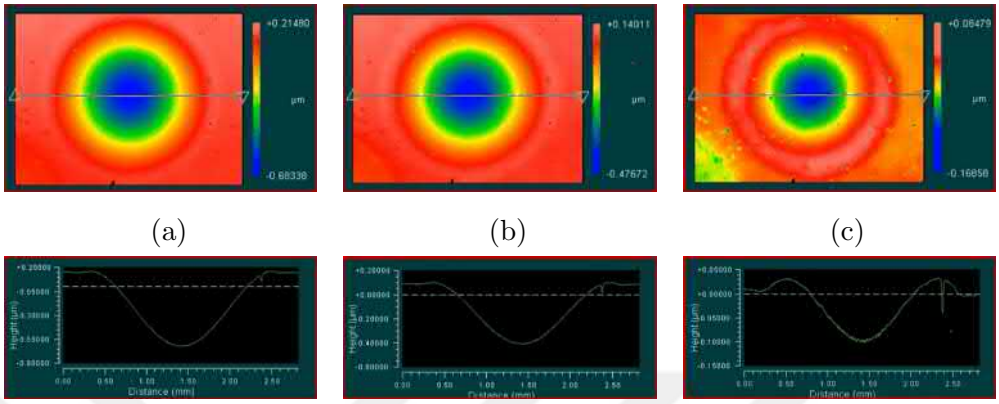
(d) (e) (f)

Figure 4.18: 3D Visualizations of the CMUT Membrane at Different Phase Angles at 215 kHz Frequency (a)150° (b)180° (c)250° (d)260° (e)265° (f)270°



(a) (b) (c)

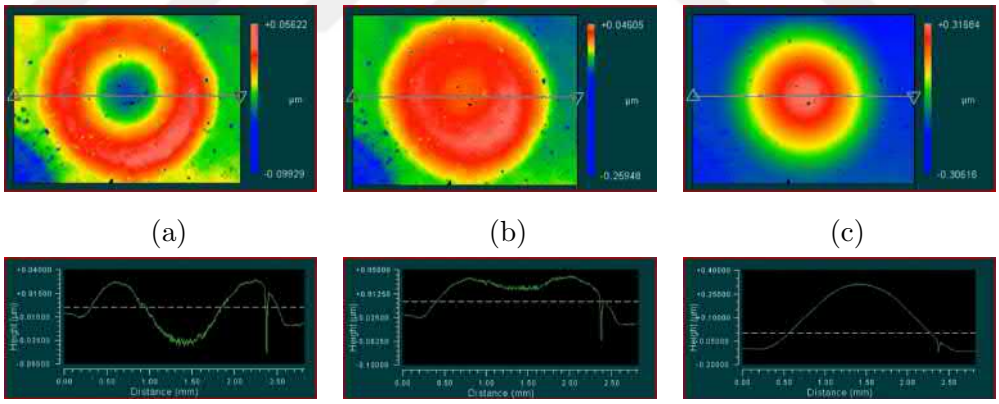
Figure 4.19: 3D Visualizations of the CMUT Membrane at Different Phase Angles at 215 kHz Frequency (a)275° (b)300° (c)360°



(a) (b) (c)

(d) (e) (f)

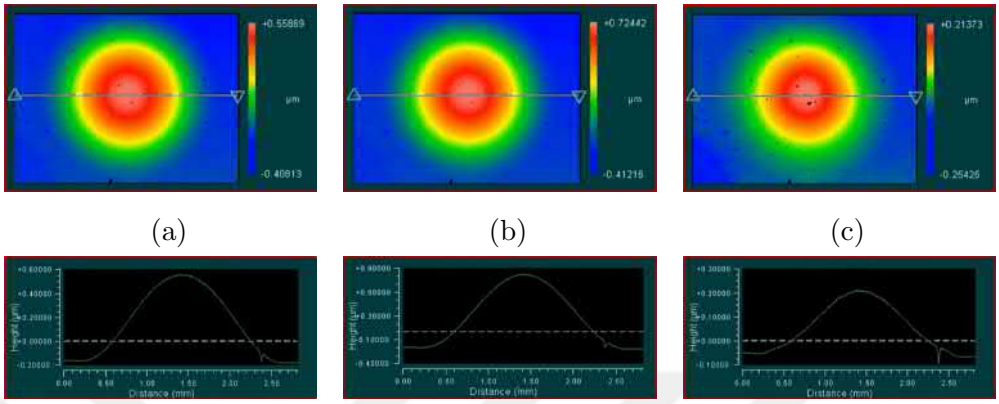
Figure 4.20: 2D Visualizations and Line Plots of the CMUT Membrane at Different Phase Angles at 215 kHz Frequency: (a) 0° (2D), (b) 45° (2D), (c) 75° (2D), (d) 0° (Line Plot), (e) 45° (Line Plot), (f) 75° (Line Plot)



(a) (b) (c)

(d) (e) (f)

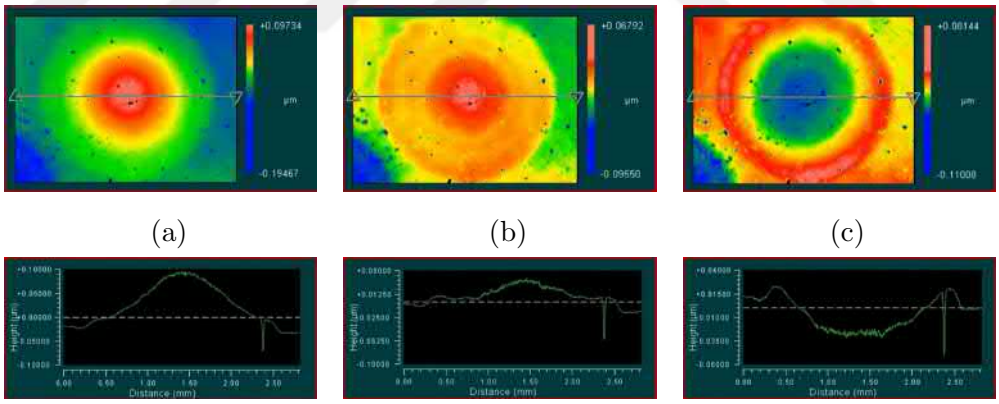
Figure 4.21: 2D Visualizations and Line Plots of the CMUT Membrane at Different Phase Angles at 215 kHz Frequency: (a) 90° (2D), (b) 95° (2D), (c) 120° (2D), (d)90° (Line Plot), (e) 95° (Line Plot), (f) 120° (Line Plot)



(a) (b) (c)

(d) (e) (f)

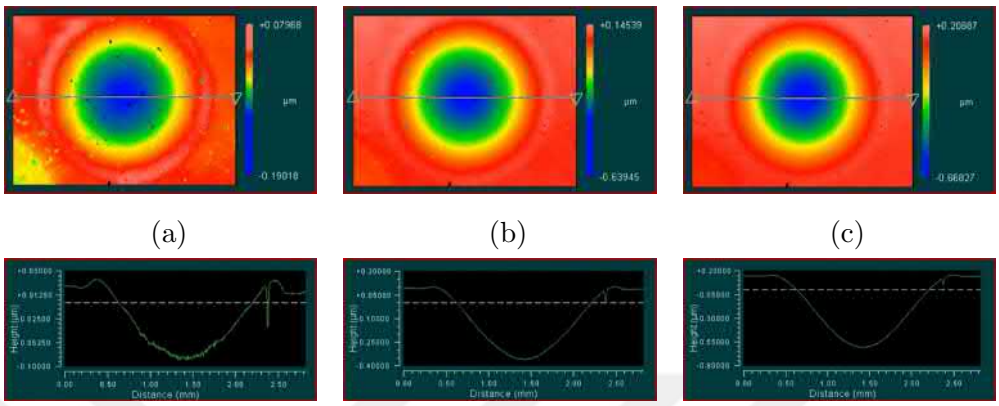
Figure 4.22: 2D Visualizations and Line Plots of the CMUT Membrane at Different Phase Angles at 215 kHz Frequency: (a) 150° (2D), (b) 180° (2D), (c) 250° (2D), (d)150° (Line Plot), (e) 180° (Line Plot), (f) 250° (Line Plot)



(a) (b) (c)

(d) (e) (f)

Figure 4.23: 2D Visualizations and Line Plots of the CMUT Membrane at Different Phase Angles at 215 kHz Frequency: (a) 260° (2D), (b) 265° (2D), (c) 270° (2D), (d)260° (Line Plot), (e) 265° (Line Plot), (f) 270° (Line Plot)



(a) (b) (c)

(d) (e) (f)

Figure 4.24: 2D Visualizations and Line Plots of the CMUT Membrane at Different Phase Angles at 215 kHz Frequency: (a) 275° (2D), (b) 300° (2D), (c) 360° (2D), (d)275° (Line Plot), (e) 300° (Line Plot), (f) 360° (Line Plot)

Chapter 5

Conclusion and Future Studies

5.1 Conclusion

In this thesis, we focused on developing microfabrication processes for PR-CMUTs. PR-CMUT is designed to improve the detection of AE signals in SHM. PR-CMUTs are promising because they use a phase-reversal technique to reduce noise interference, which can be problematic in real-world SHM applications. We aimed to develop reliable microfabrication methods to fabricate PR-CMUT devices. This entire effort was a synergistic effort by close collaboration with researchers from Jiangsu University and North University of China, who provided the theoretical designs and models based on the manufacturability guidelines that we provided to be able to develop processes with the aim of micromanufacturing functional PR-CMUT MEMS devices at our cleanroom facility at Bilkent University UNAM.

We began with selecting the appropriate materials, and methods and understanding the limits of the fabrication process. This step was important to decide the main microfabrication steps and design the necessary masks. Initially, we planned to use five different masks for the microfabrication process of PR-CMUT. As we progressed, we encountered several challenges during fabrication, which led

us to develop solutions and regularly update the fabrication process flow. Over time, we tried three different iterations of the integration processes. Through these iterations, we realized that we could reduce the number of process masks from five to four, which helped us significantly to eliminate unnecessary steps that were making the fabrication more challenging and longer. Reducing the number of masks also solved problems like crack formation, especially during the top membrane metal deposition at the regions where there are topographic height differences during the fabrication of PR-CMUT. During the process development and the integration process modifications, we have gained significant experience towards the realization of the PR-CMUT device. Due to time constraints, we could not fully test the final iteration of the microfabrication process. However, all the experiences and learnings that we have done and gained are used to design a faster and more reliable process to improve the overall quality of the MEMS devices.

During the microfabrication process, we encountered a challenge with creating the top membrane, which required a thick image reversal photoresist and thick metal deposition for lift-off. Since this specific photoresist was not available in our cleanroom, we developed a multi-layer AZ 5214E photoresist process to achieve a thick image reversal photoresist for thick material lift-off. This innovation was crucial for the successful fabrication of the PR-CMUT devices and demonstrating our ability to adapt and overcome obstacles in the microfabrication process.

In the final stages of the PR-CMUT fabrication, we reached and performed the last steps of the fabrication for many times. During these steps, we focused on etching the sacrificial layer, which was made of Poly-Si, using XeF_2 isotropic dry etching. Despite multiple attempts and various approaches, so far we have only been able to achieve partial etching of the sacrificial layer. A complete Poly-Si etch could not be accomplished within the available time frame of this thesis project, which presented a significant challenge in the finalization of the PR-CMUT devices. As a result, we were unable to obtain a fully functional device suitable for characterization testing, and thus, measurements could not be taken with the PR-CMUT device, yet. Further efforts by our research group will be put in, in the coming weeks and months to be able to obtain testable PR-CMUT

MEMS chips.

As another important part of this thesis project, we also conducted detailed dynamic characterization using a ZYGO Optical Profilometer. ZYGO Optical Profilometer with Dynamic Metrology Module allowed us to measure important properties like the resonance frequency and 3D membrane movement of a circular membrane CMUT under AC or DC voltage excitations. Circular membrane CMUT devices were characterized using this method, and the results were compared with the results obtained from an impedance analyzer. The findings confirmed that the ZYGO Optical Profilometer could accurately determine the resonance frequency and allowed us to observe the 3D dynamic movement of the CMUT membrane in great detail. This demonstrated the effectiveness of using ZYGO for the in-depth characterization of CMUT devices. As stated in the "Future Studies", there are further experimental studies to be done by our research group to understand the details of the results obtained by ZYGO Optical Profilometer.

Throughout this thesis work, I have spent over 1,300 hours in the cleanroom, carefully developing and refining the microfabrication processes for PR-CMUT devices. The journey was far from easy; it involved countless trials and adjustments, as I worked with more than 25 wafers, with 4-inch diameter, for successful microfabrication. Each wafer represented a step forward, whether it was a successful outcome or a learning experience from unexpected challenges. This demanding production process not only tested my technical skills and patience but also significantly deepened my understanding of microfabrication. The time and effort invested in this work were significant, and invaluable in shaping the final outcomes and contributing to my growth as a researcher.

Through this intensive MEMS device production work, I realized that conducting experiments is not just about performing the steps written, but also about deeply understanding why we are doing them and what we expect to achieve. It became clear to me that every experiment must be approached with great care and attention to detail, as the significance of each step can directly impact the

overall success of the process. I also learned the importance of carefully documenting each stage of the process. This thorough documentation not only made it easier to track progress but also played a crucial role in identifying, understanding, and resolving any problem that occurred. The practice of carefully recording every detail provided invaluable insights, making the problem-solving process more efficient and effective.

5.2 Future Studies

While this thesis made important progress, there are several areas where future research could further advance the microfabrication of PR-CMUTs.

One important step for future work is improving the process of releasing the Poly-Si sacrificial layer. In this thesis, we encountered difficulties in releasing this layer completely, which is essential for the proper functioning of the PR-CMUT devices. In order to solve this problem, the flow we presented as the final iteration can be applied. In case of a successful etch, the top and bottom electrodes should be "electrically short" during the release process to prevent the released membrane from sticking to the bottom surface due to uncontrolled electrostatic forces after successful release. A special PCB design will be required for this electrical short arrangement. In addition, an impedance analyzer and ZYGO Optical Profilometer may be used collaboratively to measure and visualize in 3D the resonance frequency or mechanical vibrations of PR-CMUT devices.

In addition, there are parts of the results we obtained with the ZYGO Optical Profilometer that are not clearly understood by our research group, yet. These parts are planned to be understood with, further research, further experimental measurements with ZYGO, and further literature research. The graph of this data is given in Figure 5.1. This graphs presented above, as well as the future experimental measurements with ZYGO Optical Profilometer are planned to be interpreted based on details of "Capacitive actuation with AC voltages" [56].

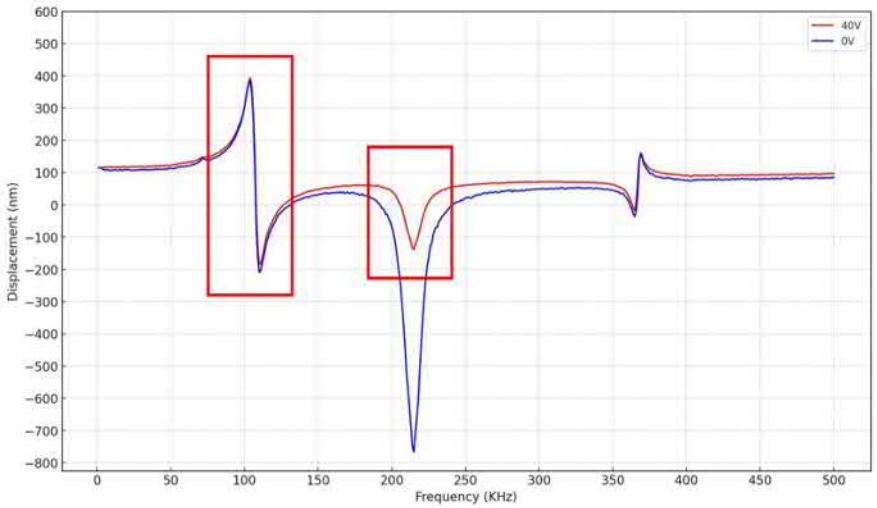


Figure 5.1: Overlay of two graphs obtained by applying 150V AC, 0V DC and 150V AC, 40V DC with a frequency sweep from 1 kHz to 500 kHz with ZYGO Optical Profilometer.

Similarly, in Figure 5.2 below taken with the impedance analyzer, the 3D membrane movements and the reason for these 3D movements will be investigated at the peak points seen outside the resonance frequency (highlighted by red rectangles).

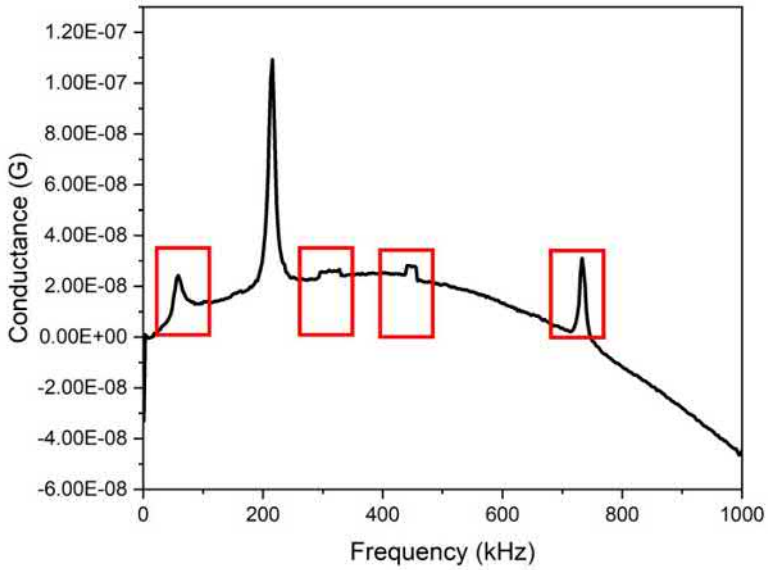


Figure 5.2: Frequency sweep from 0 kHz to 1000 kHz with applied 40V DC, 1V AC voltage impedance analyzer result

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Appendix A

Process Flows of Experiments

A.1 Initial Microfabrication Process Flow for PR-CMUTs

Description	step#	Details	
Pyrex Cleaning	1	Acetone / 3 min	Preparation
	2	IPA / 3 min	
	3	DI Water / 3 min	
	4	N_2 blow / 3 min	
	5	Hotplate at 120℃ 10 min	
Photolithography and Patterning (Mask 1)	6	HMDS Coating	Bottom electrode formation
	7	- 2000 RPM / 1000 RPM/s acc / 1 min	
	8	- Hotplate 150℃/ 5 min	
	9	AZ5214E Image Reversal Coating	
	10	- 1000 RPM / 500 RPM/s acc / 1 min / expected thickness (around 2 micron)	
	11	- Hotplate 110℃ / 1 min	
	12	- Exposure with mask 40 mj/cm^2	
	13	- Hotplate 120℃ / 1 min	
	14	- Flood exposure 250 mJ/cm^2	
	15	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP Descum	16	Tape wafer on top of another thick glass substrate	
	17	15 min Warm-up process	
	18	Descum for 10 seconds	
E-Beam Evaporation (50nm Ti & 450nm Cu)	19	Tooling Factor Calculation	
	20	- Sample 1: 50nm Ti	
	21	- Sample 2: 50nm Ti, 100nm Cu	
	22	- Sample 3: 50nm Ti, 250nm Cu	
	23	Deposition Process	
	24	- Begin with 50nm Ti as an adhesion layer	
	25	- Follow with 450nm Cu without breaking the vacuum	
	26	- Initial 10nm Cu deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	27	Precautions for Quality	
	28	- Check crystal monitor life for accurate thickness	
	29	- Inspect material inside crucible to ensure proper melting	
	30	- Cool chamber for at least 30 minutes to avoid sudden temperature changes	
Lift-off Process	31	Place wafer in acetone-filled container without sonicator	
	32	Wait until photoresist and unwanted metals are fully removed	
	33	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	34	Dry surface with N_2 blow	
Photolithography and Patterning (Mask 2)	35	HMDS Coating	Dielectric Layer Formation
	36	- 2000 RPM / 1000 RPM/s acc /1 min	
	37	- Hotplate 150℃/ 5 min	
	38	AZ5214E Image Reversal Coating	
	39	- 1000 RPM / 500 RPM/s acc / 1 min /expected thickness(around 2 micron)	
	40	- Hotplate 110℃ / 1 min	
	41	- Exposure with mask 40 mJ/cm^2	
	42	- Hotplate 120℃ / 1 min	
	43	- Flood exposure 250 mJ/cm^2	
	44	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP Descum	45	Tape wafer on top of another thick glass substrate	
	46	15min Warm-up process	
	47	Descum for 10 seconds	
E-Beam Evaporation (150nm HfO_2)	48	Tooling Factor Calculation	
	49	- Sample 1: 50nm HfO_2	
	50	- Sample 2: 100nm HfO_2	
	51	Deposition Process	
	52	- Begin with 150nm HfO_2	
	53	- Initial 10nm HfO_2 deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	54	Precautions for Quality	
	55	- Check crystal monitor life for accurate thickness	
	56	- Inspect material inside crucible to ensure proper melting	
	57	- Cool chamber for at least 30 minutes to avoid sudden temperature changes	
Lift-off Process	58	Place wafer in acetone-filled container without sonicator	
	59	Wait until photoresist and unwanted materials are fully removed	
	60	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	61	Dry surface with N_2 blow	

Figure A.1

Photolithography and Patterning (Mask 3)	62	HMDS Coating	**Sacrificial Layer Formation**
	63	- 2000 RPM / 1000 RPM/s acc / 1 min	
	64	- Hotplate 150 ℃/ 5 min	
	65	AZ5214E Image Reversal Coating	
	66	- 1000 RPM / 500 RPM/s acc / 1 min /expected thickness (around 2 micron)	
	67	- Hotplate 110 ℃ / 1 min	
	68	- Exposure with mask 40 mJ/cm^2	
	69	- Hotplate 120 ℃ / 1 min	
	70	- Flood exposure 250 mJ/cm^2	
	71	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	72	Tape wafer on top of another thick glass substrate	
	73	15min Warm-up process	
	74	Descum for 10 seconds	
E Beam Evaporation (600nm Poly-Si)	75	Tooling Factor Calculation	
	76	- Sample 1: 50nm Poly-Si	
	77	- Sample 2: 100nm Poly-Si	
	78	Deposition Process	
	79	- Begin with 600nm Poly-Si	
	80	- Initial 10nm Poly-Si deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	81	Precautions for Quality	
	82	- Check crystal monitor life for accurate thickness.	
	83	- Inspect material inside crucible to ensure proper melting.	
	84	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	85	Place wafer in acetone-filled container without sonicator	
	86	Wait until photoresist and unwanted materials are fully removed	
	87	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	88	Dry surface with N_2 blow	
Photolithography and Patterning (Mask 4)	89	HMDS Coating	**Anchor Formation**
	90	- 2000 RPM / 1000 RPM/s acc /1 min	
	91	- Hotplate 150 ℃/ 5 min	
	92	AZ4562 Positive Photoresist Coating	
	93	- 4000 RPM / 500 RPM/s acc / 1 min /expected thickness (around 6 micron)	
	94	- Hotplate 110 ℃ / 1 min	
	95	- Exposure with mask 140 mJ/cm^2	
	96	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum and BOSCH Process	97	Tape wafer on top of a thick glass substrate	
	98	15-minute warm-up process	
	99	Perform descum for 10 seconds	
	100	Continue Bosch process until the same color of HfO_2 is reached	
	101	Conduct EDX measurement to determine if etching is complete	
Photoresist Removal	102	Place wafer in acetone-filled container without sonicator	
	103	Wait until photoresist is fully removed	
	104	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	105	Dry surface with N_2 blow	

Figure A.2

Photolithography and Patterning (Mask 5)	106	HMDS Coating	Top Membrane Formation
	107	- 2000 RPM / 1000 RPM/s acc /1 min	
	108	- Hotplate 150 ℃/ 5 min	
	109	AZ5214E Image Reversal Coating	
	110	- 500 RPM / 250 RPM/s acc / 1 min / expected thickness (around 2 micron)	
	111	- Hotplate 110 ℃ / 1 min	
	112	- Exposure with mask 40 mJ/cm^2	
	113	- Hotplate 120 ℃ / 1 min	
	114	- Flood exposure 250 mJ/cm^2	
	115	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP Descum	116	Tape wafer on top of another thick glass substrate	
	117	15min Warm-up process	
	118	Descum for 10 seconds	
E-Beam Evaporation (50nm Ti & 4 micron Cu)	119	Tooling Factor Calculation	
	120	- Sample 1: 50nm Ti	
	121	- Sample 2: 50nm Ti, 100nm Cu	
	122	- Sample 3: 50nm Ti, 250nm Cu	
	123	Deposition Process	
	124	- Begin with 50nm Ti as adhesion layer.	
	125	- Wait 30min after each 500nm deposition of Cu.	
	126	- Break the vacuum of the chamber after each 1μm Cu deposition.	
	127	- Initial 10nm Cu deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	128	Precautions for Quality	
	129	- Check crystal monitor life for accurate thickness.	
	130	- Inspect material inside crucible to ensure proper melting.	
	131	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	132	Place wafer in acetone-filled container without sonicator	
	133	Wait until photoresist and unwanted materials are fully removed	
	134	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	135	Dry surface with N_2 blow	
Dicing Saw	136	Align wafer on dicing saw	Sacrificial Layer Release
	137	Make precise cuts to separate wafer into individual chips	
	138	Handle individual chips carefully to prevent damage or contamination	
BOE Cleaning	139	Immerse individual chips in Buffered Oxide Etch (BOE) for 10 seconds to remove the oxide layer	
	140	Thoroughly rinse chips with deionized (DI) water to remove residual etchant	
	141	Dry chips using a nitrogen (N_2) blow	
Xenon Diflouride Etching	142	Subject chips to an etching cycle to etch the poly-silicon layer	
	143	Monitor etch progress closely, adjusting the process as needed	
	144	Continue etching until poly-silicon is completely etched, releasing the top membrane	

Figure A.3

A.2 First Iteration of Microfabrication Process Flow for PR-CMUTs

Description	step#	Details	
Pyrex Cleaning	1	Acetone / 3 min	Preparation
	2	IPA / 3 min	
	3	DI Water / 3 min	
	4	N_2 blow / 3 min	
	5	Hotplate at 120℃ 10 min	
Photolithography and Patterning (Mask 1)	6	HMDS Coating	Bottom electrode formation
	7	- 2000 RPM / 1000 RPM/s acc / 1 min	
	8	- Hotplate 150℃/ 5 min	
	9	AZ5214E Image Reversal Coating	
	10	- 1000 RPM / 500 RPM/s acc / 1 min /expected thickness (around 2 micron)	
	11	- Hotplate 110℃ / 1 min	
	12	- Exposure with mask 40 mJ/cm2	
	13	- Hotplate 120℃ / 1 min	
	14	- Flood exposure 250 mJ/cm2	
	15	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	16	Tape wafer on top of another thick glass substrate	
	17	15min Warm-up process	
	18	Descum for 10 seconds	
E-Beam Evaporation (50nm Ti & 450nm Cu)	19	Tooling Factor Calculation	
	20	- Sample 1: 50nm Ti	
	21	- Sample 2: 50nm Ti, 100nm Cu	
	22	- Sample 3: 50nm Ti, 250nm Cu	
	23	Deposition Process	
	24	- Begin with 50nm Ti as adhesion layer.	
	25	- Follow with 450nm Cu without breaking the vacuum.	
	26	- Initial 10nm Cu deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	27	Precautions for Quality	
	28	- Check crystal monitor life for accurate thickness.	
	29	- Inspect material inside crucible to ensure proper melting.	
	30	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	31	Place wafer in acetone-filled container without sonicator	
	32	Wait until photoresist and unwanted metals are fully removed	
	33	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	34	Dry surface with N2 blow	
Photolithography and Patterning (Mask 2)	35	HMDS Coating	Dielectric Layer Formation
	36	- 2000 RPM / 1000 RPM/s /1 min	
	37	- Hotplate 150℃/ 5 min	
	38	AZ5214E Image Reversal Coating	
	39	- 1000 RPM / 500 RPM/s acc/ 1 min /expected thickness (around 2 micron)	
	40	- Hotplate 110℃ / 1 min	
	41	- Exposure with mask 40 mJ/cm2	
	42	- Hotplate 120℃ / 1 min	
	43	- Flood exposure 250 mJ/cm2	
	44	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP Descum	45	Tape wafer on top of another thick glass substrate	
	46	15min Warm-up process	
	47	Descum for 10 seconds	
E-Beam Evaporation (150nm HfO_2)	48	Tooling Factor Calculation	
	49	- Sample 1: 50nm HfO_2	
	50	- Sample 2: 100nm HfO_2	
	51	Deposition Process	
	52	- Begin with 150nm HfO_2	
	53	- Initial 10nm HfO_2 deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	54	Precautions for Quality	
	55	- Check crystal monitor life for accurate thickness.	
	56	- Inspect material inside crucible to ensure proper melting.	
	57	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift off Process	58	Place wafer in acetone-filled container without sonicator	
	59	Wait until photoresist and unwanted materials are fully removed	
	60	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	61	Dry surface with N2 blow	

Figure A.4

E-Beam Evaporation (50nm Cr)	62	Tooling Factor Calculation	**Sacrificial Layer Formation**
	63	- Sample 1: 50nm Cr	
	64	- Sample 2: 100nm Cr	
	65	Deposition Process	
	66	- Begin with 50nm Cr	
	67	- Initial 10nm Cr deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	68	Precautions for Quality	
	69	- Check crystal monitor life for accurate thickness.	
	70	- Inspect material inside crucible to ensure proper melting.	
	71	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Photolithography and Patterning (Mask 3)	72	HMDS Coating	
	73	- 2000 RPM / 1000 RPM/s acc/1 min	
	74	- Hotplate 150℃/ 5 min	
	75	AZ5214E Image Reversal Coating	
	76	- 1000 RPM / 500 RPM/s acc/ 1 min /expected thickness (around 2 micron)	
	77	- Hotplate 110℃ / 1 min	
	78	- Exposure with mask 40 mJ/cm2	
	79	- Hotplate 120℃ / 1 min	
	80	- Flood exposure 250 mJ/cm2	
	81	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	82	Tape wafer on top of another thick glass substrate	
	83	15min Warm-up process	
	84	Descum for 10 seconds	
Chromium Etch	85	Dilute chromium etchant 1:10 with DI water.	
	86	Check the etch rate every 10 seconds using an optical microscope.	
	87	Continue etching until the same color of HfO_2 before Cr deposition is reached.	
	88	Take SEM images to document the process.	
	89	Perform EDX measurement to confirm the completion of etching.	
E-Beam Evaporation (600nm Poly-Si)	90	Tooling Factor Calculation	
	91	- Sample 1: 50nm Poly-Si	
	92	- Sample 2: 100nm Poly-Si	
	93	Deposition Process	
	94	- Begin with 600nm Poly-Si	
	95	- Initial 10nm Poly-Si deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	96	Precautions for Quality	
	97	- Check crystal monitor life for accurate thickness.	
	98	- Inspect material inside crucible to ensure proper melting.	
	99	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift off Process	100	Place wafer in acetone-filled container without sonicator	
	101	Wait until photoresist and unwanted materials are fully removed	
	102	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	103	Dry surface with N_2 blow	

Figure A.5

Photolithography and Patterning (Mask 4)	104	HMDS Coating	**Anchor Formation**
	105	- 2000 RPM / 1000 RPM/s acc/1 min	
	106	- Hotplate 150℃/ 5 min	
	107	AZ4562 Positive Photoresist Coating	
	108	- 4000 RPM / 500 RPM/s acc / 1 min /expected thickness (around 6 micron)	
	109	- Hotplate 110℃ / 1 min	
	110	- Exposure with mask 140 mJ/cm2	
	111	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum and BOSCH Process	112	Tape wafer on top of a thick glass substrate	
	113	15-minute warm-up process	
	114	Perform descum for 10 seconds	
	115	Continue Bosch process until the same color of HfO_2 is reached	
	116	Conduct EDX measurement to determine if etching is complete	
Photoresist Removal	117	Place wafer in acetone-filled container without sonicator	
	118	Wait until photoresist is fully removed	
	119	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	120	Dry surface with N_2 blow	
Photolithography and Patterning (Mask 5)	121	HMDS Coating	**Top Membrane Formation**
	122	- 2000 RPM / 1000 RPM/s acc/1 min	
	123	- Hotplate 150℃/ 5 min	
	124	AZ5214E Image Reversal Coating	
	125	- 250 RPM / 250 RPM/s acc / 1 min /expected thickness (around 2 micron)	
	126	- Hotplate 110℃ / 1 min	
	127	- Exposure with mask 40 mJ/cm2	
	128	- Hotplate 120℃ / 1 min	
	129	- Flood exposure 250 mJ/cm2	
	130	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP Descum	131	Tape wafer on top of another thick glass substrate	
	132	15min Warm-up process	
	133	Descum for 10 seconds	
E-Beam Evaporation (50nm Ti & 4-micron Cu)	134	Tooling Factor Calculation	
	135	- Sample 1: 50nm Ti	
	136	- Sample 2: 50nm Ti, 100nm Cu	
	137	- Sample 3: 50nm Ti, 250nm Cu	
	138	Deposition Process	
	139	- Begin with 50nm Ti as adhesion layer.	
	140	- Wait 30min after each 500nm deposition of Cu.	
	141	- Break the vacuum of the chamber after each 1μm Cu deposition.	
	142	- Initial 10nm Cu deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	143	Precautions for Quality	
	144	- Check crystal monitor life for accurate thickness.	
	145	- Inspect material inside crucible to ensure proper melting.	
	146	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift off Process	147	Place wafer in acetone-filled container without sonicator	
	148	Wait until photoresist and unwanted materials are fully removed	
	149	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	150	Dry surface with N_2 blow	

Figure A.6

Chromium Etch	151	Dilute chromium etchant 1:10 with DI water.	**Sacrificial Layer Release**
	152	Check the etch rate every 10 seconds using an optical microscope.	
	153	Continue etching until the same color of HfO_2 before Cr deposition is reached.	
Dicing Saw	154	Align wafer on dicing saw	
	155	Make precise cuts to separate wafer into individual chips	
	156	Handle individual chips carefully to prevent damage or contamination	
BOE Cleaning	157	Immerse individual chips in Buffered Oxide Etch (BOE) for 10 seconds to remove the oxide layer	
	158	Thoroughly rinse chips with deionized (DI) water to remove residual etchant	
	159	Dry chips using a nitrogen (N_2) blow	
Xenon Difluoride Etching	160	Subject chips to an etching cycle to etch the poly-silicon layer	
	161	Monitor etch progress closely, adjusting the process as needed	
	162	Continue etching until poly-silicon is completely etched, releasing the top membrane	

Figure A.7

A.3 Second Iteration of Microfabrication Process Flow for PR-CMUTs

Description	step#	Details	
Pyrex Cleaning	1	Acetone / 3 min	Preparation
	2	IPA / 3 min	
	3	DI Water / 3 min	
	4	N_2 blow / 3 min	
	5	Hotplate at 120℃ 10 min	
Photolithography and Patterning (Mask 1)	6	HMDS Coating	Bottom electrode formation
	7	- 2000 RPM / 1000 RPM/s acc/1 min	
	8	- Hotplate 150℃/ 5 min	
	9	AZ5214E Image Reversal Coating	
	10	- 1000 RPM / 500 RPM/s acc/ 1 min /expected thickness (around 2 micron)	
	11	- Hotplate 110℃ / 1 min	
	12	- Exposure with mask 40 mJ/cm^2	
	13	- Hotplate 120℃ / 1 min	
	14	- Flood exposure 250 mJ/cm^2	
	15	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP Descum	16	Tape wafer on top of another thick glass substrate	
	17	15min Warm-up process	
	18	Descum for 10 seconds	
E-Beam Evaporation (50nm Ti & 450nm Cu)	19	Tooling Factor Calculation	
	20	- Sample 1: 50nm Ti	
	21	- Sample 2: 50nm Ti, 100nm Cu	
	22	- Sample 3: 50nm Ti, 250nm Cu	
	23	Deposition Process	
	24	- Begin with 50nm Ti as adhesion layer.	
	25	- Follow with 450nm Cu without breaking the vacuum.	
	26	- Initial 10nm Cu deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	27	Precautions for Quality	
	28	- Check crystal monitor life for accurate thickness.	
	29	- Inspect material inside crucible to ensure proper melting.	
	30	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	31	Place wafer in acetone-filled container without sonicator	
	32	Wait until photoresist and unwanted metals are fully removed	
	33	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	34	Dry surface with N_2 blow	
Photolithography and Patterning (Mask 2)	35	HMDS Coating	Dielectric Layer Formation
	36	- 2000 RPM / 1000 RPM/s acc/1 min	
	37	- Hotplate 150℃/ 5 min	
	38	AZ5214E Image Reversal Coating	
	39	- 1000 RPM / 500 RPM/s acc/ 1 min /expected thickness(around 2 micron)	
	40	- Hotplate 110℃ / 1 min	
	41	- Exposure with mask 40 mJ/cm^2	
	42	- Hotplate 120℃ / 1 min	
	43	- Flood exposure 250 mJ/cm^2	
	44	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	45	Tape wafer on top of another thick glass substrate	
	46	15min Warm-up process	
	47	Descum for 10 seconds	
E-Beam Evaporation (150nm HfO_2+50nm SiO_2)	48	Tooling Factor Calculation	
	49	- Sample 1: 50nm HfO_2+SiO_2	
	50	- Sample 2: 100nm HfO_2+SiO_2	
	51	Deposition Process	
	52	- Begin with 150nm HfO_2 and 50nm SiO_2	
	53	- Initial 10nm of HfO_2 and SiO_2 deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion	
	54	Precautions for Quality	
	55	- Check crystal monitor life for accurate thickness.	
	56	- Inspect material inside crucible to ensure proper melting.	
	57	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	58	Place wafer in acetone-filled container without sonicator	
	59	Wait until photoresist and unwanted materials are fully removed	
	60	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	61	Dry surface with N_2 blow	

Figure A.8

Photolithography and Patterning (Mask 3)	62	HMDS Coating	**Sacrificial Layer Formation**
	63	- 2000 RPM / 1000 RPM/s acc/1 min	
	64	- Hotplate 150℃/ 5 min	
	65	AZ5214E Image Reversal Coating	
	66	- 1000 RPM / 500 RPM/s acc/ 1 min /expected thickness (around 2 micron)	
	67	- Hotplate 110℃ / 1 min	
	68	- Exposure with mask 40 mJ/cm^2	
	69	- Hotplate 120℃ / 1 min	
	70	- Flood exposure 250 mJ/cm^2	
	71	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	72	Tape wafer on top of another thick glass substrate	
	73	15min Warm-up process	
	74	Descum for 10 seconds	
E-Beam Evaporation (600nm Poly-Si)	75	Tooling Factor Calculation	
	76	- Sample 1: 50nm Poly-Si	
	77	- Sample 2: 100nm Poly-Si	
	78	Deposition Process	
	79	- Begin with 600nm Poly-Si	
	80	- Initial 10nm Poly-Si deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	81	Precautions for Quality	
	82	- Check crystal monitor life for accurate thickness.	
	83	- Inspect material inside crucible to ensure proper melting.	
	84	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	85	Place wafer in acetone-filled container without sonicator	
	86	Wait until photoresist and unwanted materials are fully removed	
	87	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	88	Dry surface with N_2 blow	
Photolithography and Patterning (Mask 4)	89	HMDS Coating	**Anchor Formation**
	90	- 2000 RPM / 1000 RPM/s acc/1 min	
	91	- Hotplate 150℃/ 5 min	
	92	AZ4562 Positive Photoresist Coating	
	93	- 4000 RPM / 500 RPM/s acc/ 1 min /expected thickness (around 6 micron)	
	94	- Hotplate 110℃ / 1 min	
	95	- Exposure with mask 140 mJ/cm^2	
	96	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum and BOSCH Procces	97	Tape wafer on top of a thick glass substrate	
	98	15-minute warm-up process	
	99	Perform descum for 10 seconds	
	100	Continue Bosch process until the same color of HfO_2 is reached	
	101	Conduct EDX measurement to determine if etching is complete	
Photoresist Removal	102	Place wafer in acetone-filled container without sonicator	
	103	Wait until photoresist is fully removed	
	104	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	105	Dry surface with N_2 blow	

Figure A.9

Photolithography and Patterning (Mask 5)	106	HMDS Coating	**Top Membrane Formation**
	107	- 2000 RPM / 1000 RPM/s acc/1 min	
	108	- Hotplate 150℃/ 5 min	
	109	AZ5214E Image Reversal Coating	
	110	- 1000 RPM / 250 RPM/s acc/ 1 min /expected thickness (around 2 micron)	
	111	- Hotplate 110℃ / 15 sec	
	112	- 1000 RPM / 250 RPM/s acc/ 1 min /expected thickness (around 2 micron)	
	113	- Hotplate 110℃ / 15 sec	
	114	- 1000 RPM / 250 RPM/s acc/ 1 min / total expected thickness (around 6-7 micron)	
	115	- Hotplate 110℃ / 1 min	
	116	- Exposure with mask 40 mJ/cm^2	
	117	- Hotplate 120℃ / 1 min	
	118	- Flood exposure 250 mJ/cm^2	
	119	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	120	Tape wafer on top of another thick glass substrate	
	121	15min Warm-up process	
	122	Descum for 10 seconds	
E-Beam Evaporation (50nm Ti & 4-micron Cu)	123	Tooling Factor Calculation	
	124	- Sample 1: 50nm Ti	
	125	- Sample 2: 50nm Ti, 100nm Cu	
	126	- Sample 3: 50nm Ti, 250nm Cu	
	127	Deposition Process	
	128	- Begin with 50nm Ti as adhesion layer.	
	129	- Deposit 4-micron Cu in one shot without breaking the vacuum of the chamber	
	130	- Do not break the vacuum or stop the deposition before depositing 4-micron Cu to avoid crack formation	
	131	- Initial 10nm Cu deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	132	Precautions for Quality	
	133	- Check crystal monitor life for accurate thickness.	
	134	- Inspect material inside crucible to ensure proper melting.	
	135	- Cool chamber for at least 5 hours to avoid sudden temperature changes.	
Lift-off Process	136	Place wafer in acetone-filled container without sonicator	
	137	Wait until photoresist and unwanted materials are fully removed	
	138	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	139	Dry surface with N_2 blow	
Dicing Saw	140	Align wafer on dicing saw	**Sacrificial Layer Release**
	141	Make precise cuts to separate wafer into individual chips	
	142	Handle individual chips carefully to prevent damage or contamination	
Piranha Cleaning	143	Place individual chips in diluted Piranha solution (1:20 dilution) for 5 second	
	144	Perform this step immediately before the BOE process	
BOE Cleaning	145	Immerse individual chips in Buffered Oxide Etch (BOE) for 10 seconds to remove the oxide layer	
	146	Thoroughly rinse chips with deionized (DI) water to remove residual etchant	
	147	Dry chips using a nitrogen (N_2) blow	
Xenon Difluoride Etching	148	Subject chips to an etching cycle to etch the poly-silicon layer	
	149	Monitor etch progress closely, adjusting the process as needed	
	150	Continue etching until poly-silicon is completely etched, releasing the top membrane	

Figure A.10

A.4 Final Microfabrication Process Flow for PR-CMUTs

Description	step#	Details	
Pyrex Cleaning	1	Acetone / 3 min	Preparation
	2	IPA / 3 min	
	3	DI Water / 3 min	
	4	N_2 blow / 3 min	
	5	Hotplate at 120℃ 10 min	
Photolithography and Patterning (Mask 1)	6	HMDS Coating	Bottom electrode formation
	7	- 2000 RPM / 1000 RPM/s acc/1 min	
	8	- Hotplate 150℃/ 5 min	
	9	AZ5214E Image Reversal Coating	
	10	- 1000 RPM / 500 RPM/s acc / 1 min /expected thickness (around 2 micron)	
	11	- Hotplate 110℃ / 1 min	
	12	- Exposure with mask 40 mJ/cm^2	
	13	- Hotplate 120℃ / 1 min	
	14	- Flood exposure 250 mJ/cm^2	
	15	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	16	Tape wafer on top of another thick glass substrate	
	17	15min Warm-up process	
	18	Descum for 10 seconds	
E-Beam Evaporation (50nm Cr & 450nm Cu)	19	Tooling Factor Calculation	
	20	- Sample 1: 50nm Cr	
	21	- Sample 2: 50nm Cr, 100nm Cu	
	22	- Sample 3: 50nm Cr, 250nm Cu	
	23	Deposition Process	
	24	- Begin with 50nm Cr as adhesion layer.	
	25	- Follow with 450nm Cu without breaking the vacuum.	
	26	- Initial 10nm Cu deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	27	Precautions for Quality	
	28	- Check crystal monitor life for accurate thickness.	
	29	- Inspect material inside crucible to ensure proper melting.	
	30	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	31	Place wafer in acetone-filled container without sonicator	
	32	Wait until photoresist and unwanted metals are fully removed	
	33	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	34	Dry surface with N_2 blow	
Photolithography and Patterning (Mask 2)	35	HMDS Coating	Dielectric Layer Formation
	36	- 2000 RPM / 1000 RPM/s acc/1 min	
	37	- Hotplate 150℃/ 5 min	
	38	AZ5214E Image Reversal Coating	
	39	- 1000 RPM/s / 500 RPM/s acc/ 1 min /expected thickness (around 2 micron)	
	40	- Hotplate 110℃ / 1 min	
	41	- Exposure with mask 40 mJ/cm^2	
	42	- Hotplate 120℃ / 1 min	
	43	- Flood exposure 250 mJ/cm^2	
	44	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	45	Tape wafer on top of another thick glass substrate	
	46	15min Warm-up process	
	47	Descum for 10 seconds	
E-Beam Evaporation (150nm HfO_2+50nm SiO_2)	48	Tooling Factor Calculation	
	49	- Sample 1: 50nm HfO_2+SiO_2	
	50	- Sample 2: 100nm HfO_2+SiO_2	
	51	Deposition Process	
	52	- Begin with 150nm HfO_2 and 50nm SiO_2	
	53	- Initial 10nm of HfO_2 and SiO_2 deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion	
	54	Precautions for Quality	
	55	- Check crystal monitor life for accurate thickness.	
	56	- Inspect material inside crucible to ensure proper melting.	
	57	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	58	Place wafer in acetone-filled container without sonicator	
	59	Wait until photoresist and unwanted materials are fully removed	
	60	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	61	Dry surface with N_2 blow	

Figure A.11

Photolithography and Patterning (New Mask 3)	62	HMDS Coating	**Sacrificial Layer Formation**
	63	- 2000 RPM / 1000 RPM/s acc/1 min	
	64	- Hotplate 150℃/ 5 min	
	65	AZ5214E Image Reversal Coating	
	66	- 1000 RPM / 500 RPM/s acc/ 1 min /expected thickness (around 2 microu)	
	67	- Hotplate 110℃ / 1 min	
	68	- Exposure with mask 40 mJ/cm^3	
	69	- Hotplate 120℃ / 1 min	
	70	- Flood exposure 250 mJ/cm^2	
	71	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	72	Tape wafer on top of another thick glass substrate	
	73	15min Warm-up process	
	74	Descum for 10 seconds	
E-Beam Evaporation (600nm Poly-Si)	75	Tooling Factor Calculation	
	76	- Sample 1: 50nm Poly-Si	
	77	- Sample 2: 100nm Poly-Si	
	78	Deposition Process	
	79	- Begin with 600nm Poly-Si	
	80	- Initial 10nm Poly-Si deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	81	Precautions for Quality	
	82	- Check crystal monitor life for accurate thickness.	
	83	- Inspect material inside crucible to ensure proper melting.	
	84	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	85	Place wafer in acetone-filled container without sonicator	
	86	Wait until photoresist and unwanted materials are fully removed	
	87	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	88	Dry surface with N_2 blow	
Photolithography and Patterning (Mask 5)	89	HMDS Coating	**Top Membrane Formation**
	90	- 2000 RPM rpm/ 1000 RPM/s acc/1 min	
	91	- Hotplate 150℃/ 5 min	
	92	AZ5214E Image Reversal Coating	
	93	- 1000 RPM / 250 RPM/s acc/ 1 min /expected thickness (around 2 microu)	
	94	- Hotplate 110℃ / 15 sec	
	95	- 1000 RPM / 250 RPM/s acc/ 1 min /expected thickness (around 2 micron)	
	96	- Hotplate 110℃ / 15 sec	
	97	- 1000 RPM / 250 RPM/s acc/ 1 min / total expected thickness (around 6-7 micron)	
	98	- Hotplate 110℃ / 1 min	
	99	- Exposure with mask 40 mJ/cm2	
	100	- Hotplate 120℃ / 1 min	
	101	- Flood exposure 250 mJ/cm2	
	102	- Develop 1:4 AZ400K:DI Water / 1 min	
	103	- Flood exposure 250 mJ/cm$_2$	
	104	- Develop 1:4 AZ400K:DI Water / 1 min	
ICP-Descum	105	Tape wafer on top of another thick glass substrate	
	106	15min Warm-up process	
	107	Descum for 10 seconds	
E-Beam Evaporation (50nm Cr & 4-micron Cu)	108	Tooling Factor Calculation	
	109	- Sample 1: 50nm Cr	
	110	- Sample 2: 50nm Cr, 100nm Cu	
	111	- Sample 3: 50nm Cr, 250nm Cu	
	112	Deposition Process	
	113	- Begin with 50nm Cr as adhesion layer	
	114	- Deposit 4-micron Cu in one shot without breaking the vacuum of the chamber	
	115	- Do not break the vacuum or stop the deposition before depositing 4-micron Cu to avoid crack formation	
	116	- Initial 10nm Cu deposition at 0.3 Å/s, subsequent at 0.5-0.8 Å/s for good adhesion and uniform layer	
	117	Precautions for Quality	
	118	- Check crystal monitor life for accurate thickness.	
	119	- Inspect material inside crucible to ensure proper melting.	
	120	- Cool chamber for at least 30 minutes to avoid sudden temperature changes.	
Lift-off Process	121	Place wafer in acetone-filled container without sonicator	
	122	Wait until photoresist and unwanted materials are fully removed	
	123	Rinse wafer in DI water to eliminate acetone and dissolved residues	
	124	Dry surface with N_2 blow	

Figure A.12

Dicing Saw	125	Align wafer on dicing saw	**Sacrificial Layer Release**
	126	Make precise cuts to separate wafer into individual chips	
	127	Handle individual chips carefully to prevent damage or contamination	
Piranha Cleaning	128	Place individual chips in diluted Piranha solution (1:20 dilution) for 5 second	
	129	Perform this step immediately before the BOE process	
BOE Cleaning	130	Immerse individual chips in Buffered Oxide Etch (BOE) for 10 seconds to remove the oxide layer	
	131	Thoroughly rinse chips with deionized (DI) water to remove residual etchant	
	132	Dry chips using a nitrogen (N_2) blow	
Xenon Diflouride Etching	133	Subject chips to an etching cycle to etch the poly-silicon layer	
	134	Monitor etch progress closely, adjusting the process as needed	
	135	Continue etching until poly-silicon is completely etched, releasing the top membrane	

Figure A.13

Appendix B

Data Analysis Code

The following Python code is used for processing data and generating results:

```
import os
os.environ['DISPLAY'] = ':0'
import numpy as np
import matplotlib.pyplot as plt
from tqdm.auto import tqdm
import pandas as pd

def level_data_using_plane(data, point1, point2, point3):
    def get_median_point(data, point):
        region = data[point[0] - 5:point[0] + 5, point[1] - 5:point[1] + 5]
        median_value = np.median(region)
        abs_diff = np.abs(region - median_value)
        median_local_pos = np.unravel_index(np.argmin(abs_diff), region.shape)
        median_global_pos = (point[0] - 5 + median_local_pos[0], point[1] - 5 + median_local_pos[1])
```

```
            return (median_global_pos[0], median_global_pos
                [1], data[median_global_pos])

        p1 = get_median_point(data, point1)
        p2 = get_median_point(data, point2)
        p3 = get_median_point(data, point3)

        points = np.array([p1, p2, p3])

        A = np.c_[points[:, 0], points[:, 1], np.ones(
            points.shape[0])]
        C, _, _, _ = np.linalg.lstsq(A, points[:, 2], rcond
            =None)
        a, b, d = C[0], C[1], C[2]

        normal_vector = np.array([a, b, -1])
        normal_vector = normal_vector / np.linalg.norm(
            normal_vector)

        def rotation_matrix_from_vectors(vec1, vec2):
            a, b = (vec1 / np.linalg.norm(vec1)).reshape(3)
                , (vec2 / np.linalg.norm(vec2)).reshape(3)
            v = np.cross(a, b)
            c = np.dot(a, b)
            s = np.linalg.norm(v)
            kmat = np.array([[0, -v[2], v[1]], [v[2], 0, -v
                [0]], [-v[1], v[0], 0]])
            rotation_matrix = np.eye(3) + kmat + kmat @
                kmat * ((1 - c) / (s ** 2))
            return rotation_matrix

        rotation_mat = rotation_matrix_from_vectors(
            normal_vector, np.array([0, 0, 1]))

        x_indices, y_indices = np.indices(data.shape)
```

```
42          data_points = np.c_[x_indices.ravel(), y_indices.
               ravel(), data.ravel()]
43          rotated_data_points = (rotation_mat @ data_points.T
               ).T
44
45          leveled_data = rotated_data_points[:, 2].reshape(
               data.shape)
46
47          mean_z = np.mean([leveled_data[p1[0], p1[1]],
               leveled_data[p2[0], p2[1]], leveled_data[p3[0],
               p3[1]]])
48          leveled_data = leveled_data - mean_z
49
50          return -leveled_data
51
52      def process_file(file_path, point1, point2, point3):
53          data = np.genfromtxt(file_path, delimiter=',')
54
55          leveled_data = level_data_using_plane(data, point1,
                point2, point3)
56
57          p_middle = (330, 230)
58          region = leveled_data[p_middle[0] - 5:p_middle[0] +
                5, p_middle[1] - 5:p_middle[1] + 5]
59          median_value = np.median(region)
60
61          return median_value * 1e9
62
63      def process_folder(folder_path, point1, point2, point3)
           :
64          results = []
65          files = sorted([f for f in os.listdir(folder_path)
               if f.endswith('.csv')])
66          results = {
67              'File Name': [],
```

```
            'Displacement (nm)': [],
            'Frequency (KHz)': [],
            'Phase (deg)': []
        }
        for idx, file in tqdm(enumerate(files), desc='
           Processing files', total=len(files)):
            file_path = os.path.join(folder_path, file)
            result = process_file(file_path, point1, point2
               , point3)
            # results.append(result)
            results['File Name'].append(file)
            results['Displacement (nm)'].append(result)
            results['Frequency (KHz)'].append((idx // 73) *
                5 + 1)
            results['Phase (deg)'].append((idx % 73) * (360
                / 72))
        return results

    if _name_ == "_main_":
        import pandas as pd

        point1 = (300, 5)
        point2 = (200, 475)
        point3 = (400, 475)
        def process_all_folders(root_folder, point1, point2
           , point3):
            for dirpath, dirnames, filenames in os.walk(
               root_folder):
                if not dirnames:  # This is a leaf
                   directory
                    print(f'Processing folder: {dirpath}')

                    results = process_folder(dirpath,
                       point1, point2, point3)

```

```
                    df = pd.DataFrame(results)
                    df.to_excel(os.path.join(dirpath, '
                        results.xlsx'), index=False)

                    # Plot results
                    plt.figure(figsize=(10, 6))
                    plt.plot(df['Displacement (nm)'])
                    plt.xlabel('File Index')
                    plt.ylabel('Displacement (nm)')
                    plt.title('Displacement (nm) vs File
                        Index')
                    plt.grid(True)
                    plt.savefig(os.path.join(dirpath, '
                        middle_values.png'))

    root_folder = 'outputs'
    process_all_folders(root_folder, point1, point2,
        point3)
```