ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN AND LAYOUT OF A 1.5ns TO 8ns DELAY LOCKED LOOP FOR HIGH SPEED D/A CONVERTER APPLICATIONS

M.Sc. THESIS

Farshad PIRI

Department of Electronics and Telecommunication Engineering

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Thesis Advisor: Assoc. Prof. Dr. Türker KÜYEL

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

YÜKSEK HIZLI SAYISAL/ANALOG DÖNÜŞTÜRÜCÜ UYGULAMALARI İÇİN 1.5ns İLE 8ns ARASINDA ÇALIŞAN GECİKME KİLİTLEMELİ ÇEVRİM TASARIMI VE SERİMİ

YÜKSEK LİSANS TEZİ

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MAYIS 2015

Farshad PIRI, a **M.Sc.** student of ITU **Graduate School of Science Engineering and Technology** 504121363, successfully defended the thesis entitled "DESIGN AND LAYOUT OF A 1.5ns TO 8ns DELAY LOCKED LOOP FOR HIGH SPEED D/A CONVERTER APPLICATIONS", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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Date of Submission : 29 April 2015
Date of Defense : 29 May 2015

To my family and friends,

FOREWORD

I would like to thank my thesis supervisor Assoc. Prof. Dr. Türker Küyel for his invaluable guidance, help and encouragement. I also should thank him and ITU VLSI LABs for providing me a computer and a desk at the office to work.
I thank my family and all my friends who helped me with the problems I encountered during my studies. I would never succeeded without their help and support.

May 2015

Farshad PIRI
(Electronics Engineer)

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ABBREVIATIONS

CP	**:** Charge Pump
C2C	**:** Cycle to Cycle
DLL	**:** Delay Locked Loop
DDR	**:** Double Data Rate
DCC	**:** Duty Cycle Correction
JEDEC	**:** Joint Electron Device Engineering Council
LF	**:** Loop Filter
LSB	**:** Least Significant Bit
MSB	**:** Most Significant Bit
PFD	**:** Phase and Frequency Detector
PVT	**:** Process, Voltage and Temprature
PSRR	**:** Power Supply Rejection Ratio
SOC	**:** System On Chip
VCDL	**:** Voltage Controled Delay Line

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DESIGN AND LAYOUT OF A 1.5ns TO 8ns DELAY LOCKED LOOP FOR HIGH SPEED D/A CONVERTER APPLICATION

SUMMARY

As the VLSI technologies decreases to sub-micron and increases the clock frequencies the demand to correctly align the clock frequency with input data increases.

On the other hand, as the clock period is reduced in high-speed applications the timing jitter becomes crucial border in clock distribution networks. Also by decreasing the clock period, if the jitter and skew remain constant, the total clock phase error increases.

This issue will hugely affect synchronous system properties like setup and hold times in flip-flops, data access times and the precision of internal control signals.

The process, temperature and voltage variation effects on clock are another problems that cause timing jitter and need to be compensated with employing a DLL to stabilize the delay of the unit delay across PVT.

In this work, a 120MHz to 670MHz delay locked loop in 180nm TSMC CMOS process is presented to align the input clock and data of the 1.25GSPS high speed digital to analog converter.

Three separate voltage controlled delay lines used to achieve a wide frequency range. An 8-Bit shift register is used to select the proper VCDL according to the reference input clock, this is happened by the last 4-Bit of a serial 8-Bit input code of shift register and will be discussed in detail.

A TSPC based phase and frequency detector is used to achieve high-speed operation and acceptable rate of jitter to produce UP and DOWN pulses to control charge pump switches.

A single ended charge pump is used to convert these UP and DOWN pulses to a control voltage through a loop filter to control the delay of the VCDL and lock the DLL to a one period delayed clock signal.

In order to perform corner and monte-carlo simulations and evaluate the performance of the proposed delaye locked loop, a test bench with multiple input frequencies designed to apply different input clock frequencies to the DLL block.

The full layout of this system is drawn to evaluate the effect of the parasitics and circuit mismatch. Then cycle to cycle jitter, peak to peak jitter, duty cycle error, settling time are simulated across PVT and monte-carlo results are provided.

YÜKSEK HIZLI ANALOG/SAYISAL DÖNÜŞTÜRÜCÜLER UYGULAMASI İÇİN 1.5ns İLE 8ns GECİKME KİLİTLEMELİ ÇEVRİM TASARIMI VE SERİMİ

ÖZET

Yüksek performanslı sayısal devrelerin kullanımının artmasıyla yüksek hızlı ve yüksek doğruluklu data dönüştürücülere olan ilgi de artmıştır. Ayrıca, yüksek hızlı data dönüştürücülerle birlikte kullanılacak ve data dönüştürücüye yüksek hızda data aktarımını sağlayacak arayüz devrelerine ihtiyaç duyulmuştur. Bununla beraber, yüksek hızlı ve doğruluklu çalışma için data ile saat işareti arasındaki senkronizasyonu sağlayan devreler de kullanılmalıdır.

Çip içerisindeki sayısal analog dönüştürücüye verileri ve bu veriler ile senkron saat işaretini verebilme açısından Alanda Programlanabilir Kapı Dizileri (Field Programmable Gate Array – FPGA), düşük maliyetli ve başarılı çözümlerdir.

Ancak FPGA'dan gelecek olan saat işaretinde, sentezlenen temiz saat işaretine göre daha fazla kaymalar ve sapmalar oluşacaktır. Bu sapmalar, DAC'ın SFDR performansını önemli ölçüde düşürecektir. SFDR değerinin yine yüksek değerlerde olabilmesi için DAC'a sentezleyiciden gelen temiz saat işareti verilmelidir. Ancak bu durumda da devrede iki adet saat işareti olur ve bu işaretlerin arasında senkronizasyon sağlanmalıdır.

FPGA'dan alınan verilerin devredeki iki saat işareti arasında senkronizasyon sağlayacak olan kaydedici yapısına yazılabilmesi için, saat işaretinin, verinin tam ortasına denk getirilmesi, bunun için de gecikme kilitlemeli çevrim (Delay Locked Loop - DLL) devresi tasarlanması gerekmektedir.

Ancak yükses örnekleme hızlarına ulaşmak üzere her saat işareti periodunda iki kere data yazma ya da okuma işlemi gerçeklemek üzere (DDR) saat işaretinin 90° ve 270° kaydırılmasını gerçeklemesi amacı DLL yapısı yardımıyla yapılmaktadır.

Ayrıca, yüksek hızlı devrelerde (1 GSPS ve üzeri) saat işaretinin genliği çok küçük olduğundan, herhangi bir sebepten dolayı oluşan küçük bir kayma (Jitter) büyük INL ve DNL hatalarına neden olmaktadır.Örneğin 1.25 GSPS bir DAC uygulaması için saat işaretinin periodu 800ps ve genliği 400ps olarak hesaplanmaktadır. Bu durumda 200ps bir saat işaretindeki hata devredeki saat işaretinin genliğinin %50'sine eşittir. Bu hataları azaltmak üzere DLL yapısı kullanılmaktadır.

Jitter hatalarından rastgele ve deterministik olarak iki ayrı başlık altında bahsedilebilir. Rastgele jitter genişbantlı stokastik gaussian bir süreçtir ve genelde rastgele gürültüden kaynaklanmaktadır.

Deterministik jitterin belirli bir kaynaktan oluşturulması ve rastgele olmadığı bir etkidir ve genelikle dar bantlı ve periodiktir. Deterministik jitter türü örnek olarak bir periodik siğnalden oluşan crosstalk dan türetiliyor yada bir anahtarlanan güç kaynağından.

Çip içindeki saat işaretinin kaymalarına neden olan etkileri sıfır yapmak mümkün olmadığından bu saat işareti kaymaları (Skew) ve Jitter etkilerini minimum yapmak en basit yöntemdir ve bunun için de saat işareti dağıtma ve geciktirme yapıları kullanılmaktadır.

DLL devresinin genel yapısında bir gerilim kontrollü gecikme hattından (VCDL) yararlanılmaktadır, bu VCDL hattının gecikmesi giriş gerilimi ile orantılı olarak değişmektedir. VCDL devresinin çıkışındaki saat işaretinin, giriş saat işaretinin tam bir periodu kadar gecikmesi gerekmektedir ve bu durumda VCDL hattının dörtte birlik kısmından çıkış alınırsa 90° gecikme elde edilmektedir.

Ayrıca VCDL çıkışındaki saat işareti ile referens saat işaretinin arasındaki farkı ölçmek ve devrenin gecikmesini ona göre ayarlamak için bir faz ve ferekans detektör (PFD) yapısı kullanılmaktadır. PFD devresinin amacı çıkışta iki UP ve ya DOWN işareti üretmektir, UP işaretini anlamı, geciktirilmiş saat işaretinin referans saat işaretine göre geride kalmış olduğunu ve hızlanması gerektiğini ifade etmektedir. DOWN işaretiyse geciktirilmiş olan saat işaretinin referans işaretine göre daha hızlı olduğunu ve yavaşlanması gerektiğini ifade etmektedir.

PFD devresinden türetilen UP ve DOWN işaretlerinin VCDL gecikme hattını kontrol etmesi için yük pompası (Charge Pump) kullanılması gerekmektedir. Yük pompasının çıkışına bir alçak geçiren çevrim süzgeci (loop filter) bağlanmaktadır ve bu çevrim yardımıyla UP ve DOWN işaretlerini süzgeç kapasitesinin üzerinde gerilime çevirmek mümkündür.

Yük pompası yapısı genel olarak iki akım kaynağı ve iki anahtar yapısından oluşmaktadır, anahtarların açılıp kapanmasıyla yük pompasının çıkışındaki kapasiteye gerilim eklenip çıkarılması mümkün omkatadır, ayrıca bu da elde etmek istediğimiz gecikmeyi kontrol eden gerilimi sağlamaktadır.

Devrenin jitter'ını düşük seviyede tutmak için yük pompasının önemli bir etken olduğu ve herhangi bir kuyruk akımı dengesizliğinin büyük jitterlara sebep olduğu görülmektedir.

Ayrıca DLL devresinin çıkışındaki saat işaretinin dolluk-boşluk (duty cycle) oranın %50 civarında olması en önemli etkenlerdendir. Burada yüksek hızda çalışmalar göz önüne alındığından bu devrelerin kurulum (Setup) ve bekleme (Hold) süreleri göz önüne alınırsa, verilerin doğru yerde örneklenmesi ve herangi bir kayıp olmaması için gereken bir parametredir. Saat işaretinin dolluk-boşluk (duty cycle) aralığını sabit tutmak üzere ek bir yapı kullanılmıştır.

DLL devresinin doğru kilitlediği ya da yanlış bir çevrimde takıldığı durumu belirlemek üzere bir kilitleme durumu belirleme yapısı kurulmuştur ve bu yapı çipin içindeki seri-çevresel arayüz (SPI) tarafından okunmaktadır ve DLL'in bulunduğu durumun kontrol edilmesini sağlamaktadır.

DLL yapısının 120MHz ile 670MHz geniş bir frekans aralığında çalışabilmesi için üç farklı gerilimle kontrol edilebilen gecikme hattı kullanılmıştır, ayrıca gerekli bir durumda giriş saat işaretini direkt devreye uygulayabilmesi için giriş ve çıkış arasında bir tamponlu yol (buffer path) yapılmıştır.

Sonuçta bu tez çalışmasında 120MHz ile 670MHz frekans aralığında çalışan DLL devresi ve serimi tasarlanmıştır, DLL'i kontrol etmek üzere bir digital kontrol bloğu yapılmıştır. Toplam devrenin corner ve monte carlo benzetim sonuçları verilmiştir.

1. INTRODUCTION

Most of the logic systems have a main clock signal to provide a common timing reference for all of the components in the system. In certain cases, it is necessary to have rising (or falling) edges at precise time instants, different from those in the main clock. To create those new timing edges at the appropriate times it is necessary to use delay circuits or delay lines. This delay is used to suppress skew and jitter in such systems inside chips. Delay-locked loops have been commonly used as frequency synthesizers and clock-deskewing circuits [1], [15], inter chip communication interfaces [2], [3], and clock distribution networks [4], [5]. On the other hand, these functions can be performed with Phase-locked loops, DLL's are usually preferred due to their simplicity of design, better immunity against on-chip noise, and their stability.

In Double Data Rate (DDR) systems, the output clock must be delayed by a fixed timing delay usually 90° and 270° to capture output data twice in one clock cycle.

DLL has a first order loop characteristic that is easy to stabilize and has no jitter accumulation.

1.1 Purpose of Thesis

The DLL in this thesis is intended to work within a wide frequency range from 120 MHz to 670 MHz with a maximum 200ps skew over process, voltage and temperature (PVT). The proposed DLL will be used in a high-speed digital to analog converter to align input DDR data and clock.

1.2 DLL in High Speed DAC Interface

As data rates increase, accurate sampling of digital data becomes challenging.

In a double data rate (DDR) system, the clock comes at the same speed as data, and both edges of the clock waveform are used to sample the data. Figure 1.1 shows a basic DDR output waveform. In a D/A converter the data comes in parallel and the skew of

each bit eats into the timing margin. Plus, clock jitter also reduce the timing margins. Inside the D/A converter, the clock signal must be delayed by quarter period in order proper sampling to occur. This is demonstrated in Figure 1.2.

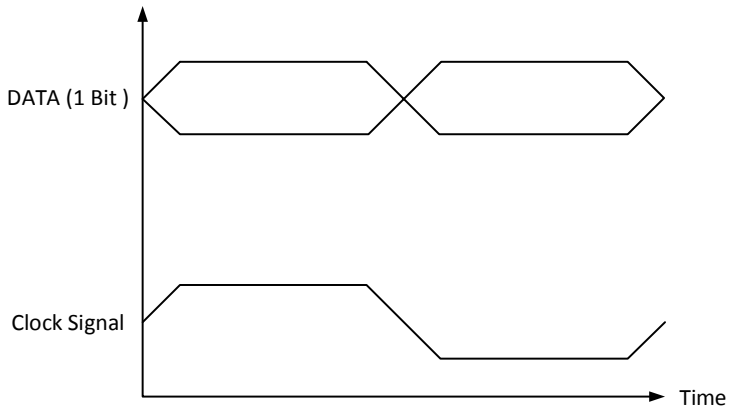


Figure 1.1: Aligned input signals

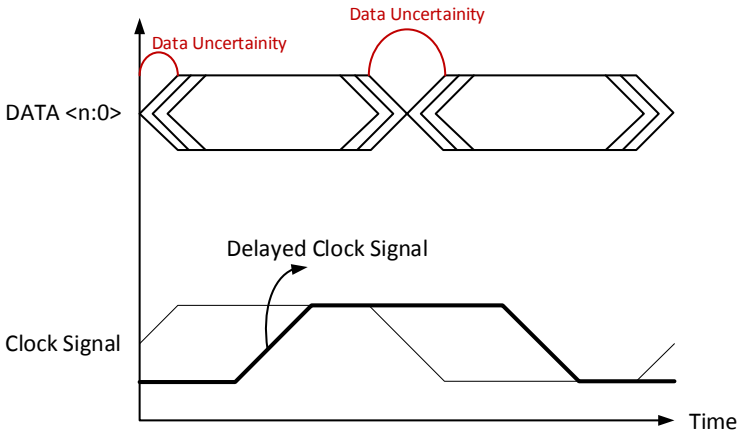


Figure 1.2: Effect of skew

For a 1.6 Gbps system, bit period is 625 ps and clock delay must be 312.5 ps, ideally speaking. This phase quadrature must be maintained across PVT by the DLL.

A D/A converter requires a low jitter external clock. A divided copy of this clock is generated by the DAC to drive the FPGA. This is called source synchronous clocking, where the DAC is the source. Once the FPGA computes the DAC data, it sends the data and the clock to the DAC using DDR LVDS. The DAC's LVDS receivers receive the data and the DLL clocks the data at correct (90 degree, 270 degree) phases. Two data streams are generated inside the DAC and two FIFO structures temporarily store these streams to phase align the FPGA data with the low jitter clock. This is shown in Figure 1.3.

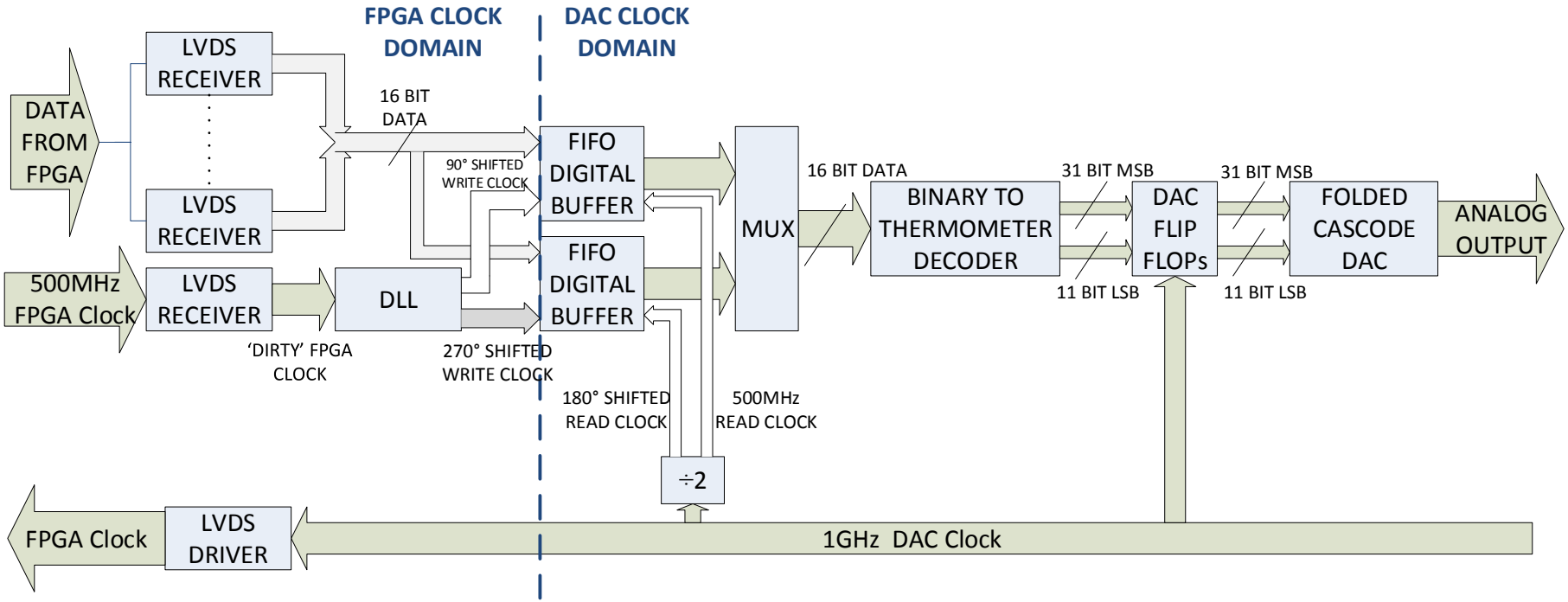


Figure 1.3: DLL in high speed DAC interface

2. LITERATURE REVIEW

Among a vast literature on delay locked loops, a few relevant examples are provided in this section.

A 2.5-Gb/s DLL based burst mode clock and data recovery circuit with 4×oversampling is presented in (Lin. J.M, 2015). With the advantage of a DLL to track the input phase, the proposed circuit can recover the burst mode data in a short acquisition time and achieve good jitter tolerance. The retimed data has a root-mean-square jitter of 8.557 ps and a peak-to-peak jitter of 32.0 ps, its calculated bit error rate is less than 10^{-10}. The total power consumption is 130mW from 1.8V supply voltage.

An All-Digital Delay-Locked Loop Using an In-Time Phase Maintenance Scheme for Low-Jitter Gigahertz Operations is presented in (Cheng, 2015). The system is constructed on a half delay line skew compensation circuit. The key design feature is a ping-pong phase maintenance scheme that allows the code adjustment to be performed in time in each clock cycle, even for gigahertz operations. The measurement results show that the DLL achieves a peak-to-peak (p-p) jitter of 3ps with 1.96mW power consumption and 8 lock-in cycles when operated at 2.5GHz.

A SAR-based all-digital Delay-Locked Loop with constant acquisition cycles using a resettable delay line is presented in (C. Y. Yao, 2015). The selected digitally controlled delay line (DCDL) is resettable such that constant acquisition-cycle DLL algorithm can apply. This work realizes the DCDL using lattice delay units in a linear manner, so the delay profile of our DCDL shows good linearity. On the other hand, the proposed ADDLL algorithm can effectively eliminate the harmonic lock. The measured power consumption of the chip is 16.2 mW at 1.2-GHz clock frequency and at 1.8 V supply voltage. The rms jitter is 1.63 ps and the peak-to-peak jitter is 12.8 ps. Both are measured at 1.2-GHz clock frequency.

A Process-Variation-Calibrated Multiphase Delay Locked Loop with a Loop-Embedded Duty Cycle Corrector presented in (Jung, 2014). The sense-amplifier-based

phase detector is proposed for reducing dithering jitter. Proposed DLL had a maximum phase error of 1.8% and a duty cycle error of 0.97% at 800 MHz.

A Wide-Range and fast locking all digital cycle controlled delay locked loop is presented in (Liu, 2005). Utilizing the cycle-controlled delay unit, the proposed DLL reuses the delay units to enlarge the operating frequency range rather than cascade a huge number of delay units. A two-step successive approximation register (SAR) controller ensures the proposed DLL to lock the input clock within 32 clock cycles regardless of input frequencies. Fabricated in 0.18 µm CMOS technology, the experimental prototype exhibits a wide locking range from 2 to 700 MHz with maximum 23mW power consumption and 17.6 ps peak-to-peak jitter at 700MHz operation frequency.

A 250MHz-2GHz wide range delay locked loop is presented in (Kim, 2005). This research describes a wide range DLL for a synchronous clocking which supports dynamic frequency scaling and dynamic voltage scaling. The DLL has wide operation range by using multiple phases from its delay line.

A clock multiplication technique using digital multiplying delay locked loop is presented in (A. Elshazly, 2013). The proposed architecture utilizes a calibration-free digital multiplying delay-locked loop (MDLL) to decouple the tradeoff between time-to-digital converter (TDC) resolution and oscillator phase noise in digital phase-locked loops (PLLs). The prototype MDLL and DPLL chips are fabricated in a 0.13 µm CMOS technology and operate from a nominal 1.1 V supply. The proposed MDLL achieves an integrated jitter of 400 fs rms at 1.5 GHz output frequency from a 375 MHz reference clock, while consuming 890 µW.

A low jitter process independent DLL and PLL based on self-biased techniques is presented in (Maneatis, 1996). Self-biasing avoids the necessity for external biasing.

A Fast-Lock low jitter DLL with double edge synchronization in 0.18 µm CMOS technology presented in (Mohammadi M. & Sabbaghi N., 2013). This describes a fast-lock, low-power, low-jitter and good duty cycle correction capability for clock and phase alignment inside a chip. Frequency range is 750MHz to 1GHz and power consumption at 1GHz is 3.4mW. Maximum rms jitter is 9.12ps and maximum peak-tp-peak jitter is 124.89ps. Locking time of DLL is less than 20ns.

3. BASIC DLL OPERATION

A basic analog DLL is composed of a Voltage Controlled Delay Line (VCDL), a Phase and Frequency Detector (PFD), a Charge Pump (CP) and Loop Filter (LF), as shown in Figure 3.1. Input clock signal passes through VCDL that is delayed for one period or 360°. The delayed output is fed back to the phase detector and compared with the input clock, then phase detector provides UP/DOWN signals according to the delay difference between its two inputs.

The CP uses the phase error information to adjust the voltage of the LF and thus to change the delay of the VCDL. Advantage of this negative feedback mechanism is that the phase error is gradually reduced until it finally becomes zero. As a result, the whole VCDL delay is set to one clock period of input clock, and the loop filter voltage stabilizes, which denotes that a locked state achieved.

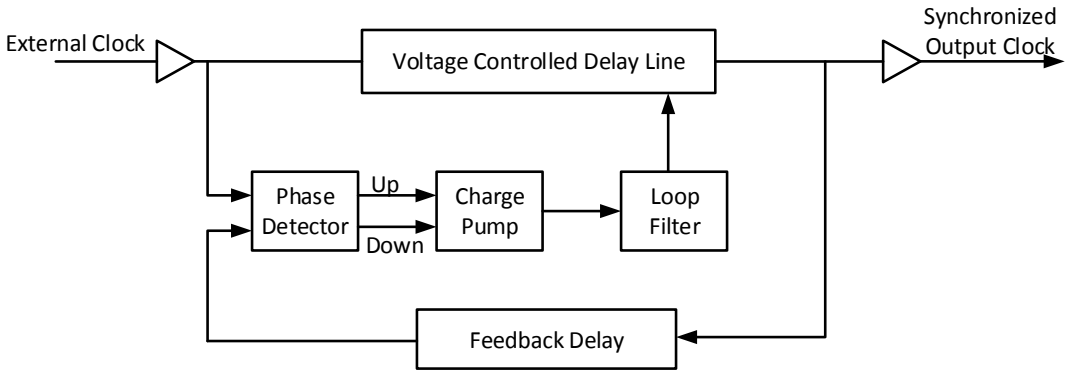


Figure 3.1: Basic DLL structure

3.1 DLL Transfer Function

The S-domain representation of delay locked loop for each loop element is depicted in Figure 3.2, in order to analyze loop dynamic of the DLL (Maneatis, 1996).

K_{PD} in figure above is the phase and frequency detector gain, I_{CP} is charge pump current, F(s) is the loop filter transfer function, which is a first order filter, which can be a single capacitor. The transfer function of the loop filter is written as:

$$F(s) = \frac{1}{sC_{loop}} \tag{3.1}$$

K_{VCDL} Variable is voltage controlled delay line gain, which is proportional to the number of delay cells.

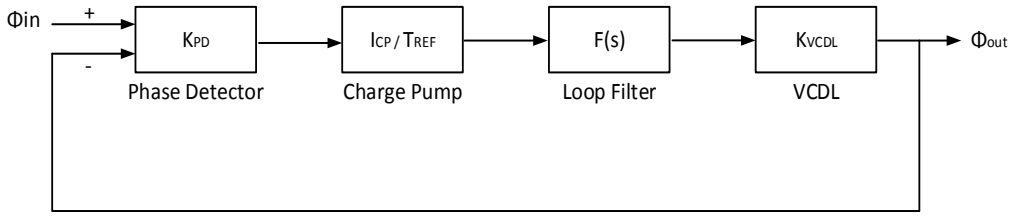


Figure 3.2: S domain model of DLL

The period of the input reference clock is assumed as T_{REF} and input/output phases are denoted by $\emptyset_{in}$ and $\emptyset_{out}$.

When the DLL is in the lock state, then its characteristic can be modeled by a first order transfer function:

$$\frac{\emptyset_{out}}{\emptyset_{in}} = \frac{1}{1 + {}^{s}/_{\omega_N}} \tag{3.2}$$

where ω_N denotes the close loop bandwidth, and corresponds to the -3db frequency

$$\omega_N = \frac{K_{PD}K_{VCDL}I_{CP}}{2\pi C_{loop}}\omega_{REF} \tag{3.3}$$

As can be seen from equations 3.2, the DLL is a single pole system. So, it is unconditionally stable.

Equation 3.3 denotes that ω_N tracks ω_{REF} if the coefficient $\frac{K_{PD}K_{VCDL}I_{CP}}{2\pi C_{loop}}$ stays constant.

In this tracking system, with increasing ω_{REF}, ω_N gets larger, which means a bigger loop bandwidth and faster acquisition time.

3.2 DLL Jitter analysis

Jitter is the key factor in the clock systems and DLL design. Jitter is a random or uncertain deviation of the clock period.

We assume that t_h is the time that h^{th} clock edge happens so the h^{th} clock cycle period can be compute as

$$T_h = t_h - t_{h-1} \tag{3.4}$$

If we consider that clock period is $\bar{T}$ in ideal case, the jitter can be defined as difference between $\bar{T}$ and T_h (M. Mansuri, Nov. 2002)

$$\Delta T_h = T_h - \bar{T} \tag{3.5}$$

Total accumulated amount of jitter or absolute jitter can be expressed by

$$\Delta T_{absolute}(M) = \sum_{h=1}^{M} \Delta T_h \tag{3.6}$$

Here M is the number of clock cycles.

Another definition for jitter is the cycle jitter which is the long term RMS of the ΔT_h.

$$\Delta T_{cycle} = \lim_{M\to\infty} \sqrt{\frac{1}{M}\sum_{h=1}^{M} {\Delta T_h}^2} \tag{3.7}$$

Cycle to cycle jitter can be denoted by the RMS difference between two adjacent clock cycles and can be expressed by

$$\Delta T_{cycle-to-cycle} = \lim_{M\to\infty} \sqrt{\frac{1}{M}\sum_{h=1}^{M} (t_h - t_{h-1})^2} \tag{3.8}$$

DLL systems are affected by two types of jitter. First type is the systematic jitter that is caused by deterministic noise sources such as 60 Hz coupling. Second type is

random jitter, which is caused by random noise source like thermal noise, substrate noise and random power supply ripples caused by digital activity.

4. DESIGNED BUILDING BLOCKS

4.1 Delay Cell

The delay cell must be capable of supporting the frequency range of interest by having minimum and maximum amount of delay. The simple continuously variable delay element is the current starved inverter as depicted in Figure 4.1 and its W/L ratios are given in Table 4.1.

The center transistors MP2, MP3, MN2 and MN3 form a normal CMOS inverter and the top and bottom (MP1 and MN1) transistors serve as variable current supplies. The maximum current supplied to the inverters controlled by the bias voltages VC_P and VC_N. A higher bias voltage increases the cell's current, thereby reducing the delay.

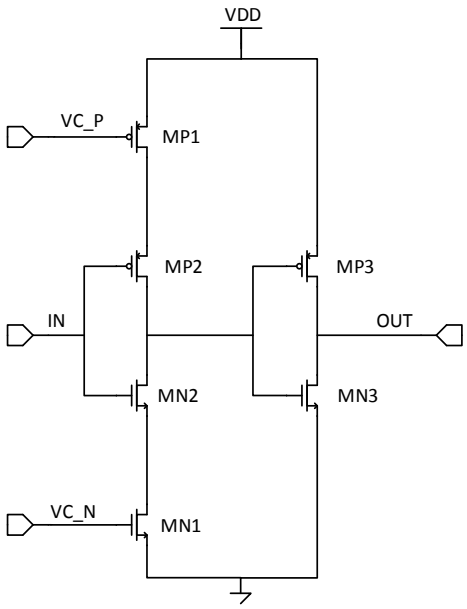


Figure 4.1: Delay element schematic.

Table 4.1: W/L ratios for delay element

	L (nm)	W (um)	Finger
MN2,MN3	300	1	1
MN1	300	1	3
MP2,MP3	300	3	1
MP1	300	3	3

In order to figure out the delay, the typical runs are performed using typical transistors and minimum-maximum delays of this delay cell are 100ps and 750ps for a 150MHz input clock signal as in Figure 4.2.

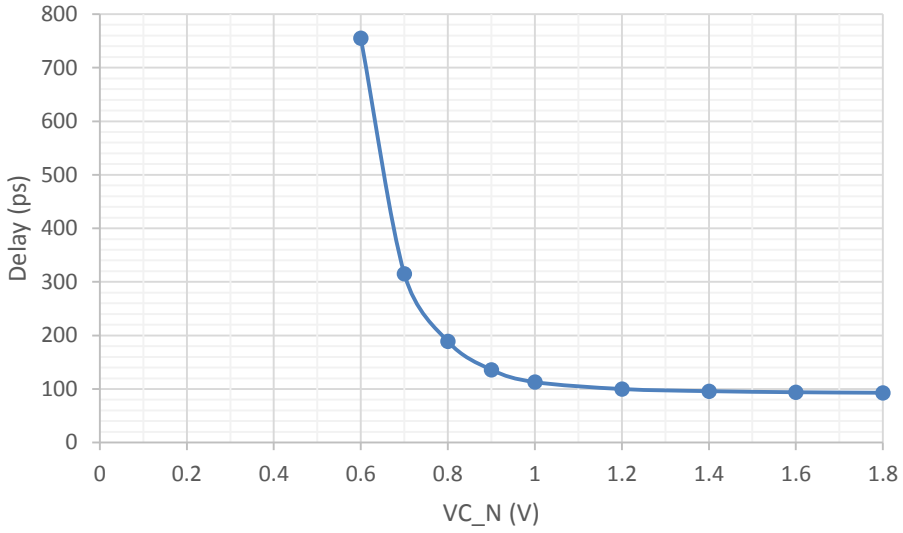
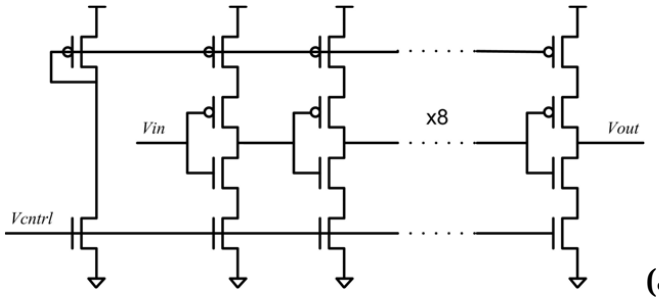
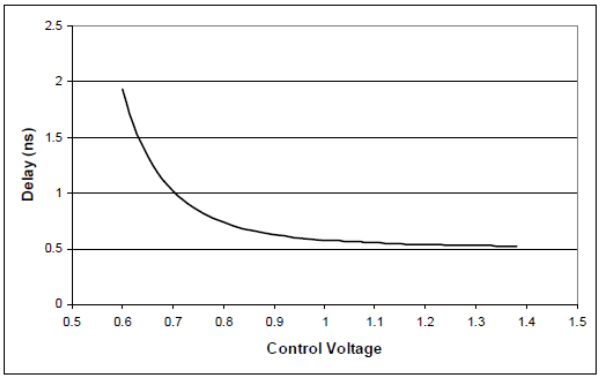


Figure 4.2: Delay versus control voltage of delay cell

To produce VC_N and VC_P to control delay cell we need a symmetric structure for NMOS and PMOS transistors as shown in Figure 4.3 (a). The transfer function of delay between input and output has a quadratic relationship as depicted in Figure 4.3 (b).



(a)

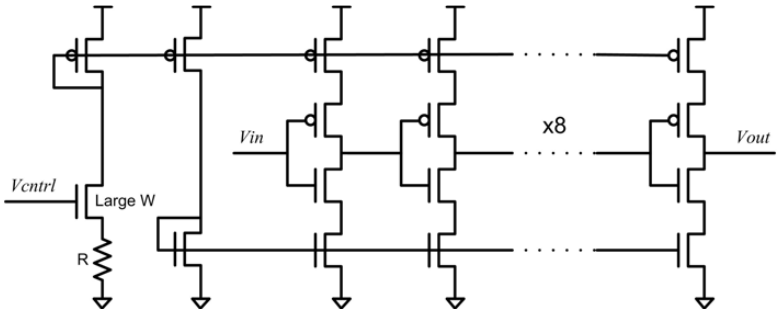


(b)

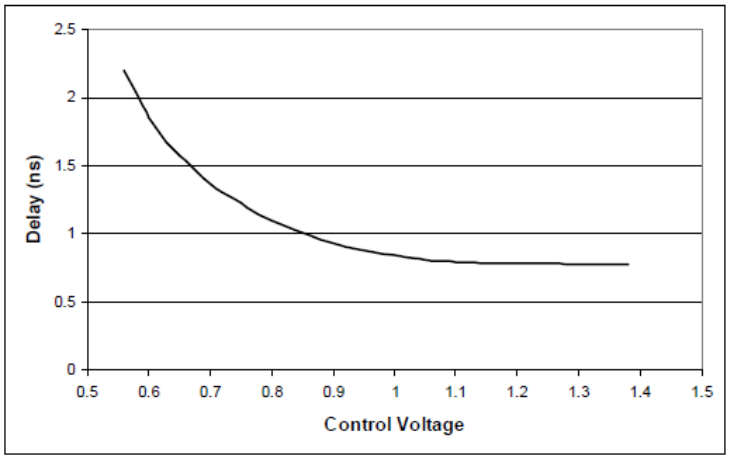
Figure 4.3: Basic control voltage structure: (a)schematic (b)delay waveform

These non-linear gain curves are one of the design challenges of an analog DLL. Figure 4.4 shows how the bias circuit can be altered so that the current is more linear with the input voltage. (Baker, 2005)

The width of M5R is wide so that its VGS is always (independent of Vctrl) approximately Vth, this eliminates the square term in the transfer function creating a wider semi-linear region in the transfer curves.



(a)



(b)

Figure 4.4: Linearized model for control voltage structure: (a)schematic (b)delay waveform

4.2 Voltage Controlled Delay Line (VCDL)

A VCDL generally comprise of number of delay elements (cells) that connected in series.

The VCDL takes two inputs, a control voltage and a clock. The output is a clock of the same frequency as the input, but phase shifted by some amount proportional to the control voltage. Figure 4.5 (a) shows schematics of a VCDL.

The total delay of the VCDL must set to one clock period T_{ref} (that is phase shift of 360°). In the locked state, all the delay elements in the VCDL are identical, thus, each

delay stage delay is $\frac{T_{ref}}{K}$ for an k stage VCDL. Increasing the number of stages improves phase resolution but also increase the minimum VCDL delay.

Double Data Rate (DDR) applications need two delayed clocks, at 90° and 270° phases. Considering the wide frequency range needed and also the granularity of phase settings, we chose to use eight delay elements in series.

Output of 2nd stage is 90° delayed, 4th stage is 180° delayed, 6th 270° delayed and 8th is 360° delayed shown in Figure 4.5 (b).

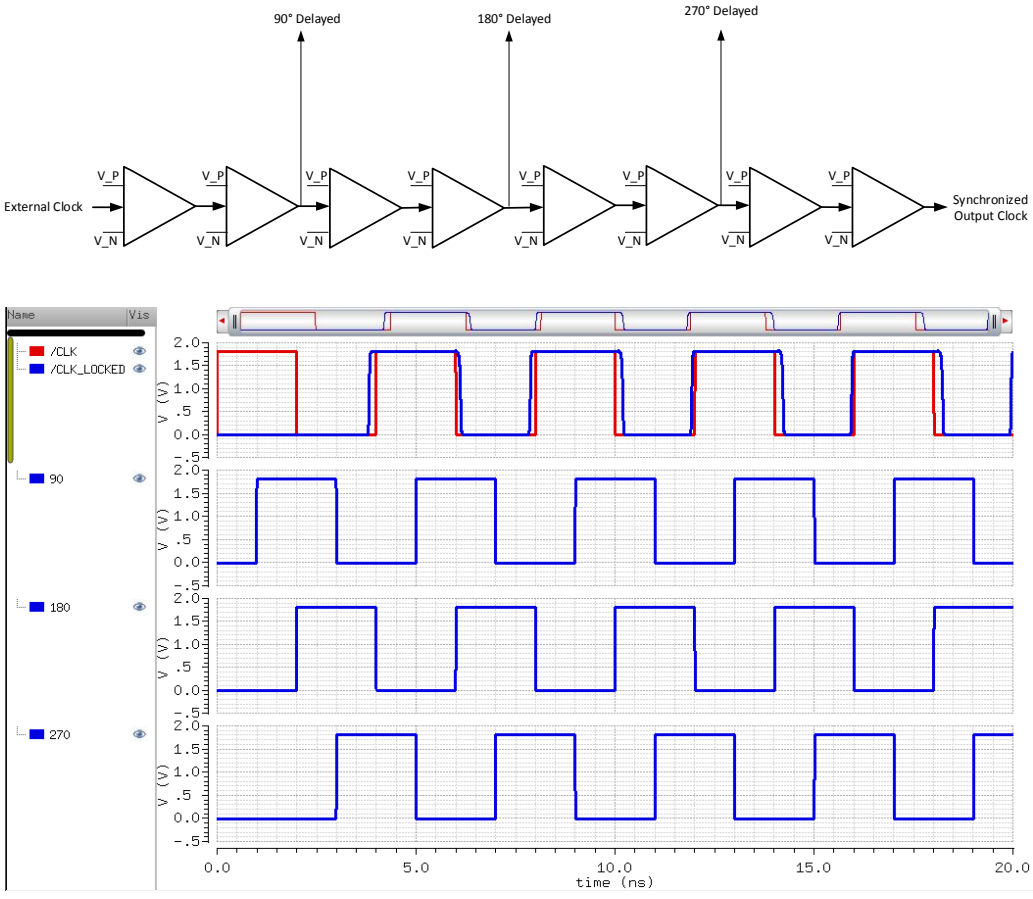


Figure 4.5: VCDL: (a)schematic (b) 90°, 180°, 270° and 360° delayed wave form

4.3 Phase and Frequency Detector (PFD)

The Phase and Frequency Detector is one of the most critical components within a DLL. The main difference of analog DLL and digital DLL is in the PFD structure. For both the analog DLL's PFD and digital DLL's PFD, one of the PFD inputs is the reference clock. For the other one a digital DLL generally uses the output of a digital tap, whose phase is the closest to the input reference clock. This tap is not certainly

the last tap of the VCDL. On the other hand, for an analog DLL, as the delay of the total VCDL must set to one clock cycle in the locked state, the other input of PFD is taken from output of the VCDL.

The PFD function is to detect the phase and frequency differences between the reference clock signal and the feedback clock signal from VCDL.

Most PFDs have a large dead zones. Dead zone occurs when the PFD does not respond to small phase errors. Dead zones create jitter in the DLL and should be avoided. Hence, this kind of PFDs cannot used at high frequencies. (Mohammadi M. & Sabbaghi N., 2013)

To overcome speed limitation and reduce the dead zone, proposed high-speed PFD structure is used as shown in Figure 4.6. (Johansson, 1998)

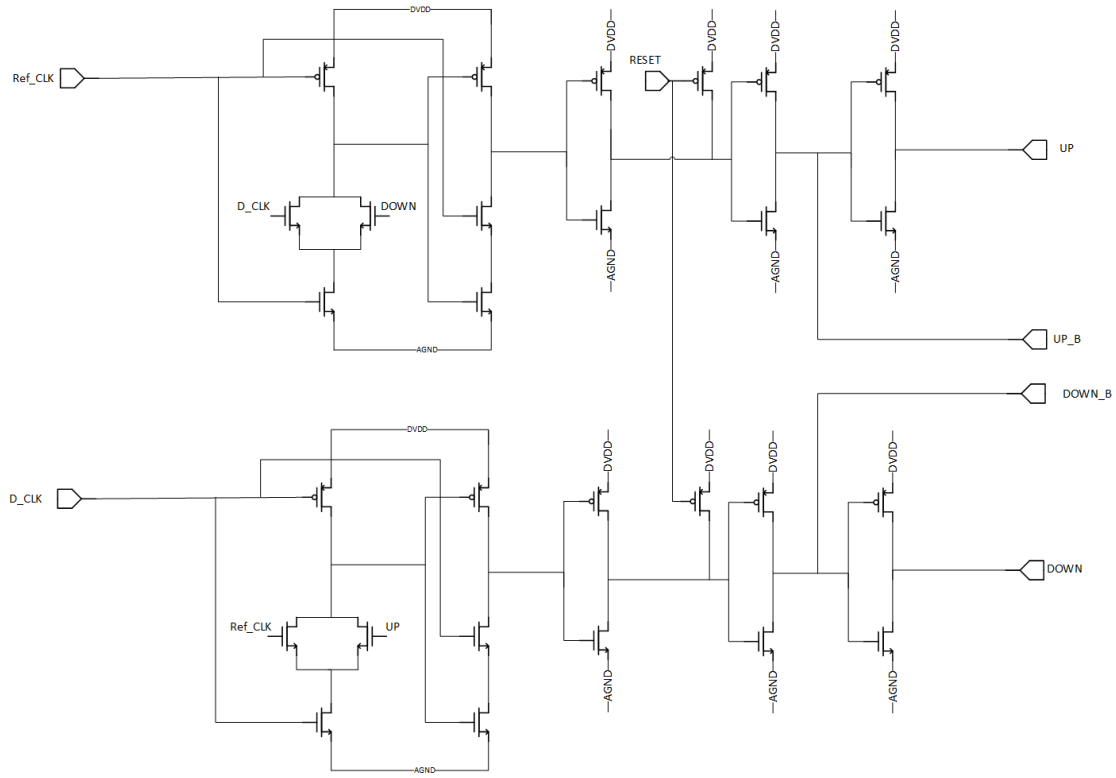
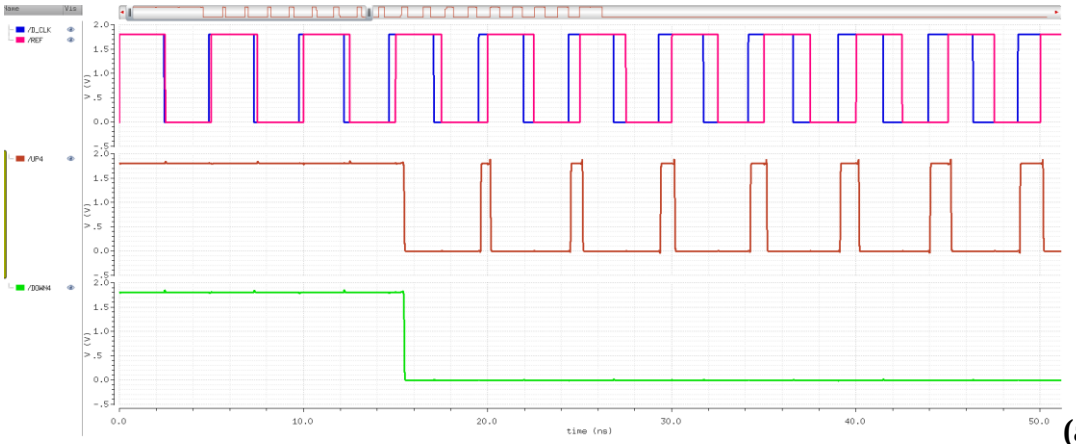


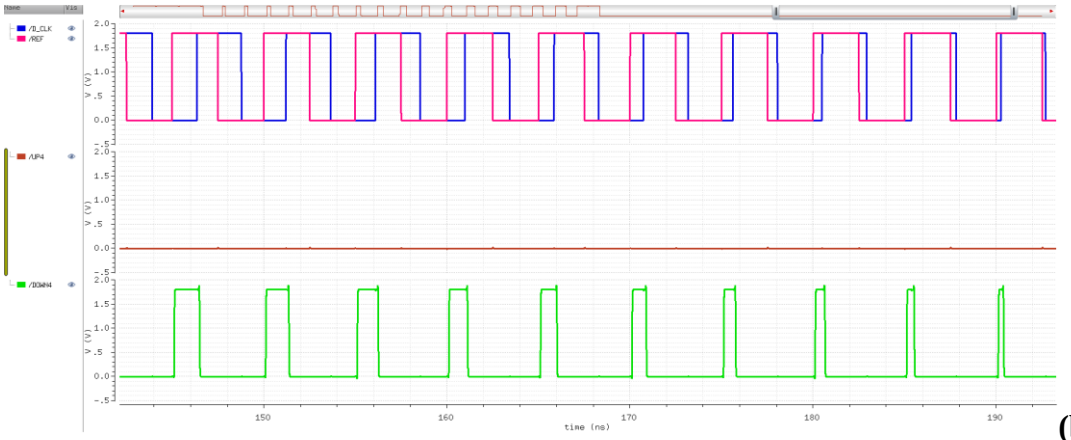
Figure 4.6: PFD Structure

The PFD structure used to detect rising pulse edge so the width of UP and DOWN signals at the output (D_CLK) are proportional to the phase difference of rising edge of the input signal (CLK) as shown in Figure 4.7.

All the transistors in PFD schematic have minimum 180nm length; PMOS transistors have 6µm width and NMOS ones have 2µm width.



(a)



(b)

Figure 4.7: PFD signal waveform: (a) UP signal (b) DOWN signal

As it seems from PFD waveforms, UP/DOWN signals are maximum $\frac{T_{ref}}{2}$ wide. Therefore, we can calculate DLL lock range as below:

$$\boldsymbol{T_{VCDL\,min} > \frac{T_{ref}}{2}} \quad \textbf{(4.1)}$$

$$T_{VCDL\,max} < \frac{3}{2} T_{ref} \quad \textbf{(4.2)}$$

For a delay line that need to be operate at 150MHz to 350 MHz, we need to have:

$$T_{VCDL\,min} > 1.43ns \quad \textbf{(4.3)}$$

$$T_{VCDL\,max} < 10ns \quad \textbf{(4.4)}$$

That means our VCDL must delay an input CLK from 1.43ns up to 10ns also considering PVT as extra margins this forces us to use three separate VCDL units in Order to cover 120MHz to 670MHz locking range.

4.4 Charge Pump (CP)

Charge pump is the circuit that translates the UP and DOWN signals of the PFD to the control voltage that will manage the VCDL delay time. The charge pump adjusts the voltage of the loop filter, and this in turn causes a change in the VCDL delay time, according to the phase error information from the PFD. In general, the CP consists of two controlled switches driving a capacitance load. One switch serves in a current source, and the other switch serves in a current sink, as shown in Figure 4.8.

The S_1 and S_2 switches are controlled by the UP and DOWN pulses of PFD, Once the switch is closed, the current source or sink will start adding charge to or removing charge from the loop filter capacitor C_L. This charging and discharging progress will stop when lock is achieved. In the lock state, the voltage of the loop filter capacitance will stay constant. In some cases equal charging and discharging can appear during lock state. In fact, it is desired to have such changes to minimize the jitter (Maneatis, 1996).

In order to have a stable control voltage, the charging and discharging currents must be identical and very small to not disturb the loop filter voltage significantly.

In the implementation, the basic structure in Figure 4.8 contains some non-ideal effects that may lead to time jitter (Rhee, 1999). One of them is the mismatch between the charging and discharging currents I_{up} and I_{Down}. Amount of unwanted phase shift due to CP mismatch can estimated by equation 4.5 (Rhee, 1999)

$$\phi_{offset} = 2\pi \frac{\Delta t_{on}}{T_{REF}} \frac{\Delta_i}{I_{CP}} \quad \textbf{(4.5)}$$

Here Δt_{on} is the turn on time (or the pulse width of the UP and DOWN pulses), Δ_i is the current mismatch and T_{REF} is the period of the input reference clock.

In order to reduce the effect of the current mismatch, the turn on time Δt_{on} should be minimized.

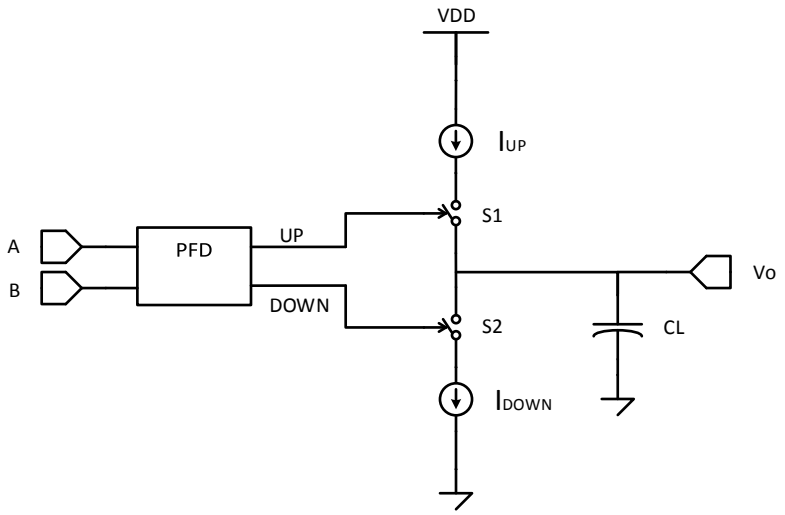


Figure 4.8: Advanced structures.

The second effect of the CP is the mismatch caused by S_1 and S_2 switches. Different characteristics of NMOS and PMOS switches results in timing mismatch during charging/discharging period. Just like to the current mismatch effect, the pulse width Δt_{on} must be reduce to minimize timing mismatch.

Both single ended and a differential CPs exist in literature. Smaller area and less power dissipation is the advantage of a single ended topology, but it is more susceptible to supply and substrate noise compared to a differential topology. We use the single ended topology in CP design to minimize area.

The designed single ended charge pump structure shown in Figure 4.9. Cascode current sources are used at the output to increase the output resistance so that the charging and discharging currents are not significantly disturbed.

In this CP, tail current is 50uA. CP can be modeled by two ideal current sources and two switches as shown in Figure 4.9. Its three states are current sink/source/off as indicated in Table 4.2.

Table 4.2**:** Charge pumps available states

UP	DOWN	Description
1	0	Source current into C_L, raising V_O.
0	1	Sink current fromC_L, reducingV_O.
0	0	Both switches are off and no changes in V_O.

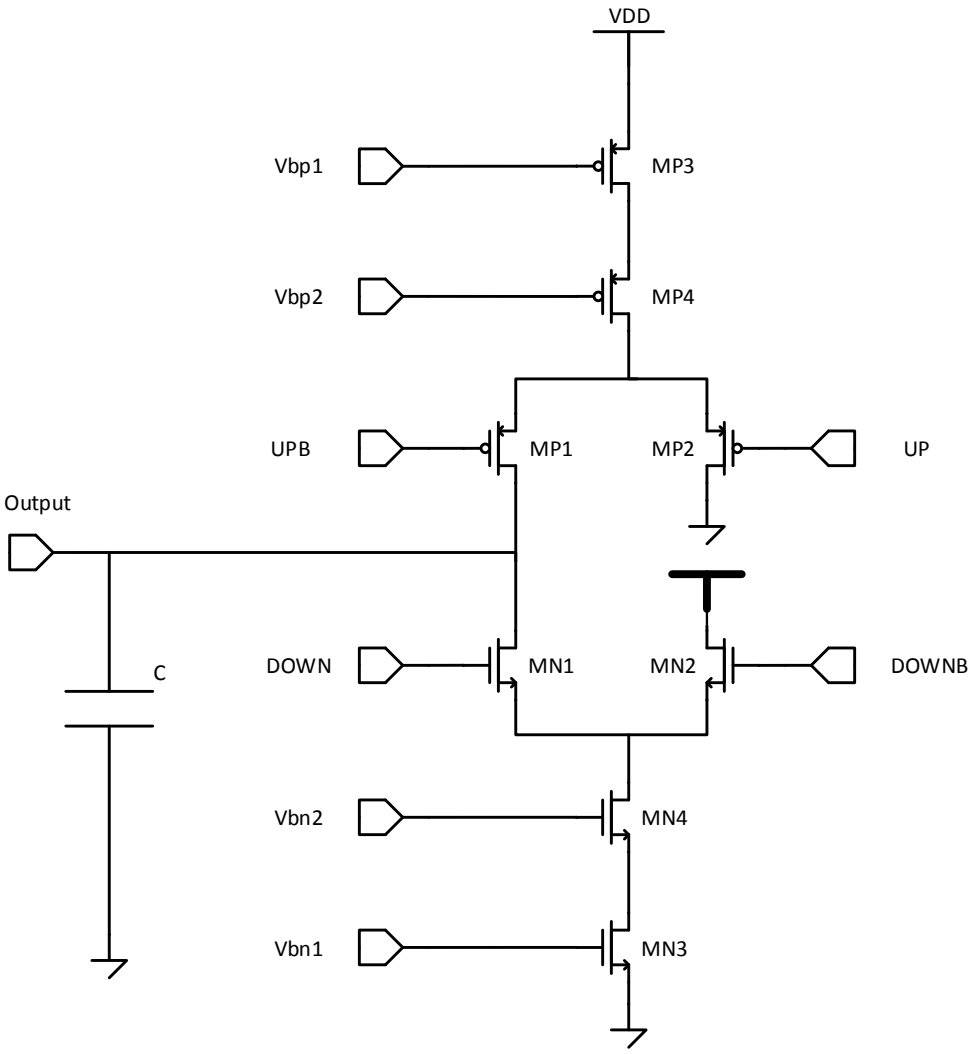


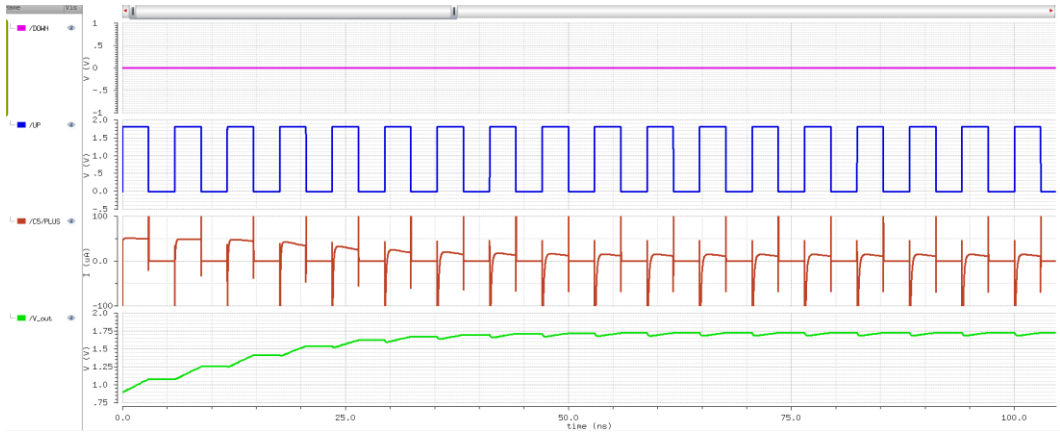
Figure 4.9: Charge pump structure

When UP pulses are applied to the CP from the PFD, it means that VCDL must be sped up. The charge pump must increase its output voltage at the input of loop filter, so, the CP sources current to the C_L in order to increase V_O , as shown in Figure 4.10(a). When DOWN pulses are applied to the CP, sinking current from C_L decreases V_O , as shown in Figure 4.10(b).

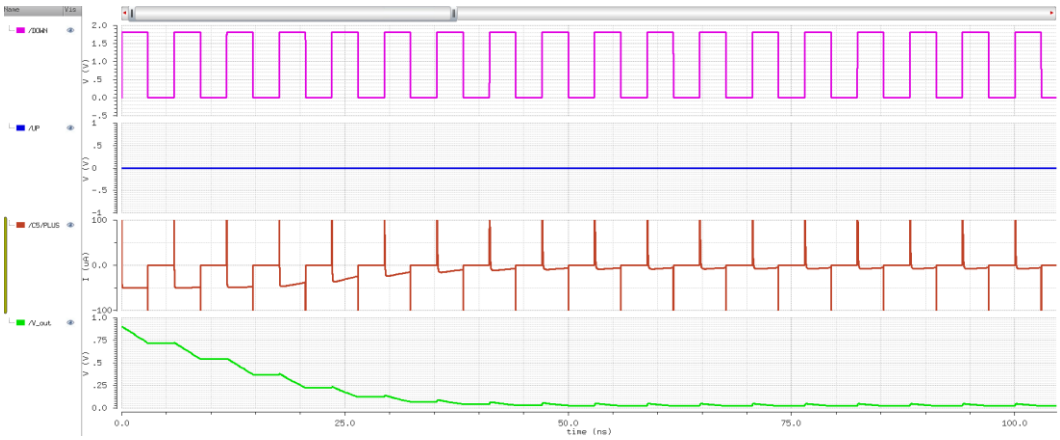
W/L ratios of CP transistors mentioned in Table 4.3.

Table 4.3: Charge pump transistors sizes

	L (um)	W (um)	Finger
MN1,MN2	0.18	1	1
MN3,MN4	1	1	10
MP1,MP2	0.18	2	1
MP3,MP4	1	2	10



(a)



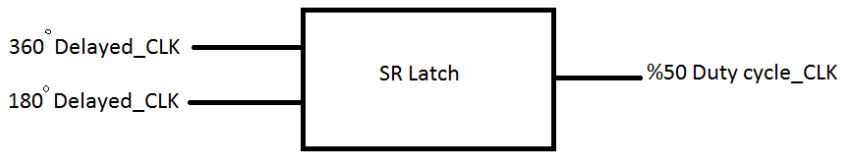
(b)

Figure 4.10: Charge pump waveforms: (a)UP signal (b)DOWN signal.

4.5 Duty Cycle Correction (DCC)

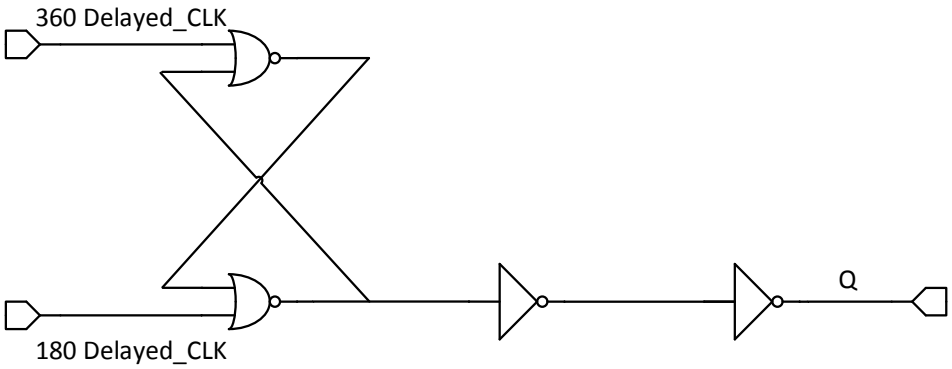
Considering setup and hold time for registers and flip-flops, duty cycle of output clock must be 50% of its period. On the other hand, our PFD is sensitive only to the rising edge that means up and down signals calculated according to the rising edge of input clock. To maintain 50% duty cycle, a DCC circuit of Figure 4.11 is used.

As shown in Figure 4.12, if we set SR latch with a reference clock and reset SR latch with a 180° delayed clock, we get %50 duty cycle without considering falling edge of any signal. This simple DCC technique assumes that the external clock duty cycle is already good.



(a)

Figure 4.11: DCC circuit: (a)model (b)shcematic



(b)

Figure 4.11 (Continued): DCC circuit: (a)model (b)shcematic

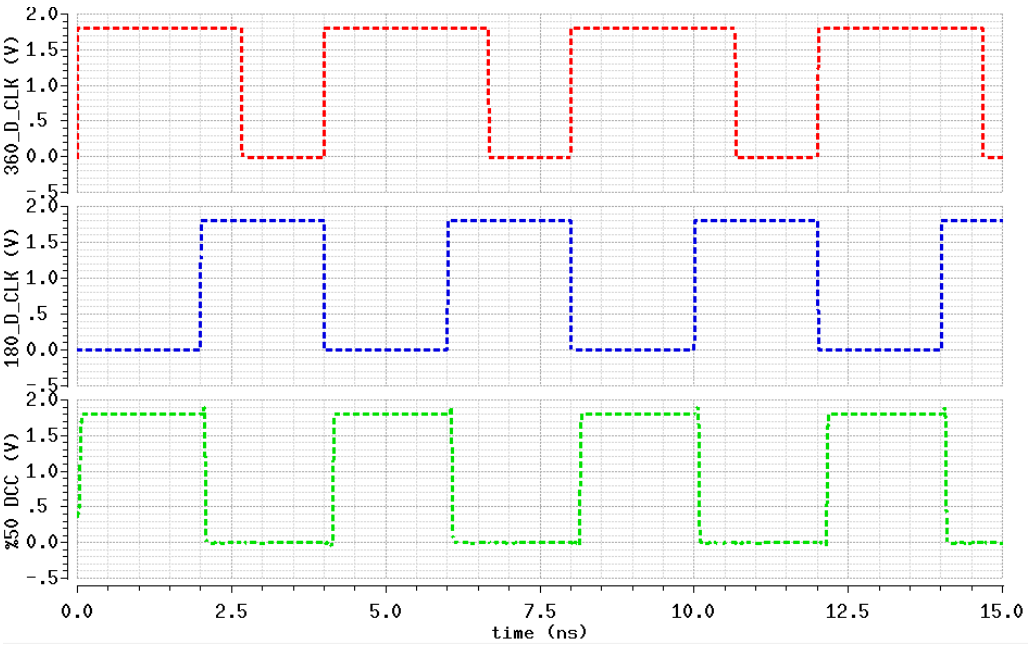


Figure 4.12: DCC circuit waveform

4.6 Lock Status

In order to check the lock status we need to write to a register and read the register whenever we need. So, basic structure of Figure 4.13 is used. This circuit is a first attempt to detect lock status, it must be altered and improved as a part of future work. Figure 4.14 shows that a lock is not detected.

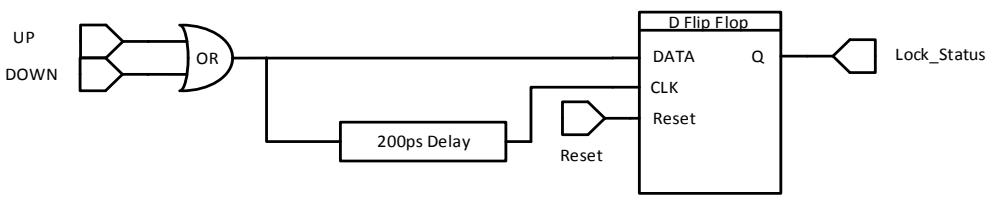


Figure 4.13: Lock status circuit

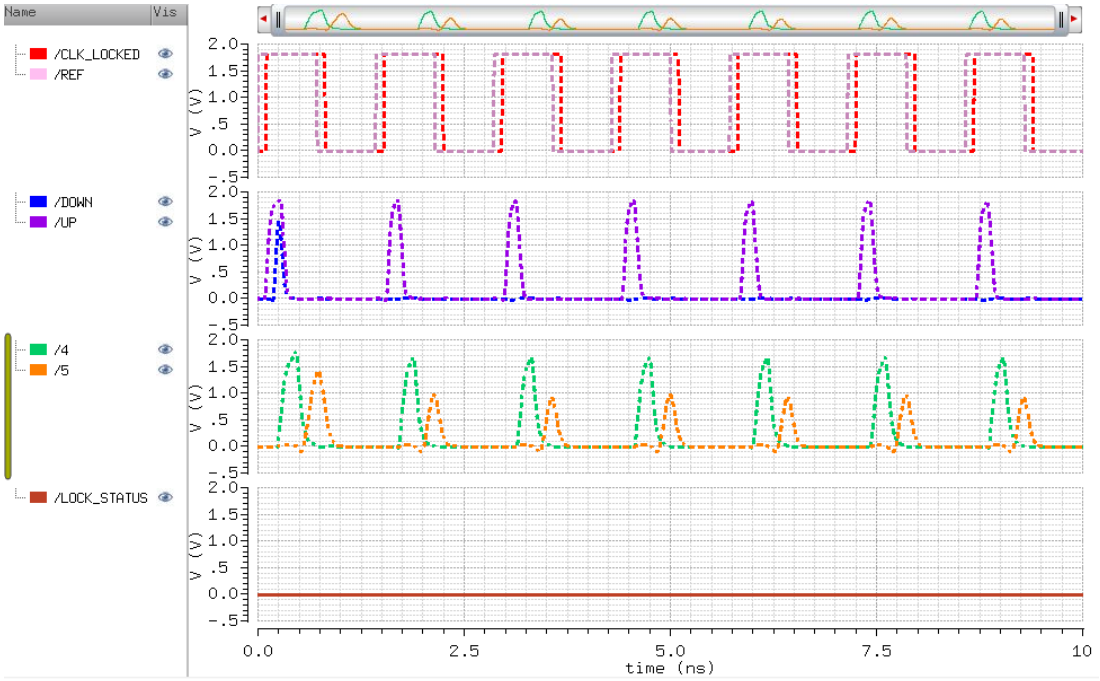


Figure 4.14: Lock status circuit waveform

4.7 D-type Flip Flop

D-type flip-flops schematic, which is used in lock state detector circuit and shift register circuit is shown in Figure 4.15. Rising edge trigged flip-flop input data, clock, reset and output waveforms are shown in Figure 4.16.

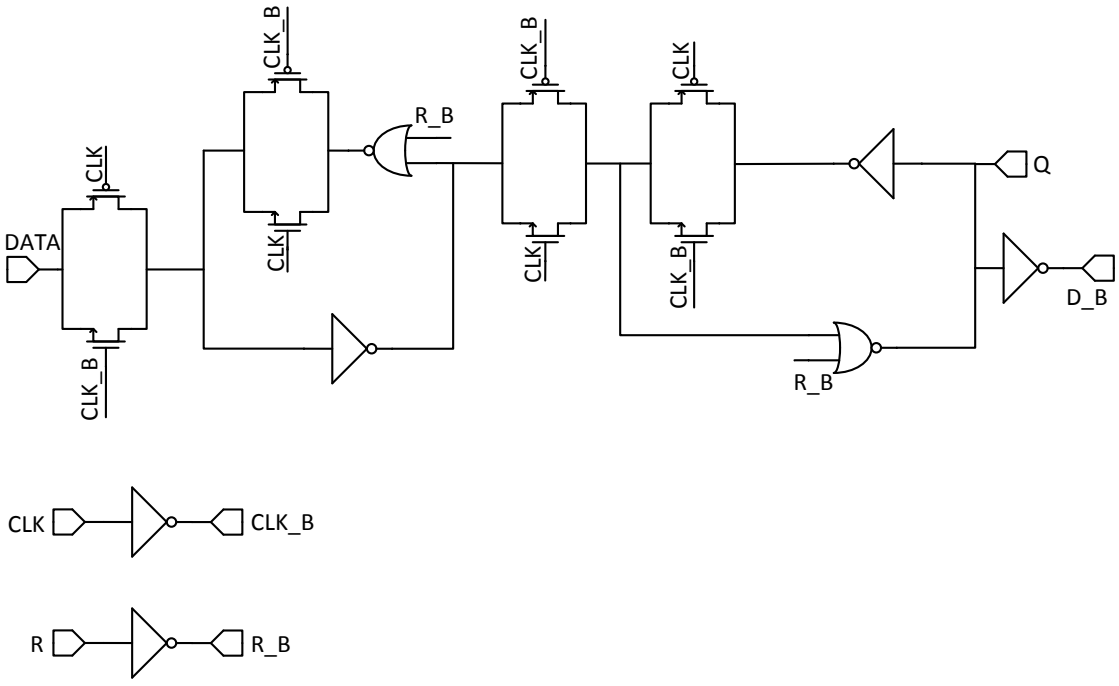


Figure 4.15: D-type flip-flop schematic

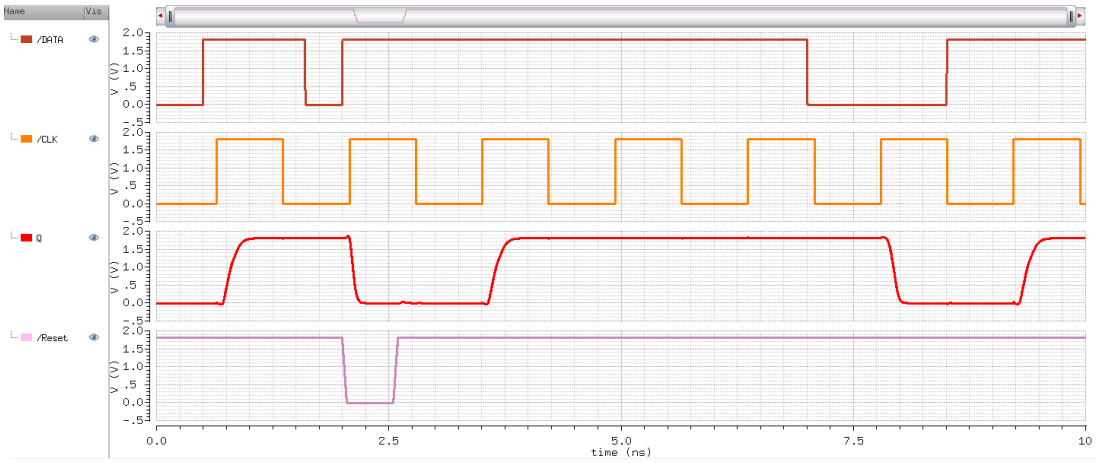


Figure 4.16: D-type flip-flop waveforms

4.8 8bit Feedback Shift Register

Programmability requirement of the DLL structure necessitates an 8-bit shift register as its structure shown on Figure 4.17.

In order to program DLL, 8-bit serial input data is sent into the shift register through its SD_IN port. To save this input data on SD_IN input port shift registers W port must set to high. Input data is MSB comes first.

Shift register D-Flip Flops are triggered by the rising edge of the input clock (SCLK). In order to apply clock signal to Flip Flops, CE (Clock Enable) port must set high.

In addition, to reset all Flip Flops in the shift register the RSTB (Reset) must be set to low.

If port CE and W both set to ‘1’, input data in the SD_IN port are shifting at every rising edge of clock, On the CE ‘1’ and W’0’ state, data inside the shift register shifted through feedback path. This enables data retention when there are 16 or 24 clock cycles with only 8-bit data.

Data on the output of each Flip Flop can used to program DLL structure. Programming is needed to select between three different VCDL structures, and also to select between different tap voltages at each VCDL.

As shown in Figure 4.18, we have ‘0110 0000’ 8-bit serial input data. W and CE ports are ‘1’ for eight clock periods, and after that they become ‘0’ for another eight clock periods. RSTB is always kept ‘1’.

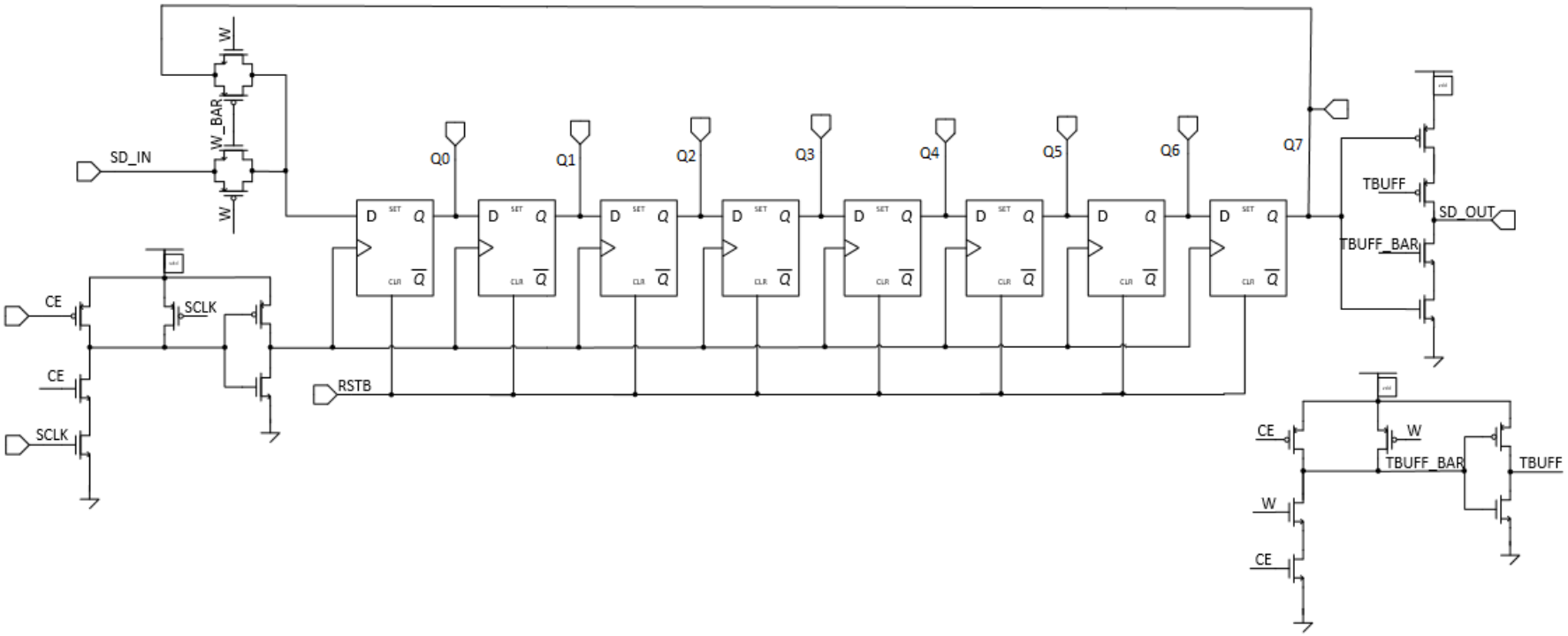


Figure 4.17: 8bit feedback shift register structure

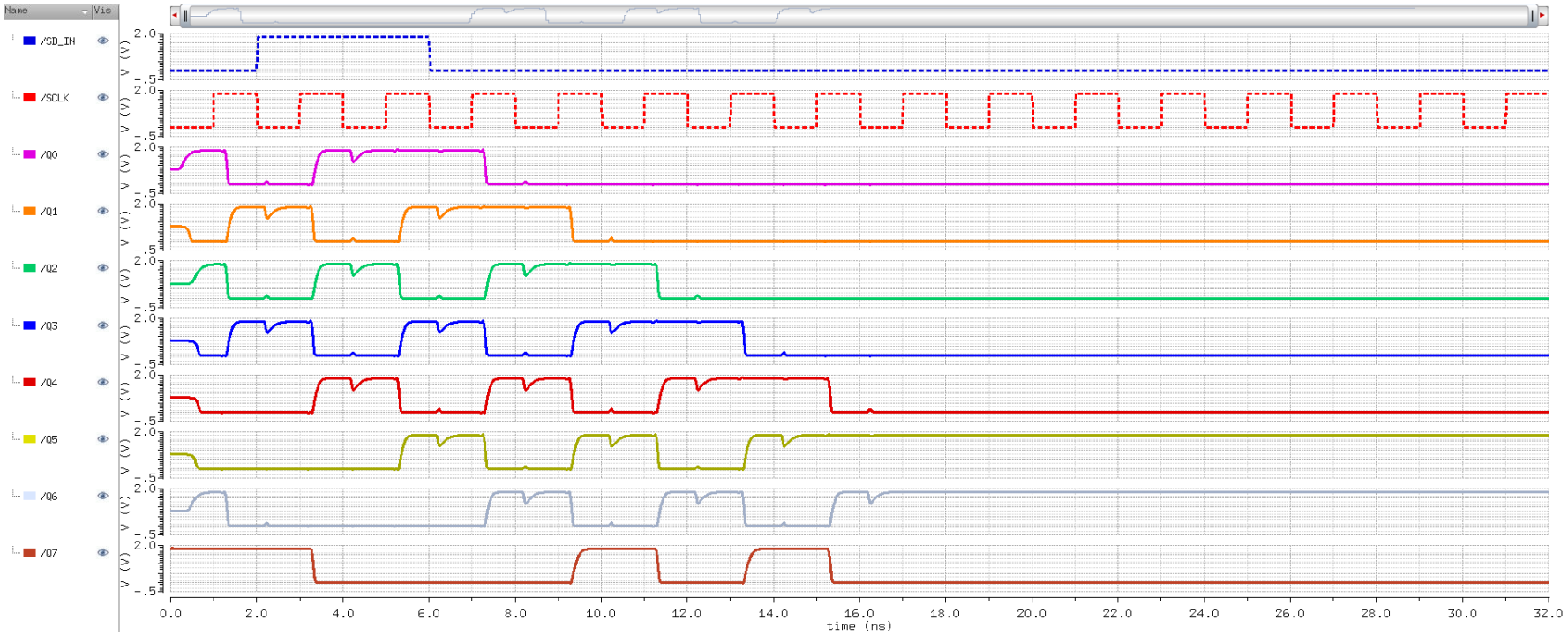


Figure 4.18: 8bit shift register waveforms

5. DLL FULL STRUCTURE

Since we need 120MHz to 670MHz frequency range with multiple clock phases, we can use a variation of the DLL shown in Figure 5.1.

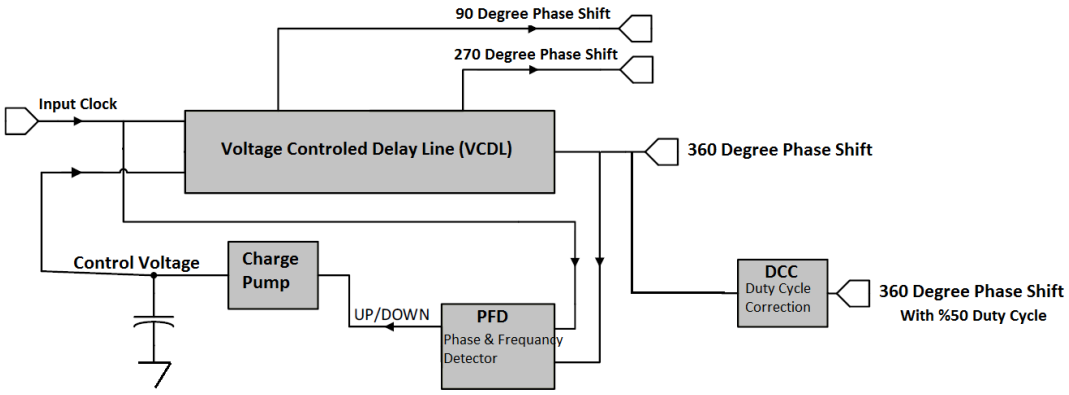


Figure 5.1: Proposed DLL structure

To achieve this wide lock range, we had to use three separate VCDL blocks and divide this range to three sub-ranges:

1st VCDL block range: 120 MHz to 250 MHz

2nd VCDL block range: 220 MHz to 430 MHz

3rd VCDL block range: 400 MHz to 670 MHz

We designed in a frequency overlap to cover all specified frequencies across PVT at post layout as Figure 5.2.

A buffered path that directly connects the input to the output is provided as a bypass feature.

To control all the switching times and to select proper blocks an 8-bit shift register used as shown in Figure 5.3, Q4 to Q7 of shift register are connected to the ϕ_0 to ϕ_3 of DLL structure. Therefore, the first bit of serial input SD_IN data connect to ϕ_0 of DLL, which means if it is '1', we are selecting buffer path between input and output of DLL. Second bit of serial input SD_IN data connect to ϕ_1 of DLL that means if it

is ‘1’, we are selecting the first VCDL block and DLL operates between 120MHz to 250MHz frequency range.

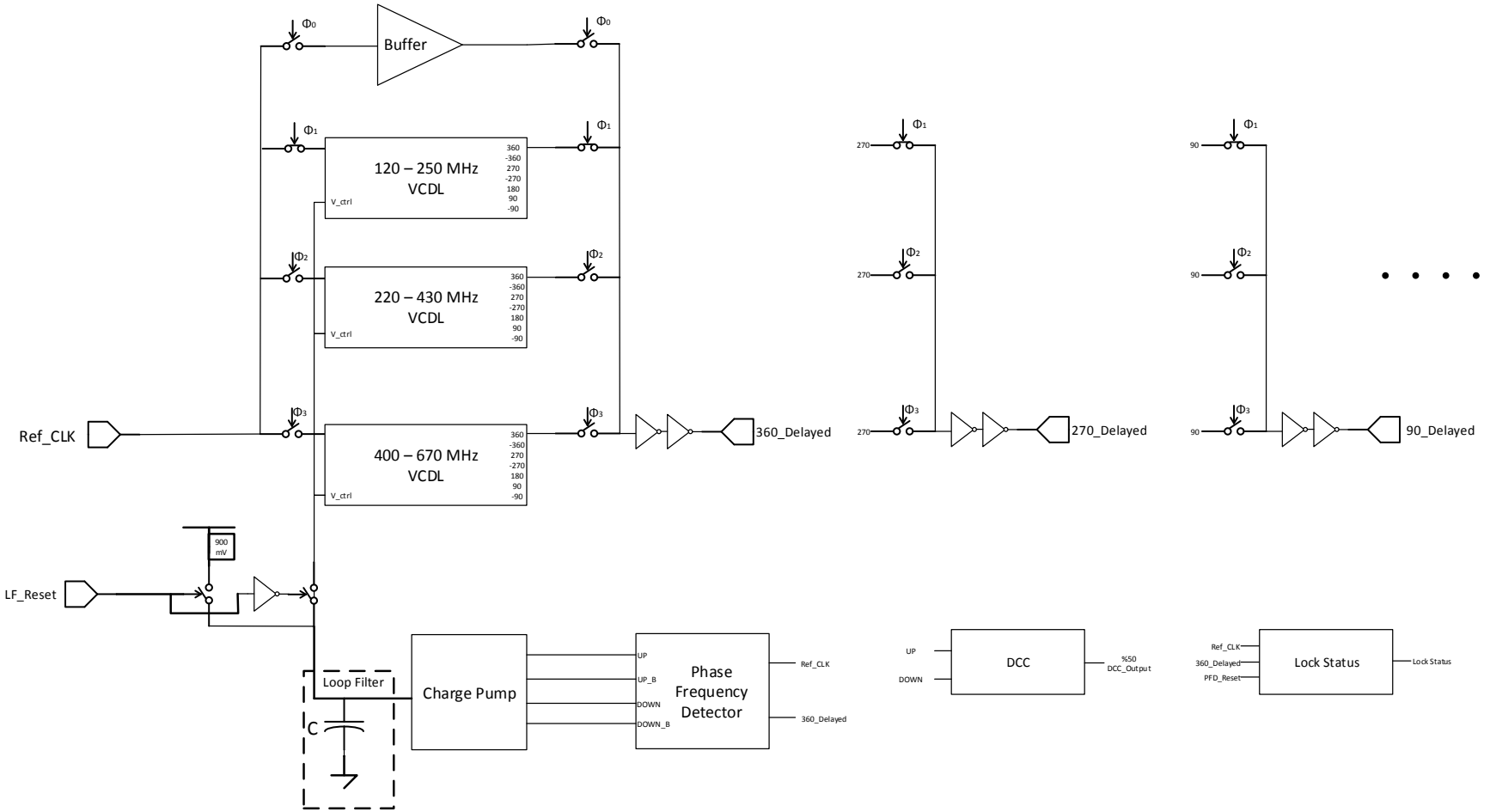


Figure 5.2: Full DLL structure

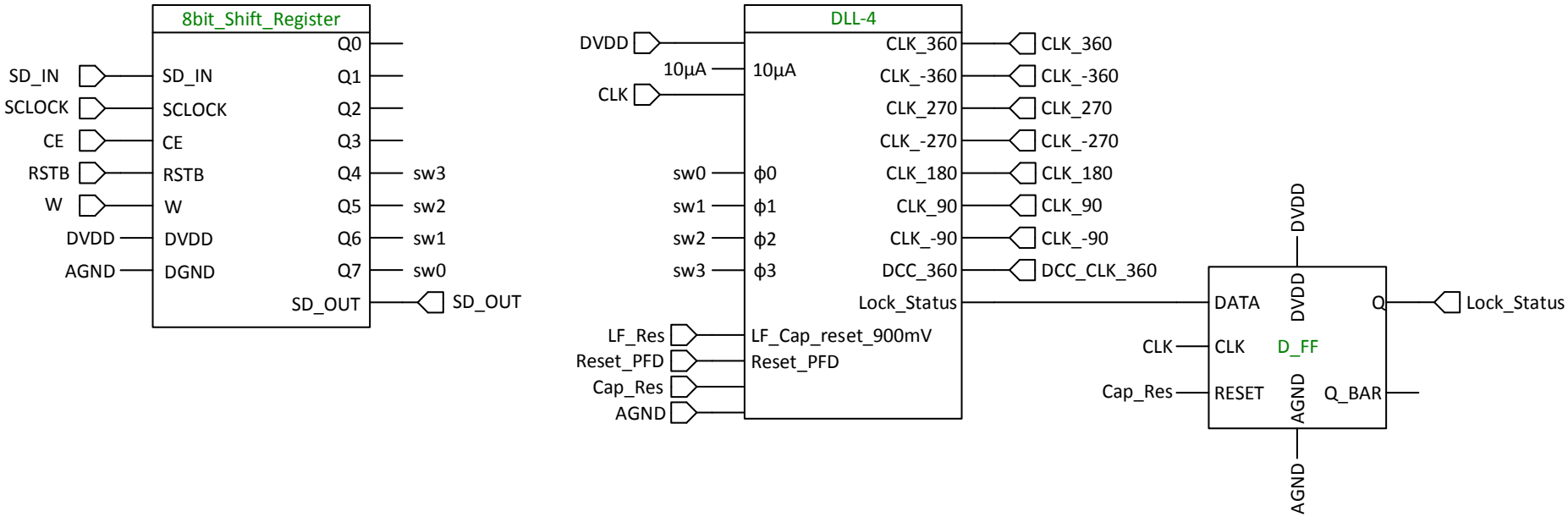


Figure 5.3: DLL control block

6. DLL SIMULATIONS

In order to test DLL we need to set a suitable test bench. Frequency range that should be 120MHz to 670MHz across PVT. The test bench must check the settling time of the DLL when the input switches from one frequency to another. This switching can be inside one VCDL range or between two different VCDLs.

Such a test bench is shown in Figure 6.1. In this test bench, for a 5.4µs transient test period, nine input clock frequencies with different ranges are set as inputs to the DLL. To select the first VCDL (120MHz to 250MHz frequency range) we need have '0100 0000' at the SD_IN port of shift register.

Every 600ns input clock frequency switches to different value and every 1800ns each VCDL changes so SD_IN data must change every 1800ns to choose proper VCDL line.

Ports 'W','CE' and 'RSTB' must follow the instructions given in section 3.7.

An important issue is reset timing of the DL. There are two important reset pins, One of them is loop filter capacitance reset, which must reset to 900mV every time frequency changes. The other one is the PFD reset.

Loop filter capacitance needs at least 25ns reset time to charge or discharge to the 900mV or VDD/2. The PFD reset time of 20ns is sufficient to avoid incorrect UP and DOWN pulses during a loop filter reset.

For the purpose of Power Supply Rejection Ratio (PSRR), a 20mV peak, 50MHz sine wave injected to the DVDD in all the simulations.

6.1 DLL Transient Simulations

As discussed in previous sections, the DLL initializes such that the delay is set to a default value according to the control voltage, which resets to 900mV at the beginning of each cycle. Then DLL searches for a lock point by adding delay to the delay line.

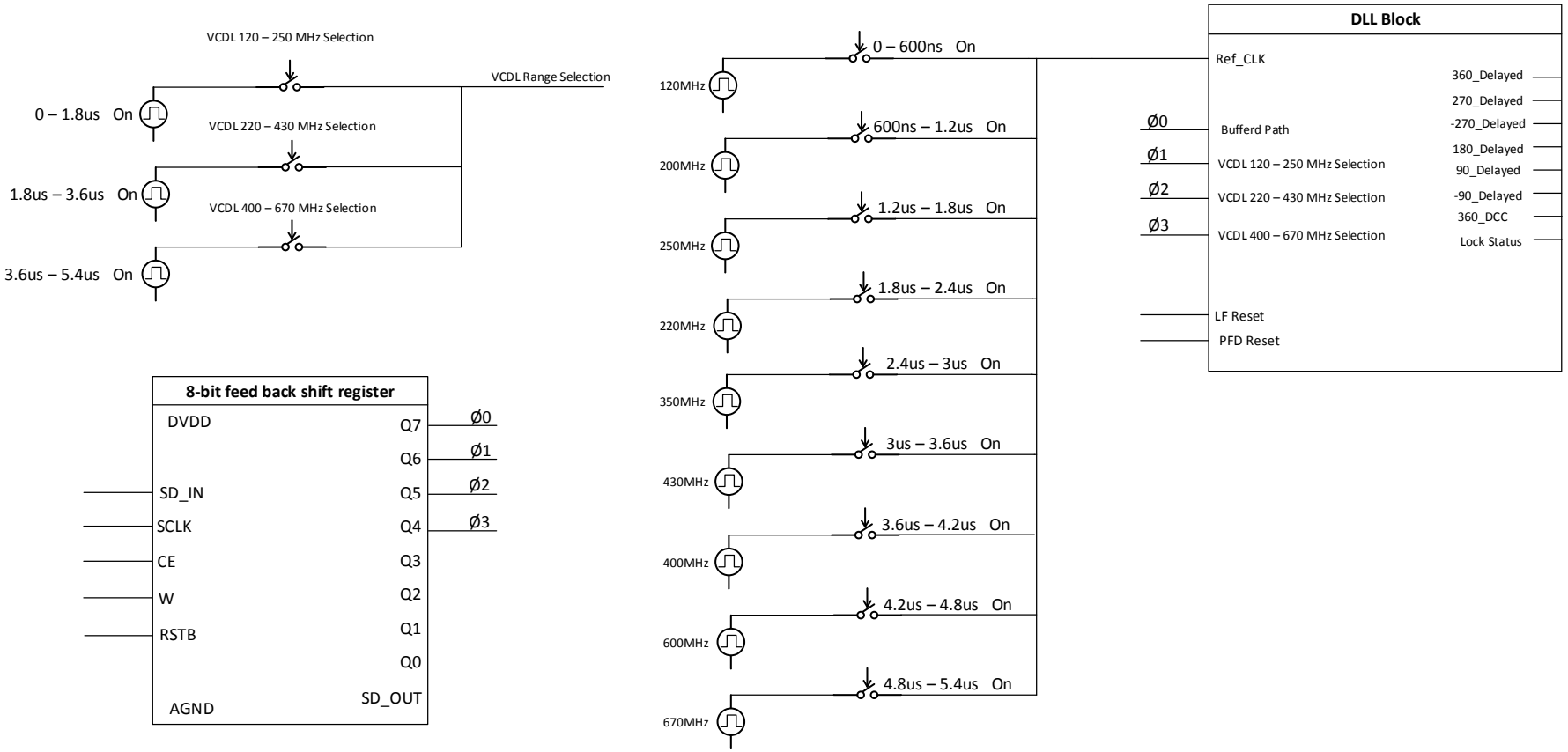


Figure 6.1: DLL test bench

Finally, when it locks to input clock, control voltage stays constant, and charge pumps current becomes zero.

In Figure 6.2 we can see the changes in control voltage and its settling to constant values. As indicated in the DLL test bench, input clock frequency changes every 600ns and control voltage changes are synchronized to that change.

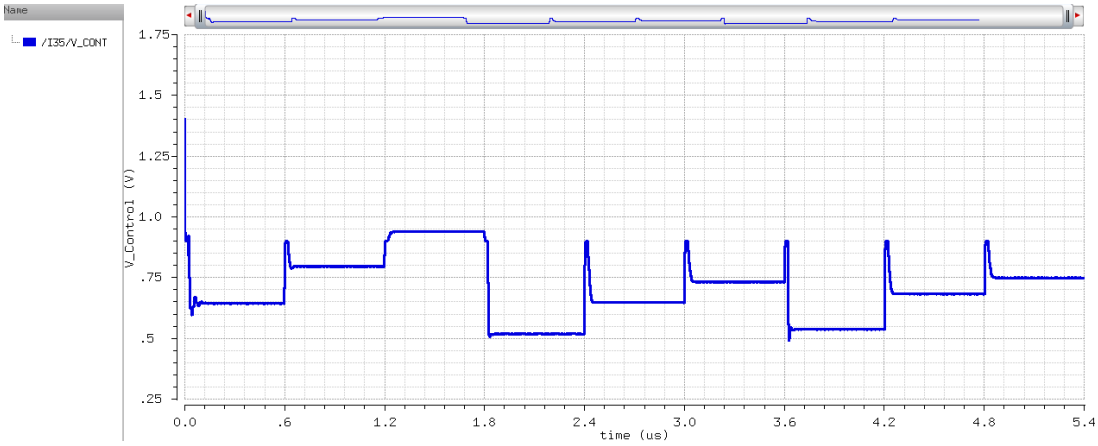


Figure 6.2: DLL Control voltage waveform

Output clock waveform for 140 MHz input clock frequency is shown in Figure 6.3.

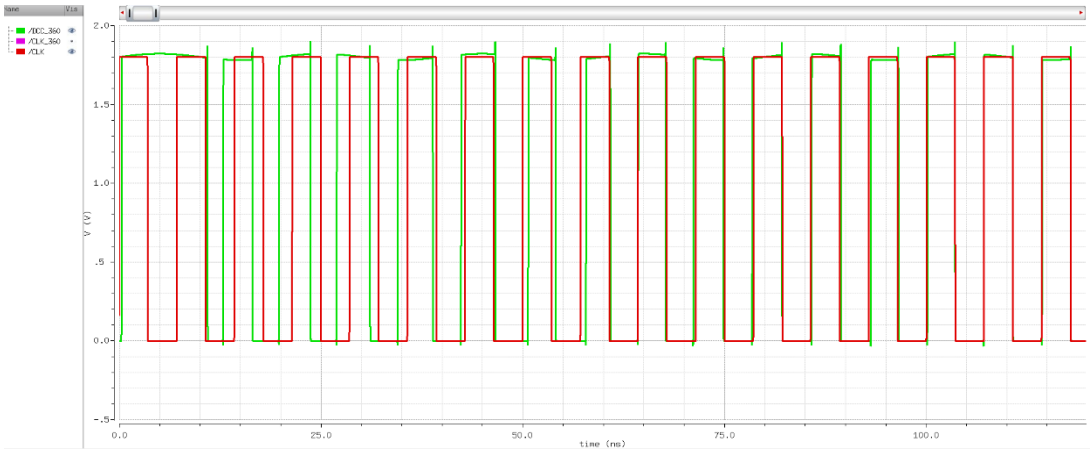


Figure 6.3: 140MHz DLL output waveform

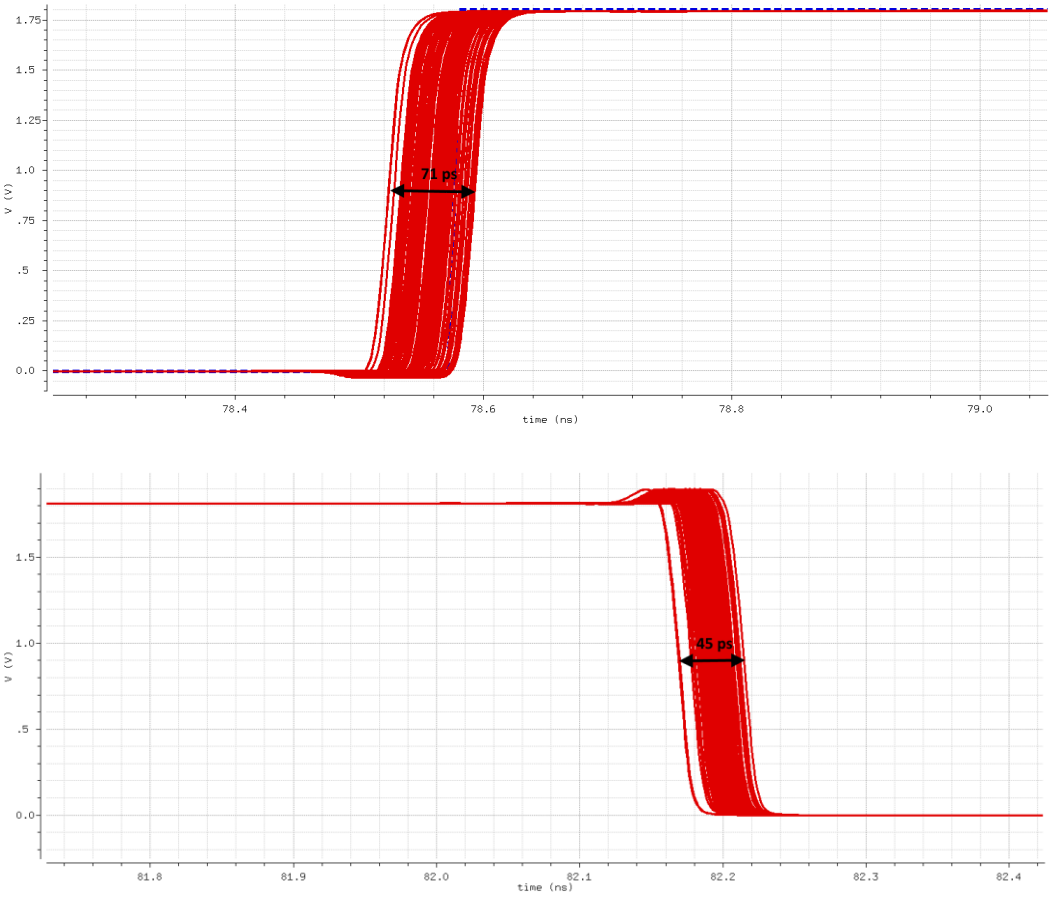
6.2 PSRR test

For all the simulation at the following sections, a 20mv peak-to-peak 50MHz sine wave is added to the supply to test the DLL Power supply rejection ratio.

6.3 Peak to Peak Jitter with Transient Noise

An important specification for this design is peak to peak jitter. Because this is the uncertainty of the sampling signal and it should not be large enough to disturb the sampling. The jitter at rising and falling edges is shown in Figure 6.4. This simulation utilizes the transient noise analysis.

These simulations have shown that the peak to peak jitter for this loop is around 71 to 45 ps. This is acceptable for 1.6 Gbps operation.



(a)

(b)

Figure 6.4: Transient Noise peak to peak jitter on a) rising edge. b)falling edge.

6.4 Cycle to Cycle Jitter

Cycle to cycle (C2C) jitter defined in Joint Electron Device Engineering Council (JEDEC) standard 65B as the variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

Cycle to cycle jitter typically reported as a peak value in picosecond, which defines

the maximum deviation between the rising edges of any two consecutive blocks (SiTime, January 2014). To do so firstly we measure two adjacent clock cycles T1 and T2 then we calculate value of T1-T2 and record the absolute value of this number Figure 6.5. As it seems from Figure 6.5 maximum jitter is 90ps that appears at 120MHz and overall jitter is less than 35ps. In frequencies, more than 250MHz maximum jitter is less than 22ps.

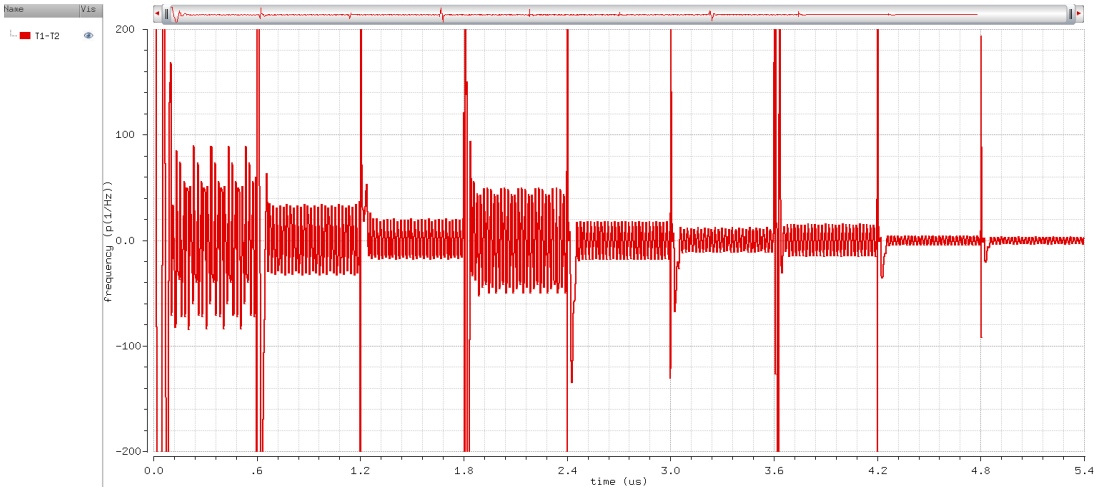


Figure 6.5: DLL jitter waveform

We can see jitter values for all nine input clock frequencies in Table 6.1.

Table 6.1: Jitter across input frequency

Frequency (MHz)	Jitter (ps)
120	90
200	34
250	22
220	50
330	18
430	13
400	15
600	4.5
670	3.5

6.5 Corner Setup for Simulations

27 corners are set to use in simulations:

Process corners: SS, TT, FF

Temperature: -20C, 27C, 105C

Supply: 1.72V, 1.8V, 1.89V

As seems in Figure 6.6, deviation of DLL output waveform across corners drawn for 27 corners mentioned above.

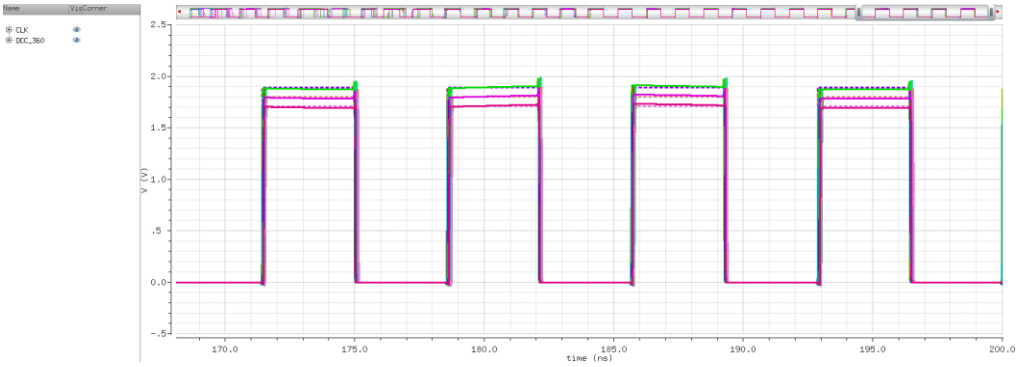


Figure 6.6: 140MHz across corners DLL output waveform

In Figure 6.7 we can see DLL input clock frequency waveform as indicated in DLL test bench input clock frequency switches every 600ns so the DLL output locked clock frequency waveform must settles exactly to the input frequency, as shown in Figure 6.8. Output period follows input period as well and settles in less than 150ns.

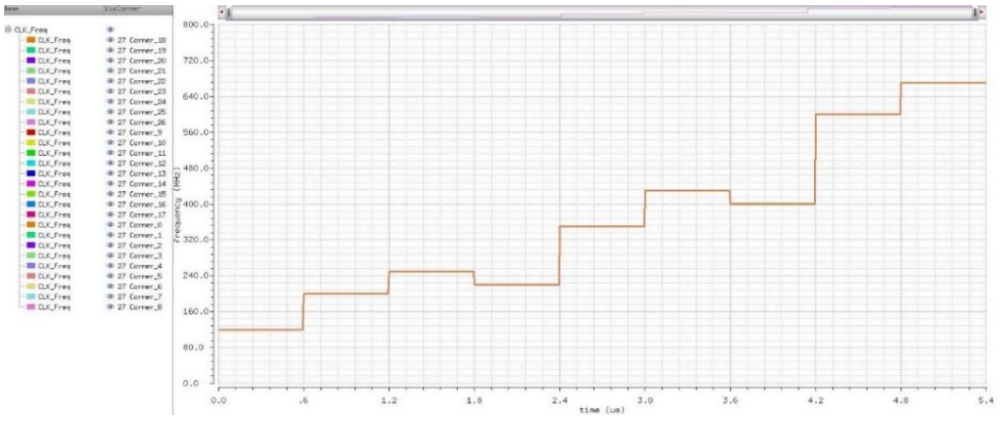


Figure 6.7: DLL input clock frequency waveform

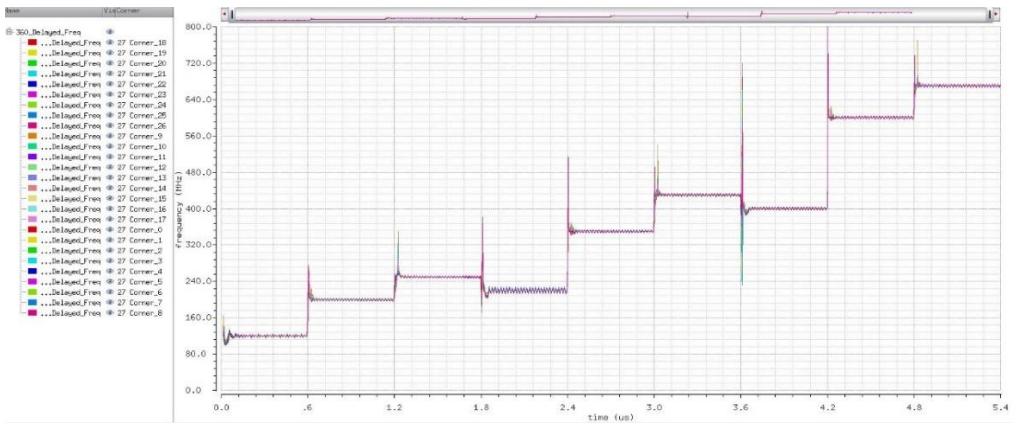


Figure 6.8: DLL output locked clock frequency waveform

As shown in Figure 6.9, maximum jitter is 100ps that appears at 120MHz and overall jitter is less than 35ps. For frequencies more than 250MHz, maximum jitter is less than 25ps.

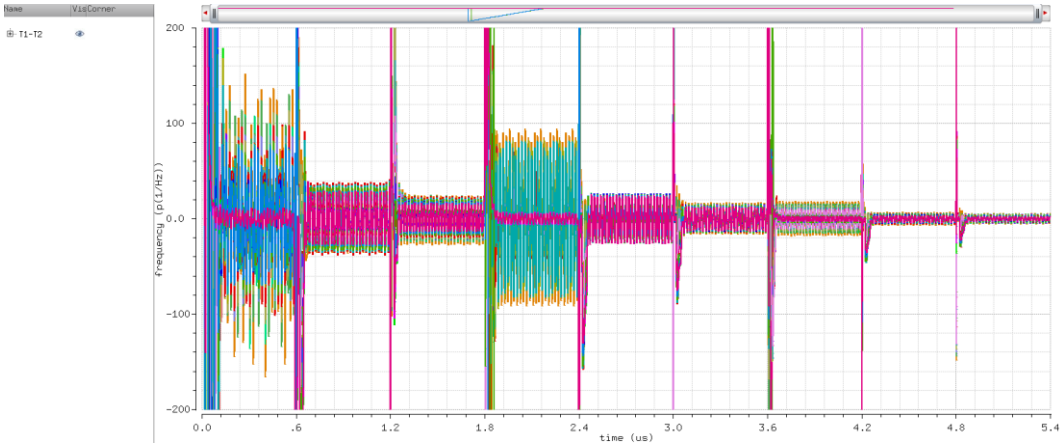


Figure 6.9: DLL jitter waveform

We can see DLL jitter across different input frequencies in Table 6.2.

Table 6.2: Jitter across input frequency

Frequency (MHz)	Jitter (ps)
120	100
200	38
250	20
220	90
330	25
430	15
400	18
600	6
670	5

6.6 Duty Cycle Error

Duty cycle error measured as input clock duty cycle minus DLL output duty cycle, 360° delayed output clock duty cycle errors across PVT are showed in Figure 6.10.

In Figure 6.11, we can see the error reduction of the DCC circuit across different input frequencies.

DLL performance is summarized with and without DCC circuit in Table 6.3.

DLL duty cycle error for 90° delayed clock and 270° delayed clock are compared in Table 6.4 below. Maximum duty cycle error for 90° delayed clock is 4% and maximum error for 270° delayed clock is 16%.

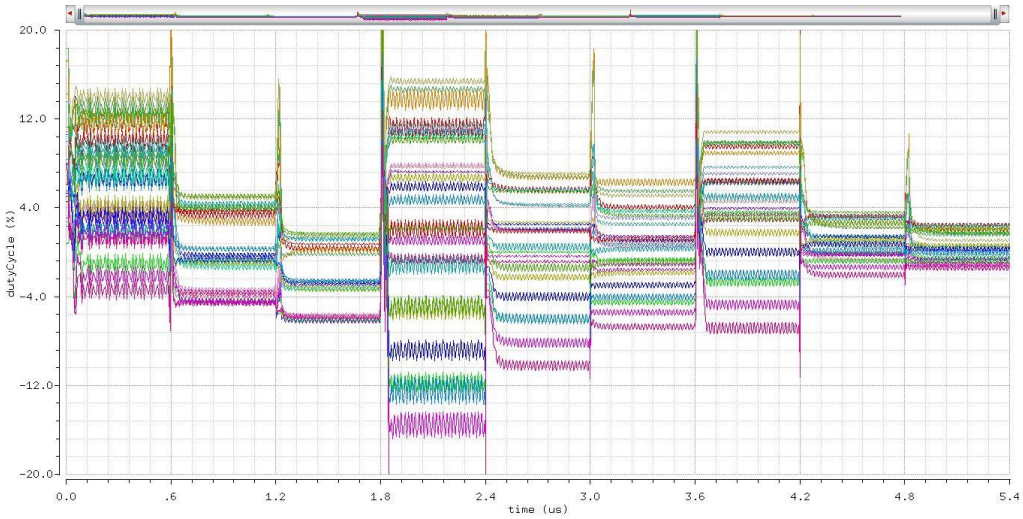


Figure 6.10: Duty cycle error for 360° delayed clock

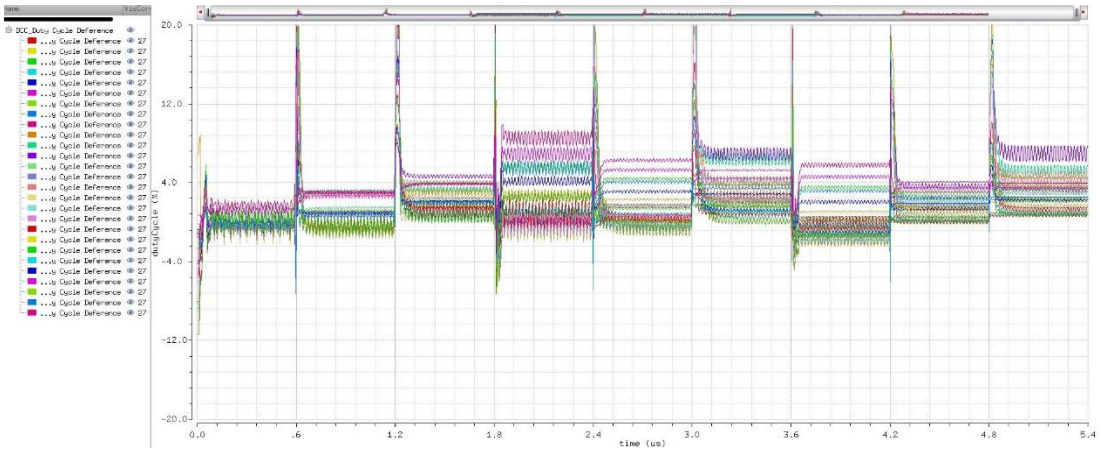


Figure 6.11: Duty cycle error with DCC circuit for 360° delayed clock

Table 6.3: DLL performance with/without DCC circuit.

Frequency (MHz)	% Duty cycle error without DCC	% Duty cycle error with DCC
120	12	1.3
200	3	2.5
250	15	6
220	6	3
330	8	4.5
430	6	4.5
400	5	5
600	2.5	3
670	2	5

Note that we ignored frequency overlap errors that are more than maximum errors.

Table 6.4: DLL duty cycle error for 90° and 270° outputs.

Frequency (MHz)	Duty Cycle Error for 90°	Duty Cycle Error for 270°
120	%3.5	%12

Table 6.4 (continued): DLL duty cycle error for 90° and 270° outputs.

200	%2.5	%12
250	%2	%9
220	%5.5	%24
350	%4	%16
430	%3.5	%15
400	%4.5	%20
600	%2.5	%10
670	%2	%8

6.7 Settling time

In order to insure the settling and stability of the DLL loop, we need to have the stable and constant control voltage at the output of the loop filter. We reset loop filter capacitance voltage to 900mV at the beginning, then the PFD starts to produce UP/DOWN pulses and charge pump starts sourcing/sinking currents to/from the loop filter capacitor. At the settled condition, we need to have constant control voltage.

The time it takes for the control voltage to settle is considered as the settling time of the DLL, as shown in Figure 6.12.

It can be seen that until 20ns, the DLL is in reset time and its loop filter capacitance resets to 900mV. Then the reset path is deactivated and the DLL starts operating and it settles in 110ns to 595mV. This means 90ns settling time.

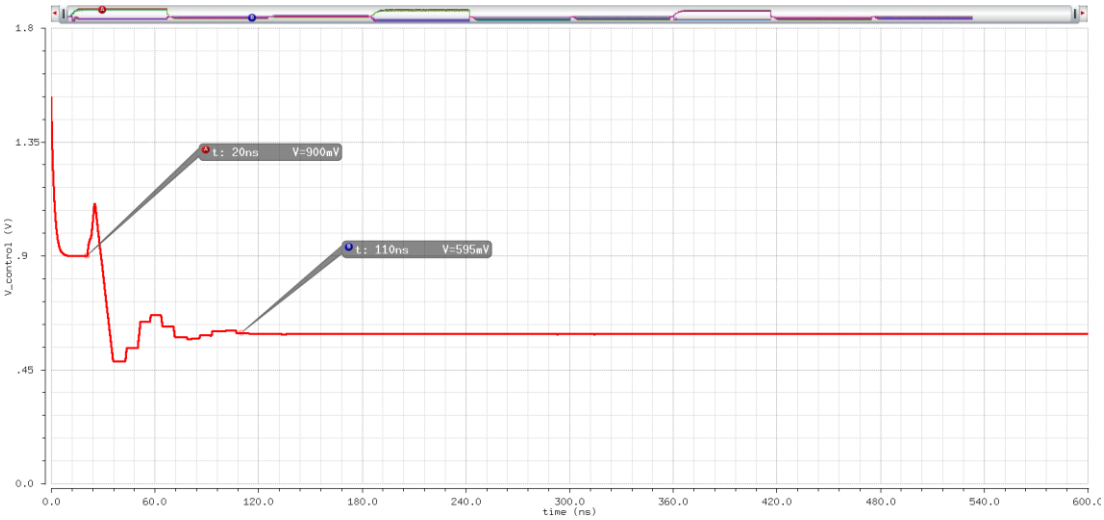


Figure 6.12: Settling time of DLL

7. DLL LAYOUT

In the proposed DLL, current mirrors in charge pump circuit and VCDL must be carefully laid out to avoid systematic and random mismatches.

Random mismatches due to process variations cannot be removed, but they can be reduced. (Hastings A. , 2006)

In a rectangular device with active dimensions W by L, mismatch can be modeled as:

$$\sigma(P) = \frac{k_P}{\sqrt{WL}} \qquad \textbf{(6.1)}$$

So to reduce mismatch by a factor of two, increase the gate area by a factor of four. However, this has so many limitations due to large die area and can be useful only to a certain extent.

Best way to manage systematic mismatch is to use common centroid interdigitating technique in layout as depicted in Figure 7.1. (Hastings A. , 2006)

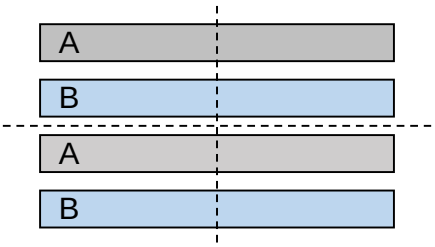


Figure 7.1: Interdigitating layout

Moreover, transistors that need to match in each delay stage divided into multiple fingers with all fingers of the same width and length.

To minimize crosstalk, the most straightforward way is to separate signal lines as much as possible. In particular, critical signal lines, such as clock, must be isolated from other signal lines as well as power lines. (Hastings A. , 2000)

Here every clock path is shielded to AGND using the same metal.

In Figure 7.2, a delay cell layout is shown as a basic part of the VCDL. There is two rails of transistors; top rail belongs to PMOS transistors and bottom rail belongs to NMOS transistors.

PMOS transistor in the top left corner has three fingers just like the NMOS transistor in the left bottom corner of the Figure 6.3. Minimum spacing for METALs and transistors are used to reduce to minimize area.

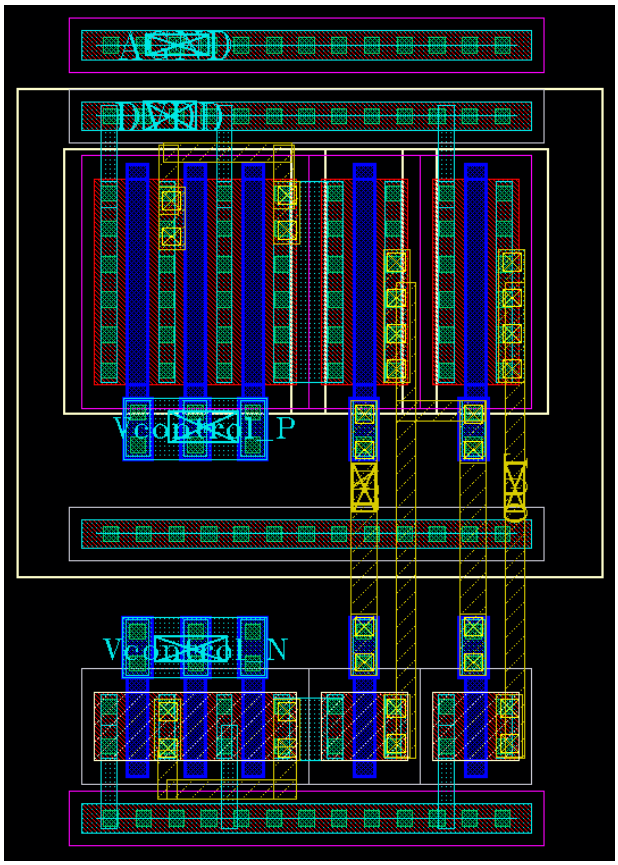


Figure 7.2: A delay cell layout.

In Figure 7.3, VCDL layout is shown, and the charge pump layout can be seen in Figure 7.4. Phase and frequency detection layout depicted in Figure 7.5 and lock status detector layout can be seen in Figure 7.6.

Full DLL layout can be seen in Figure 7.7, which has dimensions of 145µm× 76.3µm.

As it can be seen from Figure 7.8, all sub blocks gather to shape DLL full layout. Layout blocks are numbered as follows:

VCDL for 400-670 MHz range

VCDL for 220-430 MHz range

VCDL for 120-250 MHz range

Charge Pump and Loop Filter

Phase and Frequency Detector block

Locked status detection block

Output control switch bank

Duty cycle correction block

Input CLK switching bank

Middle stage control switch bank

For post layout simulations, we have an RC parasitic extraction of this layout as it shown in Figure 7.9.

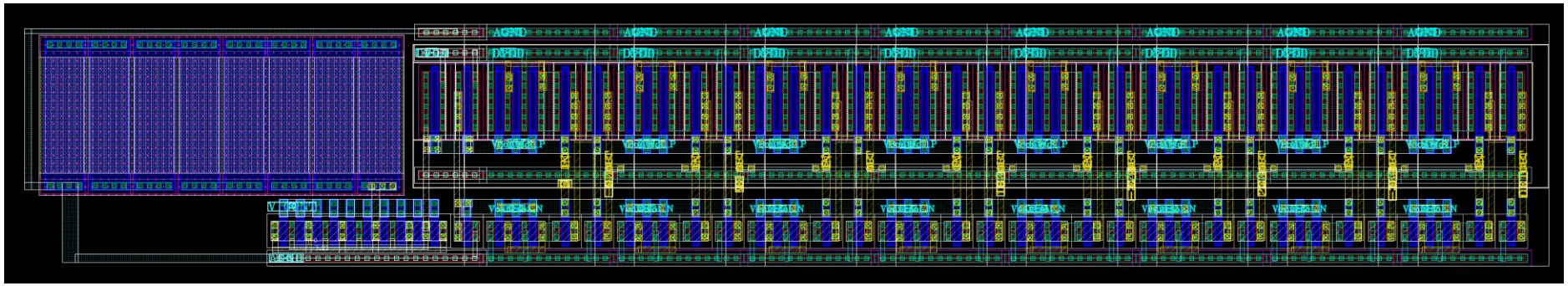


Figure 7.3: 120MHz to 220MHz VCDL layout.

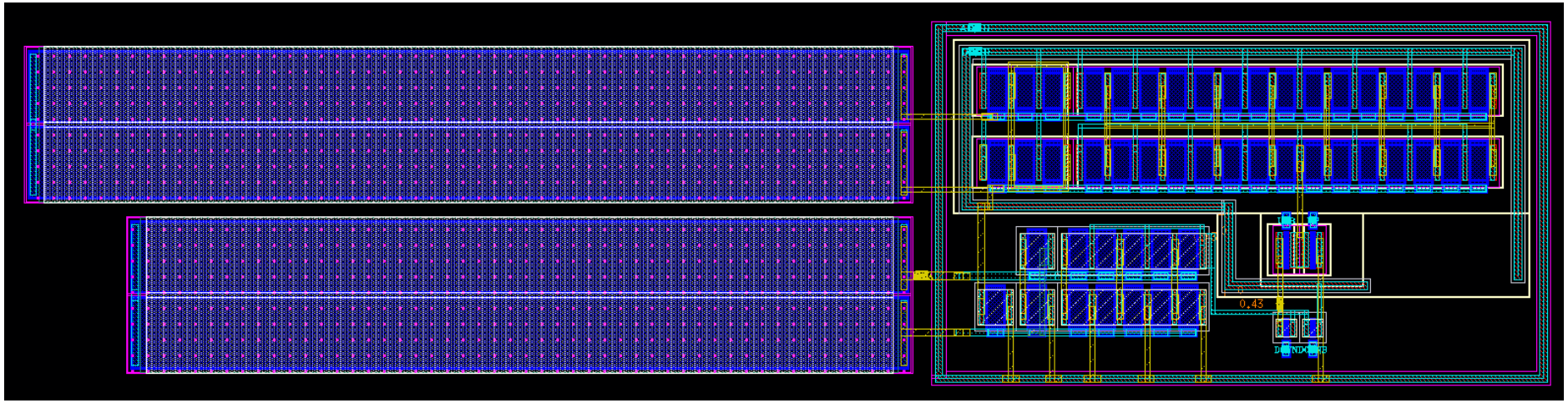


Figure 7.4: Charge pump layout.

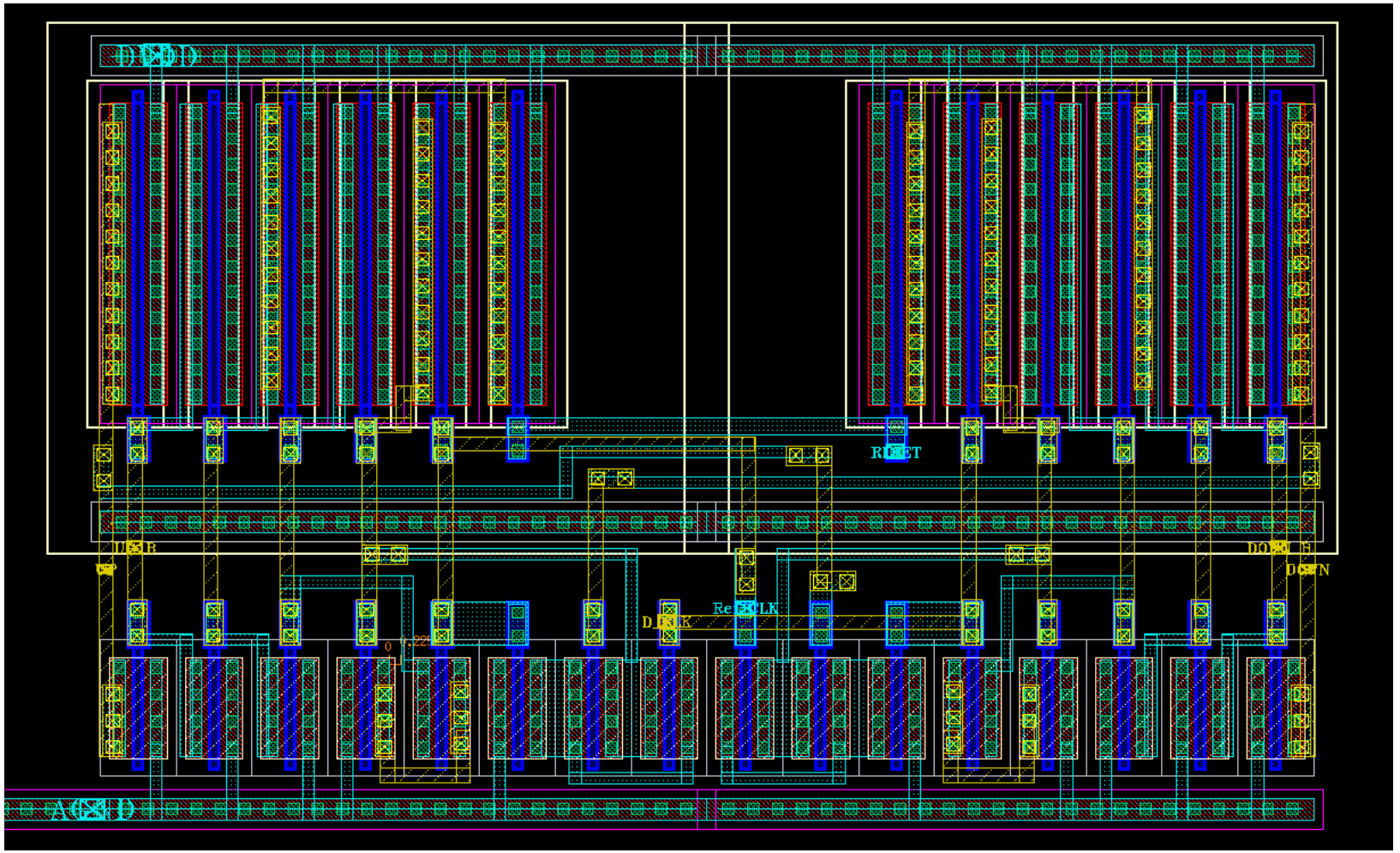


Figure 7.5: PFD layout.

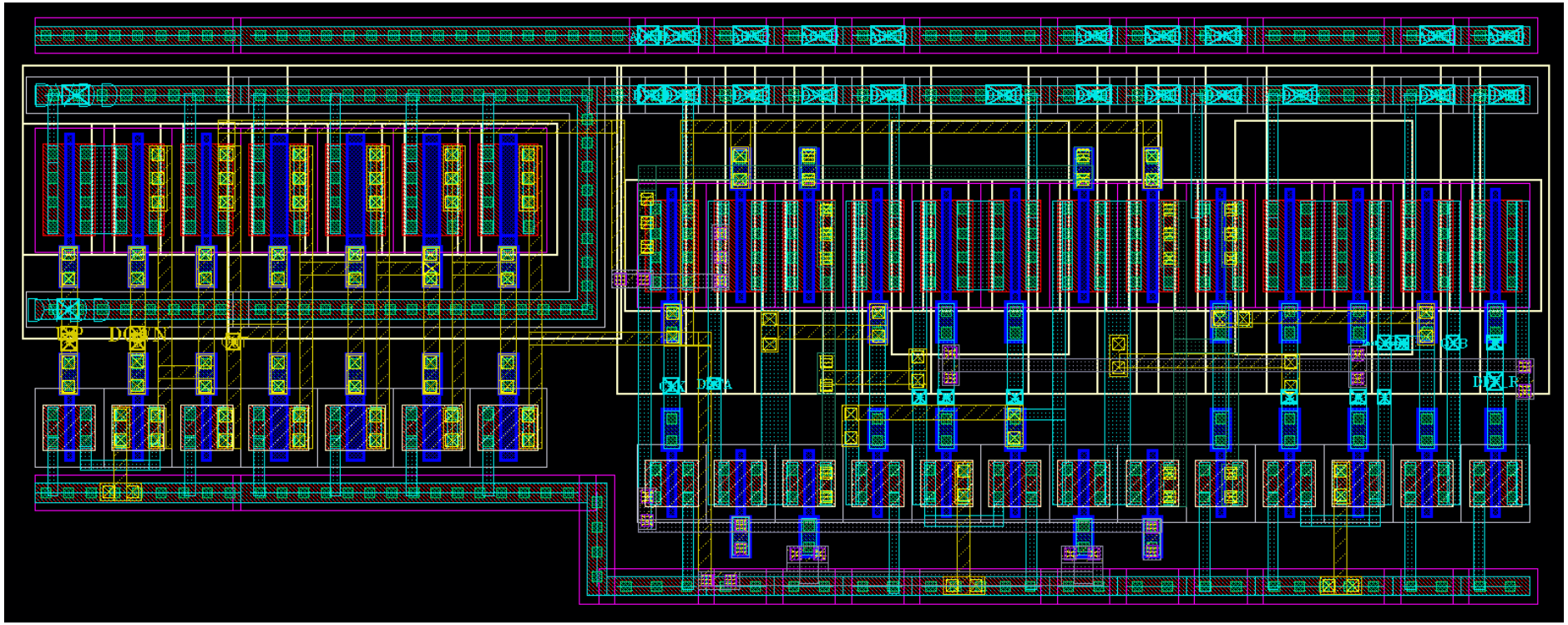


Figure 7.6: Lock status detection layout.

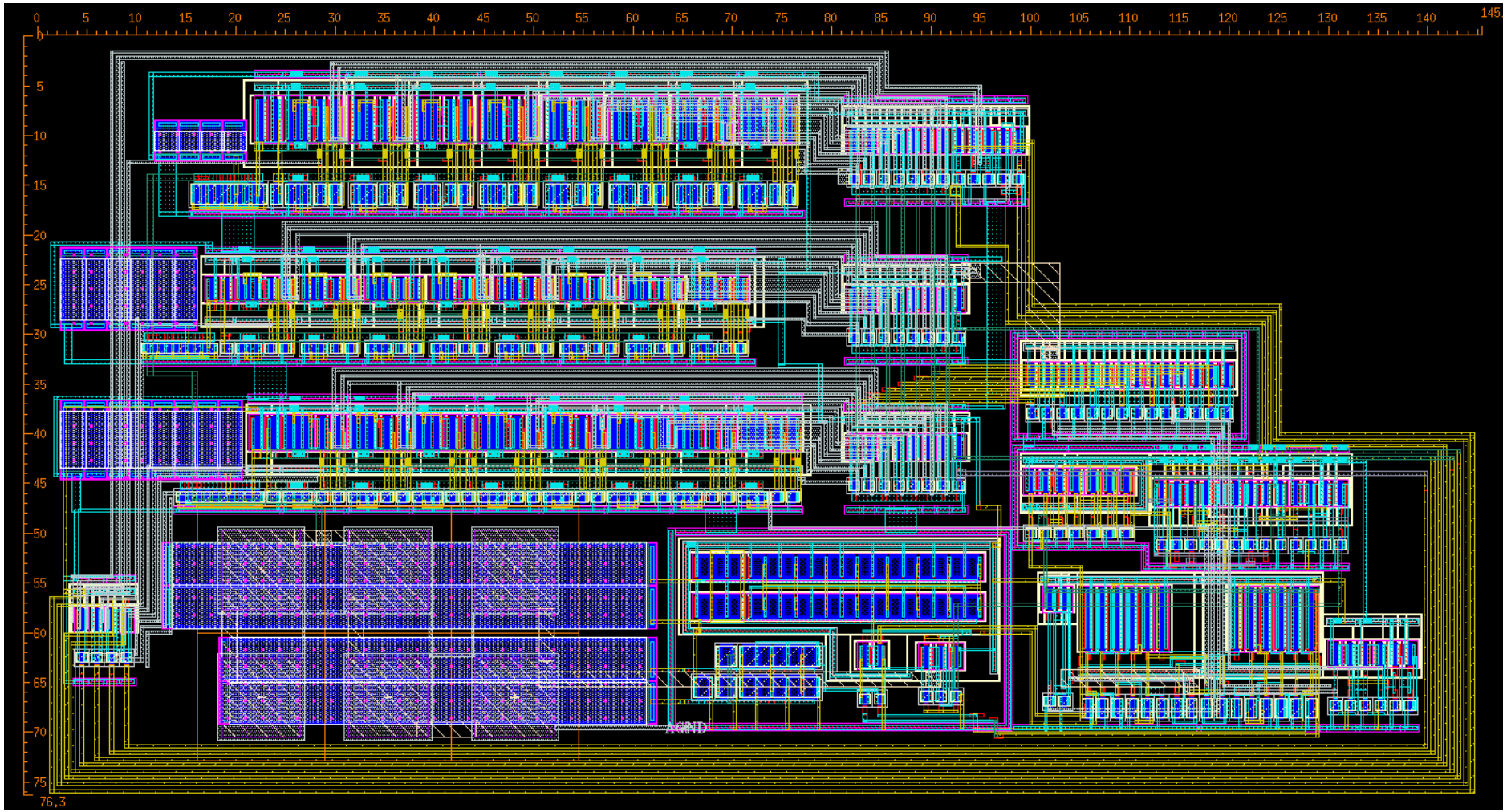


Figure 7.7: DLL full layout.

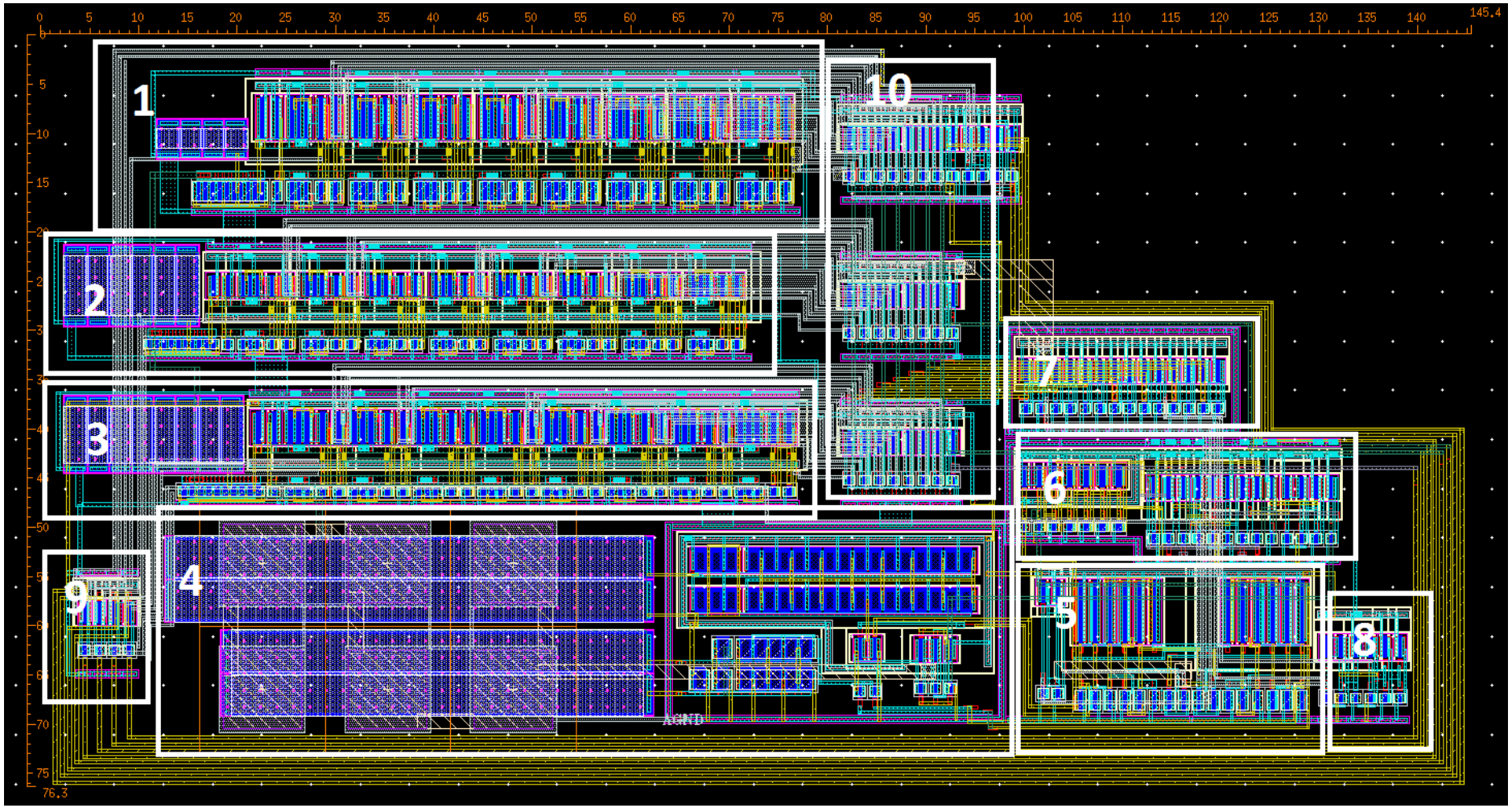


Figure 7.8: DLL full layout sub block definitions.

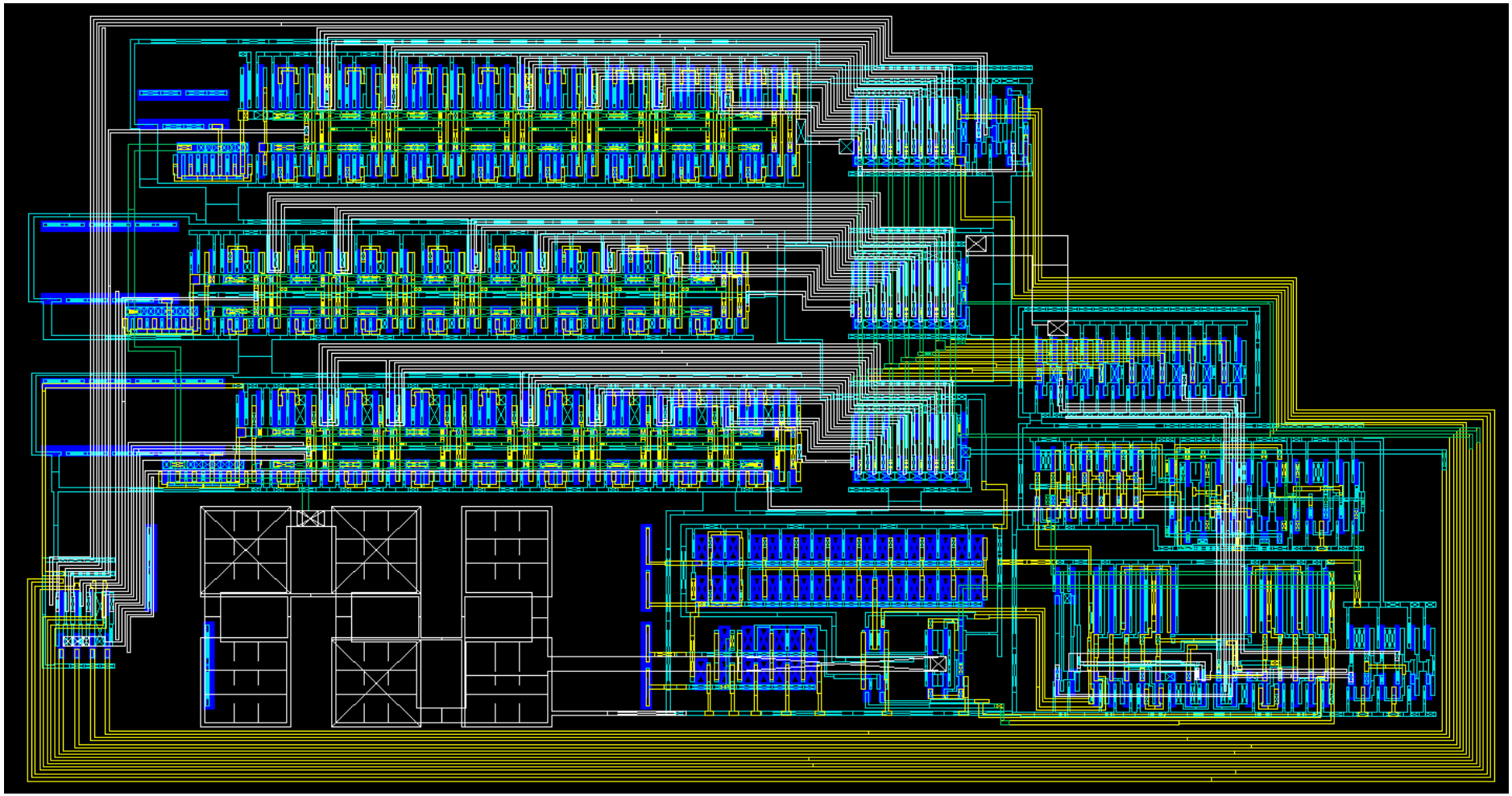


Figure 7.9: RC extraction of DLL full layout

8. POST LAYOUT SIMULATIONS

All the simulations that were performed before with schematic views are re-run including the layout of all blocks as an av_extracted view. We see some changes because of parasitics.

8.1 Post-Layout cycle to cycle Jitter

As seen in Figure 8.1, Maximum jitter is 200ps, which appears at 120MHz and overall jitter is less than 40ps. At frequencies more than 250MHz, maximum jitter is less than 25ps.

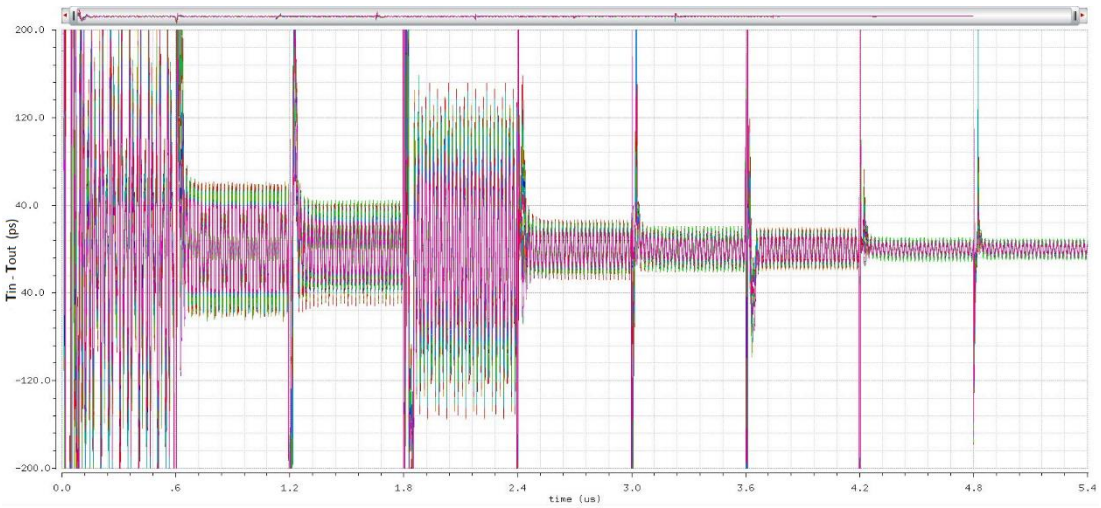


Figure 8.1: Post-layout DLL jitter waveform

We can see post layout DLL jitter simulation results for all nine input clock frequencies in Table 8.1.

Table 8.1: Post-layout jitter across input frequency

Frequency (MHz)	Jitter (ps)
120	200
200	60
250	40
220	140
330	25
430	17
400	15

Table 8.1 (continued): Post-layout jitter across input frequency

600	8
670	8

8.2 Post-Layout Peak-to-Peak Jitter

The jitter simulation includes transient noise analyses and is performed as it is described in section 6.3.

These simulations have shown that the peak to peak jitter for this loop is around 65 to 40 ps.

8.3 Post-Layout Duty cycle error

We can see DLL performance with and without DCC circuit in Table 8.2. In addition, we can find DLL duty cycle errors for 90° and 270° output clock phases in Table 8.3.

Table 8.2: DLL performance with/without DCC circuit in post-layout sim.

Frequency (MHz)	% Duty cycle error without DCC	% Duty cycle error with DCC
120	15	1.5
200	4	3
250	18	7
220	6	4
330	10	5.5
430	7	5.5
400	6	6
600	3	4
670	2	6

Table 8.3: Post-layout DLL duty cycle error for 90° and 270° outputs in post layout sim.

Frequency (MHz)	Duty Cycle Error for 90°	Duty Cycle Error for 270°
120	%3.5	%7.5
200	%1.5	%4
250	%1	%3.5
220	%4	%13
350	%3.5	%7.5
430	%3.5	%6
400	%3.5	%10.5
600	%3	%4
670	%3	%3

8.4 Post-Layout Monte Carlo Simulation

A 20 runs Monte-Carlo simulation across single corner with nine different input clock frequencies as section 6 is performed.

In Figure 8.2 Monte Carlo simulation results for cycle-to-cycle jitter is provided, it can be seen that the worst case result is 120ps and for frequencies more than 300MHz its less than 25ps at worst case as mentioned in Table 8.4.

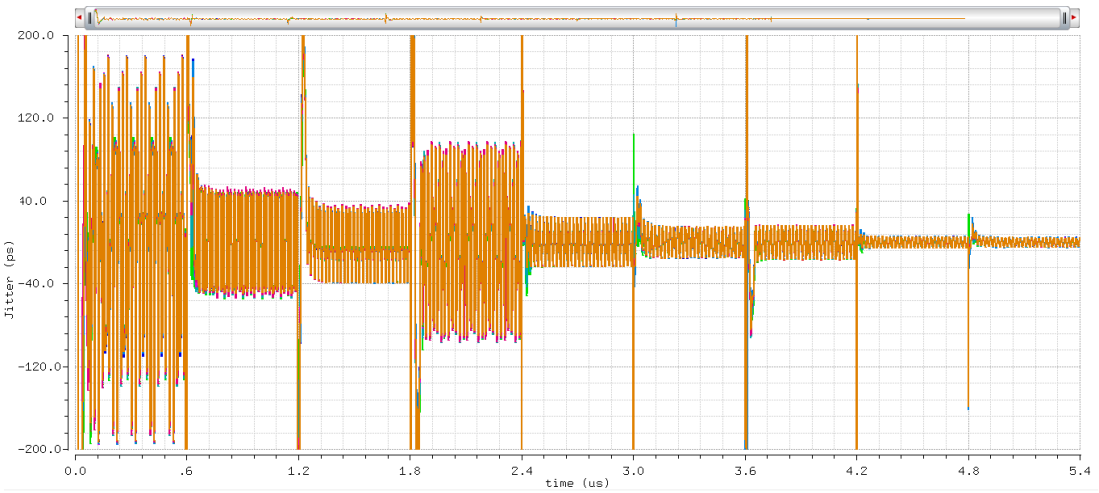


Figure 8.2: Post-layout DLL jitter waveform in Monte Carlo sim.

Table 8.4: Post-layout jitter across input frequency in Monte carlo sim.

Frequency (MHz)	Jitter (ps)
120	120
200	45
250	35
220	80
330	25
430	21
400	19
600	4
670	3

In Figure 8.3 and Figure 8.4 we can see the duty cycle error for post layout simulation of DLL using Monte Carlo analysis. Figure 8.3 shows the DLL output without any duty cycle correction and Figure 8.4 shows the DCC output.

We can see the performance of the DCC circuit, the worst case duty cycle error is %2.3 as mentioned in Table 8.5.

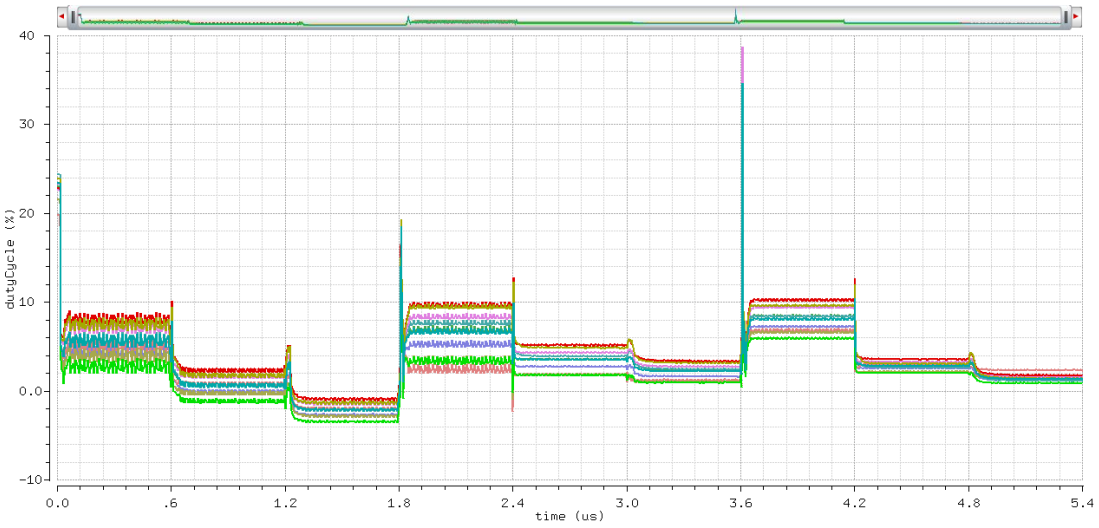


Figure 8.3: Post-layout DCC output duty cycle error in Monte carlo sim.

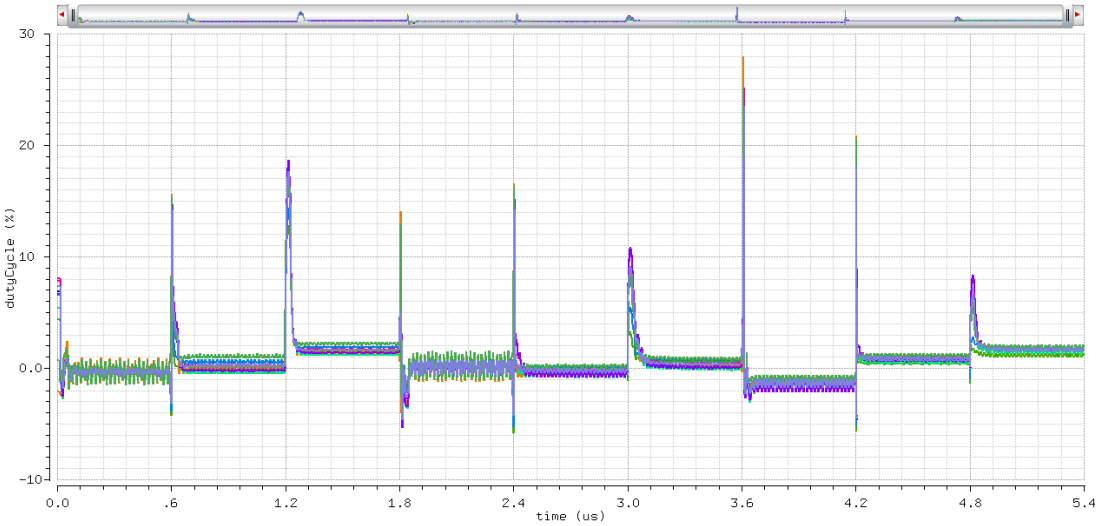


Figure 8.4: Post-layout DCC output duty cycle error in Monte carlo sim.

Table 8.5: DLL post-layout performance with/without DCC circuit in Monte-Carlo simulation

Frequency (MHz)	% Duty cycle error Without DCC	% Duty cycle error with DCC
120	8.5	1.5
200	2.5	1.2
250	3.5	2.3
220	10	1.4
330	5	0.7
430	3.5	1
400	10	2
600	3.5	1.3
670	2.5	2

8.5 Post-Layout Settling time

As it seems from Figure 8.5, worst case settling time is 100ns.

Figure 8.5: Post-layout settling time across 27 corners.

8.6 Post-Layout Power Supply Sensitivity

We increase supply voltage from zero volt slowly up to 1.8V. The supply ramp is 1us long. Then the output and settling of the DLL examined. It can be seen from Figure 8.6 that after 1us that AVDD voltage reaches to the 1.8V the Loop filter output voltage settles to a constant value and DLLs output clock lock to the input reference clock.

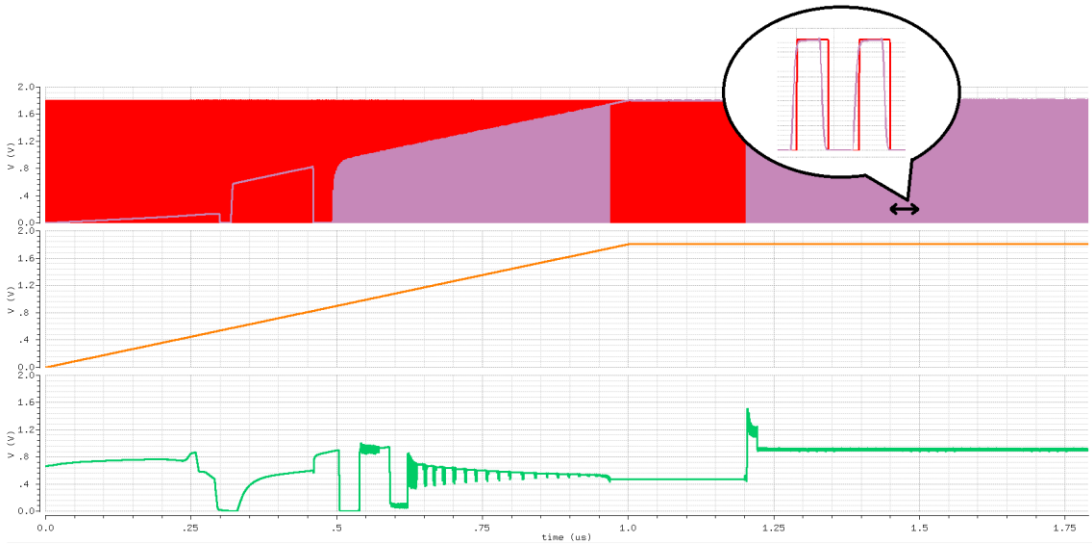


Figure 8.6: Post-layout Power supply Sensitivity

9. CONCLUSION

A conventional DLL architecture is designed and laid out in 180nm 1.8V CMOS process, to achieve a lock range from 120MHz to 670MHz, with reasonable locking time, and jitter. This DLL is suitable to be used in DDR LVDS clock and data alignment of a 1.3 Gsps digital to analog converter.

Post layout simulations across 27 corners and Monte Carlo analyses indicate that the DLL can lock within the specified frequency range within 100ns. For frequencies more than 300MHz, the worst case jitter is below 25ps, even if the jitter simulations include not only the transient noise and but also a 20mV supply ripple. The worst duty cycle error is %7, power dissipation at 600MHz input frequency is less than 1mW and the total Layout area is 145µm× 76.3µm.

A simple digital controller and a duty cycle aligner are also included in the design.

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