ABANT IZZET BAYSAL UNIVERSITY

THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

FABRICATION AND CHARACTERIZATION OF NUCLEAR RADIATION SENSING FIELD EFFECT TRANSISTORS (NürFETs) WITH HIGH-K DIELECTRICS

DOCTOR OF PHILOSOPHY

ŞENOL KAYA

BOLU, MARCH 2018

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APPROVAL OF THE THESIS

FABRICATION AND CHARACTERIZATION OF NUCLEAR RADIATION SENSING FIELD EFFECT TRANSISTORS (NürFETs) WITH HIGH-K DIELECTRICS submitted by **Şenol KAYA** in partial fulfillment of the requirements for the degree of **Doctor of Philosophy** in **Department of Physics, The Graduate School of Natural and Applied Sciences of ABANT IZZET BAYSAL UNIVERSITY in 23/03/2018** by

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DECLARATION

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Şenol KAYA

ABSTRACT

FABRICATION AND CHARACTERIZATION OF NUCLEAR RADIATION SENSING FIELD EFFECT TRANSISTORS (NürFETs) WITH HIGH-K DIELECTRICS

PHD THESIS
ŞENOL KAYA
ABANT IZZET BAYSAL UNIVERSITY GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
DEPARTMENT OF PHYSICS
(SUPERVISOR: PROF. DR. ERCAN YILMAZ)

BOLU, MARCH 2018

The continuous development of a gate stack system and continually shrinking gate-dielectric thickness, have been necessitated by the requirement of higher gate capacitance in order to reduce excessive leakage currents in Metal-Oxide- Semiconductor Field- Effect transistors (MOSFETs). To obtain high gate capacitance and inhibit tunneling, relatively thick insulators with high dielectric constants (high-k) are needed in place of SiO_2 gate dielectric in MOSFETs. In this thesis, the Hafnium Oxide (HfO_2) and Erbium Oxide (Er_2O_3) have been used as two distinct high-k dielectrics as an alternative gate dielectric materials to conventional SiO_2. Although several technological applications of the HfO_2 and Er_2O_3 dielectrics are available in microelectronics, there still exists reliability problem for the usage of them in radiation environments. The detailed investigation should be performed for the realistic microelectronic applications of high- k materials. Hence, in the scope of this thesis, the MOSFETs with HfO_2 and Er_2O_3 gate dielectrics have been fabricated and the possible device usage as a radiation sense materials for defense/space applications and/or radiation soft materials for possible dosimeter applications have been discussed. The device used for the dosimetric purposes, called Nuclear Radiation Sensing Field Effect Transistor (NürFET), is discrete p-channel MOSFET. In addition, the device failure mechanisms including the structural, morphological, electrochemical and electrical changing under radiation environment have also been discussed in details for understanding behaviors of the high- k based devices under radiation environment. The high-k device characteristics have been compared to experimentally fabricated and commercially available conventional devices with SiO_2 gate.

KEYWORDS: NürFETs, RadFETs, Irradiation Sensors, Dosimeters, Transistors, High-k Materials.

ÖZET

YÜKSEK- K DİELEKTRİKLİ ALAN ETKİLİ NÜKLEER RADYASYON DEDEKTÖRLERİNİN (NürFET) ÜRETİMİ VE KARAKTERİZASYONU

DOKTORA TEZİ

ŞENOL KAYA

ABANT İZZET BAYSAL ÜNİVERSİTESİ FEN BİLİMLERİ ENSTİTÜSÜ

FİZİK ANABİLİM DALI

(TEZ DANIŞMANI: PROF. DR. ERCAN YILMAZ)

BOLU, MART - 2018

Geçit bölgesindeki yığın yapılarda süregelen gelişmeler ve ebat olarak küçülen geçit dielektrik kalınlığındaki değişimler sonucunda Metal-Oksit-Yarıiletken Alan-Etkili transistörlerde (MOSFET'ler) oluşan kaçak akımı azaltmak için daha yüksek geçit kapasitanslarının gerekliliği ortaya çıkmıştır. Geçit kapasitans değerini arttırmak ve tünel etkisi önlemek için, MOSFET'lerde SiO_2 geçit dielektrik tabakası yerine yüksek dielektrik sabitli yeni malzemelerin kullanılması gerekmektedir. Bu tezde, geleneksel SiO_2 tabakasının yerine Hafnium Oksit (HfO_2) ve Erbium Oksit (Er_2O_3)olarak iki farklı yüksek dielektrik sabitli malzeme alternatif geçit dielektrik tabakası olarak kullanılmıştır. Mikroelektronikte HfO_2 ve Er_2O_3 dielektriklerinin çeşitli teknolojik uygulamaları bulunmasına rağmen, radyasyon ortamlarında bu malzemelerin davranışlarına ve kullanılabilirliklerine yönelik çalışmalar yetersizdir. Yüksek dielektrikli malzemelerinin gerçeğe uygun/sahaya yönelik mikroelektronik uygulamaları için detaylı bir tetkik yapılmalıdır. Bu nedenle tez kapsamında, HfO_2 ve Er_2O_3 kapı dielektriklerine sahip olan MOSFET'ler üretilmiş, savunma / uzay uygulamalarına yönelik radyasyona dayanaklıları ve/yada radyasyon doz ölçüm sistemlerinde alternatif dielektrik malzeme olarak kullanılabilirlikleri incelenmiştir. Dozimetrik amaçlar için kullanılan özel p- kanallı MOSFET yapılar Nükleer Radyasyona Duyarlı Alan Etkili Transistor (NürFET) olarak isimlendirilmiştir. Radyasyon ortamında yüksek dielektrikli cihazların davranışlarını anlama adına yapısal, morfolojik, elektrokimyasal ve elektriksel değişimi içeren aygıt bozulma mekanizmaları belirlenmiş ve sonuçlar detaylı olarak tartışılmıştır. Ayrıca, yüksek dielektrik malzemelere ait elde edilen sonuçlar, tez kapsamında ayriyeten üretilmiş ve ticari olarak bulunan SiO_2 geçit oksit tabakalı aygıtlar ile karşılaştırılmıştır.

ANAHTAR KELİMELER: NürFETler, RadFETler, Radyasyon Sensörleri, Dozimetreler, Transistörler, Yüksek Dielektrikli Malzemeler.

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LIST OF ABBREVIATIONS AND SYMBOLS

MOS : Metal Oxide Semiconductor
EOT : Equivalent Oxide Thickness
MOSFETs : Metal Oxide Semiconductor Field Effect Transistor
NürFET : Nuclear-Radiation-Sensing Field Effect Transitor
RadFET : Radiation Sensing Field Effect Transistor
ICs : Integrated Circuits
V_{th} : Threshold Voltage
Er_2O_3 : Erbium Oxide
HfO_2 : Hafnium Oxide
SiO_2 : Silicon Dioxide
Si : Silicon
V_{ox} : Voltage Drops in Dielectric
V_{fb} : Flat band voltage
V_g : Gate voltage
V_d : Drain Voltage
I_d : Drain Current
W : Width of Channel
L : Length of Channel
g_m : Transconductance
BE : Binding Energy
E_g : Band Gap Energy
eV : Electron Volt
χ_i : Electron Affinity of Dielectric layer
χ : Electron Affinity of Semiconductor
ψ_B : Fermi Potential Respect to Midgap Edge
ϕ : Fermi Poteltial Respect to Conduction/Valance Band Edge
ϕ_s : Surface Potential
q : Electrical Charge
ϕ_m : Work Function of Metal
ϕ_s : Work Function of Semiconductor
p_s : Hole Concentration
N_a : Acceptor State Density

T : Temperature in Kelvin

Q_{acc} : Charge Density in Accumulation Mode

Q_{dep} : Charge Density in Depletion Mode

Q_{in} : Charge Density in Iversion Mode

Q_m : Mobile Ionic Charges

Q_f : Fixed Charge Density in Dielectric Layer

Q_{ox} : Trapped Charge Density in Dielectric Layer

Q_{it} : Trapped Charge Density at Interface

Q_{eff} : Effective Charge Density in Device Structure

W_{dep} : Depletion Width

n_i : Intirinsic Carrier Concentration

E_c : Energy Level of Conduction Band

E_v : Energy Level of Valance Band

ε_s : Dielectric Constant of Semicondutor

ε_i : Dielectric Constant of Insulator

ε_0 : Permitivity of Free Speace

A : Area of Gate Electrode

μ_p : Mobility of Hole

μ_{ph} : Phonon Scatterired Mobility

μ_c : Coulomb Scattered Mobility

μ_{rs} : Surface Rougness Scattered Mobility

μ_s : Effective Surface Mobility

κ : Channel Length Modulation Parameter

γ : Bondy Effect Parameter

C_{ox} : Dielectric Capacitance

C_b : Depletion Capacitance

SS : Sub-threshold Swing

N_{fs} : Voltage Dependent Surface State Density

D_{it} : Interface Trap Density per Energy Level

Gy : Gray

B : Boron

P : Phosphor

e : Electron

h : Hole

XRD	: X-ray Diffractometer
AFM	: Atomic Force Microscopy
XPS	: X-ray Photoelectron Spectroscopy
MG	: Midgap-subthreshold
CP	: Charge Pumping
$\mathbf{N_{it}}$	: Interface Trap Density
$\mathbf{\Delta N_{it}}$	: Radiation Induced Interface Trap Density
$\mathbf{\Delta N_{ox}}$	: Radiation Induced Dielectric Trap Density
$\mathbf{\Delta E}$	: Sweep of Surface Potential
RMS	: Averarge Surface Rougness

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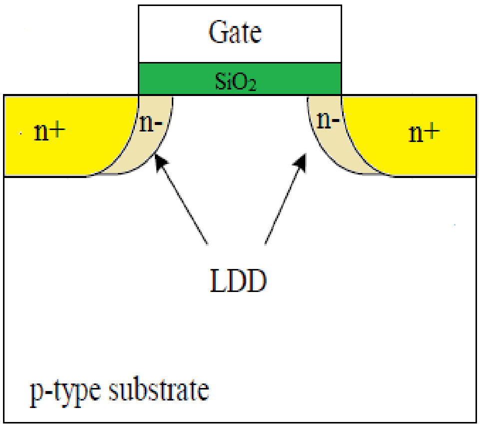
1. INTRODUCTION

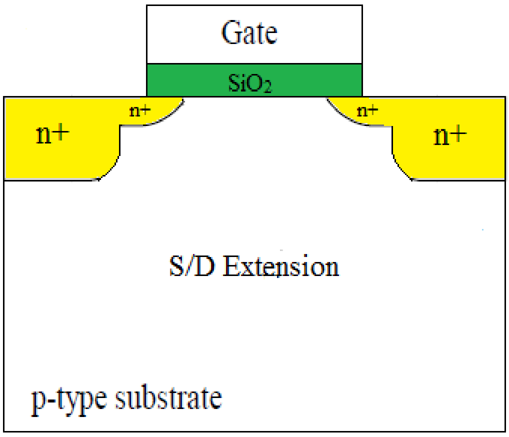
1.1 An Overview of Metal-Oxide-Semiconductor (MOS) Devices

Modern Metal-Oxide-Semiconductor (MOS) transistors were first designated in the 1930s and the revolution on the microelectronics has been achieved following the exploration of reliable oxides for MOS transistors at the beginning of the 1960s (Arora, 2007). Since 1960s, huge developments have been performed in MOS based microelectronic technology and these developments have been caused the rapid growth in all fields, particularly in military and communication electronics. In state of the art technology, MOS based integrated circuits (ICs) such as, MOSFETs, capacitors, BJTs etc., have dominated the semiconductor industry. The ICs are usually manufactured on a mono crystal silicon wafers due to critical specification of the silicon including the excellent electrical and physical feature that are necessary for microelectronics. Silicondioxide is the conventional gate dielectric. This is because of the high quality oxide/Si interface having low defect concentration and the leakage characteristics which leads to be easily fabricated onto Si wafers (Sze, 1981). These features of the SiO_2/Si interface are also exploited to scale-down the ICs in order to decrease operation power, fabrication cost and raise the reliability of the devices. Moreover, the scaling down microelectronic devices also enhances the operation speed of the signal processing; hence it improves the functionality of ICs. The downsizing of the ICs was firstly reported by Gordon Moore in the 1970s and later on has been known as Moore' law. Moore's law indicates that MOS transistor density doubled almost every two years, and this finding became future aim of the microelectronic industry (Bose, 2014).

In earlier state after invention of the MOS technology around the 1960s, aluminum (Al) gate MOS transistors were the workhorse of the micro electrics. The usage of the poly-silicon gate instead of Al is a milestone for these technologies in the late of 1970s. The self-alignment of the source and drain to gate decrease the stray capacitance evolving the signal processing time. Also, poly-Si has adjustable work function for device to have suitable sub threshold voltages (Kamins, 1990). Hence it improves this scaling of the MOS transistors. Later on, when MOS transistor channel dimensions approach to sub-micron level, high electric fields in the channel start degrading the device reliability. To solve this problem, a slightly *n*-doped area in the near of the traditional n^+ source and drain regions (LDD) was formed as seen in Figure 1.1 (a) and it decreases the electrical field and carrier leakage to oxide (Ogura et al., 1980). Afterwards, to eliminate the leak channel effects, a shallow but heavily doped n^+ region as seen in Figure 1.1 (b) has been formed near the traditional n^+ source and drain areas without occurring any issues related to high series resistance effects.



(a)



(b)

Figures 1.1: Schematic view of a-) LDD n-channel MOSFET, and b-) heavily-doped n-channel MOSFET (Adamu-Lema, 2005).

Another crucial development milestone for performance improvement of the MOS transistors is the usage of the Salicide (Self aligned) formation during the MOS based device fabrication process seen Figure 1.2. The rise in resistance of the poly-Si gate and the presence parasitic resistance of the shallow source and drain channels cause decrement in performance of the scaling MOSFETs. In the late 1980's, owing to the resistance enhance with reducing the channel depth, it has become significant to usage of the silicide layer to decrease the parasitic source and drain resistance. The decline in parasitic source and drain resistance improve drive current (Adamu-Lema, 2005).

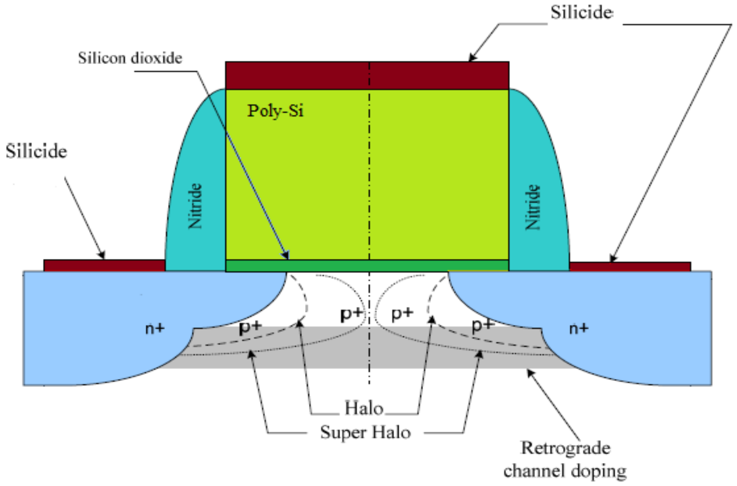
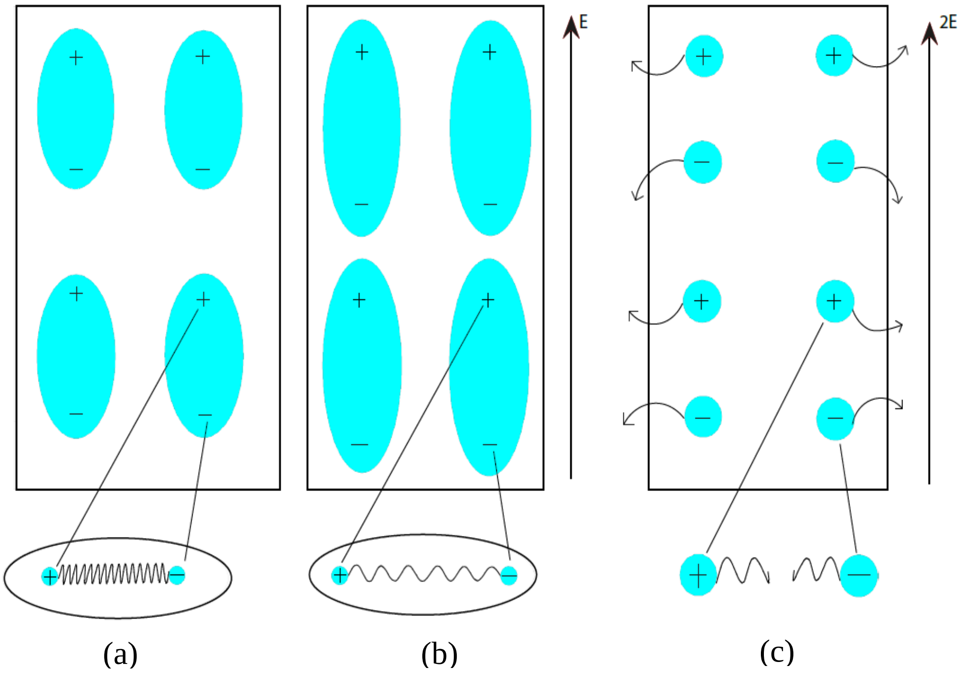


Figure 1.2: Schematic cross section self- aligned silicide in channels and on the poly-Si gate MOSFETs (Adamu-Lema, 2005).

After self-aligned fabrication process to reduce scaling of MOS devices, the channel engineering became popular in the 1990s to reduce short effects (Adamu-Lema, 2005). It was found that enhancement of channel doping in certain value can control the short channel effects. However, conventional channel doping became inadequate for the channel length, where is approaching to 100 nm, due to degraded carrier mobility at high doping levels. The new doping scheme, called super steep retrograde (SSR), was used to enhance carrier mobility and decrease the V_{th} when channel length approaching to 100 nm (De and Osburn, 1999). On the other hand, the SSR doping characteristics does not become sufficient for the sub 100 nm channel lengths. To overcome this problem, the halo doping regimes have been studied in the late of 1990s (Adamu-Lema, 2005). The halo doping regimes control the surrounding depletion layers and eliminate the over enhancement of channel doping. The strained-silicon channels MOS devices have been used to scale roadmap of microelectronics. However, in the middle of 2000s, people have been facing with degradation of device performance, sub threshold slope, off state current etc., caused by poorer short channel under gate lengths sub 65 nm (Adamu-Lema, 2005; Kuhn, 2009). Hence, researchers have introduced usage of high-k materials to replace the conventional Silicon Dioxide as gate dielectric materials (Adamu-Lema, 2005; Kuhn, 2009; Stillmaker and Baas, 2017). It has been reported that high-k materials with metal gate decrease gate leakage and enable further MOS device scaling. The usage of a metal gate instead of poly-Si prevents poly depletion (which acts like a thicker oxide, resulting in reduction inversion capacitance), and this solve the pinning issue of V_T seen with poly-Si on high-k (Chau et al., 2004). The presence of the high defect densities and trapped charges are the major problem for the high-k based devices for their reliability. The presence of the high defect densities causes various scattering mechanisms which degrades the mobility. Studies are focusing on the improvement of high-k based devices reliability. The researchers and semiconductor industry expect that it is necessary to replace the conventional silicon dioxide with suitable high-k dielectric materials in order to improvement of performance of MOS devices with novel device architectures. Nowadays, researchers are focusing on using high-k dielectrics and metal gates with technology nodes at 45 nm and smaller (Mistry et al., 2007; Stillmaker and Baas, 2017), and also focusing on the multi-gate (one dielectric/two metals or two dielectrics/one metal) approach transistors at 20 nm and smaller (Bohr, 2011; Kuhn, 2012). On the other hand, some other researchers have been also spent demanding efforts for development of future MOS technologies including the nano-electro-mechanical devices (Venkatasubramanian et al., 2011), carbon nanotube transistors (Franklin et al., 2012) or nanowire transistors (Kuhn, 2012). But these devices should be proved to become commercially viable.

1.2 High-k Dielectrics

Dielectrics can be defined as materials where the electrostatic field could persist for a long period of time. The dielectrics do not have free electrons; hence exhibits very high resistance to conduct the electricity, but their behavior may be switched under an applied electric field (Choudhary and Kumari, 2009). The dielectric phoneme comes from polarization characteristics which are Electronic Polarization, Ionic Polarization, Orientation Polarization and Space Charge Polarization, of the materials. Basically, dielectrics have positive and negative charges which are bounded by an elastic force having a spring (Gallot-Lavallée, 2013). Under applied electric field, these coupled charge pairs cannot move inside the insulator; the positive and negative charges pull the spring to opposite directions resulting in rise in the spring tension which is proportional to the applied electric field. After a critical point, continuous increase in the applied electric field is going to breaks the imaginary spring and then charge becomes; hence, free the insulating dielectric layer starts to contact current (Gallot-Lavallée, 2013). These mechanisms can be schematically seen in Figures 1.3 (a)-(c).



Figures 1.3: Spring approaches for charge coupled in polarization inside the dielectric materials, a-) for without electric field, b-) extension in string under applied electric field, c-) conduction after breakdown of string under high electric field.

Depending on several parameters, such as polarizations magnitude and band gap of materials, the dielectric constant exhibits variations between material to materials (Robertson and Wallace, 2015). The SiO_2 has been a conventional dielectric layers with permittivity of 3.9, over four decades. For the MOS technology, the high- k materials can be defined as materials which have dielectric constant value higher than silicon nitrate (k=7). Some of the high-k dielectric materials are Titanium Oxide (TiO_2) (Nath and Roy, 2015), Hafnium Oxide (HfO_2) (Park et al., 2006), Aluminum Oxide (Al_2O_3) (Mahajan et al., 2014), Erbium Oxide (Er_2O_3) (Zhu and Liu, 2004), etc. Both of these high-k materials have been used in a number of applications in optoelectronics, sensor technologies, depending on their entire material specifications.

1.3 The Use of High- k Materials in Integrated Devices

Reducing the scaling of MOS transistors caused the high gate and channel leakage current when the SiO_2 was used as gate dielectrics. This means that devices become unreliable. Hence, conventional SiO_2 had to be replaced with suitable new gate dielectrics. Due to high resistance to the passage of electric current characteristics thanks to polarization mechanism discussed in the previous section, the high- k dielectrics can be introduced as new gate dielectric materials to replace conventional SiO_2 layer for the future device approach. A MOS based- Field Effect Transistor electrical source–drain current is strictly connected to capacitance of the gate dielectric which can be expressed as $C=\varepsilon_0 kA/d_k$ where ε_0 is the permittivity of free space, k is the relative dielectric constant, A is the area of the gate contact and d_k is the thickness of dielectric layer. Leakage currents decrease almost exponentially with enhancing dielectric thickness. Thus, the usage of the physically thicker layer high- k dielectrics instead of SiO_2 may be solution of the tunneling effects. Use of the high-k materials is going to keep the same capacitance while it decreases the leakage current. In general view, electrical thickness of a novel high-k dielectrics in terms of equivalent SiO_2 thickness or 'equivalent oxide thickness' can be expressed as $EOT= d_k 3.9/k$ where, 3.9 is dielectric constant of SiO_2. In this view, it can be easily concluded that the high- k dielectrics enable scaling to continue to very lower EOT values (Robertson and Wallace, 2015).

As mentioned above, the high-k dielectrics are promising for the future gate dielectric applications, but not all high-k materials are convenient for MOS transistor applications. Some issues have to be solved for the process integration of high-k dielectrics to be used in the device applications. These requirements are listed in (Robertson, 2006; Robertson and Wallace, 2015; Wilk et al., 2001);

Permittivity. The static dielectric constant (relative permittivity) of selected materials should be higher than that of SiO_2. The convenient dielectric constant for the gate dielectric applications should be in range of 10 to 40. General trend of the high-k value of dielectrics is inversely proportional to band gap. Hence, dielectrics having large k value cause strong fringing field which degrading the channel performance.

Thermodynamically Stable with Si. The deposited dielectric materials must not react with underlying Si to form parasitic sub oxide (SiO_x) and silicide. The presence of any formation of the SiO_x is going to decrease the equivalent oxide thickness and metallic silicate (MSi_x) formation may increase the tunneling effects. Selection of dielectric layer that has large Gibbs free energy of formation to prevent reaction with Si is a suitable way to eliminate the parasitic phase formation.

Band gap and Band Offset Values: The dielectric materials have to be insulator; the expected band gap energies for the microelectronics must be higher than 5 eV. In addition, barrier potentials for electron and hole conduction should be at least 1 eV in order to prevent Schottky emission from dielectric material bands.

Kinetic stability: Dielectrics should resist the dopant activation anneal for at least 5 s at 1000 ^{0}C. Researchers have to specify either they use crystalline or amorphous dielectrics in their applications. The problem arises for some gate dielectrics having lower crystallization temperatures. Crystallized dielectrics that have grain boundaries where act as dopant diffusion path, location of the trap center lead to raise in the leakage currents (Robertson and Wallace, 2015). Also, thickness of the gate oxide can have the same dimensions with crystalline-grain size at low scales. Hence, uses of amorphous materials are more popular for MOS transistors (Cheng et al., 2013; Ding et al., 2014). On the other hand, it is also reported that crystallization of dielectric layer some time enhances the dielectric constant of the film (He and Sun, 2012). In addition, no critical leakage variations have been observed between amorphous and nano-crystalline phase of HfO_2 dielectric (Kim et al., 2004). Hence, parameters effects should be taken into account in development of novel devices.

Interface Quality: The conventional SiO_2/Si interface exhibits excellent interface quality for the MOS technologies. Interface defects are important due to the following reasons; i- the threshold voltages may shift higher values due to trapped charges, ii- the number of trapped charges may change with time, causing devices operating characteristics, iii- the carriers can be scattered by defect site in channels, leading lower carrier motilities, iv- higher number of trap may cause dielectric breakdown (Robertson and Wallace, 2015). The interface quality of the film can be generally controlled by fabrication process. To obtain good electrical performance, the grown dielectric layer must have good uniformity, low roughness and high quality interface. The interface trap density must be in the order of 10^{10} cm^{-2} for high interface quality; however, for high-k based devices it is acceptable up to 10^{13} cm^{-2} in microelectronics.

Gate Electrode: The interface structure between gate contact and dielectric layer is an important criterion for the device specification of MOS devices. Selection of the gate electrode can be changed depending on the device structure. For n-channel MOSFETs gate electrodes having low work function which is close the conduction edge of Si (4.06 eV) are suitable. However, for the p-channel MOSFETS gate electrodes having high work function, which is close the valance edge of Si (5.10 eV), are more useful. Suitable gate electrodes deplete the Si layer and the conduction band edge bends to Fermi Level. Hence only small V_{gs} is required for saturation. Such gate is necessary for low threshold voltage and sub-threshold slope for MOSFETs (Yeo et al., 2002). Poly Si gate electrode was popular for the SiO_2 based MOS technology, but it reduces the performance for the high-k base MOS devices due to presence of poly-Si depletion. On the other hand, metals can react with the underlying dielectric layer causing the effective work function of the gate stack to migrate towards the mid-gap of silicon during the alloying process. Hence, metal contact selection should be carefully performed and if it is needed, new approaches, like multi-gate, should be tried to reduce gate electrode effects on device performance.

1.4 Aim and Scope of the Study

Considering the criteria listed in the previous section, selection of the high- k materials for microelectronics should be carefully chosen. Among various high-k dielectrics, Hafnium Oxide (HfO_2) is the leading contenders for the replacement of conventional SiO_2 as gate dielectric materials in advances materials industry (O'Kane et al., 2007; Yan et al., 2016), owing to its charming features including the high dielectric constant (25) (He et al., 2005), large band gap (5.8 eV) (Chang et al., 2014), large band offset value (1.5 eV) (Tan et al., 2009), and good thermodynamic stability (Kim et al., 2005). In addition to HfO_2 dielectrics, earth oxides have also become trending materials for the high-k devices to replace SiO_2 in the future CMOS devices, because they possess a combination of high dielectric constants, large band gaps, and high band offsets values (Jo et al., 2006; Leskela et al., 2006; Lupina et al., 2006; Pan and Huang, 2009; Zhu et al., 2006). Among the rare oxides, in addition to mentioned demanding rare oxide properties, with para/ferromagnetic properties and high chemical/ thermal stability, Erbium Oxide is also another most promising dielectric for the future gate dielectric applications (Chen et al., 2006; Kao et al., 2012; Zhu et al., 2006). Although there are several technological applications of HfO_2 and Er_2O_3 dielectrics in microelectronics, there still exist reliability problem for the usage of them under radiation environment. Numerous state of the art devices lose their reliability under operation on radiation environments (French et al., 2016). Hence, detailed investigations should be performed for the realistic microelectronic applications of the high- k materials. So, in the scope of this thesis, the MOSFET having HfO_2 and Er_2O_3 gate dielectrics have been fabricated and the possible device usage and device failure mechanism under radiation environment have been investigated in details. In addition, the variations on the device characteristics have also been compared to commercial SiO_2 gate dielectric MOSFETs fabricated in NÜRDAM- Turkey and TYNDALL-Ireland which are also known as NürFETs for NÜRDAM's MOSFETs and RadFET for TYNDALL's MOSFETs.

2. BASIC PRINCIPLES OF THE NUCLEAR-RADIATION-SENSING FIELD EFFECT TRANSITORS (NürFETs)

2.1 MOS Structures

Metal-Oxide-Semiconductor (MOS) structures are still stand as core design of state of the art microelectronic systems, despite continuous development in semiconductor technology. Basically, two main MOS structures will be explained in this section. These MOS structures are MOS capacitors and MOSFETs (Metal Oxide Semiconductor Feld Effect Transistors). A MOS capacitor is the simplest form of the MOS structure. The essential information including interfacial trap density and oxide breakdown can be obtained, easily. On the other hand, MOSFETs have more complicated structure that is still the most common technology in microelectronic technology.

2.2 MOS Capacitor

2.2.1 General Introduction

The MOS capacitor is a device that consists of metal electrode on the top of dielectric layer deposited onto p- or n- type semiconductor substrate and whole back side of the wafers is deposited by ohmic contact (e.g., silver paint) to decrease signal losses. The simple MOS capacitor structure is illustrated in Figure 2.1. Examinations of capacitor performance of any dielectric materials give researchers important knowledge about the MOSFET performance. The dielectric/ interface quality, behavior of dielectric characteristics and specifications about semiconductor substrate are some of parameters that can be easily specified with simple capacitor form before the realistic MOSFET fabrications. An ideal MOS capacitor is defined as follows. i- there exists no carrier transport through the dielectric layer under even biasing condition, ii- there exist no charges at interface and dielectric layer, iii- gate electrode is thick enough to create equipotential, iv- back contact meets the ohmic contact requirements, i.e., no parasitic potential occurs in conduction of signal, v-the differences of Fermi level between metal and semiconductor should be zero at equilibrium and can be expressed as (Sze, 1981);

$$\phi_{MS} = \phi_M - \phi_S = 0 \qquad (2.1)$$

and one can find more details of Eq. (2.1) from Figures 2.2 (a)- (b) and ideally differences should be zero (Sze, 1981);

$$\phi_{MS} = \phi_M - (\chi + \frac{E_g}{2q} + \Psi_{Bp}) = \phi_M - (\chi + \frac{E_g}{q} - \phi_p) = 0 \quad \text{for p- type} \qquad (2.2\text{- a})$$

$$\phi_{MS} = \phi_M - (\chi + \frac{E_g}{2q} - \Psi_{Bn}) = \phi_M - (\chi + \phi_n) = 0 \quad \text{for n- type} \qquad (2.2\text{- b})$$

where χ and χ_i are the electron affinities for the semiconductor and dielectric layer, respectively. Ψ_{Bn}, Ψ_{Bp}, ϕ_n, ϕ_p are the Fermi potentials with respect to the midgap and band edges.

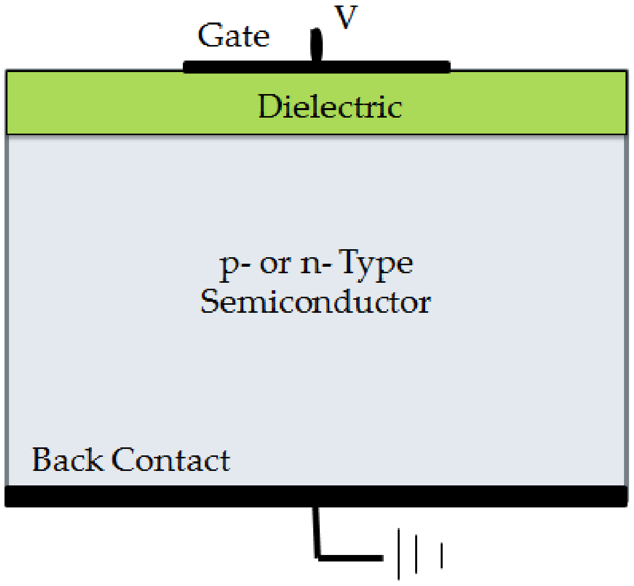
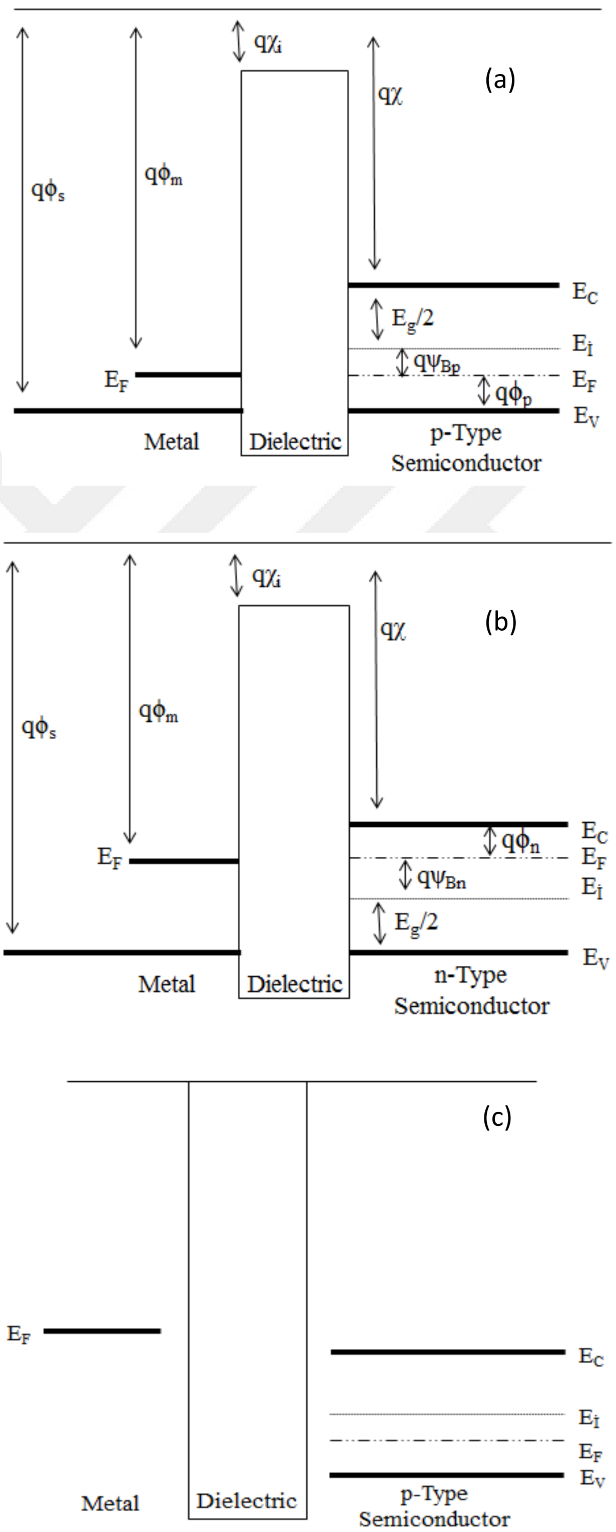
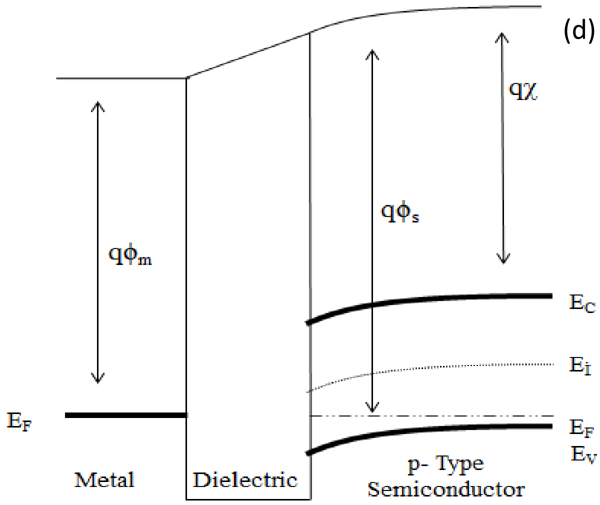


Figure 2.1: Schematic of MOS capacitor

However in the real case, there exist differences between metal and semiconductor Fermi level. These differences can be schematically seen from Figure 2.2 (c) for p-type semiconductor. When the metal and semiconductor stick to two sides of the dielectric assuming that no any impurity, charges exist at dielectric layer and interface, the semiconductor bands start bending due to the Fermi level which must be constant and vacuum level must be continuous at thermal equilibrium as illustrated in Figure 2.2 (d) for p-type semiconductor. In order to get all bands flat, a voltage has to be applied to gate electrode. This special required voltage called flat band voltages, V_{fb}, is expressed as (Sze, 1981);

$$V_{fb} = \phi_M - \phi_S \tag{2.3}$$





Figures 2.2: Energy band diagram of ideal MOS structure a-) for p-type, b-) for n-type semiconductor, c-) for real MOS capacitor, and d-) band bending after thermal equilibrium for p-type semiconductor (Sze, 1981).

The Eq. (2.3) is valid for ideal MOS capacitor condition. Since all bands of dielectric and semiconductor are flat, no charge, field and current flow exist in the device. On the other hand, an additional term will be added to flat band voltage equations in the presence of any trapped charges in the device structure.

2.2.2 Operating Modes and Surface Potential under Gate Bias

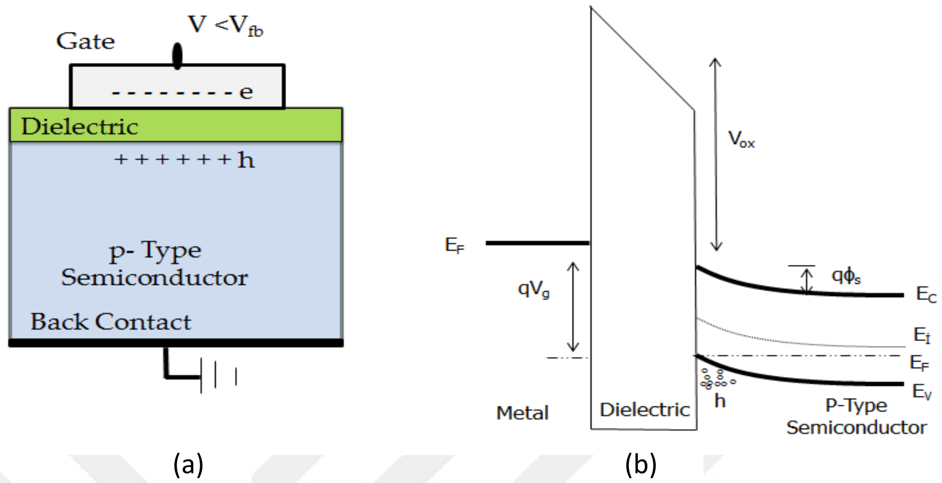
Capacitance behavior of dielectric layer exhibits variations under gate voltage. Basically, three operation modes namely accumulation, depletion and inversion have been observed under bias voltage. The details of these modes are explained in following by giving the ideal p-type MOS capacitor as an example.

2.2.2.1 Accumulation mode

When negative voltage is applied to gate, the bands near p- type semiconductor surface are bent upward which is illustrated in Figures 2.3 (a) and (b). The upward bending of energy bands at semiconductor surface enhance the surface potentials ($\phi_s = E_i - E_f$) resulting in rise of hole concentration (p_s) defined by (Hu, 2009);

$$p_s = N_a e^{-q\phi_s / kT} \tag{2.4}$$

Generally, ϕ_s varies from -100 to -200 mV and this causes rise in the hole concentration of p-type semiconductor surface. Hence, this operation mode is called as accumulation for p-type semiconductor.



Figures 2.3: a-) accumulated charges and, b-) Energy band diagram of device structure under accumulation mode (Sze, 1981).

In addition, the applied voltage from gate layer will be shared by following Eq. 2.5;

$$V_g = V_{fb} + \phi_S + V_{ox} \tag{2.5}$$

In accumulation mode, it is known that ϕ_s is very small and voltage drop capacitance become;

$$V_{ox} = V_g - V_{fb} \tag{2.6}$$

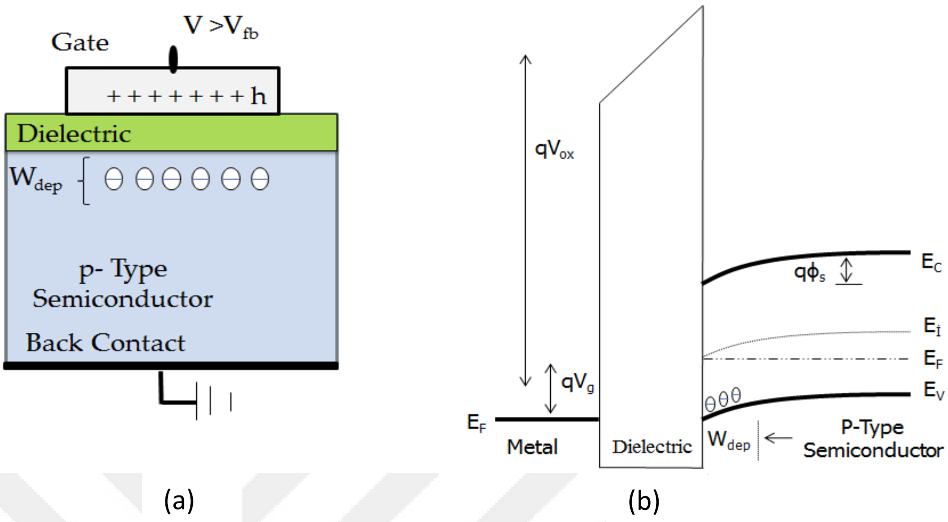
The voltage is applied to gate but the charges are accumulated on semiconductor hence negative polarization (minus sing in Eq. 2.7) occurs and also using the Gauss's law (Q_{acc}=V_{ox} xC_{ox}), Eq. 2.6 can be rewritten as;

$$Q_{acc} = -C_{ox}(V_g - V_{fb}) \tag{2.7}$$

Hence, with some shift associated with V_{fb}, the device behaves like a capacitor. Here Q_{acc} represents all charges in device structure (Hu, 2009).

2.2.2.2 Depletion mode

When more positive voltage than flat band voltages applied to MOS structure, the holes are depleted in the p- type semiconductor and band near p- type semiconductor surface are bent downward which is illustrated in Figures 2.4 (a) and (b). Owing to presence of electric field, E_F is far from both E_c and E_v, densities of electron and hole are very small.



Figures 2.4: a-) Depletion edge and, b-) Energy band diagram of device structure under depletion mode (Sze, 1981).

The depleted region has certain width, $W_{dep}= \text{sqrt}[(2\varepsilon_s\phi_s)/(qN_a)]$, then Eq. 2.7 can be rewritten (Hu, 2009)

$$V_{ox} = -\frac{Q_{acc}}{C_{ox}} = -\frac{Q_{dep}}{C_{ox}} = \frac{qN_aW_{dep}}{C_{ox}} \tag{2.8}$$

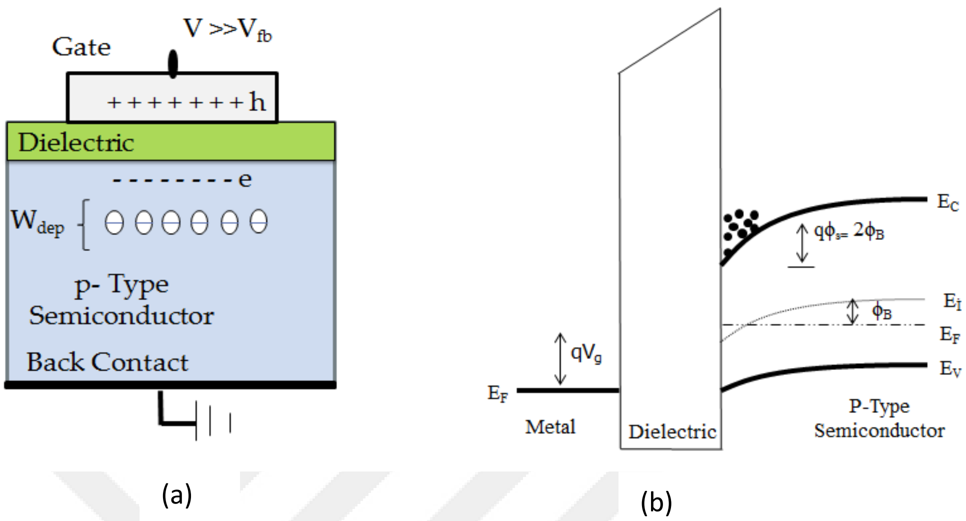
Here Q_{dep} is negative due to presence of acceptor ions, and the gate voltage relation becomes;

$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} + \frac{qN_aW_{dep}^2}{2\varepsilon_s} + \frac{qN_aW_{dep}}{C_{ox}} \tag{2.9}$$

Considering Eq. (2.9), after extracting W_{dep} values, the V_{ox} can be calculated (Hu, 2009).

2.2.2.3 Inversion mode

When large positive voltage is applied to MOS structure, p- type semiconductor and band near p- type semiconductor surface band continue to bend downward. Above the certain limit, called threshold voltage, semiconductor surface is inverted from p-type to n-type meaning that electron density becomes large at surface which is illustrated in Figures 2.5 (a) and (b). Threshold condition can be defined as the equilibrium of surface electron density, n_s, with bulk doping concentration, N_a, which means that $(E_c-E_f)_{surface} = (E_f-E_v)_{bulk}$..Higer electric field than this limits cause opposite charge accumulation.



Figures 2.5: a-) Inversion edge and, b-) Energy band diagram of device structure under inversion mode (Sze, 1981; Zeghbroeck, 2011).

Considering these discussion, threshold condition occurs when $\phi_s=2\phi_B$ which can be formulated as (Hu, 2009);

$$\phi_s = 2\phi_B = 2\frac{kT}{q}\ln\frac{N_a}{n_i} \tag{2.10}$$

where ϕ_B is bulk potential, n_i is the intrinsic carrier concentration of semiconductor. After that, the threshold voltage can be defined as (Hu, 2009);

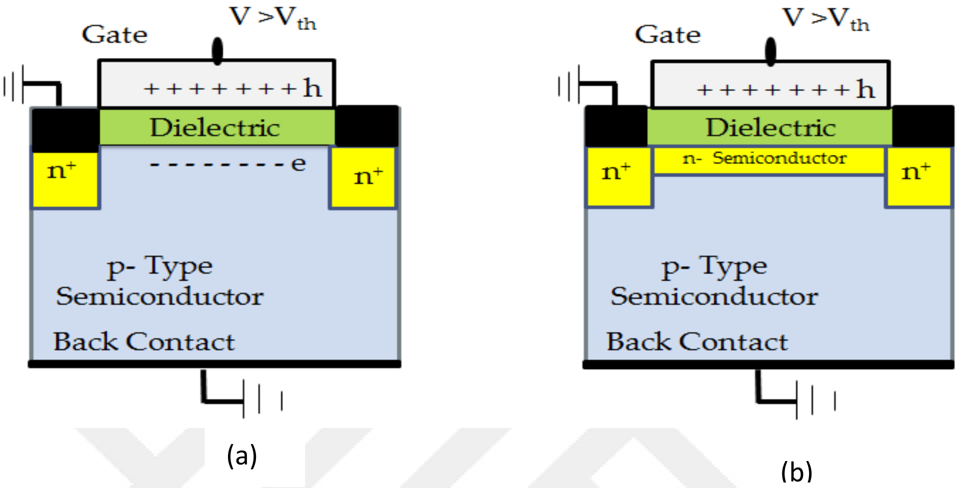
$$V_{th} = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}} \tag{2.11}$$

An applied gate voltage higher than V_{th} causes presence of inversion layer and inversion charge density occurs Q_{inv}. This means that the surface potential (ϕ_s) can not further enhance $2\phi_B$. Any further increases on the V_g are directly transmitted to dielectric layer causing the electrical stretch. On the other hand, since ϕ_s cannot further enhance, the depletion region reach a maximum as expressed in ref. (Hu, 2009);

$$W_{d\max} = \sqrt{\frac{2\varepsilon_s 2\phi_B}{qN_a}} \tag{2.12}$$

An added additional term to Eq.(2.9) comes from inversion charges (Hu, 2009);

$$V_g = V_{fb} + 2\phi_B - \frac{Q_{dep}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} = V_{th} - \frac{Q_{inv}}{C_{ox}} \tag{2.13}$$



Figures 2.6: a-) Charge location in inversion, b-) Formation of thin n- layer in the presence of high electric field at p- type semiconductor substrate.

For the MOS type transistors, when no voltage is applied to the gate source normally they do not conduct the current. In order to current start flowing, the inversion layer should be occurred, i.e., the n-semiconductor channel should be formed by applied voltage as seen in Figures 2.6 (a) and (b) to flow the current. The magnitude of the V_{th} is proportional to some parameters in Eq. (2.11)

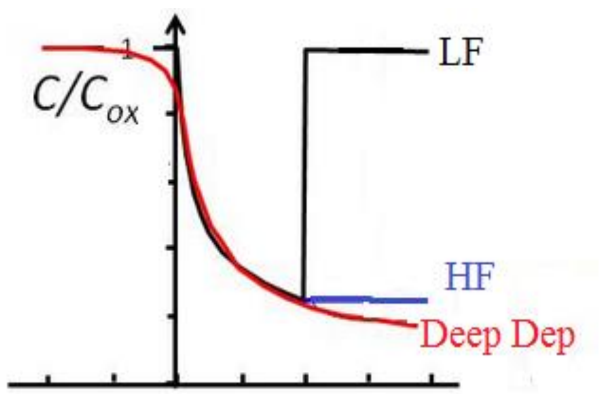


Figure 2.7: Typical capacitance voltage curves of MOS capacitor having different inversion regimes (Zeghbroeck, 2011).

The important parameters are work function of gate metal and capacitance of dielectric layer. The low value of V_{th} is expected for MOS transistor application to reduce power consumption. In the past, the doped poly-Si was useful to adjust V_{th} but they were not really appropriative for the high-k dielectric to be used as gate electrode. Hence parameters should be carefully investigated for device applications. On the other hand, in ideal cases applied voltage frequency may change inversion capacitance characteristics. The possible three regimes can be seen in inversion, namely, low capacitance, high capacitance, and deep depletion inversion capacitance as seen in Figure 2.7. Due to the MOS structure block the DC current, AC signal must be applied to gate electrode for capacitor measurements.

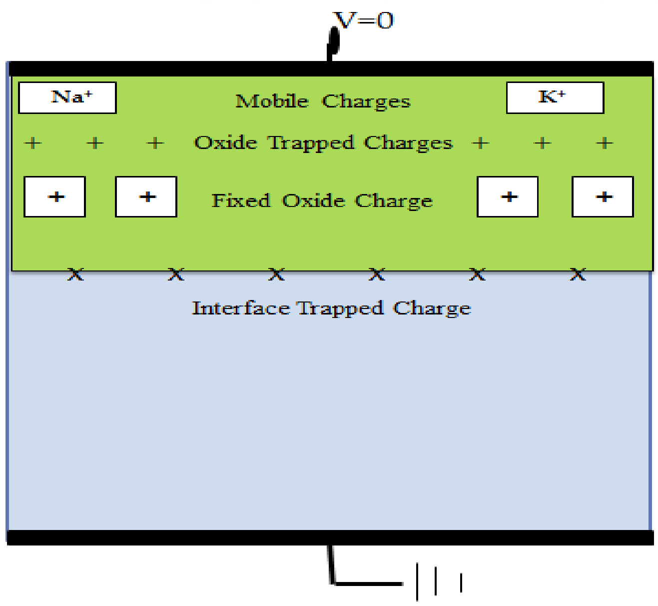


Figure 2.8: The impurities and location of impurity charges on the MOS devices

At low frequency limits, minority charges generation can follow the AC signal to balance charge at gate, hence, invasion capacitance is almost similar to the dielectric capacitance. At higher frequencies, due to large delay constant for generation and annihilation of charges, they respond to applied voltage frequency. Hence, at high frequencies, capacitance in inversion is obtained from the series connection of the dielectric capacitance and the capacitance associated with depletion layer at maximum width, W_{dmax}. In addition, sometimes deep depletion occur as inversion capacitance. In some cases at high frequencies, when applied voltage is ramped up sharply from flat bands to inversion, the structure cannot reach stable thermal equilibrium result in the inversion layer cannot be formed. This means that the depletion width keeps enhancing beyond its maximum thermal equilibrium value, W_{dmax}, with the applied bias and the small-signal capacitance will continue to follow the high frequency capacitance curve (Zeghbroeck, 2011).

2.2.3 Impurities in the MOS structures

In the ideal MOS structure, no parasitic charges exist at dielectric and interface between semiconductor and dielectric layer. However, in the real device structure, one cannot eliminate the presence of parasitic charges even in SiO_2/Si stack in which perfect interface structure is expected. In the early studies, the MOS devices have revealed that the presence of the parasitic charges strongly influence the electrical performance of MOS transistors including the threshold voltage, leakage characteristics, mobility of carrier etc (Jaksic et al., 2002b; Kaya et al., 2015; Wang et al., 2013). The charges in MOS structures are mobile ionic charges, fixed oxide charges, oxide trapped charges, and interface trapped charges as in shown Figure 2.8.

2.2.3.1 Mobile Ionic Charges

Mobile ionic charges are basically ionized alkali metal, e.g., sodium-ions or potassium-ions. These charges are relatively moveable in the dielectric layer even in low temperature and low gate voltages. Therefore, the higher density of these ionic charges causes significant ionic current and threshold voltage shift which degrade the performance instabilities. These impurities are due to cleaning process and used chemicals during the fabrication steps. Since few decades, great developments have been achieved to avoid impurities associated from mobile ions by using clean rooms and hands-free cleaning process. The orders of mobile ions are 10^{11} cm^{-2} for real MOS devices. The mobile ions are almost positively charged result in net amount of these charges cause negative voltage shift (Sze, 1981). The densities of these charges can be specified by bias- temperature stress (BTS) techniques (Zhu, 2008). In BTS, following the complete fabrication process, the capacitance curves of sample are measured. After that, devices heated over 100 ^{0}C and positive voltages have been applied to gate for 5 minutes then device capacitance is measured after cooling under positive voltage to room temperature. The second heating steps were performed under negative gate bias in the similar condition. Following the cooling of sample under negative gate voltage, the capacitance curves is measured and then the Q_m can be calculated using the following relation (Zhu, 2008).

$$Q_m = C_{ox}[V_{fb}(-voltage) - V_{fb}(+voltage)] \tag{2.14}$$

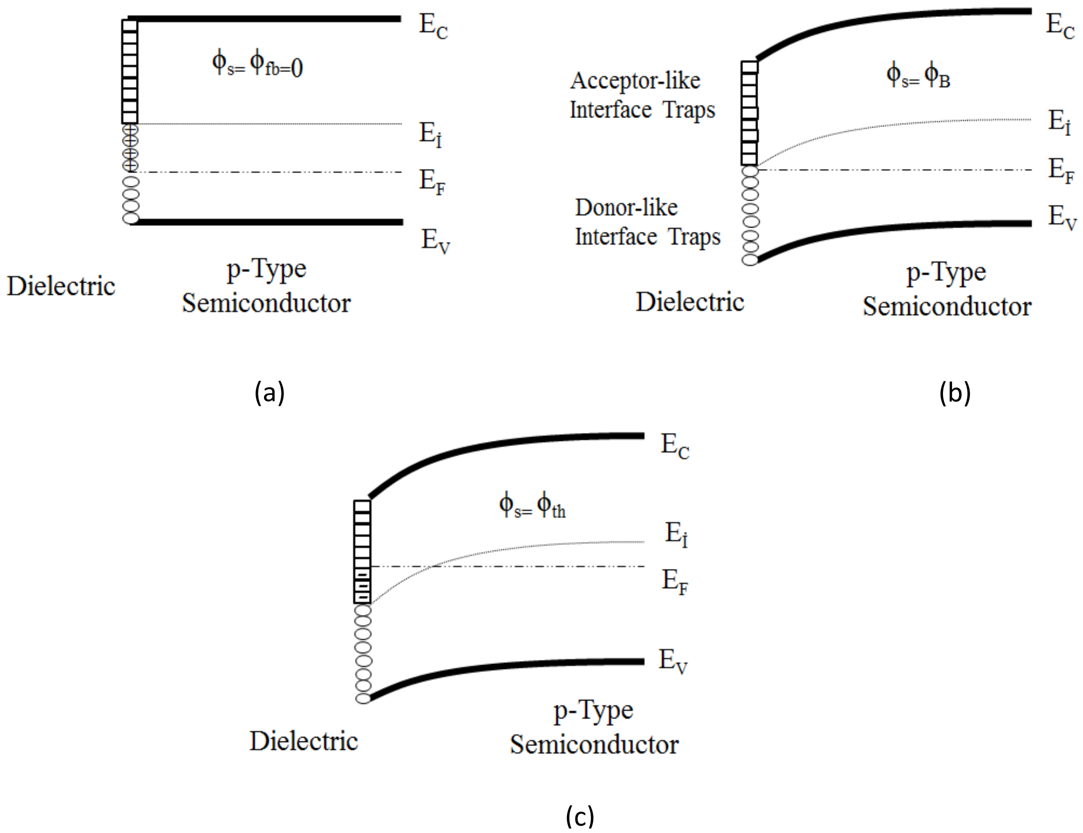
The BTS methods can be useful for the detection of high mobile ionic concentration typically 10^{13} cm^{-2}. When the concentration of the mobile ion approaches to 10^{11} cm^{-2}, the limitation occurs due to the electron/hole injection toward the gate layer. Especially, possible hole transport under gate voltage may create new defect in the dielectric layer (Cochrane et al., 2007; Zhou et al., 2005). The contribution of the created new defect to flat band voltage may deviate the real mobile ion calculation. Hence, the BTS method gives more accurate results for the devices heavily contaminated samples.

2.2.3.2 Oxide Charges

Owing to the oxidation- induced defects, impurities, or generation of defects created by irradiation or similar bond breaking processes of dielectric, the oxide charges can be generated. Roughly, these charges can be divided into two sections, i- fixed oxide charges (Q_f) and ii- oxide trapped charges (Q_{ox}). The fixed oxide charges cover positive charges inside the dielectric layer which are close to the dielectric semiconductor interface usually generated during fabrication process. These charges are immobile under applied voltage and temperature stressing. Hence, the contribution of the fixed charges to the flat band /threshold voltage shift is fixed and stable (Sze, 1981). The amount of these charges can be controlled during the fabrication process. Oxide trapped charges cover almost charges which are captured by defect site generated by irradiation and/or bias- temperature stress, etc. The fixed oxide charges are also given in subtopic of these oxide trapped charges in the literatures. The trapped charges in the oxide layer can be positive or negative but they are generally positive that are holes. The oxide trapped charges may move under applied electric field by hopping or tunneling mechanism (Oldham and McLean, 2003). The total contribution to flat band/threshold voltage can be positive or negative depending on sing of the oxide trapped charges.

2.2.3.3 Interface Charges

The interface charges refer to in this section are charges trapped at electronic energy level of the dielectric/semiconductor interface. These charges arise due to lattice mismatch between the dielectric/semiconductor interface, dangling bonds, etc (Ma and Dressendorfer, 1989). Interface traps create a kind of potential well at interface where both electron and holes can be trapped. Due to presence of additional field generated by interface trapped charges, the carrier mobility is degraded when device operated in saturation (Zhu, 2008). In addition, the presence of field causes the bending of the energy bands and shifts the flat band/threshold voltages. Localized trap site at energy band can capture/release mobile carriers depending on the applied voltage field. These behaviors decrease the device reliability. Hence, low interface trap density of device is curial to reach expected device performance.



Figures 2.9: Energy band diagram of dielectric/ p-type semiconductor interface incorporating the interface traps for the cases a-) ϕ_s=0, b-) midgap level ($\phi_{s}= \phi_B$) and c-) $\phi_s = \phi_{th}$ (Sze and Kwok, 2007).

Two types of defects exist in the forbidden band of semiconductor. The trap sites localized near the conduction band is called as acceptor- like traps where electron can be trapped while the trap sites close to the valence band is called as donor-like traps where holes can be trapped (Cetinkaya et al., 2015; Nicollian and Brews, 1982). The physical illustration of these interface traps is depicted in Figures 2. 9 (a)– (c). Acceptor-like interface traps behave like acceptor and they are neutral when empty. When they are captured electron, their charges change to negative. On the other hand, donor- like interface traps behave like donor and they are positively charged while empty. The donor- like interface traps become neutral when they are filled with electrons. On the other hand, in the mid gap level the interface trap charge is zero for $\phi_{s=}$ ϕ_B. Therefore, no additional contribution from interface traps to the voltage shift observed at midgap level (Sze and Kwok, 2007). This energy level also tends to pin the semiconductor Fermi level at the surface and also the presence of higher localized interface trap density influences the barrier height of the device [54]. It means that at accumulation, almost all the donor- like traps charges are positive and the acceptor- like traps are neutral. Hence, the total charge due to interface states, Q_{it}, will be positive. When gate voltage increases, some of acceptor- like traps moves below the Fermi level and capture electron. Since donor-like traps are neutral, the net charge due to interface states will be negative at inversion (Sze and Kwok, 2007). The amount of these charges can be calculated by the following relations;

$$Q_{it} = q\int_{E_F}^{E_{cb}+q\phi_s} D_{it}(E)dE \tag{2.15-a}$$

$$Q_{it} = -q\int_{E_{vb}+q\phi_s}^{E_F} D_{it}(E)dE \tag{2.15-b}$$

where D_{it} represent the interface trap density per energy level. Eq. (2.15-a) is valid assuming all interface traps are donor-like (accumulation of p-type semiconductor), whereas Eq. (2.15-b) is valid assuming the all interface traps are acceptor-like (inversion of p-type semiconductor) (Ma and Dressendorfer, 1989). Assume that all mentioned impurity charges including the mobile, fixed oxide, interface, and oxide trapped are positive, than the effects of these charges on the capacitance curves are illustrated in Figure 2.10. The sum of these oxide charges is also called effective oxide charge Q_{eff} and its distribution is given in Eq. (2.16).

$$Q_{eff} = Q_m + Q_f + Q_{ox} + Q_{it} \tag{2.16}$$

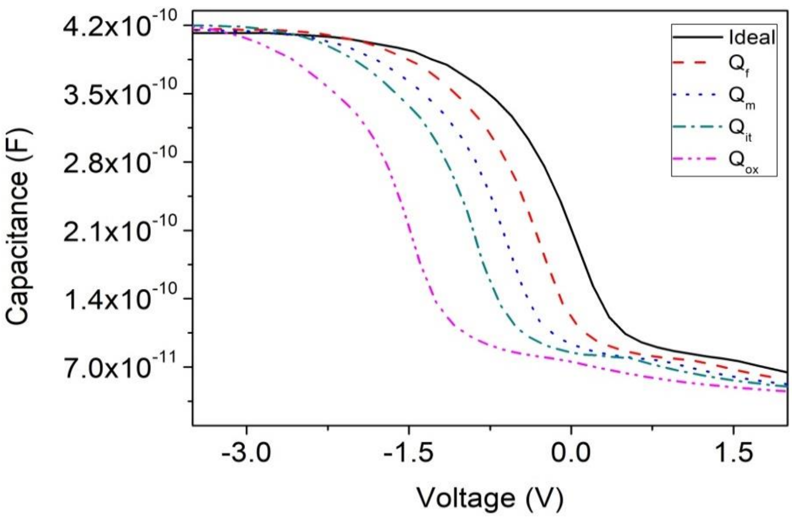


Figure 2. 10: Effect of the impurity charges on the high-frequency MOS capacitance curve.

2.3 NürFET Basis

2.3.1 General Introduction

NürFETs are the devices fabricated in Abant Izzet Baysal University Nuclear Radiation Detectors Research and Applications Center. The Nuclear Radiation Sensing Field Effect (NürFETs) transistors are discrete p-channel MOSFETs whose gate oxides of which are optimized to increase their radiation sensitivities (Ristic et al., 2011; Yilmaz et al., 2017). Hence basic operation principles are similar to p-channel MOSFETs.

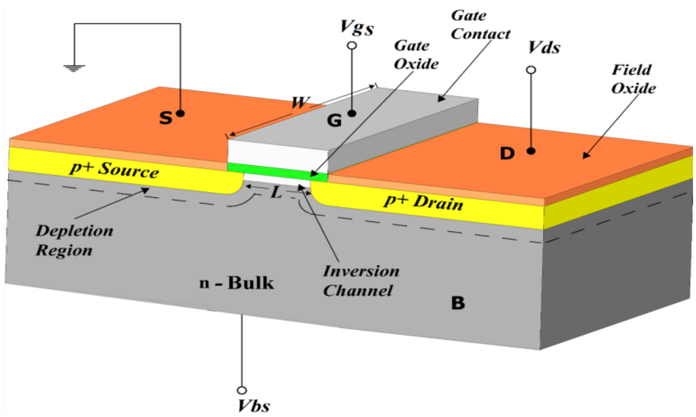
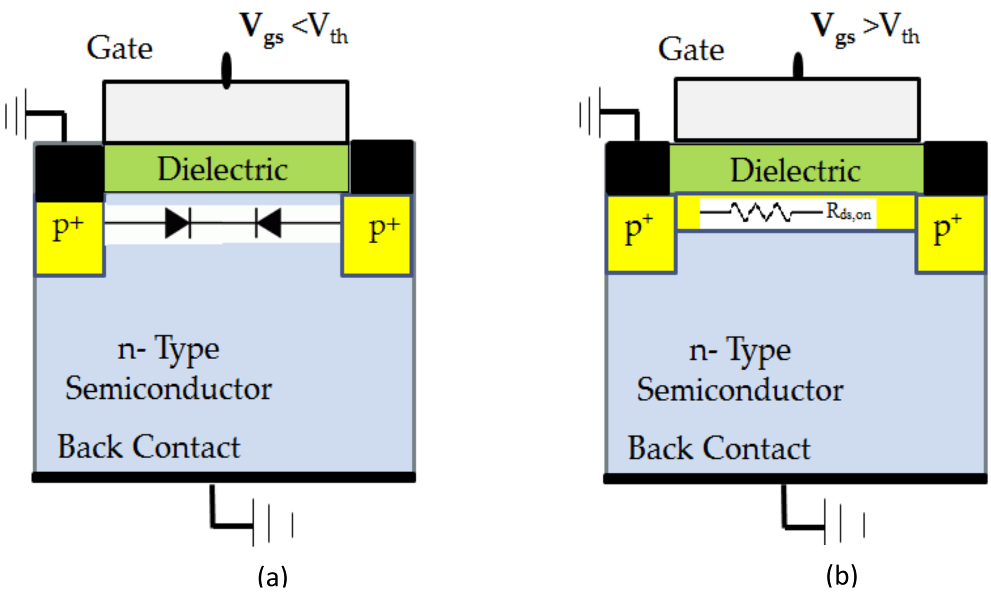


Figure 2.11: Schematic cross section of an inversion mode of p-channel MOSFET (Thomas, 2011).

The structure of MOSFET contains a MOS capacitor with doped source and drain regions. At enhancement mode (V_{gs} ~0), a p- channel MOSFET has a n- type semiconductor as substrate and p^+ source and drain regions formed by doping process. Schematic illustration of p- channel MOSFETs is depicted in Figure 2.11. When a lower voltage than threshold voltage ($V_{gs} < V_{th}$) applied to gate, no current flow occurs between the drain and source region even in existence of drain voltage (V_{ds}). In this mode, MOSFETs act like a two front-to-front pn junction. However, when $V_{gs} > V_{th}$, the semiconductor layer is inverted and a conduction channel below the gate dielectric is formed. In this mode, the current can flow from source to drain in the presence of V_{ds}. The rises in the gate voltage enhance the number of carriers in the inverted channels and allow more current flow (Thomas, 2011). The basic electronic configuration for these two modes is seen in Figure 2.12.



Figures 2.12: Electronic current flow mode for a-) $V_{gs} < V_{th}$, b-) $V_{gs} > V_{th}$ of p-channel MOSFETs (Thomas, 2011).

2.3.2 Basic Operation Modes of NürFET

2.3.2.1 Importance of Threshold Voltage

The threshold voltages are crucial for the operation of the MOSFETs, because current flow almost zero below the V_{th} values. As mentioned in the previous section, the MOSFETs act like a two pn junction (see Figure 2.12), hence, only diffusion current exists and its value is almost zero. When high V_{gs} above the V_{th} is applied to gate, MOSFET becomes current source and it start to contact current in the presence of any small voltage applied to drain-to source (V_{ds}). The V_{th} voltage was given in Eq. 2.11 including the impurity contributions which are Q_m, Q_f, Q_{it} and Q_{ox} inside V_{fb}. The initial V_{th} should be close to the theoretical values typically less than 1 V depending on the capacitance of gate dielectric. The larger values of V_{th} than ideal values basically indicate presence of high parasitic charge densities. Large V_{th} require the large power supply and this enhances the power consumption and heat generation during operation of ICs devices.

2.3.2.2 Drain Current in Linear (Triode) Region

Under sufficiently high gate voltages (V_{gs}> V_{th}), an inversion layer forms where current would flow. The higher V_{gs} enables stronger inversion, i.e., larger mobile carrier, and higher conduction between source and drain seen in Figure 2.13 (a). Under constant V_{gs} above the V_{th} value, the drain-source current is controlled by drain voltage (V_{ds}). For a small V_{ds} value, carriers start flowing from source to drain and inverted channels act as a resistor; thus, the drain current (I_{ds}) is proportional to V_{ds}. These I_{ds}- V_{ds} relations continue linearly and this region is called as Linear (Triode) Region as seen in Figure 2.13 (b). In the linear region, the V_{ds} is lower than saturation value of V_{ds} and drain current is proportional to inversion charge times velocity of carriers expressed as (Lee, 1996; Razavi, 2001);

$$I_{ds} = -WQ_{in}(y)V(y) \tag{2.17}$$

where W is the channel width and velocity defined as mobility (μ_p) times electric field (E), therefore (Razavi, 2001)

$$I_{ds} = -WQ_{in}(y)\mu_p E \tag{2.18}$$

Here charge density can be defined as $Q_{in}=C_{ox}(V_{gs}-V(y)-V_{th})$ and Eq. (2.18) becomes

$$I_{ds} = -WC_{ox}[V_{gs} - V(y) - V_{th}]\mu_p E \tag{2.19}$$

The electric field is correlated with negative gradient of voltage along the channel, hence (Razavi, 2001)

$$I_{ds} = WC_{ox}[V_{gs} - V(y) - V_{th}]\mu_p \frac{dV}{dy} \tag{2.20}$$

When we integrate the Eq. (2.20) between the channel boundaries (Razavi, 2001).

$$\int_0^L I_{ds} dy = \int_0^{V_{ds}} WC_{ox}[V_{gs} - V(y) - V_{th}]\mu_p dV \tag{2.21}$$

Solution of Eq. (2.21) give us the I_{ds} current as follows (Razavi, 2001);

$$I_{ds} = \mu_p C_{ox} \frac{W}{L}[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}] \tag{2.22}$$

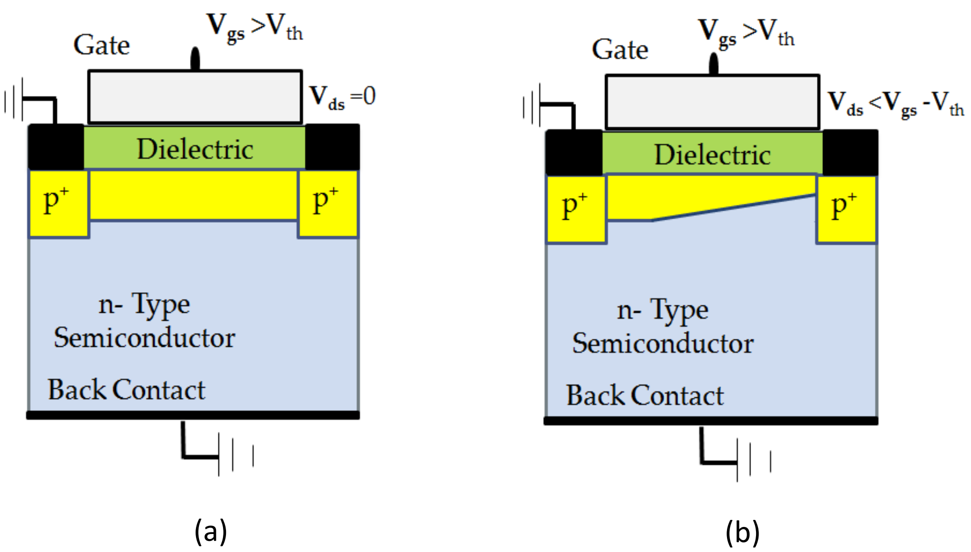
This relation is valid for linear region of I_{ds}- V_{ds} characteristics, i.e., relatively small values of V_{ds}. Hence, in this regime the MOSFETs behave like a voltage controlled resistors.

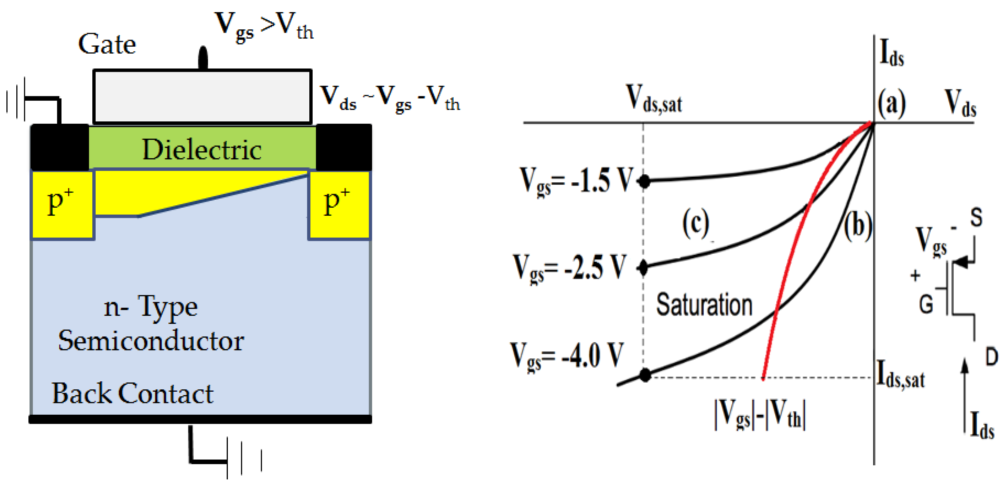
2.3.2.3 Drain Current in Saturation Region

Further increase in the V_{ds} beyond the linear region causes reduction in the inverted layer width near the drain region as seen in Figure 2.13 (c). This point is called as the pitch- off point. In this case, the cannel current remains almost constant further rise in the $V_{ds.}$ At pith-off point, $V_{ds}= V_{ds,sat}= V_{gs}-V_{th}$, $I_{ds}=I_{ds,sat}$ and Eq. (2.22) becomes (Razavi, 2001);

$$I_{ds,sat} = \mu_p C_{ox} \frac{W}{2L}(V_{gs} - V_{th})^2 \tag{2.23}$$

Therefore, in saturation the I_{ds} is directly related to square dependence of gate to source voltage (V_{gs}) and independent of drain voltages (V_{ds}) as seen in red curve in Figure 2.13 (d). The influence of variations on the V_{gs} at constant V_{ds} to I_{ds} and influence of variations on the V_{ds} at constant V_{gs} to I_{ds} incorporating to linear and saturation region are seen in Figure 2.13 (d).





(c) (d)

Figures 2.13: Schematic diagrams for both inversion layer p- channel MOSFETs, a-) V_{ds}=0, b-) V_{ds}< V_{gs}-V_{th}, c-) V_{ds}= V_{gs}-V_{th}, d-) typical I_{ds} curves depending on the V_{gs} and V_{ds} values given in a, b, c conditions (Razavi, 2001).

2.3.2.4 Transconductance Characteristics

Transconductance (g_m) can be defined as the ratio of the change in drain current to the change in the gate voltage. The transconductance of device can be found from the following relation (Razavi, 2001),

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{2.24}$$

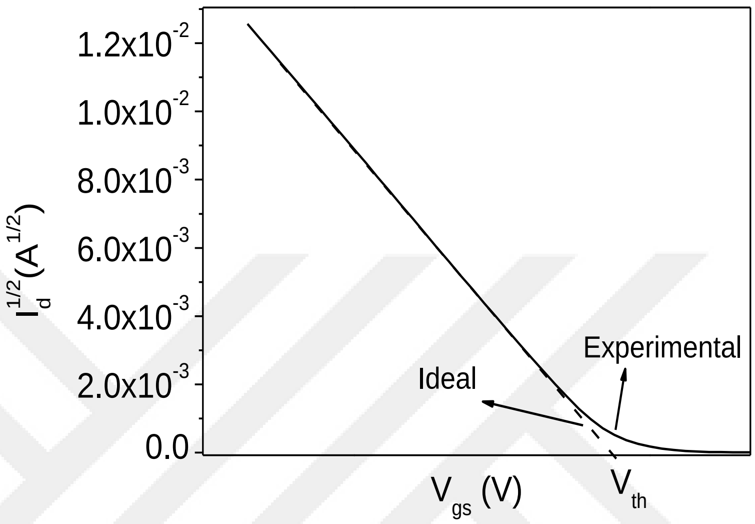
The g_m is important for specifying voltage gain in liner mode. However, the g_m value should be zero for the ideal MOSFET characteristics in saturation mode. For the real devices the g_m in saturation can be calculated by means of Eq. (2.23) and expressed as (Razavi, 2001);

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{W}{L}\mu_p C_{ox}(V_{gs} - V_{th}) \tag{2.25}$$

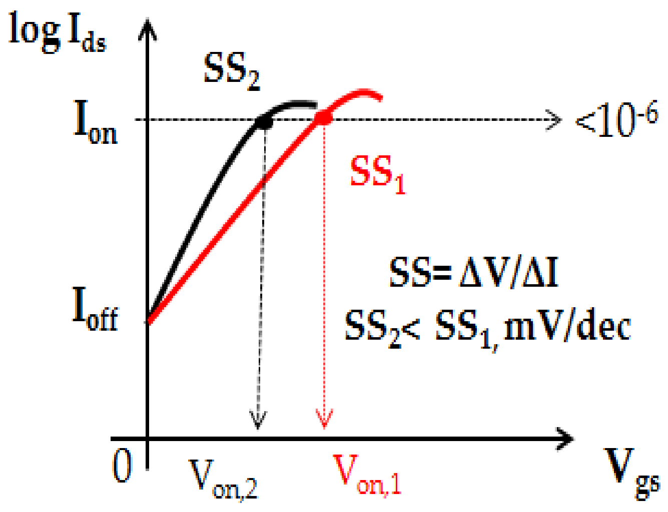
Hence, it can be conclude that g_m can be found by specifying the slope of I_{ds}- V_{gs} curve in the beyond the constant V_{ds} in saturation.

2.3.2.5 Sub-threshold Current

The drift current conduction mechanism is dominant for the current flow when the MOSFET is operated in the saturation as mentioned. However, dominant conduction mechanism is the diffusion of carriers for the V_{gs} just below the V_{th}. Hence, two different carrier flow mechanism exist for the I_{ds} current conduction. The basic conduction mechanism has been extensively explained in the previous sections for $V_{gs}>V_{th}$. Thus, the region called "sub-threshold" where is weakly inverted at $V_{gs}< V_{th}$ will be discussed in this section.



(a)



(b)

Figures 2.14: a-) sruare-root I_d curves for ideal and experimental measuremets, b-) enlargement of an experimental subthereshold region current below the V_{th} for two different slope value.

The ideal value of the drain current should be zero when gate voltage is below the V_{th} as seen ideal curve in Figure 2.14 (a). However, carriers do not disappear when gate voltage is lower than the V_{th}. Actually, the presence of minority carrier immigration occurs due to presence of PNP (NPN regimes) regimes when p channel (n channel) device is operating sub-threshold regimes (Lee, 1996). The drain current is proportional to exponential function (I_d ~ $\exp(qV_{gs}/nkT)$ in the sub-threshold regimes which can be seen experimental curve in Figure 2.14 (a). In the weak inversion regime specification of sub-threshold parameter, n, is expressed as (Kasap, 2006; Lee, 1996)

$$n = 1 + \frac{qN_{fs}}{C_{ox}} + \frac{C_b}{C_{ox}} \tag{2.26}$$

where N_{fs} is voltage- dependent surface state density, like interface traps, C_b is the depletion capacitance per unit area. Here voltage dependent surface state density is an important parameter for the sub threshold regimes. It typically varies between 2- 4 units, but may also change the fabrication process depending on the surface states.

The n parameter is directly proportional to thermal voltage in order to express the V_{gs} value which mark an arbitrary boundary between strong inversion (current proportional to square of V_{gs}) and weak inversion (current proportional to exponential function of V_{gs}). The boundary is called V_{on} expressed as (Lee, 1996);

$$V_{on} = V_{th} + n\frac{kT}{q} \tag{2.27-a}$$

The drain current at V_{on} is called I_{on}. This I_{on} current and V_{on} parameters are important because they are critical values to jump from sub threshold regime to strong inversion regimes. Because I_d current is proportional to exponential function, the semi-log plot of I_d below the I_{on} linearly change as seen in Figure 2.14 (b). Inverse slope of log (I_d)- V_{gs} characteristics in sub-threshold region is defined as sub-threshold swing (SS) which is function of n (Kasap, 2006).

$$SS = n\frac{kT}{q}\log(10) \tag{2.27-b}$$

This relation gives a factor ten change in drain current results for every 60n mV, ideally n=1 and SS= 60 mV/dec. In real devices SS values is higher than 60 mV/dec typically 70-80 mV/dec is really good for real devices. The small value of the SS is desirable for the microelectronic systems, especially, for digital electronics. As seen in Figure 2.14 (b), current drops more slowly for the higher value of SS. Lower SS (mV/dec) is required for low power consumption and low leakage below the V_{th}. This consideration is important for art-of- state scale area, where small leakage current in off devices degrades the total processor current, e.g., 10 pA sub threshold current for per MOS devices in one billion transistor causes totally 1A in off states (De and Osburn, 1999).

2.3.2.6 Channel Mobility

The mobility can be defined as an ability of the carriers' respond to external electric field. The MOSFET's performance is generally evaluated by I_d in saturation. The I_d in saturation is directly proportional to channel mobility of carriers denoted by μ_p for hole, μ_n for electrons as seen in Eq. 2.23. The bulk mobility of the Si is 480 cm^{-2}/V at $N_a=10^{16}$ cm^{-3} doping density for hole carriers, and 1430 cm^{-2}/V at $N_d=10^{16}$ cm^{-3} doping density for electron carriers (Zhu, 2008). However, mobility of the carriers near the interface is lower than bulk due to several scattering mechanism. Since MOSFETs start conduction in saturation mode, the basic scattering effects to inversion carriers are given following (Chaudhry, 2013);

Coulomb Scattering (μ_c): Depending on the fabrication process, various charged impurities are localized close the dielectric/ semiconductor interface. These charged impurities such as ionized impurity (doping concentration amount) at substrate, interface states, fixed charges may scatter the carriers in the inversion layer via Coulomb force. This Coulomb force is proportional to the impurity concentration at surface where inversion layer occurs and it is dominant mechanism when inversion carrier density is low or high depending on channel doping (Hu and Liu, 2011).

Phonon Scattering (μ_{ph}): Presence of vibration in the lattice of substrate at dielectric/semiconductor interface, bulk lattice vibration under external electric field and temperature causes lattice phonon scattering. This scattering mechanism becomes dominant in the intermediate transverse electric field (Hu and Liu, 2011).

Surface Roughness Scattering (μ_{sr}): Any discontinuity and deviation from an abrupt dielectric/ Si interface where inversion carriers are located cause extra quantum well. The rms value of dielectric/ Si interface and correlation length of oscillations in the surface should be small in order to decrease roughness scattering effects.

Considering these scattering mechanism, the effective surface mobility, $\mu_{s,}$ can be calculated by Matthiessens' rule expressed as;

$$\frac{1}{\mu_s} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{2.28}$$

2.3.3 Parameters Causes Deviations from Ideal FET Characteristics

Non-idealities in the MOSFET naturally degrade the device performance. The important non-idealities are the presence of trap sites and trapped charges in the dielectric and its interface underlying semiconductors. These impurities and their influences have been mentioned in the previous section (see 2.2.3 Impurities in the MOS structures). Together with the impurity tarp and charge influences, some other non-idealities come from design and operation of the MOSFETs which may also deviate the ideal device characteristics. The important non-idealities are explained below (Arora, 1993; Chen, 2005; Lee, 1996; Razavi, 2001);

Short Channel Effect: Due to scaling of the device geometries, influence of the applied electric field becomes important. Above the "pinch- off" voltage, explained in section 2.3.2.2 Drain Current in Saturation Region, the inverted the channel length reduces by a value ΔL seen in Figure 2.15 (a). The variations on the ΔL can be attributed to high electric field generated by V_{ds} Thus, the expression for drain current in Eq. (2.23) becomes at $V_{d,sat}< V_{ds}$;

$$I_{ds,sat} = \mu_p C_{ox} \frac{W}{2(L-\Delta L)} (V_{gs} - V_{th})^2 \tag{2.29}$$

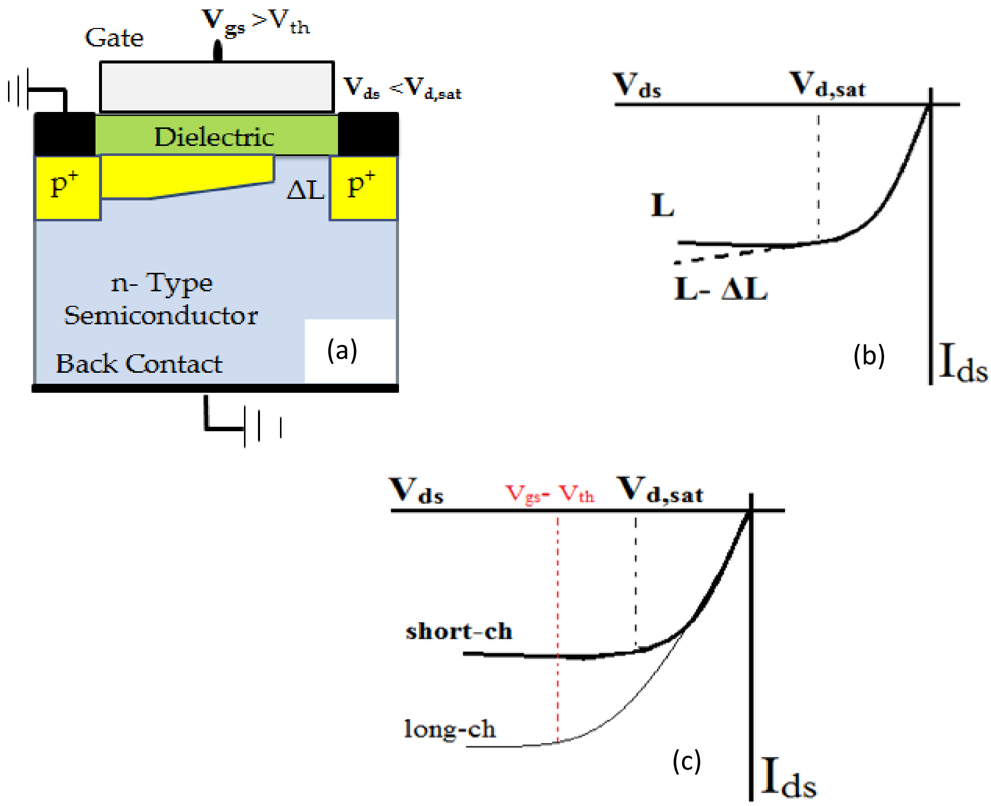
Due to ΔL< L, the Eq. (2.29) become

$$I_{ds,sat} = \mu_p C_{ox} \frac{W}{2L} (V_{gs} - V_{th})^2 (1 + \frac{\Delta L}{L}) \tag{2.30}$$

Fraction of the channel that is pinched off linearly depends on V_{ds} because the voltage across the pinch-off region is (V_{ds}-$V_{d,sat}$). Hence, ΔL/L= κV_{ds} where κ is the channel-length modulation parameter. Thus Eq. (2.30) becomes (Chen, 2005);

$$I_{ds,sat} = \mu_p C_{ox} \frac{W}{2L} (V_{gs} - V_{th})^2 (1 + \kappa V_{ds}) \tag{2.31}$$

This short channel effects cause channel modulation result in the dependence of drain current on V_{ds} even above the saturation. This influence in the drain current can be seen in Figure. 2.15 (b). On the other hand, carrier velocity is not enhanced with applied electric field, and mobility degrades in saturation regime because of scattering by the vertical electric field. This leads to earlier saturation of I_{ds} results in the low I_{ds} current as seen in Figure 15 (c). Another short channel influence is the reduction of the threshold voltages. Overlapping source and drain depletion become significant effect. This causes the depletion region under inversion layer to increase. The wide depletion region enhances the surface potential, thus this decreases the required V_{th} value of the device to form saturation regimes. This effect is also known as drain-induced barrier lowering (DIBL). In order to reduce DIBL under high drain electric field, lightly doped drain regime has been used in the state-of-the- art MOS devices.



Figures 2.15: a-) short in the channel due to high drain voltage, b-) influences of channel short in the I_{ds} characteristics, c-) I_{ds} degradation due to saturation velocity in short channel (Chen, 2005).

Substrate current: The dramatic increase near the drain region beyond the saturation V_{ds}, carriers gain high energy between scattering events to cause impact ionization upon following collision which are especially observed for short channel devices. These hot carriers generate additional e-h pairs. Generated electrons are gathered in substrate, while holes contribute to the I_{ds} in p- channel MOS devices. This substrate current is proportional to V_{ds} beyond the strong inversion and contributes the conductance term of device. The highest influence of these additional conductance become problems for one who requires minimum output conductance at high V_{ds}.

Gate current: This gate current is produced by hot carriers formed under high electric field. The hot carriers may move along the gate dielectric either creating the new trap states or hoping mechanism. Hence, it degrades the electrical performance of devices. On the other hand this movement is sometimes useful for devices used in non-volatile memories but reduces the long term reliability.

Back gate (body) effect: The V_{th} value of the devices is also affected by the voltage applied from back contact. The applied voltage difference between the source and the bulk, V_{bs}, changes the depletion layer width which causes difference in the threshold voltage. Hence, Eq. (2.11) becomes for p- channel MOS device (Arora, 1993);

$$V_{th,bs} = V_{th} + \gamma(\sqrt{2\phi_b + V_{bs}} - \sqrt{2\phi_b} \tag{2.32}$$

$$\gamma = \frac{\sqrt{2qN_a\varepsilon_s}}{C_{ox}} \tag{2.33}$$

where γ is the body effect parameter. As seen in Eq. (2.33), body effect can be controlled by doping concentration of semiconductor and dielectric layer capacitance. In order to control the bulk effect, generally bulk terminal is directly connected to source during the device operations.

Temperature effect: Two important influences exist for the MOS transistor characteristics. The threshold voltage of the devices can be varied by temperature approximately from -1 to - 3 $mV/^0C$. In addition, the mobility of the carriers decreases with increasing the operation temperature of the devices.

3. RADIATION EFFECT ON MOS STRUCTURE

3.1 Radiation Interaction with Matter

Any electromagnetic waves or energetic particle that can have enough energy to create ion pairs by interaction with matter is called as ionizing radiation. The ionizing radiation can interact with materials in several ways depending on its type, energy, charge, density of target material, etc (Knoll, 2000). Basically, radiation interacts with materials in two ways. Charged particles, like beta or alpha particles having sufficient kinetic energy, directly interact with atoms and molecules to create electrons hole pairs and free radicals. This process is known as direct ionization due to no intermediary step required. On the other hand, non-charged particles such as photons and neutrons interact with atoms and molecules release charged particles and this charged particles cause ionization in the matter by direct mechanism. This process is called indirect ionization. The details of the radiation interaction mechanism are explained below.

3.1.1 Charged Particle Irradiation Interaction with Matter:

The charged particle irradiation is a particle with an electric charge and has enough energy to cause ionization in the matter. Beta, proton, alpha and heavy ion irradiation are the most common charged particle irradiations. These kinds of particles are mainly lose/ transfer their energies with Coulomb attraction and/or repulsion with electrons of target materials.

The interaction probability of these charged particles with matter and the traveling range inside the materials is directly connected with magnification of its charge and energy (Knoll, 2000). For the proton and non-relativistic nuclei, ionizing density inversely is correlated to their energy declining with range and is proportional to square of their charge. They interact with Coulomb scattering which can induce ionization for proton with energy less than 100 keV. Excitation or displacement can occur and collision with nuclei and nuclear reaction may also occur energies higher than 10 MeV. On the other hand, charged particles having lower mass such as electron and beta irradiation are much more feebly than heavy-ion radiation. In addition to coulomb interaction, when electrons decelerate in the target material, they also lose energy by emitting Bremsstrahlung in form of X-ray.

3.1.2 Neutral Particles and Electromagnetic Irradiation Interaction with Matter

Neutron is the excellent example for un-charged particle radiation which has almost the same mass with protons. Thanks to their neutrality, neutrons cannot exhibit electrostatic interactions with materials; hence, they move in straight line until they actually collide with a nucleus to be scattered into a new direction or absorbed. Neutron can interact with materials basically in three ways. A first interaction type is nuclear reaction. When indecent neutrons are absorbed by target, the secondary particles or electromagnetic radiation, e.g., protons, gamma rays can be emitted. Elastic scattering is the second type of the interaction with matter. When neutrons collide with target nucleus, they transfer some amount of their energy and continue their path. If sufficient energy is transferred to target atom, nucleus of target materials may be displaced as ionization nuclear displacements. In elastic collision is the last important interaction type with matter. In inelastic collision, neutrons are captured by target material having relatively high atomic number of nucleus (Z) and re-emitted by target nuclease together with gamma radiation. Interaction types are correlated with the energy of neutrons. Generally, slow neutrons interact with target materials via nuclear reactions or elastic collisions, fast neutrons basically interact via elastic collisions. Also inelastic collisions dominate for extremely energetic neutrons. Another neutral radiation type is photon radiation which is actually electromagnetic wave is classified by its energy. The X-rays having energies from 100 eV to 100 keV and gamma-rays having energies from few hundred keV to a few MeV are two important photon types for the nuclear physics applications. The ionizing photon radiation interaction with target materials can be classified in three phenomena. The first interaction type is photoelectric effects. The indecent photon emits or ejects electrons from the target materials by losing all their energies. The ejected electrons come back their ground states by emitting low energy photon that can also interact with target materials. Compton scattering is the second interaction phoneme. In this phoneme, indecent photon hits the target materials and loses its energy and it emits free electron and energetic photons. The last interaction type is pair production. The indecent photons completely lose their energy creating electron-positron pairs. The positron combines with an electron. Result of this annihilation of the positron two new photons is created.

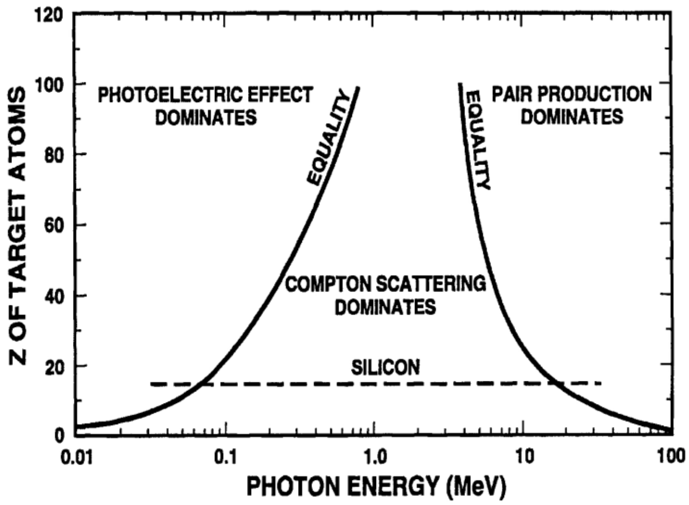
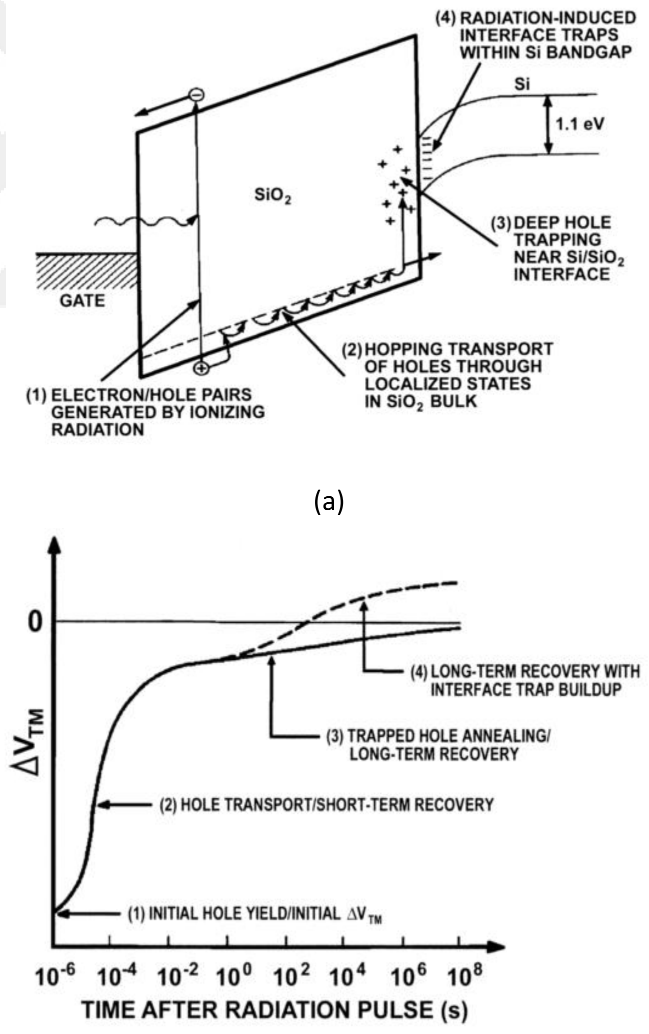


Figure 3.1: The dominant photon- matter interaction mechanism depending on incident photon energy and atomic number of target materials (Ma and Dressendorfer, 1989).

These photons may also interact with target materials (Knoll, 2000). The pair production can occur when photons have energies higher than 1.024 MeV, but to be dominant interaction mechanism the energy of the incident photon should be much higher than 1.024 MeV. All these types of interaction can be observed when materials are exposed to ionizing radiation, especially, for higher energies. However, depending on the indecent photon energy one or two phoneme dominates the basic interaction phoneme that occurs inside the material under radiation exposure. The dominant interaction phoneme depending on the atomic number of the target material and incident photon energies can be seen in Figure 3.1.

3.2 Radiation Degradation on MOS Structure

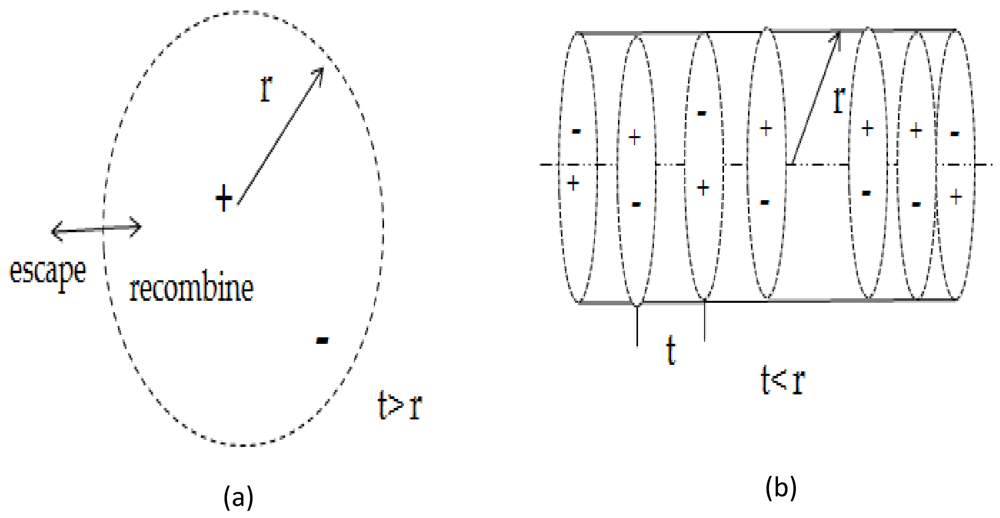
Ionizing radiation interactions with material via Compton scattering, Coulomb interaction etc. cause ionization on the target material. Enormous number of electron- hole pairs and new trap centers were generated in dielectric as result in the ionization and its interface with underlying semiconductor. Four major physical processes have been observed in the radiation responses of MOS structure. Each of these physical effects under positive voltage is applied to the gate, is illustrated in Figure 3.2 (a) and the degradation of these physical effects on the V_{th} is illustrated in Figure 3.2 (b). This physical mechanism is developed for the MOSFET having SiO_2 gate dielectric. More studies should be performed to specify radiation response of high-k materials and possible differences between SiO_2 and high-k materials (Aktag et al., 2010; Ergin et al., 2010; Yilmaz et al., 2008), but the radiation response of SiO_2 based on dielectric is going to be explained in this section to understand fundamental physical interaction phoneme. The gate dielectric layer is known to be most sensitive part of the MOS based device. The usability of the MOS device in radiation environment as a dosimeter or hard materials is determined by response of dielectric layers (Kahraman et al., 2015a; Ma and Dressendorfer, 1989; Oldham and McLean, 2003; Ristic et al., 2011; Tsui et al., 2013). When radiation passes through the dielectric layer, a large number of e-h pairs are created depending on radiation energy and interaction mechanism. Mobility of electrons in SiO_2 is 20 $cm^2V^{-1}s^{-1}$ at room temperature, while it is 40 cm^2 $V^{-1}s^{-1}$ at lower temperatures (Ma and Dressendorfer, 1989). However, hole mobility is always smaller than holes and typically varied from 10^{-4} cm^2 V^{-1} s^{-1} to 10^{-11} cm^2 V^{-1} s^{-1}depending on field, temperature etc (Ma and Dressendorfer, 1989). Hence, holes are almost immobile compared to electrons and electrons easily swept out from gate electrode in few picoseconds after generation by irradiation as seen in first steps of Figure 3.2 (a). However, large amount of the generated e-h pairs recombine with each other in a picosecond. Initial generated e-h- pairs cause significant shift to V_{th} and are demonstrated in first step of Figure 3.2 (b). The numbers of holes which are escape from initial recombination, move toward close the interface between SiO_2/Si where deep traps are located by hoping between the shallow states seen in the second step of Figure 3.2 (a). This mechanism is sensitive to the oxide processing, applied electric field and ambient temperature. Typically this movement takes less than 1 second at room temperature (Oldham and McLean, 2003). In addition, some of mobile holes can be recombining with electrons during their movement and this cause short time recovering. The contribution of this short time recovering to V_{th} can be seen in the second step of Figure 3.2 (b). When the mobile holes approach to Si interface typically few nm far from interface, some fraction of them fall into deep traps, seen in the third steps of Figure 3.2 (a), where they can be trapped in few years or may be more. These trapped holes cause remnant threshold voltage shift which are illustrated in the third step of Figure 3.2 (b). These trapped holes can be treated by high temperature annealing (Yilmaz and Turan, 2008). Last physical phoneme is the radiation - induced buildup of interface traps localized at the SiO_2/ Si interface as seen in the fourth step of Figure 3.2 (a). The radiation generated holes or electrons can be trapped in acceptor or donor like interface states as explained in the previous sections in details. The accumulation of the trapped charge at interface also cause the positive or negative shift in V_{th} as seen in fourth step of Figure 3.2 (b). The general physical phoneme for the radiation response of the MOS based devices has been explained. In order to clarify basic physical mechanisms of radiation responses of the MOS devices the following sub-titles should be also explained;



Figures 3.2: a-) Schematic of physical radiation interaction mechanism, and b-) its influence the threshold voltages (Oldham and McLean, 2003).

3.2.1 Initial Recombination/Initial Hole Yield

The initial threshold voltage shift is directly related to the initial created hole yields in the dielectric structure. The magnitude of the initial shift depends on the e-h pair creation energy and field dependent holes escape from initial recombination. The fabrication parameters i.e., dielectric type, thickness of dielectric, device geometry, exposed dose, etc. are also some other important parameters, but e-h pair creation energy and field dependent holes escape from initial recombination have prime effect and they should be explained in details. The e-h pair creation energy is related to the bonding structure of the materials including the band gap energies. It is 18 eV for the conventional SiO_2 dielectrics (Ausman and Mclean, 1975) and 9.8 eV for $PbCl_2$ (Kitaura et al., 2003). It is seen that the pair creation energy of the materials is roughly proportional to double times of the band gap energy of material.

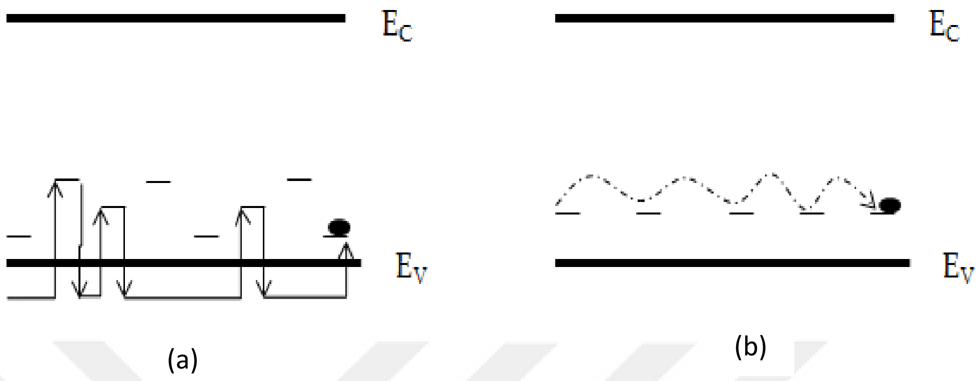


Figures 3. 3: a-) separated electron hole pairs (geminate), b-) overlapping e-h pairs (columnar) recombination model, where r is the thermalization distance that e-h recombine below it and t is the average charge pair separation distance (Ma and Dressendorfer, 1989).

A large number of e-h pairs are created after radiation interaction with dielectric layer, but this initial density is reduced by initial recombination just before the electrons swept out from gate in picoseconds. The number of the final hole yields that cause the V_{th} shift in long time is proportional to the magnitude of the electric field in the dielectric and initial line density of e-h created by indecent radiation. The pair line density can be determined by linear energy transfer (LET) and it is a function of incident particle type and energy but it is inversely proportional to average separation distance between electron and hole. This means that close average separation distance of pair causes more recombination and this decrease the number of final hole yields. Models for the separation distance can be seen in Figures 3.3 (a) and (b). In the germinate model, the separation distance, t, of isolated single charge pairs is higher than thermalization distance, r, where e-h pair easily recombine, thanks to Coulomb interaction. On the other hand, if average pair separation distance is less than thermalization distance columnar recombination can be observed. Here the e-h pairs lose their identity and recombination occurs between electrons and holes lying track under cylindrical distribution around track. Here recombination probability is much higher than germinate model due to recombination encounters between opposite charges. These two model work successfully depending on the pair separation distance. For instance, low-LET particles, like beta radiation or secondary electron come from Compton scattering, create discontinuous charge pairs in its path, e.g., average separation distance is 50 nm for 1 MeV electron radiation, hence germinate model is valid. On the other hand, for high- LET particles like proton and alpha particle, they create high density of pair along their path, e.g., average separation distance is 0.3 nm for 1 MeV proton radiation; hence, columnar model gives more appropriative results. It should be noted that when electron hole density enhances, columnar model behavior becomes more convenient. It is also important to note that fraction of hole yield is associated with particle source. For examples, yield fraction varied from 90 percent for low- LET particles (12 MeV electron and Co-60 gamma radiation) to 6 percent for the high LET particles (2 MeV alpha radiation) at constant applied electric field (Oldham, 1999). Hence, different sources may cause variations on the radiation responses of MOS devices.

3.2.2 Hole Transport/ Short Time Recovery

Two types of hole transport mechanisms are basically expected by researchers. The first transport mechanism is described as carriers move in shallow trap states in extended band. The localized states are distributed in energy range and exhibit large fluctuations in the thermal release rates from trap states; thus, the fluctuations are temperature dependent. The second transport mechanism is described as hopping transport where carriers move directly between localized trap sites via phonon- assisted tunneling (Ma and Dressendorfer, 1989). In addition to hoping transport mechanism is temperature dependent, the hopping distance is also important for the hoping hole transport. The transport models are schematically illustrated in Figure 3.4.



Figures 3.4: Hole transport mechanism a-) trap modulated transport, b-) hoping transport between localized states via tunneling (Ma and Dressendorfer, 1989).

The small polaron hopping of the holes, seen in Figure 3.4 (b), between localized shallow trap states having a random spatial distribution is more popular hole transport mechanism for the movement of the generated holes toward the interface (Oldham and McLean, 2003). The transport of holes in the dielectric layer is responsible for the short time recovery. The hole transport mechanism and short time recovery have also following specifications; i- Hole movement is dispersive, it may take many decades just after radiation exposure. ii- Any small changes in temperature, applied field, dielectric thickness do not cause variations in the recovery curve. These variances only influence the time scale of the curve. iii- The transport is field and strongly temperature activated. iv- The hole transport and/or recovery time has a strong linear power law dependence on dielectric thickness (Oldham and McLean, 2003).

3.2.3 Dose rate effects

The changes can be observed in the MOS device parameters with time after radiation exposures. Hence, non-linear dependencies in the total dose accumulated at different dose rates can be observed due to long term interface traps build up and rebound effect. Researchers have reported that the device responses with different dose rate under same total exposed doses exhibit different sensitivities. They have demonstrated that at higher dose rate V_{th} shifts to negative, while it was positive at lower dose rate. These differences caused by reduction of the trapped oxide charges at lower dose rates due to tunnel annealing and increase in the interface trap charges due to long term build- up of interface traps. However, at the intermediate dose rates, the dependence on dose rate the sensitivity can be small. On the other hand, at higher dose rates (higher than few kilo-rads in second), the presence of electric field due to generated holes may degrade the electric field of dielectric layer. These generated charges may cause reduction on the internal electric field resulting in enhancement of the recombination effect. Hence less radiation damage can be observed compared to low dose rates (Ma and Dressendorfer, 1989). As it can be understood, dose rate dependencies can be different for the devices, even in same circuit. The parameter variations on the devices should be carefully considered to make accurate analysis.

3.2.4 Effects on Other Transistor Parameters

Radiation influences exhibit variation depending on several device parameters; hence, the parameters effects should be investigated in details in order to understand radiation induced effects on the MOS transistors. Before explain the parameters' influences in this section, it should be noted that these parameters' influences are valid for SiO_2 based MOS transistor. Hence, the parameters variation can give different result for different gate dielectrics.

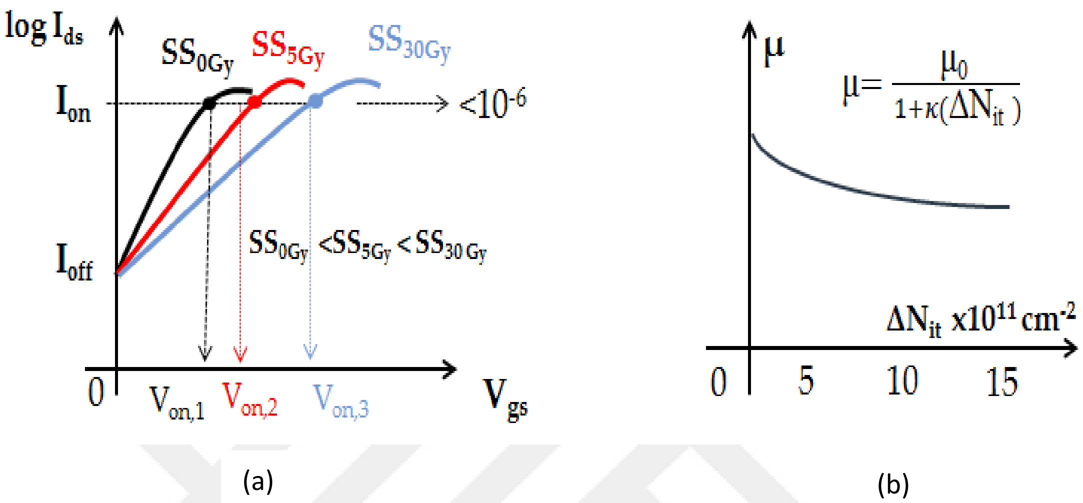
Gate Voltage Influences: The most observable radiation effects are variations on the V_{th} value of the MOS transistor due to accumulation of the trapped charges in device structure. When the voltages have been applied to gate electrode, it directly influences the number of generated e-h densities and magnitude of initial recombination. Minimum threshold voltage shifts have been observed when the gate voltage is equal to flat band voltage of the MOS transistor in which internal electric field is equal to zero. This minimum threshold voltage shift is due to large number of generated e-h pair recombination. On the other hand, when positive voltage is applied to gate, the large V_{th} shifts have been observed than the negative applied voltages. Under positive electric field large numbers of holes are move toward SiO_2/Si interface where deep oxide traps are located. Hence, positive voltage applied to gate electrode cause the higher voltage shift than negative applied voltage. On the other hand, the minimum V_{th} shift is observed, when magnitude of flatband voltage is applied to gate electrode (Ma and Dressendorfer, 1989).

Sub-threshold Influence: As mentioned in the previous sections, the sub-threshold characteristics of devices strictly depend on the surface state densities including the interface trap. The generation of the traps where especially located at the interface causes rise in the leakage current between off states and on states operation. As seen in Figure 3.5 (a), the SS value is enhanced with irradiation doses which cause current drops slowly and enhance the leakage. These variations have crucial influences on the performance of the integrated circuits.

Mobility Influence: The mobility of the carriers in the channel is degraded with increasing irradiation doses. The influence of irradiation on the channel mobility is seen in Figure 3.5 (b). As seen from figures, the rises in the interface state density decrease the channel mobility. The mobility degradation is associated with rise in the impurity scattering due to generated new trap centers at the interface where is very close to the channel. On the other hand, the degradation of the mobility reduces the current drive capability of the MOS transistors (Ma and Dressendorfer, 1989).

Degradation of Surface Recombination Velocity: The surface recombination velocity may be increased with the generation of the interface tarps by irradiation. This leads to large surface generation current where semiconductor surfaces were passivized with dielectric layer. Hence junction leakage current may enhance with irradiation exposure.

Geometric Effects: The geometry and device design can change the radiation response of the MOS transistors. Firstly, it is known that the thick gate dielectric layers trap more charges. Hence, the radiation sensitivity of the device is enhanced with enhancing the gate dielectric thickness. In addition, the variations on the channel length may also influence the radiation responses of the MOS transistors. Although it is known that channel lengths influence the device response, the net contribution to the device sensitivity is not clear. Some studies have reported that the smaller threshold voltage shift occurs after channel length decrease, while other studies have been reported that the threshold voltage shift is enhanced with decreasing the channel length for exposed doses (Ma and Dressendorfer, 1989). These differences are possibly due to different fabrication conditions (annealing environment, substrate/channel doping level etc.) and variance in the internal electric field in the device structure. However, the rise in the threshold voltage shift for shorter channel length is more expected result. Because of enhanced charge build- up in the field oxide at the edge of channel relative to that in the gate dielectric, fringing field should be large influence in the smaller channel length up to a limit (Ma and Dressendorfer, 1989).



Figures 3.5: Radiation influence on a-) sub- threshold characteristics, and b- mobility of carriers (Ma and Dressendorfer, 1989; Oldham, 1999).

3.3 Theory of the Radiation Induced Traps

Understanding the basic charge generation and trapping mechanism under irradiation influence on the dielectric and its interface with underlying semiconductor is important for the device reliability. The possible radiation induced trap generation mechanism has been created for SiO_2/Si gate stack. The possible bonds between Si and O are given in Figures 3.6 (a)- (d). In Figure 3.6 (a) the SiO_4 bonds, (b) Si_2O configuration, (c) two structural non-strained/strained Si-O bonds and (d) Si-O bonds in the vacancy on the oxygen have been demonstrated. A bond distance, t, between O and Si in the SiO_2 bonds varies from 1.52- 1.69 Angstrom and the angle θ varies from 120 to 180 degree. For the non- strained SiO_2 bonds the t and θ are equal to 1.62 A and 109^0, respectively (Ristic, 2008).

3.3.1 Defect Generated by Secondary Electrons in Impact Ionization Process

When radiation passes through the dielectric/semiconductor, it interacts with electrons of the materials (breaks bonds of the materials) mainly via Compton Scattering for the gamma irradiation. These interactions release secondary electrons and holes. For the conventional SiO_2/Si interface, these released electrons, which are highly energetic, travel in the SiO_2/Si structure until they recombine or leave the device by losing their kinetic energy through collision with other secondary electrons or bonded electrons of Si_0-O and Si_0-Si_0 in the oxide. Here, the index "$_0$" is used for bonds in oxide. The collision of one secondary electron with bonds in the oxide can break lot of covalent bond in the oxide layer (SiO_2), and generate the new secondary electrons and new trap centers where mobile carriers can be trapped. Hence, the secondary electron degradation has mare important role in bond breaking phoneme than energetic photon. In addition, interaction probability of charge particle with dielectric materials is much higher than photon radiation (Oldham and McLean, 2003) which also enhance the bond breaking probability of the secondary electron irradiation. Some basic bond breaking mechanisms are explained as following;

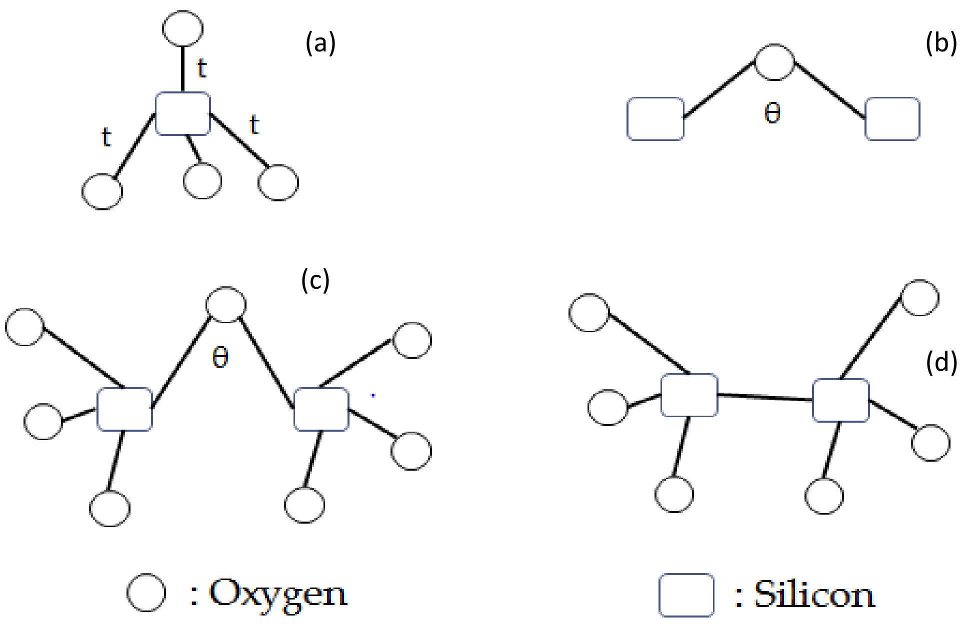


Figure 3.6: Schematic between a-) SiO_4, b-) Si_2O, c-) Two structural units of Si-O bonds and d-) an oxygen vacancy bonds (Ristic, 2008).

When non-strained Si-O bonds, (see Figure 3.6 (c)) $\equiv Si_0 - O - Si_0 \equiv$, interact with secondary electrons following reactions occur

$$\equiv Si_0 - O - Si_0 \equiv \xrightarrow{e-} \equiv Si_0 - O^{\bullet} + {}^{+}Si_0 \equiv +2e^{-} \tag{3.1- a}$$

$$\equiv Si_0 - O - Si_0 \equiv \xrightarrow{e-} \equiv Si_0 - O^{+} + {}^{\bullet}Si_0 \equiv +2e^{-} \tag{3.1-b}$$

where ≡ indicates three Si_0-O bonds, Si_0 is the Si bonds in oxide and $^{\bullet}$ is the unpaired/uncoupled electron. The reaction probability of the $\equiv Si_0 - O^{\bullet}\,{}^{+}Si_0 \equiv$ is higher than $\equiv Si_0 - O^{+}\,{}^{\bullet}Si_0 \equiv$, since these are numerous centers. The trap center in Eq. 3.1-a is energetically very shallow and they are forming the temporary hole centers (Ristic, 2008). On the other hand, approaching the interface between oxide and semiconductor but located at the oxide side, the strained Si-O bonds can be easily broken usually generating the amphoteric non-bridging-oxygen (NBO) centers which are $\equiv Si_0 - O^{\bullet}$ and positively charged E' centers, and $\equiv Si_0^{\;+}$ known as E_s' centers generated same degradation mechanism as Eq. 3.1-b. At NBO centers holes and electrons can be trapped, that could be negatively charged than positively by trapping the electrons.

$$\equiv Si_0 - O^{\bullet} + e^{-} \rightarrow \equiv Si_0 - O^{-} \tag{3.2}$$

These NBO centers are energetically deeper which is the main precursor of the negatively charge trap in the oxide and interface. The secondary electron radiation may also interact with strained oxygen vacancy bonds, (seen Figure 3.6-d), and brakes this bond by ejecting their electrons and form the E_γ' centers

$$\equiv Si_0 - Si_0 \equiv \xrightarrow{e-} \equiv Si_0^{\;+} + {}^{\bullet}\,Si_0 \equiv +2e^{-} \tag{3.3}$$

In the presence of the oxygen mono vacancy, a hole can be trapped. The oxygen vacancy bonds are distributed in the vicinity of the interface. These above mentioned reactions can occur anywhere of the SiO_2/Si gate stack. In the created defect centers both electrons and holes can be trapped but the probability of the hole trap is much more higher than the electron traps because three types of the trap centers may capture the holes which are E_γ', E_s' and NBO (Ristic, 2008). These trapping centers are valid for the SiO_2/Si gate stack, for the high-k interface additional trapping centers can be formed and the probability of charge trapping types can change.

3.3.2 Defect Generated by Hole

During the motion of the hole toward the SiO_2/Si interface, the holes can also react to the weak bonds, especially, hydrogen passivized dangling bonds and the following reactions occur;

$$\equiv Si_0 - H + h^+ \rightarrow \equiv Si_0^{\bullet} + H^+ \tag{3.4-a}$$

$$\equiv Si_0 - H + h^+ \rightarrow \equiv Si_0^{+} + H^0 \tag{3.4-b}$$

$$\equiv Si_0 - OH + h^+ \rightarrow \equiv Si_0 - O^{\bullet} + H^+ \tag{3.4-c}$$

$$\equiv Si_0 - OH + h^+ \rightarrow \equiv Si_0 - O^{+} + H^0 \tag{3.4-d}$$

The secondary electron radiation can also interact with similarly, but these mechanisms are not really important for the secondary electron radiation since the number of interface defect generation is significantly less than the defect generation in the oxide reaction given in Eq. 3.3 and 3.4. The holes have not ability to break non-strained Si-O bond; thus, the reactions given in Eq. 3.4 (a)- (d) are important for holes which take part in defect generated at particularly SiO_2/Si interface. The amount of these H- dependent bonds depends on the annealing environment and the interface trap generation mechanism will be described in the next section.

The holes cannot break the non- strained Si-O but they have ability to break strained Si-O and strained oxygen vacancy bonds. The strained bond breaking mechanisms of holes are given in the following;

$$\equiv Si_0 - Si_0 \equiv + h \rightarrow \equiv Si_0^{\bullet} + \equiv Si_0^{+} \tag{3.5-a}$$

$$\equiv Si_0 - O - Si_0 \equiv + h \rightarrow \equiv Si_0 - O^{\bullet} + \equiv Si_0^{+} \tag{3.5-b}$$

Due to the occurred reaction in Eq. 3.5 (a) and (a), the new E_{γ}’, E_s’ and NBO trap centers have been generated. It is important to note that energetic levels of defect centers (E_{γ}’, E_s’ and NBO) generated by holes can exhibit different charge trap behaviors. Depending on the bond structure, e.g., localized energy levels in the band gap, angles and distances between the surrounding atoms, chemically identical defects may exhibit different behaviors. These defects can be positive, negative and also neutral. The holes traps at strained oxygen vacancy bonds are special trap centers, which are basically expected as slow switching oxide traps, that exhibits switching electric field annealing. They may capture and emit electron from dangling Si orbitals without changing the structure of the hole part of the Si_0^+ defect. This compensation and reverse annealing process can be given as

$$\equiv Si_0^{+\bullet} Si_0 \equiv + e^- \rightarrow \equiv Si_0^{+-} Si_0 \qquad (3.6\text{-a})$$

$$\equiv Si_0^{+-} Si_0 \equiv \rightarrow \equiv Si_0^{+\bullet} Si_0 \equiv + e^- \qquad (3.6\text{-b})$$

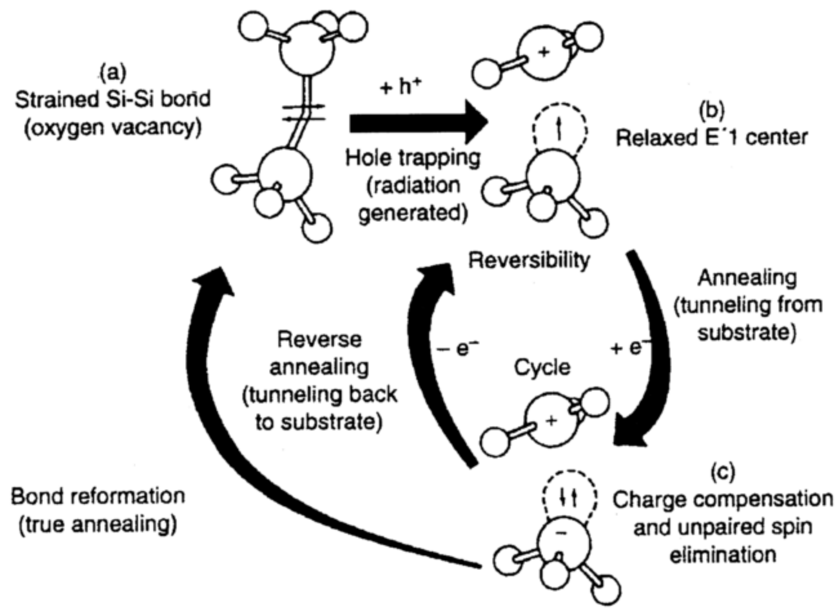


Figure 3.7: The charge trapping/ de-trapping and annealing schematic of oxygen vacancy bonds (Oldham and McLean, 2003).

During the reverse annealing model in Eq (3.6-b), the stable Si-Si bond can occur. Paramagnetic part of the defect, $^{\bullet}Si_0$, captures an electron, the resultant doubly occupied silicon dangling orbital would result in a high-energy metastable state, therefore, the hole ($\equiv Si_o^+$)–electron ($\equiv Si_o^-$) pair will be easily recombined and create stable Si-Si bond which not emits extra electron (Ristic, 2008). These trapping mechanisms in the oxygen vacancy bond and the switching annealing electric field can schematically be seen in Figure 3.7.

3.3.3 Defect Generation at Gate Oxide/ Semiconductor Interface

The defects located at the interface known as interface traps or fast switching traps (FST) and these FST are representing by $Si_3{\equiv}Si_s^{\bullet}$. Here index s represent the silicon atom at the interface back bounded the silicon atoms at the substrate. The interface traps can be directly created by indecent photon but the direct creation magnitude of the generated interface trap density by incident irradiation can be neglected. The direct creation magnification of interface traps/ FST is important for the interface traps created by hot electrons accelerated by applied electric field. Beside the direct generations, the FST created by trapped holes (h^+) and by hydrogen released in oxide (H-model), are the two main models for the generation of the FST in the radiation association (Ma and Dressendorfer, 1989; Ristic, 2008).

In h^+ model, the FST are generated by hole trapping near the interface, i.e., electron hole recombination is responsible for the generation of the FST. In other words, as soon as holes are trapped at the interface, electrons are injected from substrate and recombine with hole. The realized energy comes from the recombination can form the new FST. This mechanism can be expressed as;

$$\equiv Si_0^{\;+} + e^- + \equiv Si_s - Si_s \equiv \rightarrow \equiv Si_0^{\bullet} + \equiv Si_s^{\bullet} + Si_s^{\bullet} \qquad (3.7)$$

The main problem of the h^+ model is to explain why generations of the FST delay. However, researchers still have expected that some part of the FST is created by h^+ model.

In H model, the FST is generated by H^+ ions which are realized from the reaction given in Eqs. (3.4-a) and (3.4-b). When the H^+ ions reach the interface, they capture an electron from substrate and become reactive H^o atoms. These reactive H^o atoms react with the interface creating the FST by following reactions;

i- Reaction between interface trap precursor generates the interface traps, $Si_s^{\bullet}$

$$\equiv Si_s - H + H^0 \rightarrow \equiv Si_s^{\bullet} + H_2 \qquad (3.8\text{-a})$$

$$\equiv Si_s - OH + H^0 \rightarrow \equiv Si_s^{\bullet} + H_2O \qquad (3.8\text{-b})$$

The interface trap centers are localized at band gap of (100) Si called P_{bo} and P_{b1} centers. The P_{b0} defects are illustrated as the $Si_3{\equiv}Si_{s0}^{\bullet}$, while the P_{b1} defects are denoted as $\equiv Si_{s1}^{\bullet}$. Due to three rest bond of $P_{b1,}$ the P_{bo} centers have more dominant effects on the rise of interface traps. It should be noted that the theory of the interface traps is still not known exactly; hence, additional different trapping center, which are still not known, may exist (Ristic, 2008).

ii-The H^o may react with the interface traps during the fabrication process, and this reaction passivizes the interface traps

$$\equiv Si_s^{\bullet} + H^0 \rightarrow \equiv Si_s - H \tag{3.9}$$

iii-When the H^o approaches to interface, it reacts with another H^o and forms the H_2 gases

The reaction probabilities given in Eq. (3.8-a) and (3.8-b) are higher than others for the creation of interface traps, i.e., the FST. The source of these hydrogen containing bonds are the used H_2 gases during the deposition of the gate dielectric layer and annealing of the device.

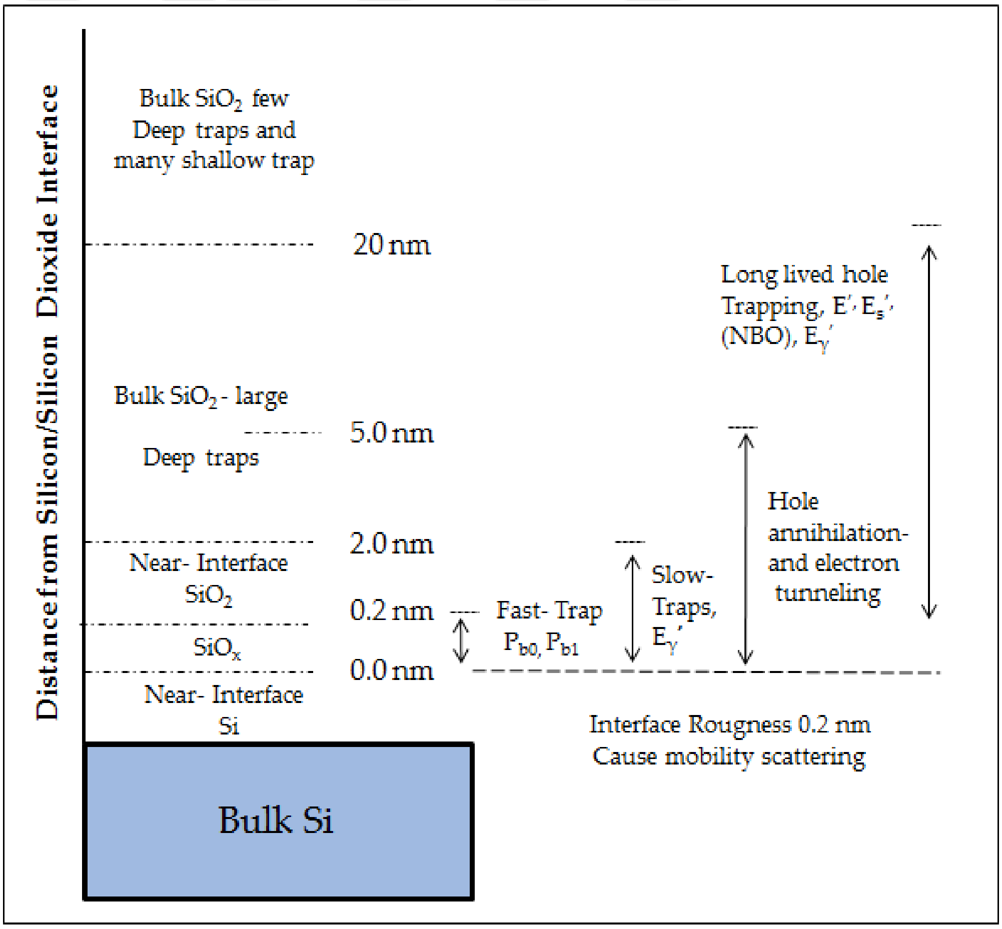


Figure 3.8: The schematic cross section of SiO_2/ Si interface including the trap states (Holmes-Siedle and Adams, 1994).

In order to understand the charge trapping behavior, the possible locations of these trap sites are illustrated in Figure 3.8 (Holmes-Siedle and Adams, 1994). Here, sometimes slow switching traps (SST) and fast switching traps (FST) can be distinguished. The important difference between SST and FST is that the SST located in the deeper side of the oxide and it slowly responds the electric field. Hence, the responses of the SST to electric field also make it the special trap, because SSTs are the only oxide traps that easily respond the fluctuation of the electric field, i.e., capture and release mobile carriers by the field (Ristic, 2008).

4. MATERIALS AND METHODS

4.1.1 Processing

The Al-gate Metal Oxide Semiconductor Transistor MOSFETs devices were fabricated in Nuclear Radiation Detectors Research and Applications Center, Abant Izzet Baysal University Bolu, Turkey. Starting materials were 6 inch (100) n-Si wafers with resistivity of 1-4 ohm-cm. The width (*W*) to length (*L*) (W/L) ratios were design to be 300 µm /50 µm. The required photomasks were designed by my supervised. The patterning of the masks was done by photolithography. The process details and flow chart are given in Figures 4.1 (a)- (h) and the processing is explained in the following order:

(a) Wafer Cleaning: The standard Radio Corporation America (RCA) cleaning procedure has been done (Reinhardt and W., 2008). The RCA cleaning procedure consists of three different chemical cleaning steps which are;

a- Organic Cleaning: The aim is to clean organic contamination using 5:1:1 DI-H_2O: H_2O_2: NH_4OH solution

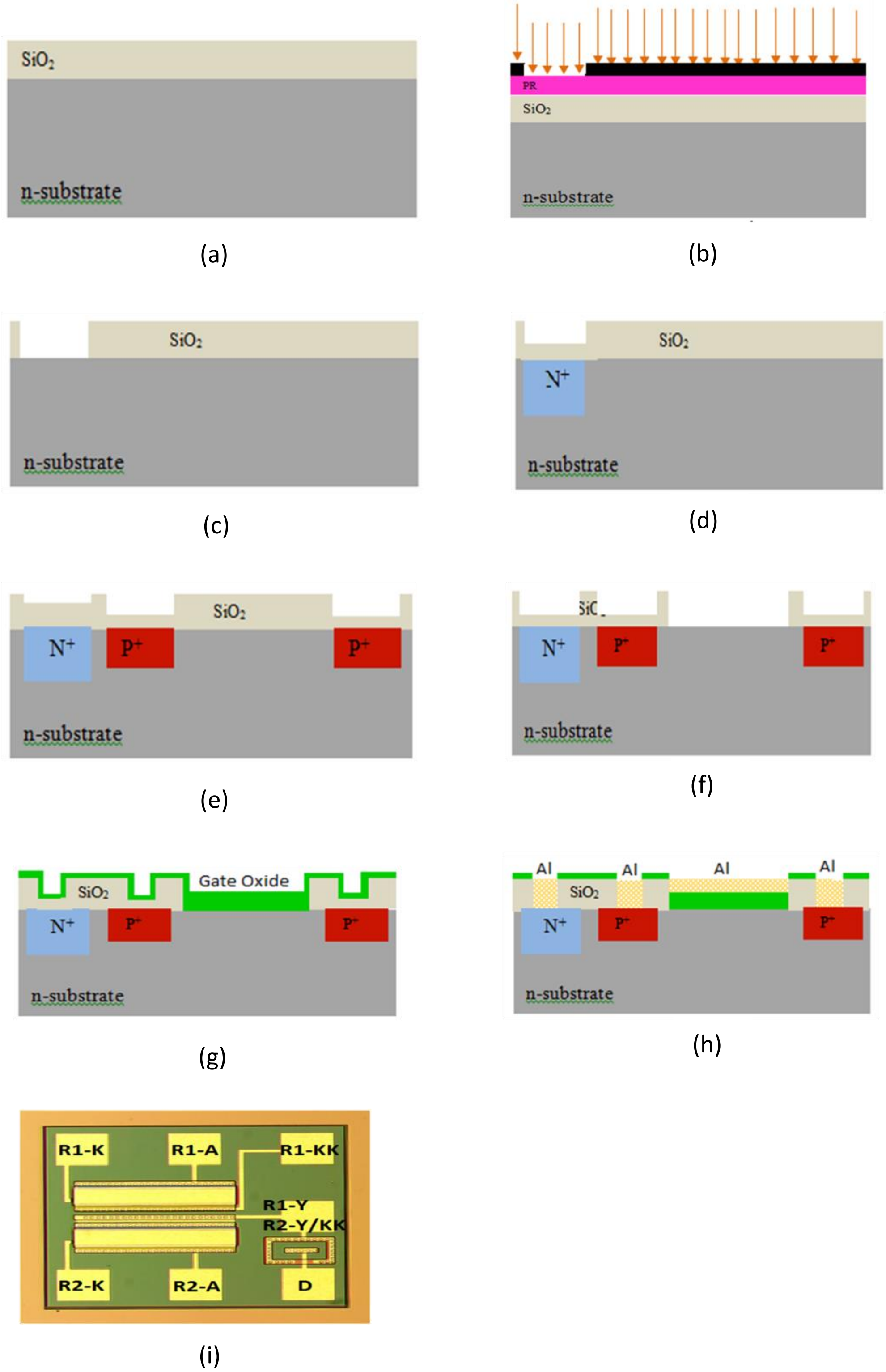
b- Ionic Cleaning: The aim is to clean ionic contamination using 6:1:1 DI-H_2O:H_2O_2:HCl solution

c- Native Oxide Cleaning: The native SiO_2 layer may grow onto the wafer; therefore, this layer should be removed from surface by 100:1 DI-H_2O:HF solutions

After the RCA cleaning process the wafers were dried by pure nitrogen.

(b) Field Oxide Growth: The field oxide layer was grown on RCA cleaned Si wafer using the diffusion furnace. The wet oxidation technique was followed to deposit SiO_2 layer. The schematic diagram of the samples after layer growth can be seen in Figure 4.1 (a).

(c) Phosphorus Deposition for Bulk Contact: To form bulk contact of the NürFETs, the Phosphorus (P) depositions have been performed. Before the P doping, the first lithography proses had been done. For the lithography process, firstly the wafer surfaces were coated with photoresist using spin coater and then the photo masks were placed on the wafers in mask aligner.



Figures 4.1: Some basic fabrication steps of NürFETs, a-) filed oxide grown, b-) first lithography, c-) BHF etching for formation of bulk contact, d-) wafers after phosphorus doping and drive in process, e-) schematic view of wager after boron doping and drive in process, f-) field oxide etching before the gate dielectric grown, g-) wafers after deposition of gate dielectric, h-) NürFETs schematic after complete fabrication, and i-) picture of the NürFET under metallurgical microscope.

After that the wafers were exposed to UV light as seen in Figure 4.1 (b) and then exposed parts of the photoresist were removed with solution. Following these steps, the SiO_2 layer were etched by buffered HF solution and then the remaining photoresists were removed from whole wafer surface using the oxygen plasma. The present wafers are seen in Figure 4.1 (c), schematically. The Phosphorus (P) depositions were performed using the $POCl_3$ flow at diffusion furnace. The doping densities of the wafers were controlled by four-point resistivity measurement system and surface resistivity was decreased after phosphor doping as expected. The following P deposition, the drive-in processes were carried out and the schematic of proceed wafers have is seen in Figure 4.1 (d) after these processes.

(d) Boron Doping to form Source and Drain Channels: To form source and drain channels of the NürFETs, the Boron (B) deposition was performed. Similarly, with P doping process as done before, the B doping, the second lithography processes have been carried out. The Boron (B) depositions were performed using the BBr_3 at diffusion furnace. The formations of the channel were controlled by P/N checker and the doping densities of the wafers were controlled by four-point resistivity measurement system. The obtained measurements demonstrate that p-channel formations have been successfully achieved. The following B deposition, the drive-in process were carried out and the schematic of one of the proceed wafers is shown in Figure 4.1(e).

(e) Gate Dielectric Growth: Before the deposition of the gate dielectric, the third lithography processes have been performed. After the third lithography, the wafer schematic is seen in Figure 4.1 (f). As extensively explained in the previous sections, the gate dielectric layer is the most crucial part of the device performance and it is naturally most sensitive part of the devices to ionize irradiation. Hence, the structural, morphological, electrical and electrochemical parameters before/after the irradiation exposure have been considered in details. Three different gate dielectric materials were grown onto three separate proceeded wafers;

i-Firstly, the conventional SiO_2 as gate dielectric layer has been grown on the Si wafer. Dry oxidation method at 1000 ^{0}C was used to grow the SiO_2 layer. Following the SiO_2 deposition, wafers were annealed for 30 min at 1000^{0}C in nitrogen. The thickness of the gate dielectric was measured to be 110 nm by spectroscopic reflectometer.

ii-Secondly, the high-k HfO_2 materials were deposited as another gate dielectric material. The HfO_2 gate layer was deposited by RF sputtering at 300 W with 16 sccm ultra-pure Ar flow. A four-inch HfO_2 target having purity of 99.99 % was used during the sputtering. The HfO_2 layer was also grown on the identical separate Si wafer following the same procedure to enable structural, morphological and chemical characterizations before and after radiation exposure. The thickness of the deposited HfO2 layer was measured to be 100 nm by spectroscopic reflectometer. Following the deposition of the HfO_2 layer, the samples were annealed at 300^0C in Nitrogen environment for 30 minutes.

iii-Thirdly, the high-k Er_2O_3 material was deposited as the last gate dielectric material.

The Er_2O_3 gate dielectric layer was deposited by RF sputtering. 99.99 % pure four-inch Er_2O_3 target was used and the sputtering power was adjusted to be 300 W with 16 sccm ultra-pure Ar flow. The Er_2O_3 layers were also deposited on the separate similar Si wafer following the same procedure to study structural, morphological and electrochemical characterizations of gate dielectrics. After that, the devices and deposited films were annealed at 350 ^{0}C in N_2 environment for 30 minutes. The thickness of the dielectric layer was measured to be approximately 100 nm using spectroscopic reflectometer.

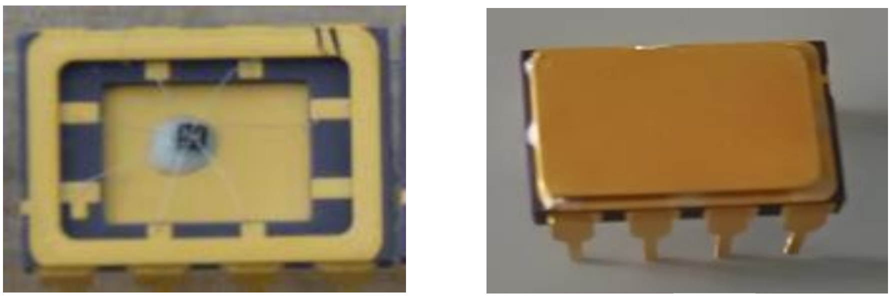
After the depositions of the gate dielectric layer, the schematics of the wafers can be seen in Figure 4.1 (g). The green part in the Figure 4.1 (g) symbolizes the three distinct gate dielectric layers.

(f) Metallization Procedure: In order to formation of metal contact to get electrical measurements, the Al depositions were performed. Before forming the metal contact, the forth lithography processes have been done. Following these steps, the SiO_2 and other gate dielectric layers were etched by HCl and HF-based solutions and then the remaining photoresist is removed from whole wafer surface. The Al depositions on the wafers were performed by sputtering method. The sputtering power was adjusted to be 150 W during the Al sputtering. In order to separate the source, bulk, drain and gate contacts, the last lithography was performed. Following these steps, the lift off procedure was applied and the Al layers were etched with nitric, acetic, phosphoric acid mix solutions. After that, the post-metallization anneal was performed at 450 ^{0}C in forming gas environment for 30 minutes for NürFETs having SiO_2 gate oxide layer, while others were annealed at 150^{0}C for 30 minutes in nitrogen.

The final NürFET diagram after complete fabrication procedure is shown in Figure 4.1 (h) schematically, and NürFETs pictures obtained from microscope are also shown in Figure 4.1 (j). In addition, as seen in Figure 4.1 (j), two distinct NürFETs have been fabricated in the per chip. R1-K, and R2-K are the gate contact, while R1-A and R2-A are the drain electrode of the first and second NürFET, respectively. In addition, R1-KK and R1-Y are symbolized the source and bulk electrode of the first NürFET. On the other hand, source and bulk electrode of the second NürFETs is connected together and their contact can be taken from R2-Y/KK electrode.

4.1.2 Packaging of Devices

The fabricated NürFET chips was diced by using dicing saw. Four NürFET chips for each deposited dielectrics (four HfO_2 NürFETs, four Er_2O_3 NürFETs and four SiO_2 NürFETs) were stick to 8-pin DIP package and each electrode was bond to a distinct package pin. The bonded device pictures are seen in Figure 4.2 (a).



(a) (b)

Figures 4.2: a-) Bonded NürFETs on the 8-pin DIP package, b-) NürFET with the suitable cover.

Observations indicate that lid cover causes variation on the NürFET responses (Kahraman et al., 2015b). The variations caused by difference of scattered primary and secondary particles from its lid. The densities of the lid materials are also effective for the scattering variations. Hence the same Kovar package lids have been used to close upper surface of the NürFETs. The packaged NürFETs used in the irradiation experiment is seen in Figure 4. 2 (b). Tyndall RadFET lid cover also changed with same KOVAR package to obtain accurate results.

4.2 Irradiation Experiment

The irradiation experiments were performed at the Turkish Atomic Energy Authority Gamma Irradiation Facility in Ankara. All these samples were exposed to Co-60 gamma irradiation doses up to 1600 Gy, with certificated Ob-Servo Sanguis Co-60 gamma irradiator seen in Figure 4.3 with approximate dose rate of 417 Gy/h. The devices were irradiated under zero gate bias (all terminals grounded) configuration. Dimensions of the irradiation chamber were 220 mm x 250 mm and the samples were placed into middle of the irradiation chamber. The samples were also placed perpendicular to irradiation sources in order to eliminate angle dependency on the irradiation response of the devices. The required electrical I_{ds}- V_g measurements were performed immediately after the each exposed irradiation doses. Sample to sample variations in the related measurements are given in error bars for the related figures.

Figure 4.3: Co-60 gamma irradiation sources at TAEK

On the other hand, the HfO_2 and Er_2O_3 thin films have been also exposed to two different gamma irradiation doses (200 Gy called low dose and 1.6 kGy called high dose) to investigate irradiation influence on the structural, morphological and electrochemical characteristics of high-k/Si stack and also specification of possible radiation degradation mechanism. In order to enhance the reliability of the work, four distinct commercial RadFETs having 100 nm SiO_2 gate dielectrics fabricated by Tyndall National Institute- Ireland were also used and obtained results were also compared to fabricated devices in this study.

4.3 NürFETs Characterizations and Their Radiation Responses

4.3.1 Structural Characterizations

The structural evolutions of the dielectric layers after annealing and irradiation exposure were investigated by X-Ray diffractometer (XRD) measurements which are based on constructive interference of monochromatic X-rays and a crystalline sample. The phase identification and crystallization degree of the films are crucial for the devices due to the conduction mechanism and dielectric characteristics are directly related to structural evolution of the deposited layer (Kahraman et al., 2016; Singh et al., 2012). Hence, measurements were performed before and after irradiation by Rigaku MultiFlex diffractometer with Cu Kα radiation (=1.5418 Å) in the range between 15° and 60° at a scan speed of 3.5°/min. The obtained XRD spectra were indexed by The International Centre for Diffraction Data (ICDD) data base and the phases of the dielectric layer have been identified using the indexed peaks. The radiation influences on the crystallographic structure were determined by variations on the peak shift, intensity changes and broading of the peaks obtained from XRD spectra after the radiation exposure.

4.3.2 Morphological Characterizations

Morphological characterizations of the dielectric layers have been investigated by Atomic Force Microscopy (AFM) measurements. A cantilever of AFM probe, having sharp tip, scan over sample surface. When the tip approaches the sample surface, attractive force between the surface and the tip cause deflection on the cantilever. Due to these forces, cantilever was raised and lowered depending on the sample surface. Using this motion, AFM pictures have been generated. Since carrier scattering from the rough surface degrade the electrical conduction mechanism (Kim and Kim, 2002), the possible variations on the surface roughness under radiation should be examined. Hence, AFM measurements were performed by Nanomagnetic Instruments' ambient AFM systems. The topographic AFM images were taken in the contact mode under room conditions and typical scanning rate was 0.15 micron/minute. The AFM images analysis were carried out with special software developed by Nanomagnetic Instrument group. The average surface roughness (RMS) values were calculated using this software and the variations under the radiation exposure were discussed.

4.3.3 Electrochemical Characterizations

X-ray photoelectron spectroscopy (XPS) is typically accomplished by exciting a samples surface with mono-energetic Al kα x-rays causing photoelectrons to be emitted from the sample surface. An electron energy analyzer is used to measure the energy of the emitted photoelectrons. Using the binding energy and intensity variations of a photoelectron peak, the elemental composition, chemical sub-oxidation and electronic state of elements can be analyzed. Depth analysis of materials in XPS measurements is approximately 5 nm -10 nm. The variations in the chemical compositions, the generation/breaking bond and possible radiation interaction mechanism under irradiation exposure have been investigated by XPS spectra of the virgin and gamma exposed the films. During the XPS analysis, all peaks were calibrated to C 1s peak at 284.5 eV to eliminate the possible charging effect that may occur due to surface contamination. During the detailed analysis, the measured XPS spectra have been analyzed by peak de-convolution software to specify sub- peaks. Following the peak de-convolution, distributions of the sub oxidation states have been discussed by using the obtained sub-peaks.

4.3.4 Electrical Characterizations

Two main charge separation techniques have been used to analyze electrical performance of the fabricated and commercial devices. Firstly, charge pumping (CP) techniques were used to calculate initial interface trap densities in order to specify the interface quality of the device to be used microelectronic applications. Secondly, the Midgap-subthrehold (MG) technique was used to determinate the radiation induced oxide trap (ΔN_{ox}) and interface trap (ΔN_{it}) densities. The details of these techniques have been explained below;

4.3.4.1 Charge Pumping Technique

In this technique, when the surface is pulsed from inversion to accumulation, substrate current, $I_{cp,}$ is measured. The inversion mobile carriers are trapped by interface traps and these traps recombine with majority carriers when surface goes to accumulation. Due to this recombination some substrate current occurs. The maximum point of the this I_{cp} can be expressed as;

$$I_{cp,\max} = fqAD_{it}\Delta E \tag{4.1}$$

where A is the gate area, f is the applied voltage frequency, ΔE is the sweep of surface potential electric field. The average value of the interface trap density can be calculated by using $N_{it}=D_{it}\Delta E$;

$$N_{it} = \frac{I_{cp,\max}}{fqA} \tag{4.2}$$

Here, frequency of the applied voltage is in the order of few hundred kHz.

4.3.4.2 MidgapTechnique

The threshold voltage of the devices can shift (ΔV_{th}) due to contribution of the radiation induced interface trap voltages (ΔV_{it}) and radiation induced oxide trapped voltage (ΔV_{ot}), where $\Delta V_{th}= \Delta V_{it} + \Delta V_{ot.}$ Threshold voltage (V_{th}) values were determined as voltage values at the specified current level (10 μA for HfO2 NürFETs, SiO_2 RadFETs, and 1 μA for Er_2O_3 NürFETs) in this study. The values of radiation induced ΔN_{it} and ΔN_{ot} can be calculated using the changes on the ΔV_{it} and $\Delta V_{ot.}$ As mentioned in the above sections, the contribution of the interface traps to voltage at midgap level is almost zero and just trapped oxide charges influence the midgap voltages. Hence, the V_{ot} values can be found from midgap level, i.e., $V_{mg}=V_{ot}$. The determination of the V_{mg} can be found from regression of the linear region of sub-threshold current. The midgap current can be calculated by using the sub-threshold current in saturation (Ristic, 2008);

$$I_D = \frac{\sqrt{2}\beta\varepsilon_s}{2C_{ox}L_d}\left(\frac{kTn_i}{qN_d}\right)^2\left(\frac{q}{kT}\phi_s\right)^{-0.5}\exp\left(\frac{q}{kT}\phi_s\right) \quad (4.3)$$

where $\beta = W\mu C_{ox}/L_{eff}$ and $L_d = [(\varepsilon_s kT/(q^2 N_d)]^{0.5}$ is the Debye length. It is well-known that in the midgap level the condition is $\phi_{s=}\ \phi_B$ (see section 2.2.3.3 Interface Charges). Hence, using the straight line of the $\log(I_d)= aV_g+b$ which was obtained from linear fit of subthreshold curve, the V_{mg} that correspond to the $I_d=I_{mg}$ can be found, i.e., $V_{gm}=(\log(I_{mg})-b)/a$. Using these procedure, the different V_{mg} values were obtained after the irradiation stress and the $\Delta V_{mg}=\Delta V_{ot}$ can be calculated from (Jun et al., 2003);

$$\Delta V_{mg} = \Delta V_{ot} = V_{mg,1} - V_{mg,0} \quad (4.4)$$

where $V_{mg,0}$ and $V_{mg,1}$ are the midgap voltage values before and after gamma irradiation.

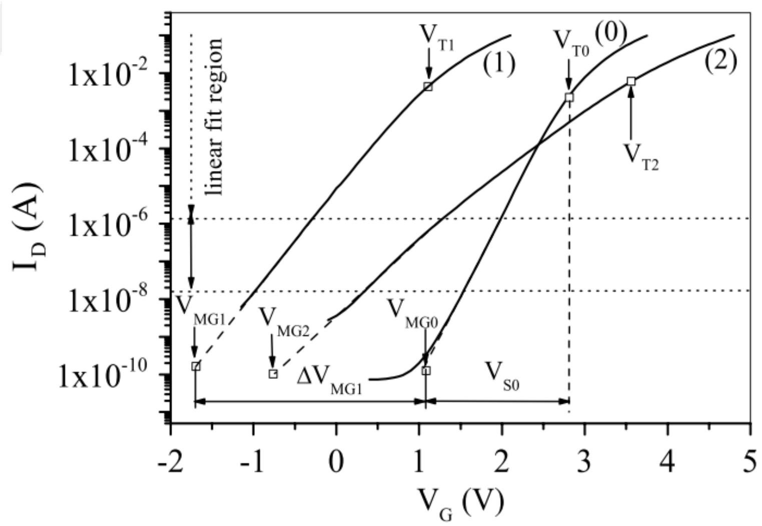


Figure 4.4: The relation between V_{th}, V_{mg}, and V_{so} (Ristic, 2008).

The second important parameter is the determination of the stretch-out voltage, V_{so}. In order to calculate V_{so}, one needs to determine the threshold voltage. The easiest way to obtain V_{th} is the above-threshold method. In this method, the extrapolated threshold voltages (V_{th}) can be found from drain current curve in saturation (Sze, 1981). In other words, the extrapolated threshold voltages is determined from the intersection of linear curve fit of the square root saturation drain current curve as a function of voltage (see the Figure 2.14). The following determination of the V_{th} value, the V_{so} can be calculated from (Mcwhorter and Winokur, 1986);

$$V_{so} = V_{th} - V_{mg} \tag{4.5}$$

The relation between V_{th}, V_{mg} and V_{so} can be seen from Figure 4.4. Using these procedures the different V_{so} values were obtained after the irradiation stress and its value is equal to ΔV_{it}, i.e., $\Delta V_{it} = \Delta V_{so}$ and they can be calculated by means of (Jun et al., 2003):

$$\Delta V_{it} = \Delta V_{so} = V_{so,1} - V_{so,0} \tag{4.6}$$

where $V_{mg,0}$ and $V_{mg,1}$ are the midgap voltage values before and after gamma irradiation. Finally the ΔN_{it} and ΔN_{ot} values can be calculated from (Ristic, 2008);

$$\Delta N_{it} = \frac{\Delta V_{it} C_{ox}}{qA} \tag{4.7-a}$$

$$\Delta N_{ot} = \frac{\Delta V_{ot} C_{ox}}{qA} \tag{4.7-b}$$

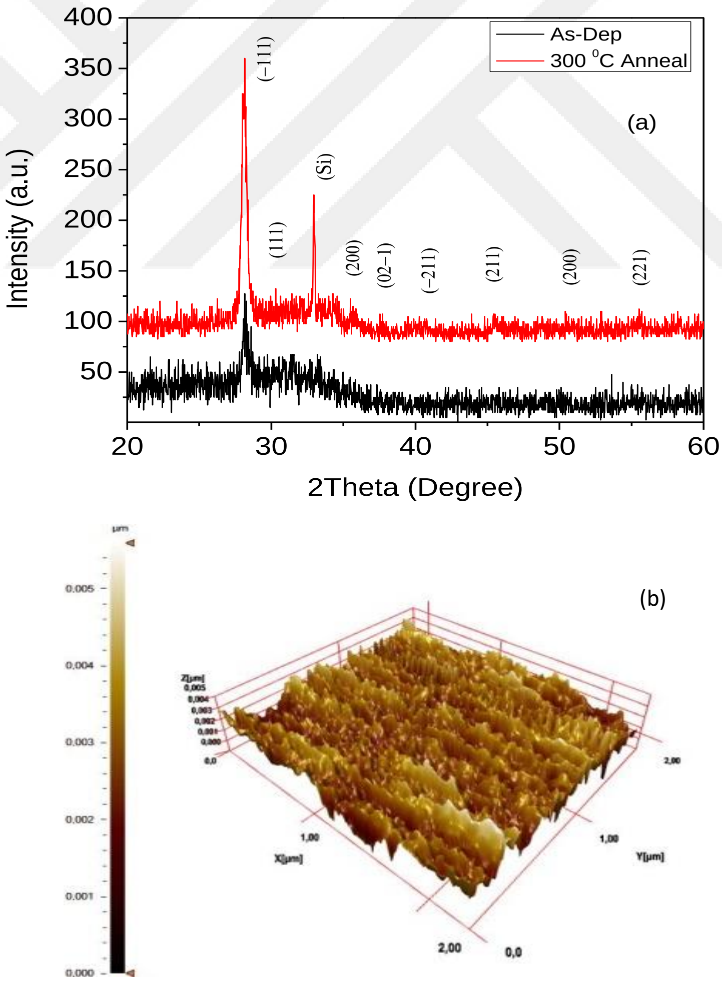
Here the extracted values give the density of the radiation induced in interface and oxide trapped charge; hence, their units are generally given cm^{-2}.

5. RESULTS AND DISCUSSION

5.1 Radiation Responses of NürFETs with HfO_2 Gate Dielectrics

5.1.1 Pre-Irradiation Device Characteristics of HfO_2 NürFETs

The crystal phase and morphology of HfO_2 films are directly affecting the devices electrical characteristics, e.g., conduction edge, trapping states, radiation response, etc (Kahraman et al., 2015c; Lucovsky et al., 2006; Lucovsky et al., 2004). The initial device characteristics should be considered before the radiation exposure.



Figures 5.1: The (a) XRD and (b) AFM measurements of the deposited and annealed HfO_2/Si thin films

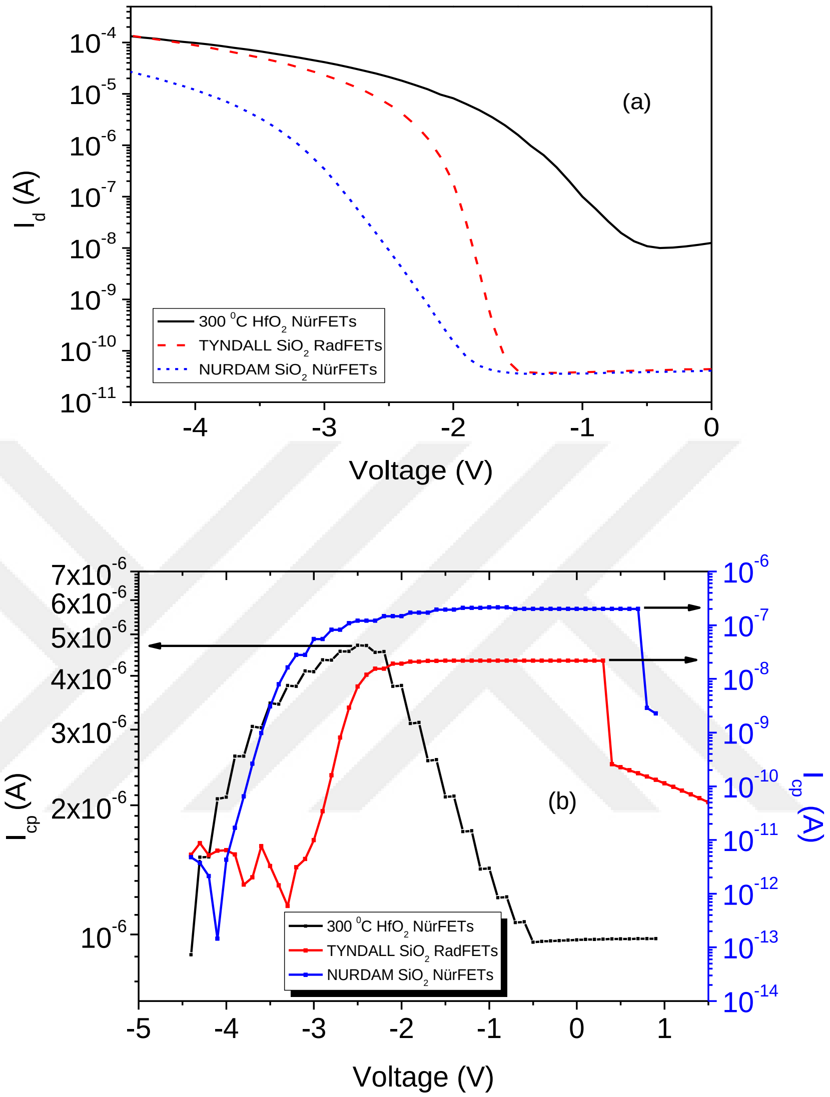
The XRD and AFM measurements are given in Figures 5.1 (a) and (b) for HfO_2/Si films to specify annealing effects. The peaks in Figure 5.1 (a) corresponds to (-111), (111), (-211) and (211) planes are match with cubic phase of the HfO_2 layer. The peak having low intensity indicates that the HfO_2 layer is poorly crystallized with annealing and the preferred orientation belongs to the (-111) plane as expected due to lowest surface energy exists in (-111) texturing (Vargas et al., 2014). The grain sizes of the sample were calculated from strongest peak (-111) using Scherrer's equation (Kahraman et al., 2016) and found to be 17.95 nm. The presence of expected Si peaks is probably related to rising in the penetrating distance of incident/reflected X- ray in the crystalline structure.

On the other hand, morphology of the films investigated by AFM measurements is given in Figure 5.1 (b) for annealed films. It has been analyzed that surface roughness (RMS) is 2.95 nm. The obtained RMS of the film is relatively low compared to the film thickness fabricated by sputtering. This low RMS value implies uniform surface morphology which is good for eliminating the contact resistance and scattering effect during the electrical measurements.

Table 5.1: The V_{th} and D_{it} parameters of the NüRFETs with HfO_2, with SiO_2 and TYNDALL devices with SiO_2 before irradiation.

	V_{th} (V)	D_{it} ($x10^{10}cm^{-2}$)
HfO_2 NürFET	-1.50	188
NÜRDAM- NürFET	-2.95	7.71
TYNDALL- RadFET	-2.61	1.05

In order to investigate compatibility of HfO_2 NürFETs for microelectronics and compare the initial device characteristics with SiO_2 NürFETs and RadFETs having similar gate dielectric thickness, the I_d-V_{gs} and charge pumping measurements were performed and the results of measurements are given in Figures. 5.2 (a) and (b), respectively. A gate bias of around 0 V corresponds to OFF-state operation of the transistor. The drain current of HfO_2 NürFETs in off state is higher than in the SiO_2 gate devices due to leakage effect (Gurfinkel et al., 2009; Rana et al., 2010). This leakage effect may be attributed to crystallization of the HfO_2 dielectric; because the grain boundaries may form conduction path. The above-threshold method was used to obtain extrapolated threshold voltages (V_{th}) from drain current curve in saturation for HfO_2 based devices (Sze, 1981). This method to find V_{th} can be seen from section 2 and Figure 2.14



Figures 5.2: The (a) Drain current in saturation and (b) Charge pumping current measurements of the HfO_2 NürFETs, NÜRDAM-NürFETs and TYNDALL-RadFETs.

The obtained V_{th} values are given in Table 5.1 and, as accepted, depending on the capacitance of the devices, threshold voltages varied from -1.50 V to -2.95 V. In addition, the densities of interface trap occurred from fabrication procedure were calculated from Eq. 4.2 (Ristic et al., 2011), using the peak values in charge pumping curves in Figure 5.2 (b). The calculated N_{it} values are given in Table 5.1. Calculated N_{it} values are still within acceptable limits for devices used in microelectronics (Cetinkaya et al., 2015; Kaya et al., 2015; Tirmali et al., 2011).

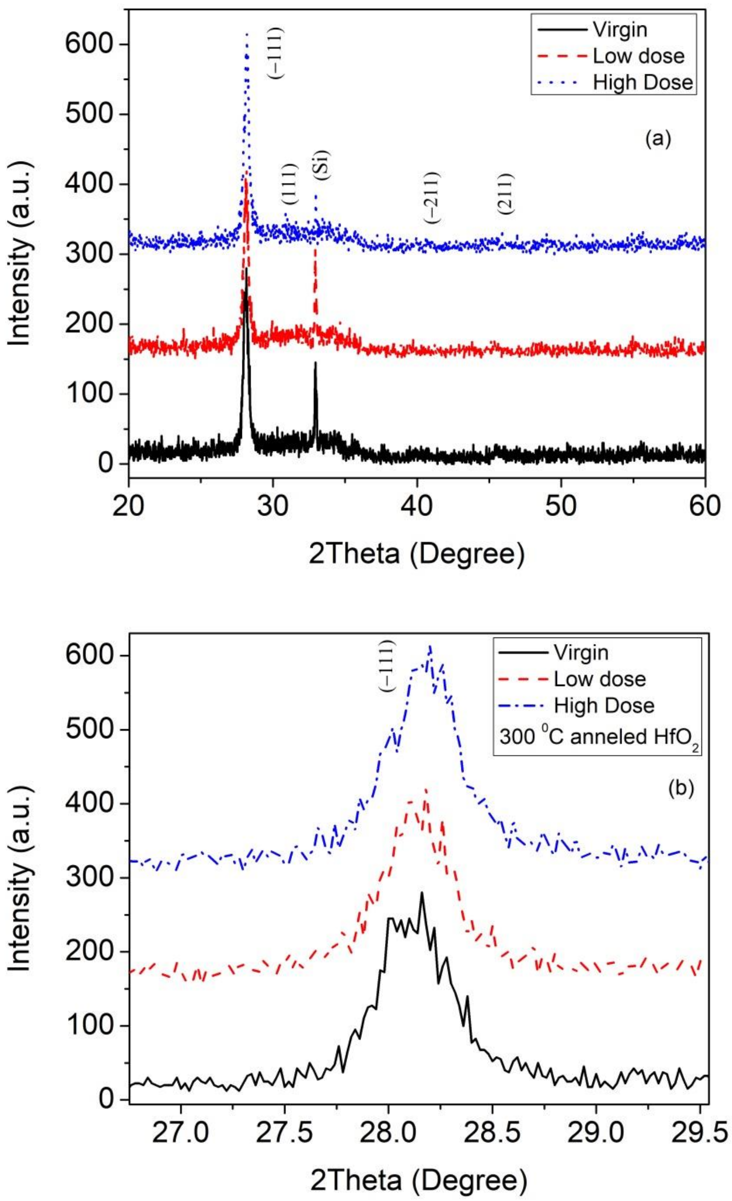
5.1.2 Physical Modifications of the HfO_2 Gate Oxide under Irradiation Exposure

The irradiation effects on the crystallization of the HfO_2 thin films have been investigated by XRD measurements and results are illustrated in Figures 5.3 (a) and (b). It has been observed that the intensity of the peak oriented in (-111) direction enhances with enhancing the irradiation dose, while other minor peaks remain almost constant. The required Gibbs' energy to collision of the grains in the other orientation is possibly higher than the (-111) direction (Vargas et al., 2014). Hence, the unchanged peak intensities for the other orientations after irradiation exposure are possibly related to insufficient local energies generated by irradiation exposure. The net change in peak intensities in (-111) can be seen from Figure. 5.3 (b) and Table 5.2. This observation indicates that the additional local heating of Nano-scale particle discharge the local stress/ strains between grains. This discharge provides the rise in the crystalline structure (Lavanya et al., 2016).

Table 5.2: Variations on the some physical parameters of HfO_2 film under gamma irradiation

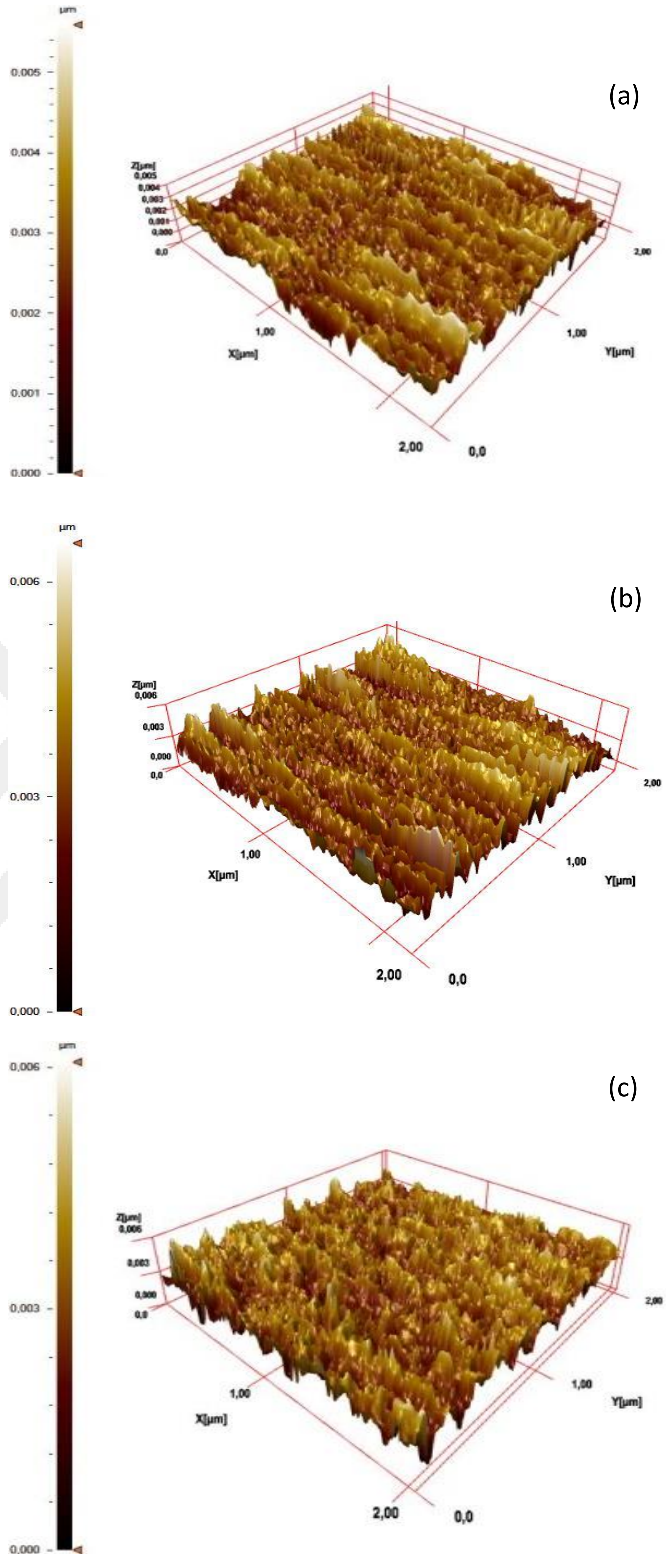
Irradiation Dose	Grain Size (nm)	Max. Peak Intensity	RMS Roughness (nm)
Virgin	17.95	241	2.95
Low Dose	18.57	250	2.99
High Dose	19.96	282	3.25

Average grain sizes (P) of the films have been calculated depending on the irradiation doses using the boarding of the peak in Figure 5.3 (b). The Scherrer's relations in the following equation have been used to calculate P values. The P values of the films are listed in Table 5.2. The observed rise in the P value also indicates the coalitions of smaller grains in bigger cluster. This observation is associated with the changes in the lattice volume due to crystallization after high energy impact with gamma radiation. On the other hand, Ding et al. have reported that irradiation degrade the crystallization of the HfO_2 (Ding et al., 2014). The deposition parameters including the film thickness, deposition methods and amount of exposed doses affect the degradation level of the films (Lucovsky et al., 2006; Ryan et al., 2005). Therefore, variations between results are associated with processing conditions. Consequently, the XRD results in this study reveal that no phase change have been observed under given gamma radiation doses, despite the slight improvement of the film crystallization.



Figures 5.3: The XRD measurements of HfO_2 thin films a- before and after the gamma irradiations, b- Enlargement of the (-111) peak.

The irradiation influences on the surface morphology of the HfO_2 thin films were investigated by AFM measurements which are illustrated in Figures 5.4 (a)- (c). The obtained measurements do not have a considerable effect which can be seen by naked-eye. The high compressive stress cause some hillock formation can be observed. However, no hillock has been observed indicating the radiation induced surface stress and tension was not too high to degrade morphology.

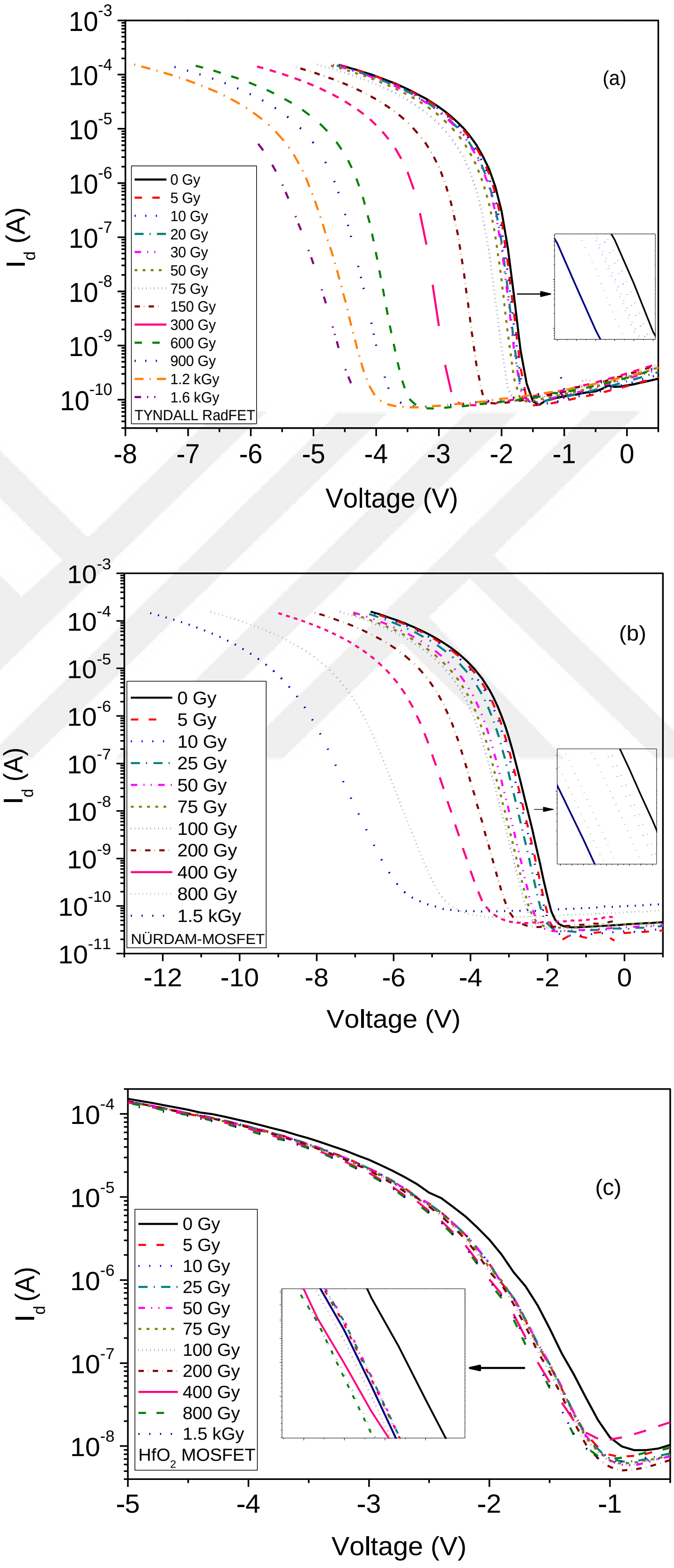


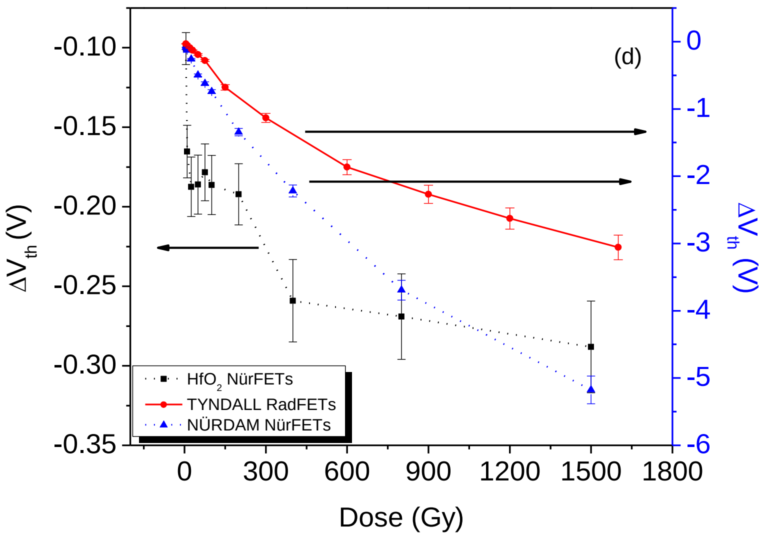
Figures 5.4: The AFM pictures of the HfO_2 thin films a-) before, b-) low and c-) high dose radiation exposure.

In order to analyze deeply, the RMS of the films were calculated by using the AFM analyze program and the results are given in Table 5.2. The slight rises in the RMS values have been observed by enhancing the irradiation doses. The rises in the RMS values are presumably due to the swelling caused by the gamma irradiation. The radiation energy causes volume enlargement, because crystallizations of the amorphous track in the oxide structure (Hazem et al., 2013). These results are in agreement with the XRD analysis.

5.1.3 Radiation Induced Effects on Electrical Characteristics of HfO_2 NürFETs

Electrical I_d-V_g characteristics of the irradiated samples to the Co-60 gamma-ray exposure are shown in Figure. 5.5 (a)- (c) for three sample groups, and the threshold voltage shift vs. irradiation dose is depicted in Figure 5.5 (d). The radiation response of the devices with SiO_2 gate dielectric has been extensively studied and basic device behavior is currently well-known (Ma and Dressendorfer, 1989). Briefly, the basic mechanism is: radiation creates large number of defects and electron-hole (e-h) pairs. Due to higher mobility of electrons, they are easily swept out from the gate, while holes which escape initial recombination move toward SiO_2/Si interface where deep traps are located. Generated defects and the trapped holes in the defect centers degrade the device performance and cause the shift in threshold voltages as seen in Figures 5.5 (a) and (b). For the devices with high-k dielectrics, the radiation response is rather complex, as seen in Figure 5.5 (c). The Monte Carlo Simulation studies demonstrate that the average deposited energy is much higher in HfO_2 than SiO_2 layer (Dasgupta et al., 2010; Kahraman et al., 2015a). High deposited energy indicates that the radiation interaction result in the generation of e-h pair densities is higher than SiO_2. Hence the expected results are that the threshold voltage shift of HfO_2 should be higher than in SiO_2 based devices. However, it is observed in Figure 5.5 (c), the radiation dose does not have significant effect on the measured I_d- V_g characteristics of HfO_2 NürFETs. Only the small and non-unidirectional shifts toward negative voltages have been observed. The changes of the threshold voltage shift in Figure 5.5 (d) show that the sensitivity of HfO_2 devices is ten times lower than that of SiO_2 devices. Similar results were also observed in thinner HfO_2 layers grown by ALD techniques (Liang et al., 2017; Rafi et al., 2013; Suria et al., 2015).

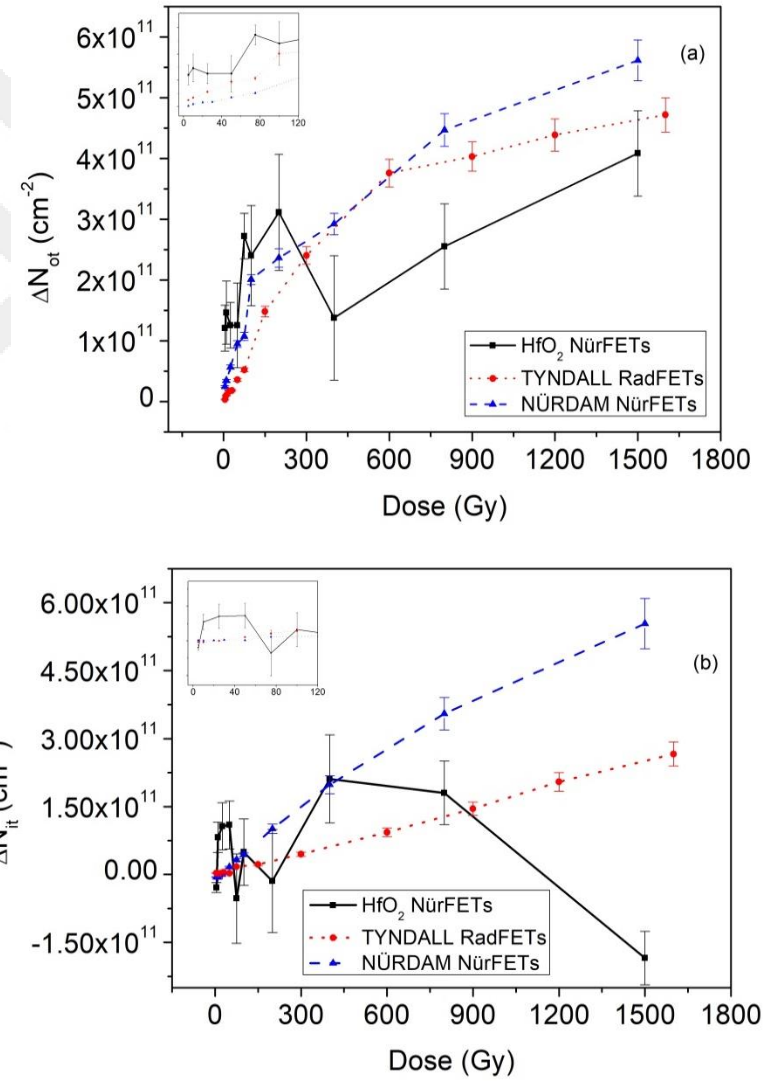




Figures 5.5: The I_d-V_g characteristics of a-) TYNDALL-RadFETs, b-) NÜRDAM-NürFETs, c-) HfO_2 NürFETs under various Co-60 gamma doses, and, d-) Threshold voltage shift dose relations for devices.

Although the higher energy are deposited in HfO_2 under gamma radiation, the observed less effects on electrical characteristics can be attributed to the less trapping efficiency of the generated mobile charges in HfO_2. The possible radiation degradation and charge trapping mechanism will be investigated in further sections in detail. Comparing the two groups of SiO_2 samples, the reasons for higher sensitivity of NÜRDAM NürFET compared to TYNDALL RadFET in Figure 5.5 (d) can be attributed to differences in processing conditions and variations in the gate dielectric thickness, i.e. 100 nm for TYNDALL RadFETs vs. 110 nm for NÜRDAM NürFETs (Francis et al., 2012; Kelleher et al., 1992).

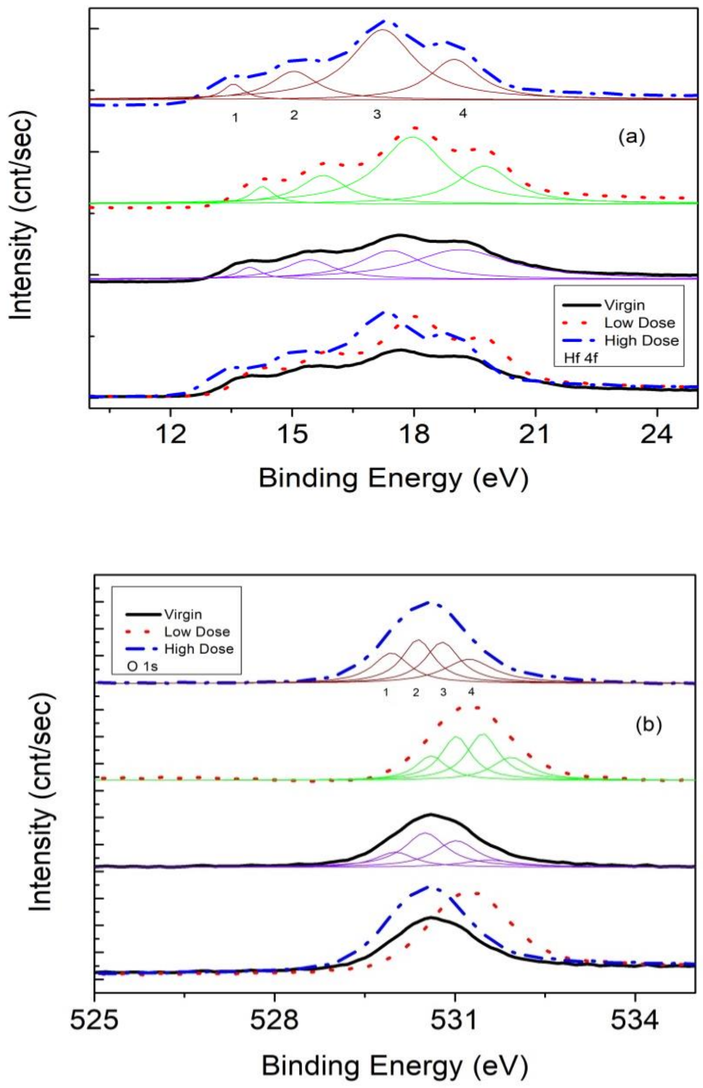
The radiation induced trapped charge densities in the dielectric layer (ΔN_{ot}) and dielectric/Si interface (ΔN_{it}) have been calculated from analysis of I_d-V_g characteristics of devices using MG technique. The obtained ΔN_{ot} and ΔN_{it} characteristics are illustrated in Figures 5.6 (a) and (b), respectively, for all sample groups. The continuous enhancement in the charge trapping with radiation exposure is observed in SiO_2 layers as expected. However, the ΔN_{ot} and ΔN_{it} behaviors of the HfO_2 seem more complex than SiO_2 layer. In addition, the large standard deviations (shown in error bars) for HfO_2 NürFETs are probably related to more pronounced device-to-device in-process variations and especially influence of the passivation variance depending on radiation dose which will be discussed in detail. In HfO_2 devices, hole trapping in the oxide layer dominates the charge trapping distribution with the possible passivation of the dielectric layers at some doses as seen in Figure 5.6 (a). However, charge trapping distribution is rather complex for the HfO_2/Si interface – both e-h trapping and possible passivation are observed at the interface as seen in Figure 5.6 (b). The combined behaviors have been observed in the previous studies for e-h trapping, but the gate dielectric layers fabricated by sputtering show more complex behavior than previously reported ALD grown layer studies (Rafi et al., 2013; Sun et al., 2013). In addition, the fluctuating behavior of radiation induced trapped densities have been also observed in other studies (Kahraman and Yilmaz, 2017; Kaya and Yilmaz, 2014; Maurya, 2016; Singh et al., 2012).

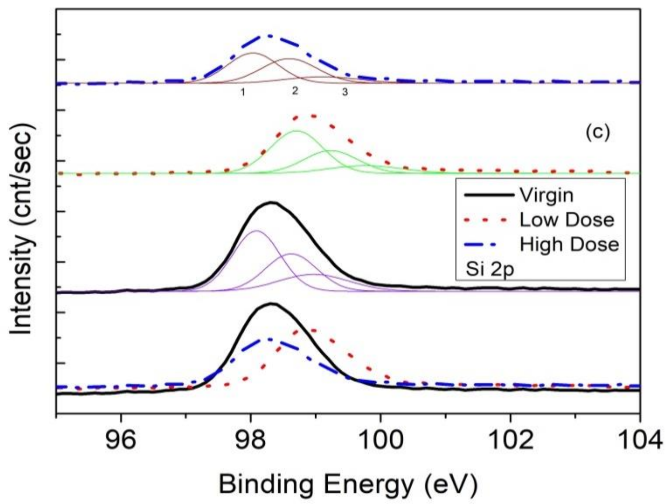


Figures 5.6: Radiation induced a-) oxide trap density, and b-) interface trap density at various doses.

5.1.4 Radiation Effects on HfO_2/Si Interface Chemistry

To specify possible radiation interaction and charge trapping mechanism, the XPS measurements of the HfO_2/Si layers were carried out before and after irradiation exposure for low (200 Gy) and high (1.5 kGy) doses. Due to the existence of deep level traps close to HfO_2/Si interface, the HfO_2 layer was etched with Ar^+ sputtering and the XPS measurements were performed approximately sub- 10 nm. The core levels of HfO_2 thin films in XPS spectra before and after radiation exposures are illustrated in Figures. 5.7 (a)- (c) for Hf4f, O1s and Si2p core levels, respectively. It has been observed that the core levels of Hf4f, O1s and Si2p have more than one peak in their detailed scans, demonstrating that each element has more than one valence state. In order to investigate these sub-states, multi-peak resolution was applied and results are also illustrated in Figures 5.7 (a)- (c).





Figures 5.7: Interface XPS spectra of HfO_2 thin films a-) Hf 4f, b-) O 1S, and c-) Si 2p core levels before and after irradiation.

The sub-peaks for the each core level were also numbered for detailed investigation. In general view, the intensities of the Hf 4f and O 1s states enhance with irradiation, while the intensity of the Si 2p core level decreases. In addition, all core levels shift toward higher binding energies after low irradiation exposure, but they shifted to lower binding energies after higher irradiation exposures.

Table 5.3: Variations on the Hf4f, O1s and Si2p states under radiation exposures.

	Hf 4f			O1s			Si 2p		
Sub-Peak	Virgin BE (eV)	Low Dose BE (eV)	High Dose BE (eV)	Virgin BE (eV)	Low Dose BE (eV)	High Dose BE (eV)	Virgin BE (eV)	Low Dose BE (eV)	High Dose BE (eV)
1	14.05	14.15	13.55	529.9	530.6	529	98.72	98.9	98.24
2	15.4	15.76	15.02	530.5	531	530.4	99.01	99.2	98.6
3	17.43	17.95	17.20	531	531.5	530.8	99.2	100.11	99.12
4	19.25	19.72	19.01	531.6	531.8	531.2	-	-	-
	Virgin Int.	Low Dose Int.	High Dose Int.	Virgin Int.	Low Dose Int.	High Dose Int.	Virgin Int.	Low Dose Int.	High Dose Int.
1	2593	3981	3546	2644	4480	5332	6007	4182	2973
2	4489	6734	6706	6212	8049	7887	3744	2225	2412
3	6706	16053	16807	4759	8400	7420	1696	756	549
4	6944	8947	9563	1169	4096	4272	-	-	-

These initial observations demonstrate that both passivation and bond breaking (generation of trap centers) are observed together during irradiation exposures. For the detailed investigation, the sub-peaks were analyzed and their distributions are given in Table. 5.3. For the core level of Hf 4f having 15.4 eV and 17.73 eV binding energies (BE) (Yang et al., 2011), together with core level of O 1s having 529.9 eV and 530.5 eV BE (Fu and Chang, 2011; Gao et al., 2015), are signed to the O-Hf–O bond. In addition, the peak values located in 14.05 eV possibly come from Hf-Si bonds (Smirnova et al., 2009). Moreover, the signal comes from sub Hf 4f states located in the 19.25 eV BE (Lee, 2005), sub O 1s states having 531 eV BE (Smirnova et al., 2010), and sub Si states having 99.01 eV BE are forming the possible Hf-O-Si bonds. Lastly, the O 1s states having 531.6 eV BE and Si having 99.2 eV BE are composed of the interfacial Si-O layer. These results demonstrate that the deposited gate stack of HfO_2/Si has complex chemical bonding and electronic structure. After the low dose irradiation exposure binding energies of all sub-peaks shift to higher energies up to 0.57 eV and the intensities of the peaks enhance except the Si core level. This intensity distribution and especially the energy shift demonstrate oxygen penetrate deeper level with irradiation exposure; hence, more effective oxidation occurs and the passivation of the dangling bonds can be observed (see some doses in Figures 5.6 (a) and (b)) (Yan et al., 2016; Yang et al., 2011). This low dose effect dominates the oxidation states of O-Hf-O and Si-O, when comparing the intensities from Table 5.3.

When the deposited HfO_2/Si layer is exposed to the higher radiation doses, the binding energies shift toward lower energies up to 0.75 eV. Compared to other peaks, the higher energy shifts have been observed for O-Hf-O and Si-O bonding states; hence, radiation breaking one of the oxygen bonds results in formation of the sub oxidation states (HfO_x and/or SiO_x). These broken bonds may act as trapping centers and it is known that oxygen vacancy may act as hole trapping center (Foster et al., 2002; Ryan et al., 2005). Hence the observed small V_{th} shift on HfO_2 NürFETs in Figure 5.5 (d) is due to oxygen vacancies in HfO_x and SiO_x where holes can be trapped. The explained passivation and trap generation behavior cause the sensitivity deviation device-to-device. So, the large deviations for the ΔN_{ot} and ΔN_{it} in Figures 5.6 (a)- (b) are probably related to variations on the passivation amounts device- to-devices.

5.2 Radiation Responses of NürFETs with Er_2O_3 Gate Dielectrics

5.2.1 Pre-Irradiation Device Characteristics of Er_2O_3 NürFETs

The initial device parameters should be considered to enhance reliability of the study. The XRD and AFM measurements are given in Figures 5.8 (a) and (b) for Er_2O_3/Si films.

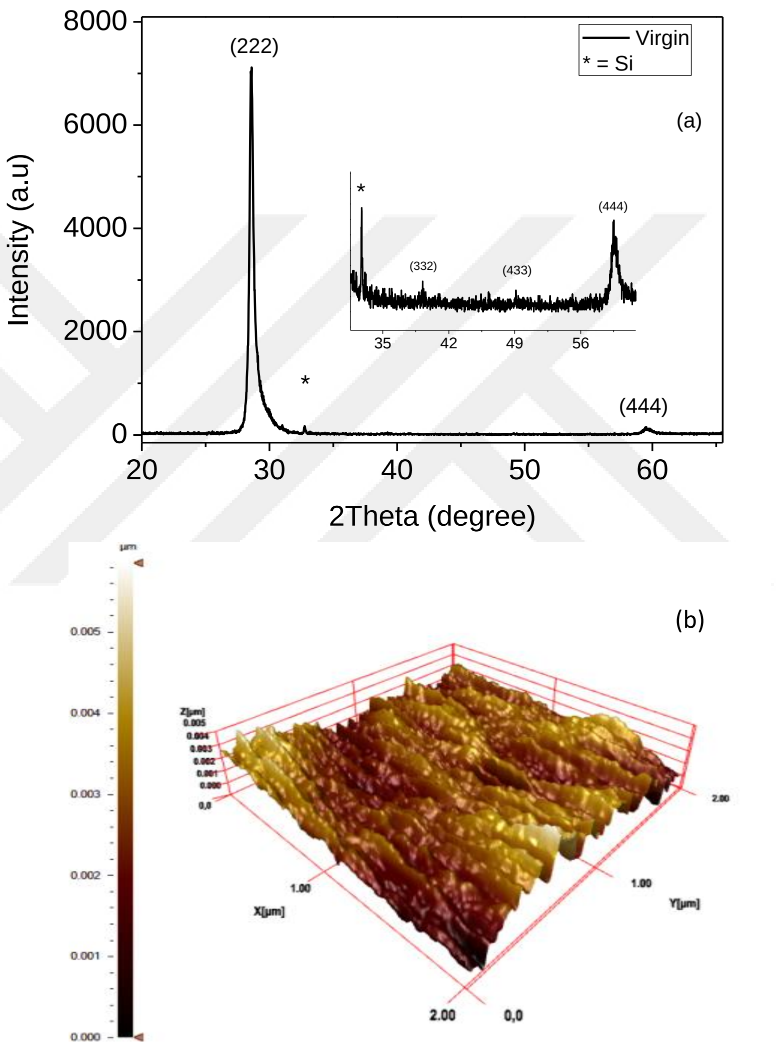
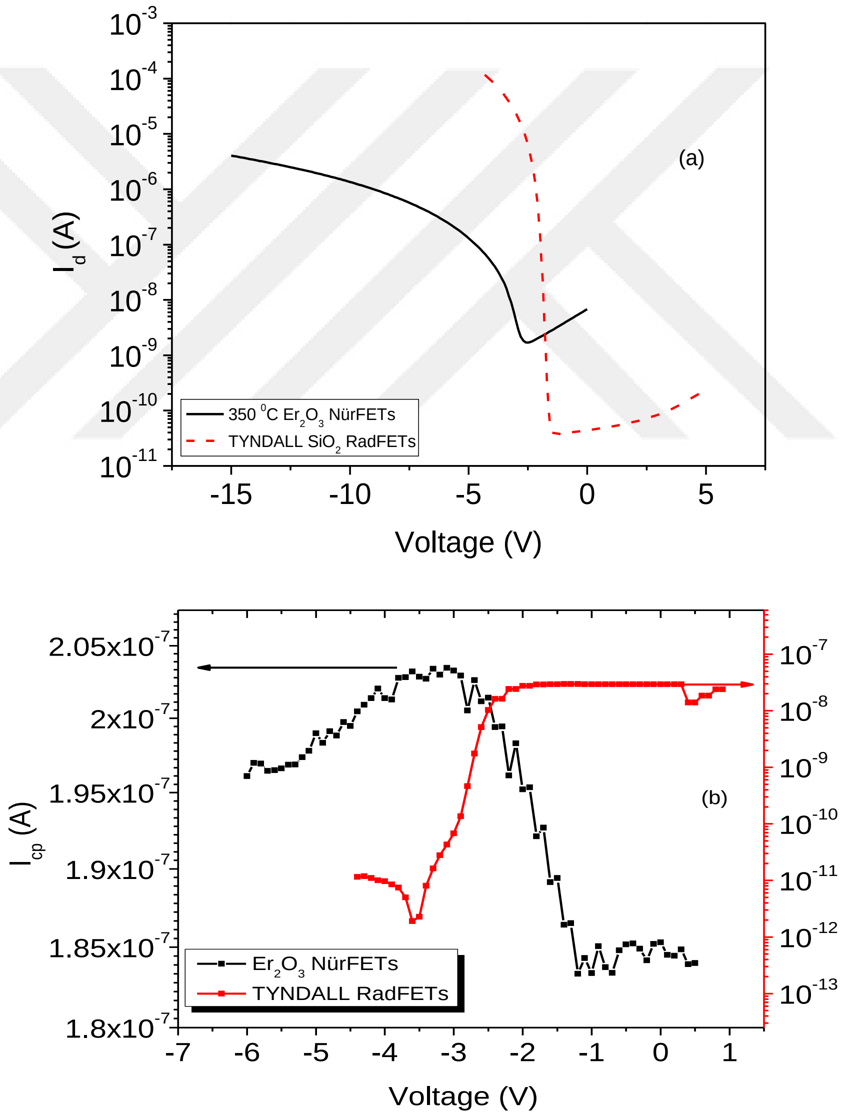


Figure 5.8: The (a) XRD and (b) AFM measurements of the deposited and annealed Er_2O_3/Si thin films.

The Er_2O_3 thin film was in amorphous phase before the annealing and it starts to crystalline after annealing. The peaks were indexed by International Centre for Diffraction Data (ICDD) base and the indexed peaks are in agreement with the peaks of the Er_2O_3 cubic phase with card no: 77-0463 (Kahraman et al., 2016). It has been observed that the films highly oriented in (222) and (444) orientations and minor peaks intensities were vaguely seen in enlargement of the XRD scans. In addition, the grain size of the films were calculated from broadening of intense peak (222) using Scherrer's equation (Kahraman et al., 2016), to be 22.15 nm. On the other hand, the AFM measurement is depicted in Figure 5.8 (b). The surface roughness (RMS) has been calculated and found to be 2.8 nm. The calculated RMS is relatively low compared to the Er_2O_3 thin films deposited by PVD methods (Kao et al., 2012; Mikhelashvili et al., 2004) indicating more uniform surface morphology has been obtained.



Figures 5.9: The (a) transfer current and (b) Charge pumping current measurements of the Er_2O_3 NürFETs, and TYNDALL-RadFETs

The initial electrical device parameters for assessment of Er_2O_3 NürFETs in microelectronics have been analyzed and the obtained results were compared to RadFETs having the same thick SiO_2 gate oxide. To do this, the I_d-V_{gs} and charge pumping measurements were performed and measurements are given in Figures 5.9 (a) and (b), respectively. As expected, no anomalous kinks have been observed in the transfer curves, although the large shift toward more negative values and higher transfer current has been observed at low voltages compared to SiO_2 MOSFETs. The reason of the higher transfer current at low voltages is associated with leakage effect (Gurfinkel et al., 2009; Rana et al., 2010) and the large shift is due to trapped charges in the device structure during the fabrication process (Kaya and Yilmaz, 2015).The V_{th} values for the devices are given in Table 5.4. Owing to trapped positive charges during the fabrication, initial threshold voltages of Er_2O_3 NürFETs are higher than conventional SiO_2 NürFETs.

Table 5.4 : The V_{th} and D_{it} parameters of studied devices before irradiation.

	V_{th} (V)	D_{it} ($x10^{10}cm^{-2}$)
Er_2O_3 NürFET	-9.00	8.51
TYNDALL- NürFET	-2.61	1.05

In addition, the initial interface traps (D_{it}) were calculated from Eq. 4.2 (Ristic et al., 2011), using the peak values in charge pumping curves in Figure 5.9 (b). The D_{it} values for the Er_2O_3/Si interface were tabulated in Table 5.4. This value is close to the conventional SiO_2/Si interface trap density and such low D_{it} values for Er_2O_3/Si interface have been also reported in the previous studies (Giangregorio et al., 2008; Kahraman et al., 2016).

5.2.2 Physical Modifications of the Er_2O_3 Gate Oxide under Irradiation Exposure

The measured XRD spectra of the films before and after gamma irradiation exposures are illustrated in Figure 5.10. Comparing the XRD measurements of the virgin and irradiated samples, no evident complex crystallographic change, such as phase transformation (Muller et al., 2003), have been observed for the given gamma radiation exposures. On the other hand, in the detailed analysis it has been observed that the most intense (222) peak has been narrowed and the peak values slightly shift toward the higher angles. These variations in the crystallites structure are due to radiation generated local heating and/or variations in the lattice planes caused from atomic displacement. In addition it is known that macro-stress causes line shifting, micro-stress causes diffraction line broadening/narrowing (Mallick et al., 2005). In other words, the gamma radiation does not have enough energy to break down the Er_2O_3 crystalline phase but it has still enough energy to displace the individual atoms of crystal from their lattice sites. This displacement occurs through kinetic energy transfer (El All et al., 2007) via scattering for the gamma irradiation and via elastic collision for secondary electron irradiation generated by gamma irradiation exposure. Vacancies and self- interstitial atoms, i.e., new defect and disordered regions are formed by irradiation result in this atomic motion (Korchuganov et al., 2016; Madiba et al., 2017; Sahasrabudhe et al., 2007).

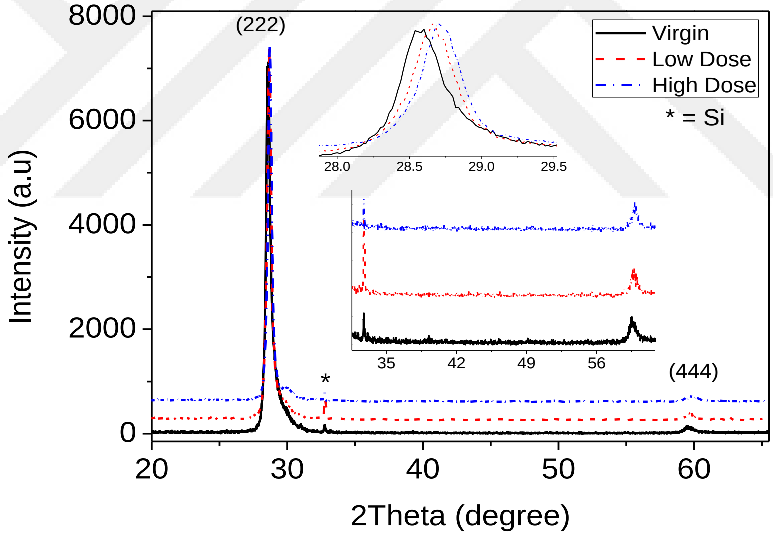
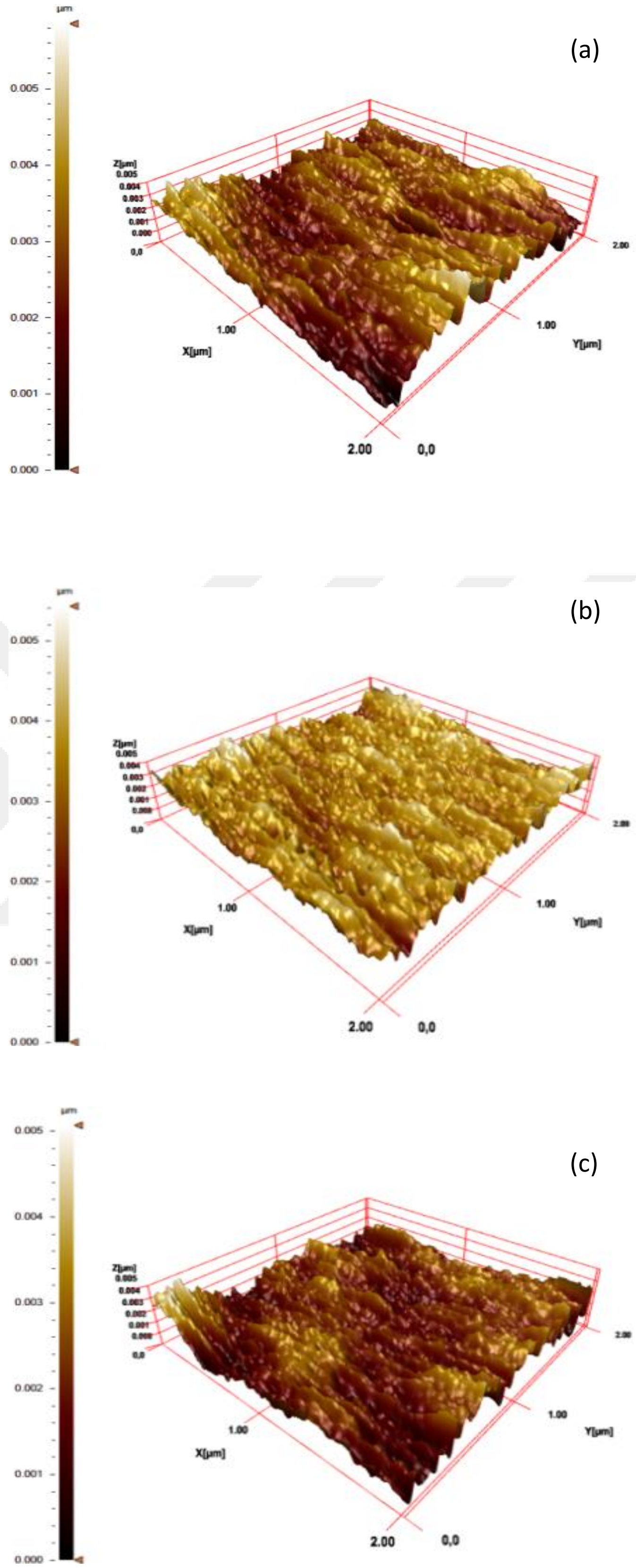


Figure 5. 10: Radiation effect on XRD characteristics of Er_2O_3 thin films

Changes in the grain size, (P), under radiation exposures has been also investigated by using the boarding of the (222) peak. The *P* values were calculated to be 22.15 nm, 22.76 nm and 24.10 nm for virgin, low dose exposed and high dose exposed samples, respectively. The released local heating (Galkin et al., 2013; Ishfaq et al., 2017; Laha et al., 2012) may cause microscopic immigration (El All et al., 2007) and this microscopic immigration combine the smaller grains in bigger cluster. Hence, rise in the P values may be attributed to presence of released local heating.



Figures 5.11: Variations in the AFM measurements for a- Virgin, b- Low dose exposed, c- High dose exposed Er_2O_3/Si thin films.

Since carrier scattering from the rough surface degrade the electrical conduction mechanism (Kim and Kim, 2002), the possible variations on the surface roughness under radiation should be examined. The film surface morphology under radiation exposures have been examined by AFM measurements which are illustrated in Figures 5.11 (a)- (c). No hillock and significant degradation have been observed. This indicates that the radiation induced surface stress and tension was not too high to degrade morphology (Vlasukova et al., 2017). In addition, the average surface roughness (RMS) found to be 2.8 nm, 2.5 nm, 2.2 nm for the virgin, low dose exposed and high dose exposed samples, respectively. The obtained results demonstrate that irradiation improves the surface roughness of the Er_2O_3 thin films. The improvement of the RMS values are correlated to the surface atoms under radiation exposure gain enough mobility to migrate to substrate (Kim and Kim, 2002). Hence, this microscopic immigration may reduce surface roughness. The rise in the grain size values and decrease in the surface roughness demonstrate that the exposed radiation doses improve the film uniformity and density (Wei et al., 2007).

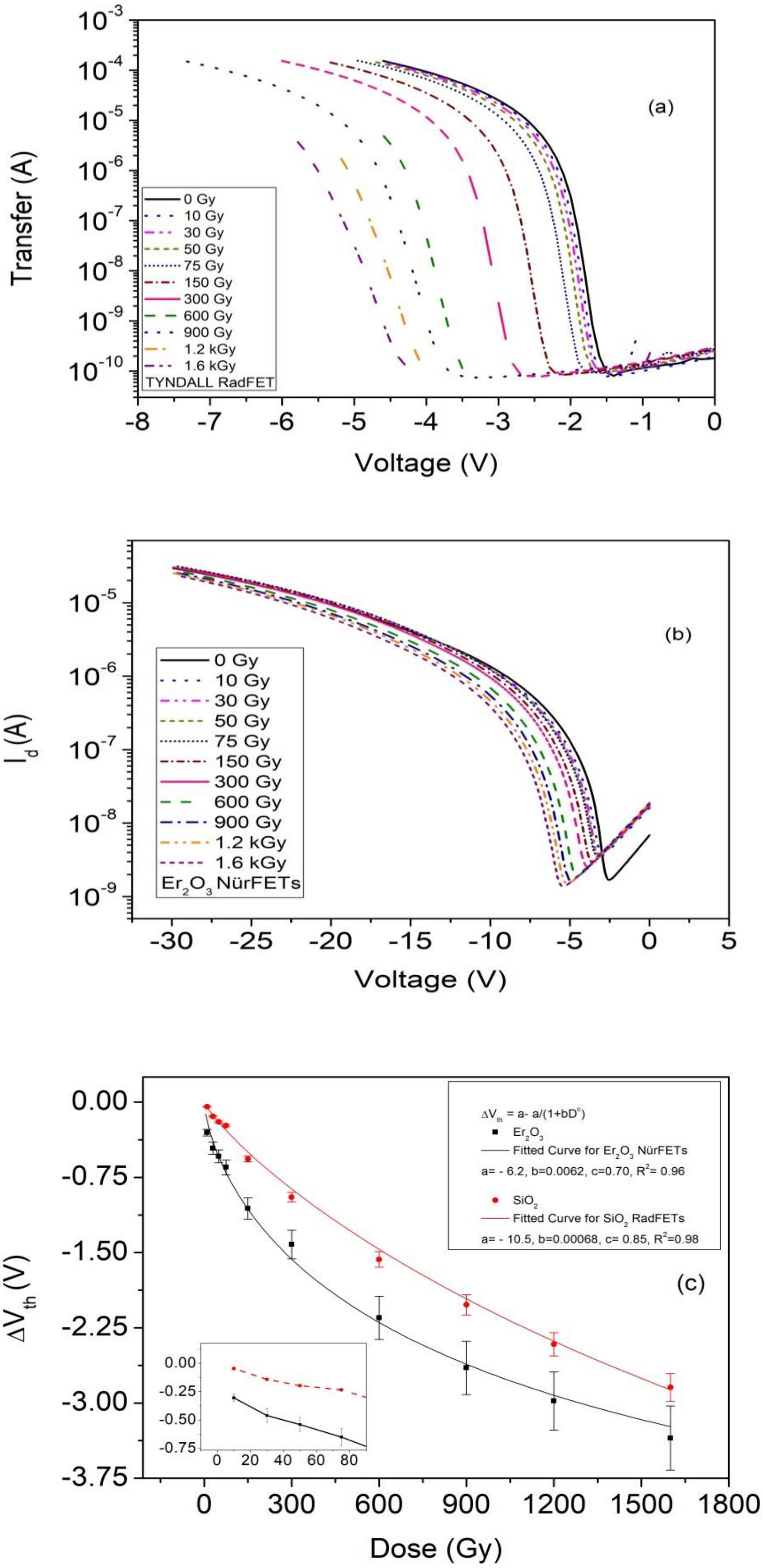
5.2.3 Radiation Induced Effects on Electrical Characteristics of Er_2O_3 NürFETs

The irradiation influences on the electrical I_d- V_g characteristics of SiO_2 RadFETs and Er_2O_3 NürFETs are illustrated in Figures 5.12 (a) and (b). Threshold voltage shift with respect to exposed irradiation doses is also given in Figure 5.12 (c). The I_d- V_g characteristics of the both devices shift toward more negative voltages. The irradiation responses of devices having SiO_2 gate dielectrics and the basic mechanism of the irradiation induced effects is well-known (Ma and Dressendorfer, 1989; Ristic, 2008). The brief mechanism is that irradiation generates numbers of new defects and electron-hole (e-h) pairs. Owing to higher mobility of e, they are easily swept out from the gate, while holes which escape initial recombination move toward SiO_2/Si interface where deep traps are located. Created defects and the trapped holes cause the shifts in threshold voltages as seen in Figure 5.12 (a). Similar negative voltage shift on the Er_2O_3 NürFETs under irradiation exposures indicates that the holes are trapped in the device structure (Jaksic et al., 2002a; Kahraman et al., 2016; Ma and Dressendorfer, 1989; Ristic et al., 2011). The detailed distributions of the ΔV_{th} – dose relations are illustrated in Fig. 5.12 (c).

Almost similar trend have been observed for both samples. Relatively large standard deviations shown in error bars for Er_2O_3 NürFETs are probably associated with device-to-device in process variations during the Er_2O_3 deposition by sputtering. The radiation induced shift in V_{th} (in Fig. 5.12 (c)) can be expressed by a fitted non-linear Equation given in following (Ristic et al., 2011);

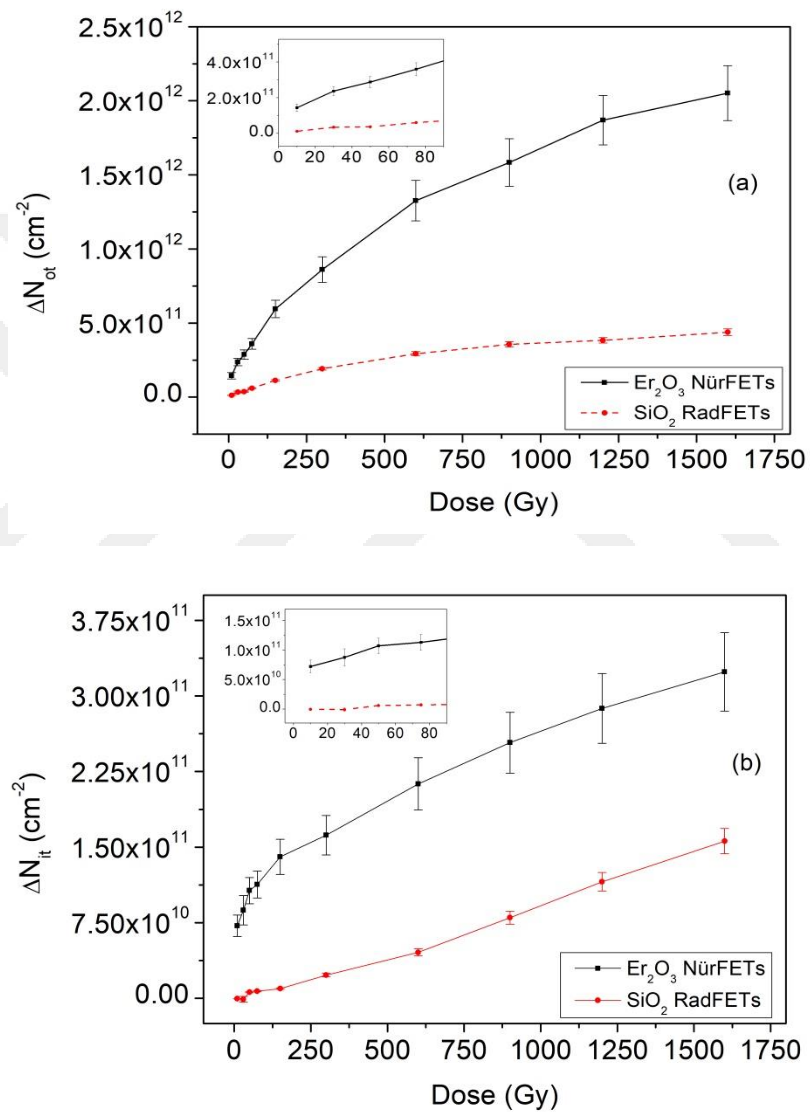
$$\Delta V_{th} = a - \frac{a}{1+bD^c} \tag{5.1}$$

the values of the fitting coefficients, a, b, and c, were found as shown in Fig. 5.12 (c). The high values of the goodness of fitness, (R^2), in Fig 5.12 (c) were demonstrating the obtained results are in good agreement with the model given by Eq. (5.1). The radiation sensitivity (S= $\Delta V_{th}/D$) of the Er_2O_3 is higher than that of SiO_2, and this is particularly pronounced at lower dose levels. For example, sensitivity of Er_2O_3 NürFETs at 30 Gy is 15 mV/Gy vs. only 4.6 mV/Gy for SiO_2 RADFETs. However, the SiO_2 RADFET's response is more linear with those than Er_2O_3 NürFET's as the latter's saturation is more pronounced (Yilmaz et al., 2017). Thus the difference in sensitivities decreases with dose up to 2.1 mV/Gy (Er_2O_3) vs. 1.88 mV/Gy (SiO_2) at 1600 Gy. In addition, the linearity of the ΔV_{th} – dose relations of devices decrease at higher doses. The accumulation of the radiation-induced oxide trapped charge leads to electric field screening at higher doses, causing the sub-linear behavior of the sensor (Martinez-Garcia et al., 2015; Yilmaz et al., 2017). On the other hand, it has been obtained that the sensor sensitivities of devices have been critically enhanced by using Er_2O_3 as a gate dielectric materials. To the best of our knowledge, these are the first data that show comparable sensitivities of transistors with high-k dielectrics to those with standard SiO_2, thus Er_2O_3 looks as a good candidate to replace SiO_2 in dosimetry. The radiation sensitivity of the dielectrics depends on several factors, such as the Z_{eff} constant of the gate dielectric, film quality, trapping efficiency, etc. Higher Z_{eff} number enhances the radiation interaction probability with gate dielectrics. Hence, larger number of initial hole yields and defects, where holes are trapped, can be generated. Higher sensitivity of the Er_2O_3 dielectrics is possibly associated with higher Z_{eff} value of Er_2O_3 than SiO_2. It should be noted that Z_{eff} is not only the factor to be enhance radiation sensitivity of devices. Some dielectrics, like HfO_2, have also higher Z_{eff} number than SiO_2 but they exhibits lower radiation sensitivity due to charge trapping distribution/efficiency (Dixit et al., 2007).



Figures 5.12: The I_d-V_g characteristics of a-) TYNDALL-MOSFETs, b-) Er_2O_3 MOSFETs under various Co-60 gamma doses, and c-) Threshold voltage shift dose relations for devices.

The irradiation induced oxide trapped charge (ΔN_{ot}) and interface trapped (ΔN_{it}) charge densities are illustrated in Figs. 5.13 (a) and (b). Both the ΔN_{ot} and ΔN_{it} distributions for the Er_2O_3 and SiO_2 devices enhance with irradiation doses. It has been seen that sign of trapped charges are positive for both dielectric and interface layer. It means that accumulation of the trapped holes enhance with enhancing irradiation doses.



Figures 5.13: Radiation induced a-) oxide trap density, and b-) interface trap density at various doses.

Due to this continuous and almost linear generation of hole and hole trap centers, the V_{th} voltage shift towards more negative values regularly. This radiation induced single type of hole trap centers (basically oxygen vacancies in Er_2O_3

obtained from radiation induced XPS analysis in following section) are contributes the radiation sensitivity of the high-k dielectric layer, significantly. Due some alternative gate dielectrics may trap both electrons and holes, or passivation of trapped charges observed under radiation exposures (Dixit et al., 2007; Kahraman and Yilmaz, 2017), the device sensitivity and dosimetric applications of high- k based devices decrease. Moreover, large numbers of the charges are trapped in dielectric layer, comparing the number of ΔN_{ot} and ΔN_{it} for both Er_2O_3 and SiO_2 dielectrics. This demonstrate that oxide trapped charges are dominates the V_{th} shift. In addition, the number of both types of trapped charge is by far the high in Er_2O_3 samples. Higher densities of the trapped charges are correlated to higher density and Z_{eff} number of Er_2O_3 which enhance the radiation absorption probability of materials. The Monte Carlo simulation results have been also confirmed the energy deposition in the dielectric and electron-hole generations are significantly enhanced in high-k dielectrics (Dasgupta et al., 2010; Kahraman et al., 2015a). Therefore, the negative charge traps at low doses at interface (in Figure 5.13 (b)) decrease the device sensitivity of Er_2O_3 NürFETs. Therefore, studies should be focused on the improvement of interface quality and enhance positive charge trap sites at lower doses to enhance the Er_2O_3 NürFETs sensitivity in radiation sensor applications.

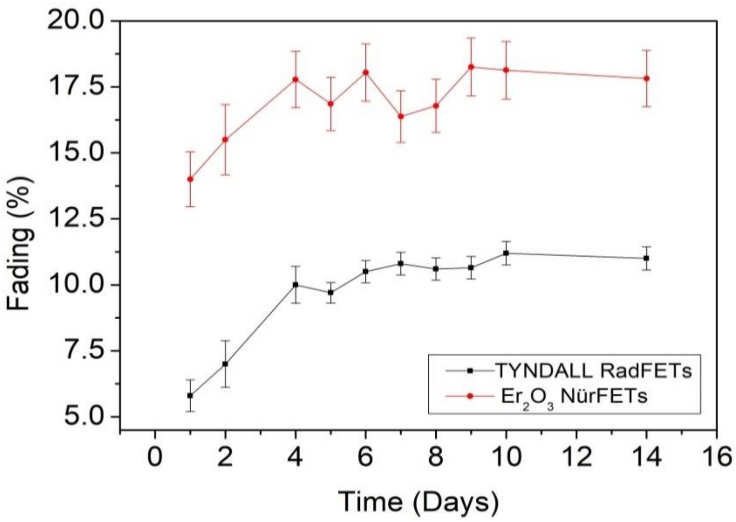


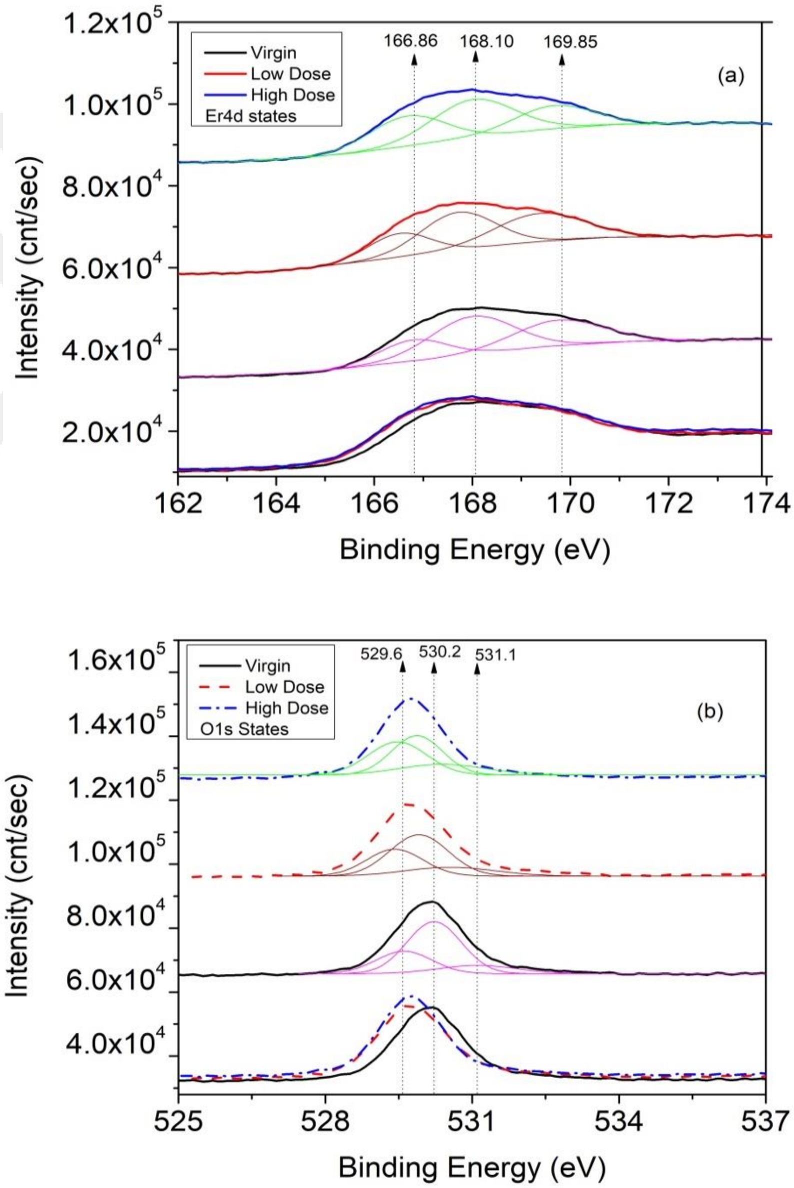
Figure 5.14: The post-irradiation fading values of the TYNDALL RadFETs and Er_2O_3 NürFETs

The long term stability of ΔV_{th} after irradiation exposures is also crucial parameter for the reliability of NürFET devices to be used in the pMOS dosimeters.

The fading characteristics of devices have been obtained at room temperature after the total radiation exposed doses. The measured fading characteristics are illustrated in Figure 5.14. The 10% percentage even above fading characteristics is in harmony with the literature for the SiO_2 RadFETs (Pejovic et al., 2013; Ristic et al., 1995). The percentages of the fading are associated with the recombination of the trapped charges basically located in the shallow trap sites which were degrade the threshold voltages shift in dosimetric purposes (Yilmaz et al., 2017). Both of the two SiO_2 and Er_2O_3 dielectrics exhibited the fading characteristics, but Er_2O_3 has a bit larger fading values. Large numbers of the charges are trapped in both oxide and interface in the Er_2O_3 NürFETs. Thus, it may be normal to observe higher recombination of the trapped charges. In addition, the higher fading values of device also demonstrate that the number of the shallow trap sites at Er_2O_3 dielectrics is relatively higher than SiO_2 dielectrics.

5.2.4 Radiation Effects on Er_2O_3/Si Interface Chemistry

The variations in the chemical compositions and the generation/breaking bond under irradiation exposure have been investigated by XPS spectra of the virgin and gamma exposed the Er_2O_3 films. During the XPS analysis, all peaks were calibrated to C 1s peak at 284.5 eV to eliminate the possible charging effect that may occur due to surface contamination. The measured XPS spectra of Er 4d and O 1s XPS core level spectra for prior to irradiation are illustrated in Figures 5.15 (a) and (b), respectively. In the general view, it can be seen that the Er4d, and O1s have more than one single peak, which indicates the existence of the multi-oxidation states in core levels of Er4d and O1s. Therefore, the sub-peaks have been revealed by peak de-convolution to obtain accurate discussion. The de-convoluted sub-peaks are also illustrated in Figures 5.15 (a) and (b). The sub oxidation states of the elements have been discussed using their binding energies. Binding energy (BE) represents the difference in energy between the ionized and neutral atoms. For each and every element/compounds, there exists a characteristic binding energy associated with each core atomic orbital i.e. each element gives a characteristic set of peaks in the photoelectron spectrum at kinetic energies determined by the photon energy and the respective binding energies. Hence, using the binding energy and its intensity variations of a photoelectron peak, the elemental composition, chemical sub-oxidation and electronic state of elements can be analyzed (Zhang et al., 2008). As seen from Figures 5.15 (a), the first peak of Er has been observed at 166.8 eV BE. It is known that metallic bonding energies of the element have lower BE than their oxidation states due to the less coulomb interaction between the photo-emitted electron and the ion core (Zhang et al., 2008). Hence, since oxidized Er binding energy has been obtained at 168 eVs, the observed Er sub-peak in Figure 5.15 (a) having 166.86 eV possible belongs to metallic Er bonding in Er-Er and/or Er-Si rather than Er-O bonds for the virgin sample (Gokhale et al., 1990; Powell, 2012).



Figures 5.15: XPS spectra of a-) Er4d core level and b-) O1s core level of the virgin and gamma irradiated Er_2O_3 thin films.

In the previous studies, Guerfi et al. have reported (Guerfi et al., 2005) that Er4d peak in Er_2O_3 observed to be 170.4 eV BE, while Xu et al. have reported (Xu et al., 2012) that Er4d peak in Er_2O_3 observed at 168.8 eV BE and higher BE than this values for Er4d states belongs to silicate containing bonds. For the present study, considering the virgin sample peak intensity of Er4d states having 169.86 eV BE in Figures 5.15 (a) and fabrication condition, i.e. low annealing temperature, the intense silicate formation could not be seen. Hence Er4d states having 169.85 eV BE in Figure 5.15 (a) together with O1s states having 530.2 eV (Technology, 2017) in Figure 5.15 (b) can be attributed to Er- O bonds in Er_2O_3. The oxide bonds in the vicinity of the $O^{\sigma-}$ have lower binging energies compared to their fully oxidized states (Prasanna et al., 2014; Wang et al., 2011). Therefore, the sub peaks of Er4d having 168.1 BE and O1s having 529.6 eV BE can be attributed to the $O^{\sigma-}$ defect related Erbium sub oxide (Er_xO_y) bonds. On the other hand, the remaining sub- O peak corresponds to 531.1 eV BE may belong to interfacial O atoms in non-stoichiometric SiO_x and also may be $ErSi_xO_y$ and/or bonds (Kao et al., 2012) in the virgin sample. As expected, the changes in the oxidation states have been observed under gamma irradiation influences. The net changes of the binding energies of the all Er4d and O1s states have been shift toward lower energies compared to virgin sample. The shifts to lower energies indicate that the oxidation of the elements one order reduce and the more metallic bonding states occurs.Although the net lower binding energy shift compared with virgin sample, a rise in the binding energies of sub Er4d states located approximately 168.1 eV and 169.85 eV BE from low dose to high dose exposures may be attributed to formation of new Er sub oxide (Er_xO_y) bonds due to incorporation of oxygen (Yan et al., 2016; Yang et al., 2011) thanks to generated local heating by irradiation. The intensity change of the O1s states has been observed more obviously than E4d states indicating the oxygen is more sensitive to the radiation exposure (Ishfaq et al., 2017). On the other hand, areal intensities indicate that the amount of oxygen deficient Er_xO_y peaks (sub O1s states having approximately 529.6 eV BE and Er4d states having approximately 168.1 eV BE) and Er-Si peak increase, while amount of the Er_2O_3 bonds (sub O1s states having approximately 520.2 eV BE and Er4d states having approximately 169.86 eV BE) decrease with irradiation exposures. Slight rises on the possible SiO_x and/or $ErSi_xO_y$ have been also observed under irradiation exposure. Briefly, these intensity changes and BE shifts demonstrate that predominantly irradiation breaks the Er_2O_3

bond and forms the oxygen deficient Er_xO_y. Furthermore, some Er_2O_3 or Er_xO_y is also broken by irradiation which is generated the metallic Erbium bonds. This variation points out the presence of oxygen vacancy enhance with irradiation influence. The generation of oxygen vacancy may dominate the oxide charge trapping where mobile holes can be trapped (Ding et al., 2014). These accumulations of the trapped holes cause the observed threshold voltage shift for the Er_2O_3 NürFETs.

6. CONCLUSIONS AND RECOMMENDATIONS

In this dissertation, usability of HfO_2 and Er_2O_3 high-k dielectrics in the Nuclear Radiation Sensing Field Effect Transistors as gate dielectric materials has been investigated. Following the initial device assessment, the device performance and possible degradation mechanism in radiation environment have been also discussed. The major conclusions obtained from this work are listed in following:

The outcomes for the HfO_2 NürFETs by comparing the SiO_2 NürFETs and TYNDALL RadFETs

- The initial interface trap density was found to be 1.88×10^{12} cm^{-2} for cubic crystalline phase HfO_2 MOSFETs, which is convenient for microelectronic applications.
- The XRD measurements for HfO_2/Si gate stack have been demonstrated that intensity of the peak oriented in (-111) direction enhances with enhancing the irradiation dose, while other minor peaks remains almost constant. In addition, the P value also enhances with the radiation exposures. This observation is associated with the changes in the lattice volume due to crystallization after high energy impact of gamma irradiation.
- The slight rises in the RMS values of HfO_2/Si gate stack have been observed by enhancing the irradiation doses. The rises in the RMS values are presumably owing to the swelling caused by the gamma irradiation. The radiation energy cause volume enlargement because of crystallizations of the amorphous track in the oxide structure.
- Only the very slight threshold voltage shift toward negative values has been observed during the irradiation test of the HfO_2 NürFETs, while large and continuous shifts have been observed as expected in SiO_2 NürFETs and RadFETs. The sensitivity of the SiO_2 gate dielectrics has been found to be more than 10 times higher than that of the comparable HfO_2 layer.
- Both passivation and trap generation behavior have been observed from XPS analysis of HfO_2/Si gate stack. The passivation of the dangling bonds dominates the radiation influence at lower doses, while trap generation due to oxygen bond breaking in O-Hf-O and Si-O states dominates the radiation

influences at higher doses. The passivation of the dangling bonds reduces the radiation sensitivity of the HfO_2 MOSFETs. In addition, the observed small shift toward negative voltages due to breaking of oxygen bonds in HfO_x and SiO_x caused oxygen vacancy where holes can be trapped.

- The obtained results indicate that HfO_2 is almost insensitive to the irradiation and HfO_2 is suitability to be used in radiation environments, e.g. for space/nuclear applications. as a radiation hard gate dielectric materials.

The outcomes for the Er_2O_3 NürFETs by comparing the TYNDALL RadFETs

- The initial D_{it} values were calculated to be $8.51x10^{10}$ cm^{-2} for cubic crystalline phase Er_2O_3 NürFETs, which is convenient for microelectronic applications.
- No evident complex crystallographic changes, like phase transformation, have been observed for the given gamma radiation exposures. On the other hand, the peak values slightly shift toward the higher angles due to the atomic displacement in the Er_2O_3 lattice with irradiation. In addition, the P value also slowly enhances with the radiation exposures due to generated local heating by radiation exposure.
- Irradiations improve the surface roughness of the Er_2O_3 thin films. The improvements of the RMS values were correlated with the surface atoms which gain enough mobility to migrate to substrate under radiation exposure. Hence, this microscopic immigration may reduce surface roughness. The rise in the grain size values and decrease in the surface roughness demonstrate that the exposed radiation doses improve the film uniformity and density.
- The V_{th} values are shifting toward the more negative voltages for both of Er_2O_3 and SiO_2- based devices due to accumulation of positive trapped charges. The linearity of the dose and ΔV_{th} relation of Er_2O_3 NürFETs is good as SiO_2 RadFETs. The devices' sensitivity of Er_2O_3 NürFETs is significantly higher than SiO_2 RadFETs. In addition, the higher positive charge trapped densities have been observed in the Er_2O_3 dielectric layer comparing to SiO_2, as expected.
- Electrochemical characterizations reveal that oxidation states are shifting more metallic bonding states. In other words, radiation breaks basically the Er_2O_3 bond and form the oxygen deficient Er_xO_y. Also, some Er_2O_3 or Er_xO_y were also broken and the metallic Erbium bonds (Er-Si or Er-Er) are

generated under radiation exposures. These changes imply the vicinity of oxygen in the structure enhances with irradiation exposures. The irradiation, generated oxygen vacancies where holes are trapped, has significant influence on the threshold voltage shift of the Er_2O_3 NürFETs.

- These initial results are demanding for the possible usage of Er_2O_3 to be used in pMOS dosimeter as new gate dielectric materials. The observed remarkable rise in the device sensitivities can be milestone for the improvement of the pMOS dosimeters, but the more investigations and different fabrication conditions should be performed in order to enhance device reliability.

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List of Publications

International Publications (In SCI)

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18- Saleh Abubakar, **Senol Kaya**, Aliekber Aktag and Ercan Yilmaz, Yttrium Oxide Nanostructured Thin Films Deposited by Radio Frequency Sputtering: The Annealing Optimizations and Correlations between Structural, Morphological, Optical and Electrical Properties, J Mater Sci: Mater Electron (2017) 28:13920–13927

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2- S. Kaya, A. Aktag and E. Yılmaz, Structural and Electrical Characterizations of $BiFeO_3$ MOS Capacitor, 2nd Global Conference on Materials Science and Engineering (CMSE 2013), November 20-22, 2013, Xianning, China. (Oral)

3- S. Kaya, H. Malkaş and E. Yılmaz, Influence of Sputtering Temperature on Surface Morphology of CdZnTe Thin Film, International Semiconductor Science & Technology Conference ISSTC 2014, January 13-15, 2014, Istanbul, Turkey. (Oral)

4- A. O. Cetinkaya, **S. Kaya**, E. Yilmaz, N. D. Vasovic, A. Jaksic, C. Jackson, R. Duane, " Miniature silicon photomultiplier (SIPM) based scintillator system for low power high performance detection applications", Second International Conference on Radiation and Dosimetry in Various Field of Research RAD2014, May 28-30, 2014, Nis, Serbia. (Poster)

5- S. Kaya, A.O. Cetinkaya, A. Aktag and E. Yılmaz, Effects of Gamma-Ray Irradiation on Interface States and Series-Resistance Characteristics of Si_3N_4 MIS Capacitors, Second International Conference on Radiation and Dosimetry in Various Field of Research RAD2014, May 28-30, 2014, Nis, Serbia. (Oral)

6- S. Kaya, A.O. Cetinkaya, A. Kahraman, H. Karacali, A. Aktag and E. Yılmaz, Usability of Sm_2O_3 as a Dielectric Layer in MOS-Based Applications, MRS Spring Meeting and Exhibit 2015, April 6-10, San Francisco, USA. (Poster)

7- A.O. Cetinkaya, **S. Kaya**, H. Karacali, A. Aktag and E. Yılmaz, Investigating Sm_2O_3 Thin Films In Terms Of Sputtering Power And Substrate Temperature, MRS Spring Meeting and Exhibit 2015, April 6-10, San Francisco, USA. (Poster)

8- A. Kahraman, **S. Kaya**, A.O. Cetinkaya, A. Aktag R. Turan and E. Yilmaz, "Effects of Package Materials on the Sensitivity of RadFET for Electron and Photon Sources", Third International Conference on Radiation and Dosimetry in Various Field of Research RAD2015, June 8-12, 2015, Budva, Montenegro. (Oral)

9- S. Kaya, E. Yilmaz, R. Lok, A. Aktag, H. Karacali, A Detailed Investigation on the Electrical Characterization of the ZrO_2 MOS Capacitors, MRS Spring Meeting and Exhibit 2016, 28 March- 01 April, 2016 Arizona, USA (Poster).

10- E. Yilmaz, **S. Kaya**, R. Lok, A. Aktag, H. Karacali, and A. Jaksic, New-Generated Nuclear Radiation Sensing Field Effect Transistor (NürFET) for Irradiation Detection, Forth International Conference on Radiation and Dosimetry in Various Field of Research RAD2016, May 23-27, 2016, Nis, Serbia. (Oral)

11- S. Kaya and E. Yilmaz, Fabrication Optimization of ZrO_2 Thin Films Deposited onto Si by Reactive Sputtering for Microelectronic Technologies, Cost To-Be Fall Meeting 2016, 28- 30 September, City Hotel, Ljubljana, Slovenia (Poster).

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National Publications

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