ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN OF SLEW-RATE CONTROLLED DIFFERENTIAL OUTPUT DRIVER

M.Sc. THESIS

Atılım ERGÜL

Department of Electronics and Communications Engineering

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Thesis Advisor: Prof. Dr. Ali Toker

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YÜKSEK LİSANS TEZİ

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Atılım ERGÜL, a M.Sc. student of ITU Graduate School of Science Engineering and Technology 504121356 successfully defended the thesis entitled **"DESIGN OF SLEW-RATE CONTROLLED DIFFERENTIAL OUTPUT DRIVER"**, which he/she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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Date of Submission : **04 May 2015**
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To the memory of my father,

FOREWORD

First of all, I would like to express my appreciation to my supervisor Prof Dr. Ali Toker for his guidance and encouragement.

I would like to thank my co-workers from MKR-IC, for their discussions and supports. They give me a new insights to solve several problems in my thesis.

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Finally, I would like to inform that this thesis is dedicated to the memory of my beloved father, Ahmet Ergül. It is your shining example that I try to emulate in all that I do. Thank you for everything.

May 2015 Atılım ERGÜL

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ABBREVIATIONS

CMOS	**:** Complementary Metal Oxide Semiconductor
CTAT	**:** Complementary to Absolute Temperature
DC	**:** Direct Current
DC-DC	**:** Direct Current to Direct Current
DLL	**:** Delay Locked Loop
D/A	**:** Digital to Analog
FPGA	**:** Field Programmable Gate Array
I/O	**:** Input/Output
MOS	**:** Metal Oxide Semiconductor
MIM	**:** Metal-Insulator-Metal
OPAMP	**:** Operational Amplifier
PMOS	**:** P-Channel Metal Oxide Semiconductor
PTAT	**:** Proportional to Absolute Temperature
PVT	**:** Process-Voltage-Temperature
QFN	**:** Quad Flat No-leads
XFAB	**:** X-FAB Silicon Foundries

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LIST OF SYMBOLS

μm	:	Micrometer
mm	:	Milimeter
nm	:	Nanometer
ppm	:	Part per Million

DESIGN OF
SLEW-RATE CONTROLLED
DIFFERENTIAL OUTPUT DRIVER

SUMMARY

In the last two decades, usage area of integrated circuits have been gradually increased with the developments in the process technology. Moreover, Due to developments in process technology, the area of integrated circuit is reduced and digital blocks has been able to switch at high speeds.

Although the switching activities is performed in the digital blocks of the integrated circuit, these activities may reveal an undesired noise which effects the performance of both analog and digital blocks in the integrated circuits. This noise is called as a simultaneous switching noise or inductive noise. The simultaneous switching noise increases depending on the frequency of switching activity and the amount of a current which sourced to a load. Various techniques is proposed to solve this phenomena up to the present. However, the proposed circuits provides solution for specific application and they can not create the desired effect for different load types. For instance, inductive loads cause an voltage spikes at the output signals when they are driven by a rapid current changes. This ringings reveal an distortion at the output signals, even they may reach the voltage levels which cause an permanent damage to the circuit

In this study, an output driver structure, which is capable to drive low impedance load in a controlled manner, is discussed. The sensitivity to the simultaneous switching noise is reduced by adding a slew rate and amplitude control system to the circuit. Moreover, the circuit is optimized to drive inductive loads which is common element in the industrial applications. Proposed output driver is implemented with XFAB's $0.35\,\mu$m CMOS process with high voltage option. Drain terminal breakdown voltage of high voltage transistors is 10 V. Designed circuit consumes 52.8 mW in the high power mode and 33 mW in lower mode under typical conditions. These values does not represents the power which is transferred to the load. The current transferred to the load is maximum 200 mA in the high power mode and maximum 100 mA in the low power mode. Total area of the chip is $2x2.45\,\text{mm}^2$ and it consists two output drivers which are independent from each other.

YÜKSELME EĞİMİ KONTROLLÜ FARKSAL CIKIS SÜRÜCÜSÜ TASARIMI

ÖZET

Son yirmi yıl içerisinde, üretim teknolojilerinin gelişmesiyle elektronik sistemlerdeki tümdevre kullanım alanları giderek artmıştır. Buna ek olarak, gelişen üretim teknolojileri, tümdevre boyutlarının küçülmesine ve tümdevrelerde bulunan sayısal blokların yüksek hızlarda anahtarlanabilmesine sebep olmuştur.

Anahtarlama işlemleri her ne kadar sayısal devrelerde gerçekleştirilse de, eşzamanlı anahtarlama işlemleri tümdevrenin sayısal ve analog bloklarının performansına etki edebilecek şekilde gürültü ortaya çıkarmaktadır. Bu gürültü eşzamanlı anahtarlama gürültüsü veya endüktif gürültü olarak adlandırılmaktadır. Gürültünün sebebi, kırmık üzerindeki bağalama noktaları ile buna eşdeğer düşen paket üzerindeki bağlama noktaları arasında gerçekleştirilen bağlama hatlarıdır. Bu hatların uzunluğu 2mm ile 5mm arasında değişmekte ve elektriksel olarak endüktans olarak davranmaktadırlar. Eşzamanlı anahtarlama gürültüsü, anahtarlama olayının frekansı ve çıkış yüküne basılacak olan akım miktarına bağlı olarak artmaktadır. Bu sebeple, eşzamanlı anahtarlama gürültüsünün en baskın olduğu sistemler çıkış sürücülerinin bulunduğu sistemlerdir. Çıkış sürücüleri, alıcı tarafında bulunan yük empedansını sürebilmek için kullanılmaktadır. Alıcı katınını girişinde bulunan yüksek empedansı genellikle düşük değerli bir empedans olmaktadır. Düşük değerli yük empedansı üzerinde istenlien gerilim salınımı sağlayabilmek için yüksek miktardaki akımın kısa bir süre içerisinde besleme üzerinden yüke aktarmaktadırlar. Dolayısıyla sistem içerisinde yüksek miktarda eşzamanlı anahtarlama gürültüsüne sebep olmaktadırlar. Özellikle gürültü etkisinin önemli olduğu sistemlerde, örneğin analog-sayısal çeviriciler, sayısal-analog çeviriciler, sensörler v.b. blokların bulunduğu sistemlerde, sistem içerisinde oluşan eşzamanlı anahtarlama gürültüsü çıkış işaretlerinde bozulmaya sebep olmakta ve sistemin gürültü marjını azaltmaktadır.

Günümüze kadar, bu problemin çözülebilmesi için farklı devre yöntemleri önerilmiştir. Fakat önerilen devre yapıları uygulamalara özel çözümler sunmakta ve farklı yük koşulları için istenilen etkiyi yaratamamaktadır. Buna ek olarak, önerilen bu yapılar endüktif yükleri sürebilecek şekilde optimize edilmemişlerdir. Endüktif yükler, endüstri ve otomotiv alanlarında yaygın bir şekilde kullanılmaktadır. Bu yükler, entegre devre dışında gerçeklendiği için çok yüksek kalite faktörlerine sahiptirler. Ayrıca bu entegre dışından gerçeklenen endüktansların değerleri mH'lere kadar varmaktadır. Bunların sonucu olarak, endüktif yükler hızlı akım değişiklikleri ile sürüldüğü takdirde, çıkış işaretlerinde yüksek zaman sabitli ve yüksek genlikli çınlamalara sebep olabilmektedir. Bu çınlamalar çıkış işaretlerinin bozulmasına sebep olmakla birlikte, devrede bulunan aktif devrelere kalıcı zarar verebilecek seviyelere kadar çıkabilmektedir.

Bu çalışma kapsamında, düşük empedanslı yükleri kontrollu bir şekilde sürebilmek için bir çıkış sürücüsü yapısı ele alınmıştır. Devrenin oluşturacağı anahtarlama gürültüsünü azaltabilmek amacıyla yükselme eğimi kontrol sistemi devreye eklenmiştir. Yükselme eğimi kontrol sistemi, gecikme hücreleriyle kontrol edilen anahtarlar ile gerçeklenmiştir. Bu anahtarlar ile belirli zaman dilimlerinde belirli akım kaynakları aktive edilmiştir. Böylelikle çıkış işaretinde sabit yükselme eğimi elde edilmiştir. Çıkış işaretlerinin lineerliğini iyileştirebilmek için genlik kontrol sistemi kullanılmıştır. Genlik kontrol sistemi çıkış işaretinin belirli bir değeri aşamasını engelleyerek, çıkış transistörülerinin V_{DS} gerilimlerinin $V_{DS_{sat}}$ değerinin altına düşmesinin önüne geçmiştir. Genlik kontrol sistemi, devrenin yükselme eğimi kontrol sistemi ile entegre halde çalışabilecek şekilde gerçeklenmiştir, böylelikle çıkış işaret seviyesindeki değişimler, işaretin yükselme eğimine etki etmemiştir. Ayrıca, genlik kontrol sistemi, devrenin çıkışında yükten bağımsız olarak sabit bir genlik elde edebilmek için kullanılabilmektedir. Devrenin sıcaklık ile sabit yükselme eğimine sahip olabilmesi için, devre içerisine sıcaklık sezici bir yapı gerçeklenmiştir. Sıcaklık sezici yapı ile, belirli sıcaklıklar için gerekli kompanzansyon akımını oluşturarak, çıkış sürücüsü devresinde, -55° ile 125°C sıcaklık aralığında sabit yükselme eğimi elde edilmesi amaçlanmıştır. Sıcaklık sezici devresinden üretilen geri besleme sinyali, üretim prosesinde bulunan negatif ve pozitif sıcaklık katsayılı dirençler yardımıyla oluşturulmuş akımların belirli oranda toplanılması sonucu elde edilmiştir. Tasarlanan devre resistif ve endüktif yükleri sürebilecek şekilde optimize edilmiştir. Simulasyonlar sırasında endüktif yük olarak transformatör kullanılmıştır. Ölçümlerde kullanılacak olan transformatör, empedans analizörü ve devre analizörü kullanılarak modellenmiştir. Böylelikle simulasyonlarda bu modelden yararlanılarak devrenin endüktif yük sürerken performansı incelenebilmiştir. Modellenen transformatörün primer katındaki kaçak endüktansı $0.2\,\mu$H sekonder katındaki kaçak endüktansı ise $5\,\mu$H değerindedir. Manyetik çekirdek endüktansı ise primer tarafında 4.5 mH, sekonder tarafında ise 28.4 mH'dir. Modelleme pasif devre elemanları ile gerçekleştirilmiş ve 2. derece etkiler göz ardı edilmiştir. Buna rağmen modellenen devrenin ölçüm ile simulasyon sonuçları karşılaştırıldığında %95'e varan doğruluk gözlemlenmiştir. Önerilen çıkış sürücüsü yapısı yüksek gerilim dayanımlı transistörlerin de bulunduğu $0.35\,\mu$m CMOS teknolojisi kullanılarak tasarlanmış ve üretilmiştir. Devrede kullanılan yüksek gerilim dayanımlı transistörlerin savak kırılma gerilimleri 10 V olarak verilmiştir. Önerilen devre, literatürde önerilmiş olan devrelerden, genlik kontrolü ve eğim kontrolünün birbirine entegre çalışması, endüktif yükleri sürebilmesi ve -55° ile 125°C aralığında sabit yükselme eğimine sahip olması ile ayrılmaktadır. Tasarlanan devrenin tipik koşullar altındaki güç harcaması, yüksek güç harcaması konfigurasyonu altında 52.8 mW, düşük güc harcaması konfigurasyonu altında 33 mW olmaktadır. Bu değerler yüke aktarılan güçten bağımsız elde edilen değerlerdir. Yüke aktarılan akım, yüksek güç harcaması konfigurasyonu için maksimum 200 mA, düşük güç harcaması konfigurasyonunda ise maksimum 100 mA olmaktadır. Tasarlanan entegre 2MHz giriş işareti frekansına kadar çalışabilmektedir. Tasarlanan entegre devrenin yüzey alanı $2x2.45\,\text{mm}^2$'dir ve içerisinde birbirinden tamamen izole iki adet sürücü bulunmaktadır. Bu iki izole sürücü tamamen farklı besleme gerilimi hatlarına ve toprak hatlarına sahiptir. Giriş ve çıkışları da birbirlerinden bağımsızdır. Her bir sürücü devresinin referans akım ve gerilim üretçeleri de birbirinden bağımsızdır. Tasarlanan devre tipik simulasyon koşullarında $8\,\Omega$'luk yük sürerken, yükselme eğiminin değeri $8\,\text{V}/\mu\text{s}$ olmaktadır. Aynı koşullar altında yapılan serim sonrası simulasyonlarda yükselme süresi değeri

$7.6\,\mathrm{V}/\mu\mathrm{s}$ olarak elde edilmiştir. Gerçeklenen devrenin ölçüm sonuçlarında ise $7.4\,\mathrm{V}/\mu\mathrm{s}$ yükselme eğimi elde edilmiştir. Sürücü devre 1:2.5 primer - sekonder oranlı trafo ile yüklü iken trafo sekonderi $200\,\Omega$'luk yük ile sonlandırılmıştır. Bu değer primer tarafında diferansiyel $32\,\Omega$'luk değere denk düşmektedir. Belirtilen yük durumu için çıkış işaretinin yükselme eğimi $16\,\mathrm{V}/\mu\mathrm{s}$ değerindedir. Aynı koşullar altında %95 doğruluklu trafo modeli kullanılarak yapılan serim sonrası simulasyonlarda $15.6\,\mathrm{V}/\mu\mathrm{s}$ yükselme eğimi olarak gözlemlenmiştir. Ölçümlerde ise $15.4\,\mathrm{V}/\mu\mathrm{s}$'lik yükselme eğimi değeri elde edilmiştir. Yükselme eğiminin sıcaklıkla değişimini incelemek üzere, tümdevre endüstriyel bir fırın içerisinde ısıtılıp soğutulmuştur. Yapılan ölçümler sonucu yükselme eğiminin -40° ile 80°C sıcaklık aralığında yaklaşık olarak %4 değiştiği gözlemlenmiştir. Bu değer, serim sonrası simulasyonlarda ise -55°C ile 125°C aralığı için %3.4'tür. Çalışma sonucunda, serim sonrası elde edilen simulasyon sonuçlarıyla paralel ölçüm sonuçları elde edilmiştir. Devre endüstriyel ve otomotiv uygulamalarında yaygın bir kullanıma sahip olan yükek değerli endüktansıların sürülmesinde kullanılaiblmektedir. Yapının modülerliği sayesinde herhangi bir sisteme ufak değişiklikler ile adapte edilmesi mümkündür.

1. INTRODUCTION

Today's integrated circuits have been widely used in electronic systems as they provide low cost and high functionality. I/O driver is one of the main integrated circuit which is used in electronic systems as they generate the signal that controls the other sub-circuits and the subsystems. Main feature of the driver is translating the input signals to output signal which is applicable for the other circuitry. Output drivers are optimized to drive specific load which may be capacitive, resistive or an inductive load. The object of this research is that slew rate controlled output driver which is capable to drive low resistive loads and inductive loads which has a high quality factor.

As the process technology develops, the transistor sizes have shrunk and this led to an increase in transistor speed. Nowadays, high speed data acquisition become significant feature in electronics. Therefore, large amount of current must be provided by a driver circuit in a short time when driving a load. (Maloberti & Torelli, 1991). That high amount of current is supplied from supply line which has a parasitic inductance that arise from the bond wire between pads of the die and package lead. The voltage drop on the supply line, caused by the parasitic of bond wire, can be represent as $v(t) = L^{\mathrm{di}}/_{\mathrm{dt}}$. Where L is the parasitic inductance of the bond wire and $v(t)$ is the time domain voltage on the inductance which is defined as simultaneous switching noise mostly known inductive noise. Simultaneous switching noise cause a degradation on the noise margin of system, output signal distortion, V_{DD} and ground bounce e.t.c. Fast transition edges cause high frequency components at the output which may cause a crosstalk between signals (Shin et al., 2005). Furthermore, driving an inductive load with fast transition cause a bouncing in the output signal which may harm the driver transistors by exceeding the breakdown voltage of the transistors. To solve this problem, slew rate of the output signal must be controlled properly as far as desired system performance is obtained.

Several techniques have proposed in order to control the slew rate of the output driver, up to today. This techniques can be split two different schemes which are analog

control architectures and digital control architectures. One of the analog control architecture is obtaining the slew rate compensation by external resistor (Senthinathan & Prince, 1993). Capacitive feedback architecture is another analog scheme which rely on the current-voltage equations of the capacitor (Garcia et al., 1998). Digital control architectures based upon adding delay between the output driver transistors to create constant rise and fall times at the output signal (Song, 2001). However these schemes are not suitable to drive inductive elements and PVT (Process, Voltage and Temperature) variations have a major impact on slew rate of the output signal.

In this study a slew rate controlled output driver with a single supply voltage of 3.3V is presented. Slew rate of the output signal is controlled by digital control schemes. Temperature compensation is added by using PTAT (Proportional to Absoule Temperature) and CTAT (Complementary to Absolute Temperature) currents to obtain constant slew rate within temperature. Furthermore, an amplitude control system which consists of an comparator and reference voltage generator is used to obtain proper operation regions for the output transistors while driving an inductive load. Driver is implemented using a standard CMOS 0.35 μm with high voltage option.

1.1 Organization of Thesis

The organization of the thesis can be summarized as follows:

In chapter 2, evolution of slew rate control architecture is examined. The application areas and design requirements are presented.

In chapter 3, modeling phases of transformer, which is used in simulation environment as inductive load, is presented. Design, operation details and simulation results of the sub-blocks and top level are given. Furthermore, layout of the sub-blocks and top level are presented. Effects of capacitive and resistive extraction are examined.

In chapter 4, measurement setup is explained and measurement results are given for different load configurations. Measurement and simulation results are compared and discussed.

Finally, chapter 5 summarizes the study and discusses possible developments of the slew rate controlled output driver.

2. BACKGROUND

In this section, an extensive review about the simultaneous switching noise is focused on. After that, it will be explained how ringing affects the output driver performance when driving an inductive load. Finally, previous works on the literature are presented and discussed.

2.1 Overview of Simultaneous Switching Noise

Simultaneous switching noise is originated from the large currents that propagates on supply or ground lines in a short time. Primary contributor is the switching activity of the transistors in the integrated circuit (Ding & Mazumder, 2003). Amplitude of the switching noise directly related to parasitic inductance of the bond-wire as seen from 2.1.

$$v(t) = L\frac{di}{dt} \tag{2.1}$$

A length of bond wire changes corresponding to die size, package type, assembly technique e.t.c. Even different bonding materials are used in wire bonding operation, self parasitic inductance of bond wire does not change significantly due to fact that it is determined by wire length dominantly (Yang & Yuan, 2003). Self parasitic inductance of a bond wire is defined following

$$L_s = \frac{\mu_o \ell}{2\pi}\left[\ln\left(\frac{\ell}{\rho}+\sqrt{1+\left(\frac{\ell}{\rho}\right)^2}\right)-\sqrt{1+\left(\frac{\rho}{\ell}\right)^2}+\frac{1}{4}+\frac{\rho}{\ell}\right] \tag{2.2}$$

where ℓ is length of bond wire, ρ is the radius of the conductor. Gold is the mostly used material for wire bonding and the common diameter of bond wire is .0254 mm which corresponds to 1 mil (Electronic Industries Alliance Engineering Department, 1997). Self parasitic inductance of a bond wire is assumed as 1 nH per mm as a rule of thumb in integrated circuit design (Lee, 2003). As process technology progresses, die sizes of the integrated circuits are getting smaller, but package dimensions does not change relatively. Therefore, the length of bond-wire has increased gradually over the

past years and switching noise becomes considerable problem for the integrated circuit design.

2.1.1 Ringing effect of the inductive load

Inductive loads are commonly used in several application fields such as automotive, industrial avionics e.t.c. (Wouters et al., 2004). Even inductive load may be a relay, transformer or a motor according to application requirements, electrical behaviour of these devices is same. As the amplitude over the inductance is directly related to its current change in a certain time, a current which is sourced to inductive load must be well considered (Pasetti et al., 2012).

To understand ringing effects or voltage spikes, physical mechanism of the inductive load must be well understood. When a current sourced to a inductive load, a magnetic field occurs around the coil and it stores energy. If the current of the inductive load is interrupted, the magnetic field collapses. According to Lenz's Law which is given in 2.3, change in a magnetic field induce a current flow in the opposite direction. Therefore, the inductor acts like a power source for the circuit and generates much greater potential differences between its terminals. Theoretically, it can create infinite voltage between its terminal when current change rate is infinite.

$$\varepsilon = \frac{\partial \phi}{\partial t} \tag{2.3}$$

This scenario also happens while energizing the inductor. This time inductive loads reveals inrush current which could be many times larger than the operating current and voltage spikes occurs (Geeter & Furrer, 2014). These voltage spikes which occurs when energizing or de-energizing inductive load may exceed the level which harm the other circuitry. This voltage level is related to the value of the inductance and the current change in a certain time. As the inductance value is predefined, current change rate is the only parameter which can be controlled.

2.2 Previous Works

There are several architectures that provides slew rate control in the literature. As data rates increases different slew rate control topologies are presented that are convenient specific application. In this chapter, conventional slew rate control methods are presented and discussed.

2.2.1 Slew rate control by capacitive feedback

Slew rate control by capacitive feedback was first published in 1998 by Coll, Garcia and Anvergne which is shown in Figure 2.1. The output transistors M_{P1} and M_{N1}

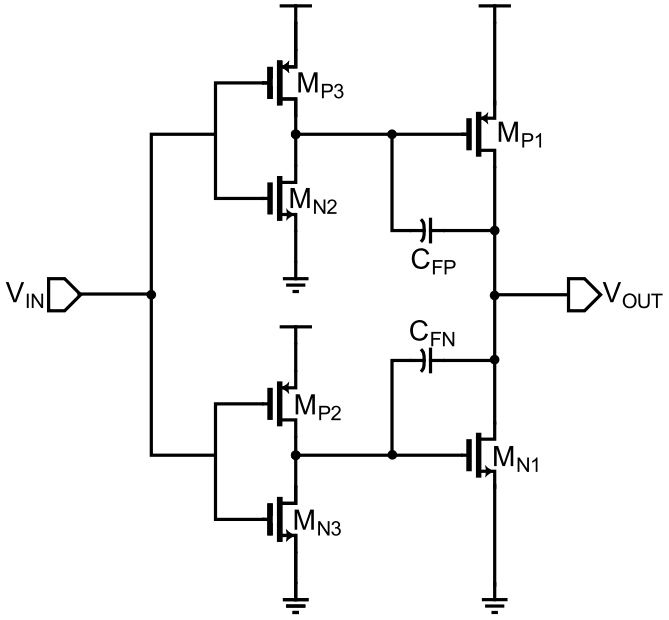

Figure 2.1 : Slew rate controlled output driver using feedback capacitor (Garcia et al., 1998).

are the output driver transistor. The output transistors are controlled by M_{P2} and M_{N2} current generators. Feedback capacitance provides that gate voltages of the output transistors are clamped to a certain value. Clamping voltage level may variates corresponding to the value of output load, but slew rate of the output signal will be same as as long as the current of current generators and the feedback capacitance is constant (Garcia et al., 1998). Although this method is useful to control the slew rate for different capacitive load value, it still has a large slew rate change over PVT

variations because of the change in the current flow of current generator transistor M_{P2} and M_{N2}.

The capacitive feedback structure is reconsidered by Soon-Kyun Shin, Wang Yu et. all and developed structure, which compensates the PVT variations, is proposed in 2007. Figure 2.2 demonstrate the proposed output driver.

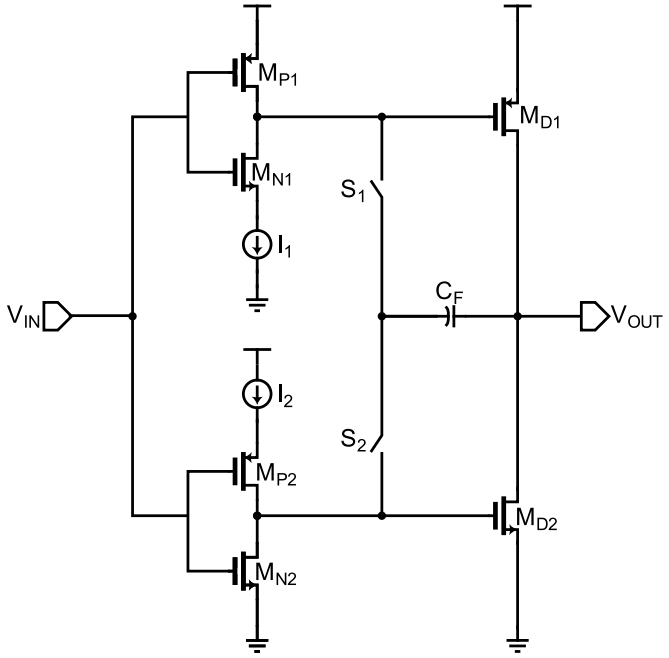

Figure 2.2 : Slew rate controlled output driver using feedback capacitor (Shin et al., 2005).

Main operation principle is summarized as following, first assume that input of the driver rises logic 0 to logic 1. The transistors, M_{P1} and M_{P2} are off, then S_2 is off when M_{N1} and M_{N2} transistors is on. After S_1 switch is on, gate voltage of PMOS driver M_{D1} begins falling from V_{DD}. When the gate voltage drops to one threshold voltage below V_{DD}, M_{D1} starts to source a current to load that cause an increase in output voltage, V_{OUT}. A change of voltage at the output creates a current flow at the feedback capacitor as following

$$i_{C_F} = C_F \frac{dV_{OUT}}{dt} \tag{2.4}$$

It is clear that i_{C_F} cannot be larger than the current which is flew from M_{N1}. When the feedback capacitor current equals to I_1, highest slew rate is achieved and cannot be exceed. Circuit performs same in the falling transition (Shin et al., 2005).

Proposed circuit reduces the slew rate variations which originates from the PVT variations by using new current bias scheme. However, gate-drain parasitic capacitance

changes the effective feedback capacitance which leads to a mismatches in the desired slew rate. Even using a large feedback capacitance may reduce the parasitic capacitance, it consumes much area and power in order to obtain desired slew rate.

In 2011, another circuit which uses capacitive feedback topology to control slew rate is published by Liu, Huang, Ying and Kuo. The development of the circuit is that it is optimized to be suitable for driving inductive loads in the DC-DC converter applications. Figure 2.3 demonstrates the schematic of output driver. As shown in

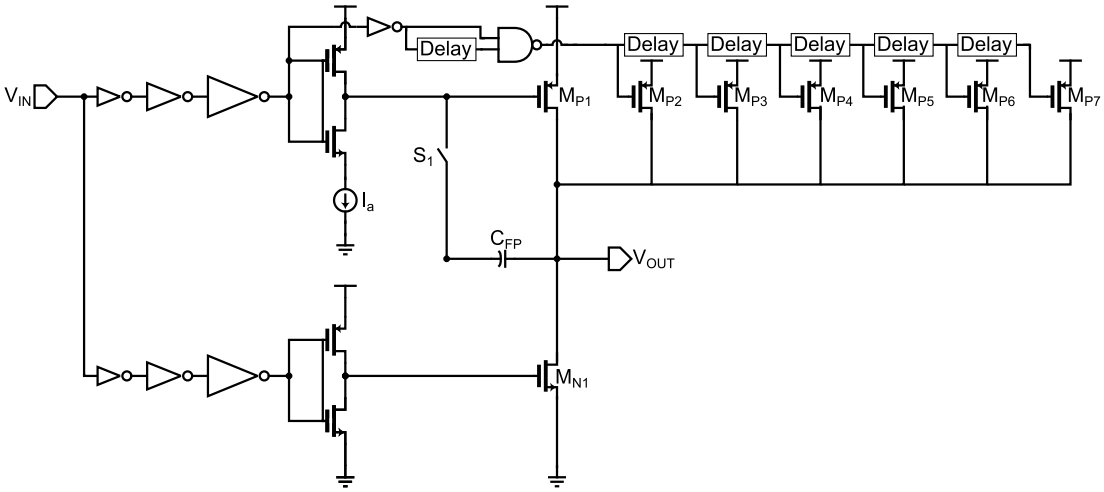

Figure 2.3 : Slew rate controlled output stage (Liu et al., 2011).

Figure 2.3 rising slope control is controlled by feedback capacitor which gives a slew rate as following

$$S_R = \frac{dV_{OUT}}{dt} = \frac{I_a}{C_{FP}} \tag{2.5}$$

The main difference of the circuit is that the falling time is not controlled by feedback capacitance, it is controlled by distributed and weighted output stage which is seen in Figure 2.3. Operation principle of the distributed and weighted power stage as follows; after M_P is turned off, the transistor array in the distributed and weighted power stage is activated step by step due to increase the fall time sourcing a current to a load (Liu et al., 2011). Since rise and fall times are controlled by different mechanisms in the circuit, it is possible that there is a systematic difference between each other.

2.2.2 Slew rate control by replica bias circuit

In 2004, an output driver with slew control using replica bias circuit is proposed by Choi and Park. As seen in Figure 2.4 output driver consists of two different section which are main driver and replica bias circuit. The main idea behind the slew rate

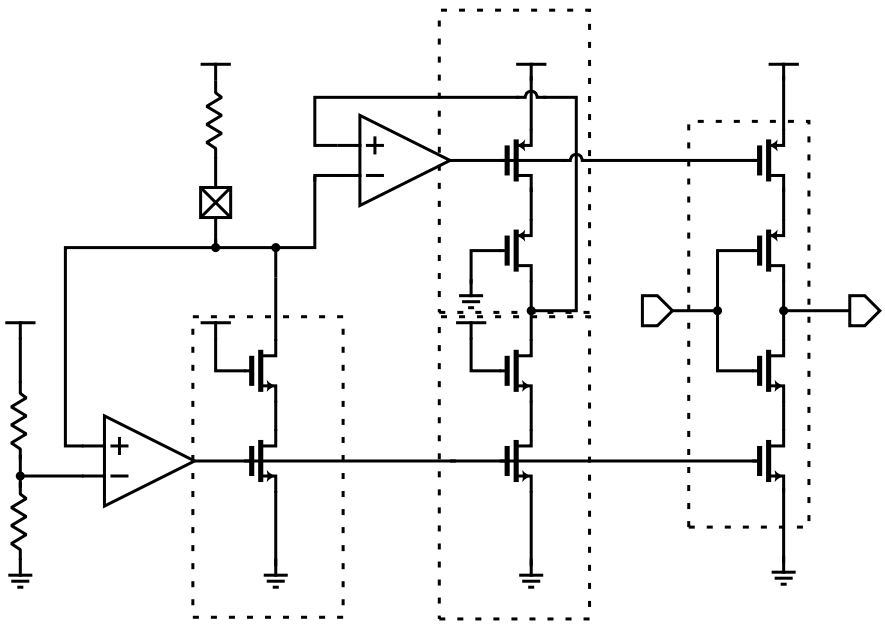

Figure 2.4 : Slew controlled driver with replica bias circuit (Choi & Park, 2004).

control is obtaining a fixed RC time constant at output node. The main driver is biased using replica bias circuit which has a operation principle as follows; first, Due to negative feedback loop, Op-amp A forces the V_{B1} node to the voltage V_{REF}, which is $V_{DD}/2$. Therefore voltages on the R_{EXT} equals to $V_{DD}/2$. Same current flew from the R_{EXT} and pull down path A. Assume that this current flow is I_{REF}, as pull down path B is biased by pull down path A, same current flow is provided by this path. It is obvious that Opamp-B forces its positive input to the negative input due to fact that it is in the negative feedback configuration. So V_{B2} equals to $V_{DD}/2$. Therefore pull up path A try to source a same amount of current, I_{REF}. As the main driver is biased by replica bias circuits which are the pull down path B and pull up path A, current flow is fixed at the output nodes. It can be easily shown that I_{REF} equals to

$$I_{REF} == \frac{\frac{VDD}{2}}{R_{EXT}} \tag{2.6}$$

As seen output current can be easily adjusted by changing the value of R_{EXT}. Therefore, output driver can be modified according to the value of the load or the ambient conditions such as temperature, supply voltage e.t.c.

It is obvious that, the circuit is optimized for capacitive loads, adding a resistive load to the output affects the resistance of pull down path or the resistance of pull up path whether a load is connected to the ground or supply. Besides, using an external component causes an increase in the required printed circuit board area and application cost.

2.2.3 Slew rate control by delay cells

A CMOS output driver with slew rate control by using RC time delays which is seen in Figure 2.5 is published in 1993. As seen from Figure 2.5, slew rate control is achieved

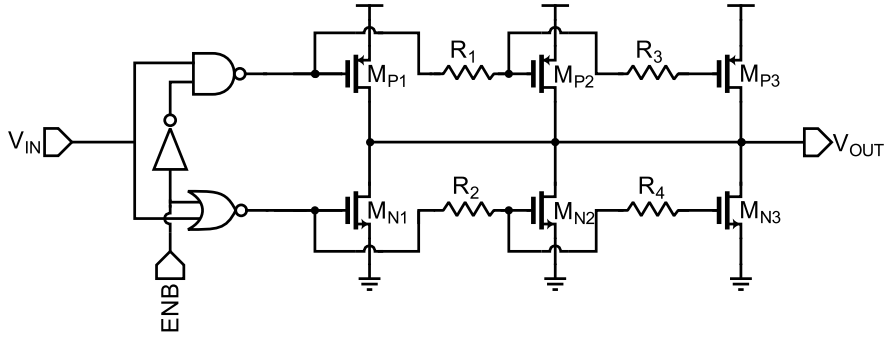

Figure 2.5 : Tristatable, controlled slew rate CMOS output driver (Senthinathan & Prince, 1993).

by controlling the gate voltages of three CMOS drivers. Adding a skew between these drivers by modifying arrival time of input signals of transistor cause a reduction in output current of the main driver. The skew is generated by using resistor serial to the input of the transistors. The parasitic capacitance of the MOS transistor and the added resistors creates a RC time constant which cause a skew between drivers. As weighted power architecture is used in the output drivers, there is a increase in the transistor sizes from driver 1 to driver 3. Therefore, there is a increase in parasitic capacitance of the transistor from driver 1 to driver 3 which cause different time delays for drivers. For instance, as first RC time constant cause a time delay t_0, the time delay of second RC is $t_0 + \Delta t_1$ (Senthinathan & Prince, 1993).

Another architecture which controls the slew rate by using delay elements is published in 2001 by Song. The output driver is separated to N bit-slices and each slice is controlled by its own enable signal. Figure 2.6 demonstrates the slew rate control scheme. Logic input signal controls the first output driver, second driver is controlled

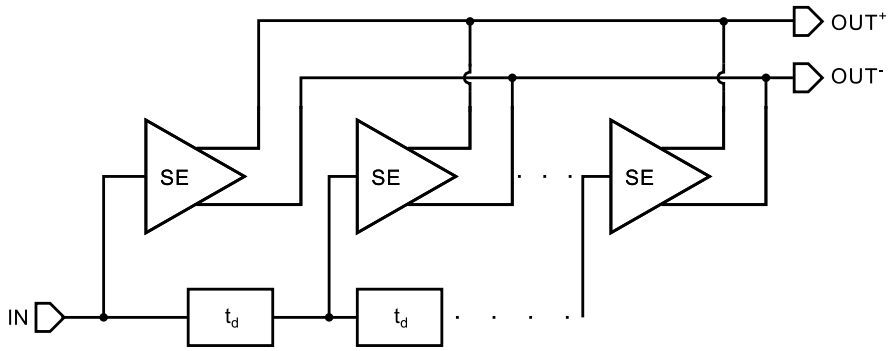

Figure 2.6 : Adaptive slew controlled output driver (Song, 2001).

by the signal which is delayed from input logic signal by delay element. That operation principle continues until the last driver is activated and generates a desired output ramp at the output (Song, 2001). The delay time of the delay elements is determined by using DLL that provides a delay time which is independent from process, temperature relatively.

Although, delay time controlled architectures creates a stable rise and fall time control, they are not optimized to drive inductive load. Furthermore, due to the absence of any control in the output voltage level, the circuits dissipates more power than the desired in some cases.

3. PROPOSED SLEW RATE CONTROL OUTPUT DRIVER

The main purpose of this study is to design a output driver with slew rate control, that is optimized for resistive and inductive loads, due to minimize the simultaneous switching noise. The circuit has two digital inputs which are positive and negative, and corresponding that it has positive and negative analog outputs. Furthermore, adjustable slew rate control system is implemented in order to provide different specifications of different application standards. Therefore proposed output driver is compatible with almost all transmitter applications which has a requirement to drive inductive or resistive load. A transformer is used as inductive load. However, ideal transformer may give a misinformation about the driver performance. To match simulations with the realized results, a transformer model must be designed which adds 2nd order effects of the transformer.

3.1 Transformer Modeling

Due to fact that the output driver must be capable to drive and inductive loads, large signal behaviour of inductive load must be well understood. Although, there are several transformer models which is created by using ideal inductance or veriloga code in the Cadence Design Environment, these transformer models is deceptive due not to consider secondary effects of real transformers which is arise from parasitic elements of transformer.

An ideal transformer can be described as lossless transformer which is given in Figure 3.1, and the relations between transformer primary and secondary can be found using transformer turn ratio.

$$V_2 = V_1(\frac{N_2}{N_1}) \tag{3.1}$$

$$i_2 = i_1(\frac{N_1}{N_2}) \tag{3.2}$$

As seen in 3.1 and 3.2, voltages are transformed directly proportional to turn ratio, when the current is transferred inverse of turn ratio.

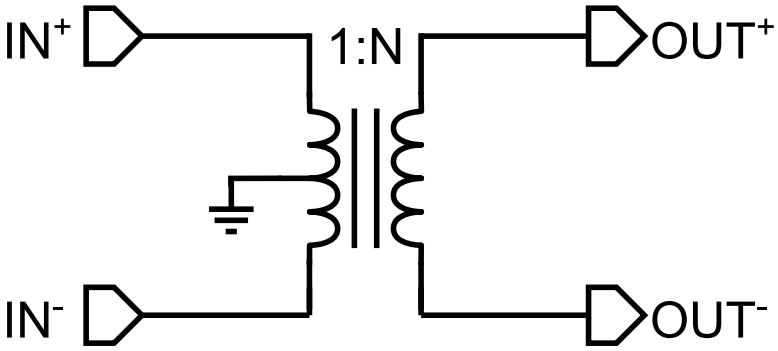

Figure 3.1 : Ideal (lossless) transformer.

In a real transformer, out of that the magnetic flux between primary and secondary may not link completely, a leakage flux, which store or discharge energy, occurs. The leakage flux can be represented as an inductive element series with windings and called as leakage inductance. The effects of leakage inductance is causing a voltage spikes which are arisen from stored energy in leakage flux (McLyman, 2011). Parasitic capacitance of the transformer are the another important parasitic element that may affect circuit performance. There are different mechanism that generates a parasitic capacitance in the transformer. For instance, winding to ground capacitance, winding to winding capacitance, terminal capacitance of primary winding, capacitance of secondary winding e.t.c. (López-Fernández, Ertan, & Turowski, n.d.). Amongst these parasitic capacitance, distributed capacitance of windings and the inter-winding capacitance are the most significant parasitic capacitance in the transformer because of the their larger value and effects to large signal behaviour (Coleman, 2011). If the winding layers of transformers is modelled as two coaxial cylinder, static capacitance can be found as following

$$C_{static} = \frac{2\pi\varepsilon_0\varepsilon_r h}{\ln\frac{b}{a}} \tag{3.3}$$

where ε_r is relative dielectric constant of insulation thickness, a is radius of inner layer, b is radius of outer layer and h is the height of cylinder (López-Fernández et al., n.d.). The secondary winding capacitance is calculated as follows;

$$C_s = \sum_{k=0}^{n-1} \left(\frac{1}{C_{k_{static}} \left(\frac{(3k^2+3k+1)}{n^2} \right)} \right)^{-1} \tag{3.4}$$

where n is the number of secondary layer in coil and $C_{k_{static}}$ is the static capacitance between k and k+1 layers (López-Fernández et al., n.d.). The calculation of primary-secondary winding capacitance is more complicated than secondary winding

capacitance because of the fringing effect. Carter coefficient can be used to approximately calculate the fringing effect as seen in 3.5

$$C_{ps} = \sum_{k=0}^{n-1} C_{k_{static}} \frac{3k^2+3k+1}{3n^2} F_{carter}(A,B) \tag{3.5}$$

where $C_{k_{static}}$ is the static capacitance between primary and k_{th} secondary layer (López-Fernández et al., n.d.). However, those parameters which can be used to design a model of transformer, such as radius of coaxial cylinder, layer number in the coils e.t.c. cannot be given from the transformer supplier. Therefore the device values in the equivalent transformer model must be determined by measuring the impedance characteristics of transformer. Figure 3.2 demonstrates the equivalent model of real transformer with parasitic.

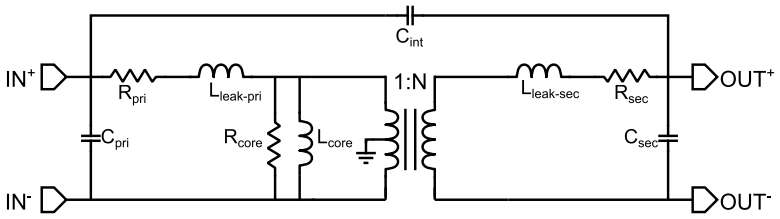

Figure 3.2 : Equivalent model of transformer with parasitic.

A transformer with a 1 : 2.5 primary to secondary ratio is measured and analyzed by an impedance analyzer. Test setup is given in Figure 3.3. Used transformer is the PM-DB2726 dual transformer of Premier Magnetich which has a test frequency between 75 kHz to 1 MHz in its datasheet.

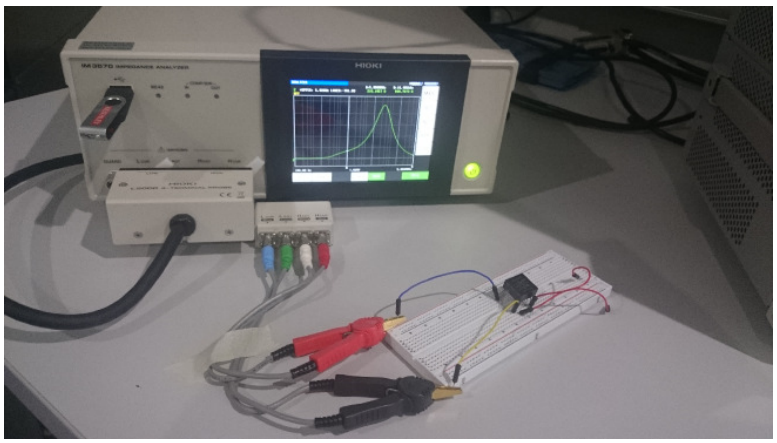

Figure 3.3 : Transformer test setup.

First secondary of the transformer is open-circuited and the impedance analyzer is connected to the primary of the transformer. Result is given in Figure 3.4.

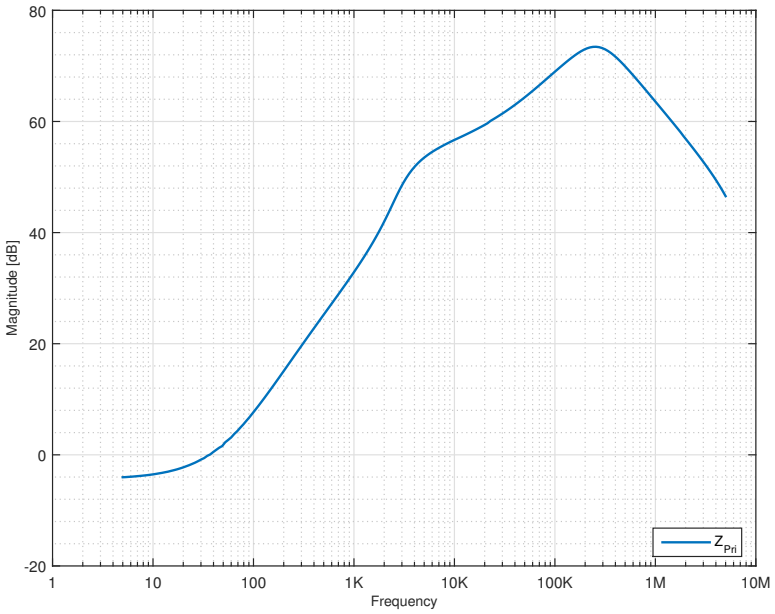

Figure 3.4 : Impedance of the primary when secondary is open-circuited.

It is obvious that DC resistance R_{pri} will be effective at the low frequencies, after a significant frequency core inductance and leakage inductance will be effective and the impedance starts to rise with a 20dB per decade. So, at that point total inductance of the primary can be calculated as follows

$$\begin{aligned} Z_{pri}[dB] &= 20log(2\pi fL) \\ L_{pri} &= \frac{10^{\frac{Z_{pri}[dB]}{20}}}{2\pi f}) \\ L_{pri} &= \frac{10^{\frac{68}{20}}}{2\pi 90.985e+3} \\ L_{pri} &\cong 4.55613\text{mH} \end{aligned} \tag{3.6}$$

As seen from Figure 3.2 there are two individual inductance at the primary side. So, the inductance value which is found by 3.6 represents the sum of these two inductance. Secondary of the transformer is shorted to find the exact values of these inductance. In this configuration, voltage difference between the secondary pins will be 0 V and corresponding to that voltage difference between primary core inductance pins will be 0 V. Therefore, magnetizing core inductance of the primary can be accepted as short circuit and leakage inductance will be the only component which affects the impedance over frequency (Voltech Instruments, 2001) (Infineon Technologies AG, 2011) (Agilent Technologies, 2013). Measurement results are given in Figure 3.5.

As seen from Figure 3.5, value does not change at the low frequencies as it was originated from the R_{pri}. Its value is approximately 0.628 Ω. Leakage inductance

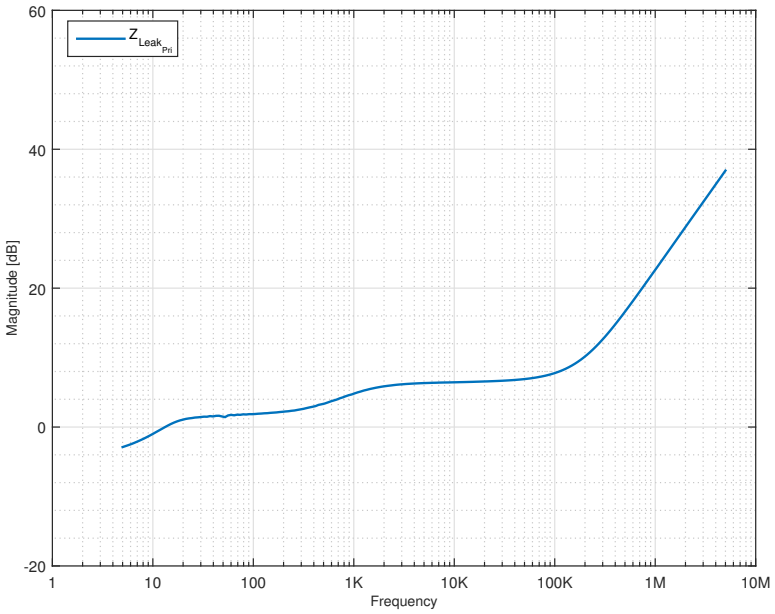

Figure 3.5 : Impedance of the primary when secondary is short-circuited.

value is found as follows

$$\begin{aligned} Z_{leak_{pri}}[dB] &= 20log(2\pi fL) \\ L_{leak_{pri}} &= \frac{10^{\frac{Z_{leak_{pri}}[dB]}{20}}}{2\pi f}) \\ L_{leak_{pri}} &= \frac{10^{\frac{31}{20}}}{2\pi 2.6852e+6} \\ L_{leak_{pri}} &\cong 144.15\text{nH} \end{aligned} \tag{3.7}$$

As a result magnetizing core inductance can be calculated as follows

$$\begin{aligned} L_{mag_{pri}} &= L_{pri} - L_{leak_{pri}} \\ L_{mag_{pri}} &= 2.64365m - 255.93n \\ L_{mag_{pri}} &\cong 4.556\text{mH} \end{aligned} \tag{3.8}$$

After the primary resistance and inductance are determined, secondary of the transformer is analyzed. First theoretical calculations are made by using equivalent model parameters of primary. It is obvious that, magnetizing core inductance of the secondary and the magnetizing core inductance of the primary determines the turn ratio of the transformer. As it is given as 2.5, magnetizing core inductance of the secondary can be found as follows

$$\begin{aligned} L_{mag_{sec}} &= \left(\frac{N_S}{N_P}\right)^2 L_{mag_{pri}} \\ L_{mag_{sec}} &= \left(\frac{2.5}{1}\right)^2 4.556m \\ L_{mag_{sec}} &\cong 28.475\text{mH} \end{aligned} \tag{3.9}$$

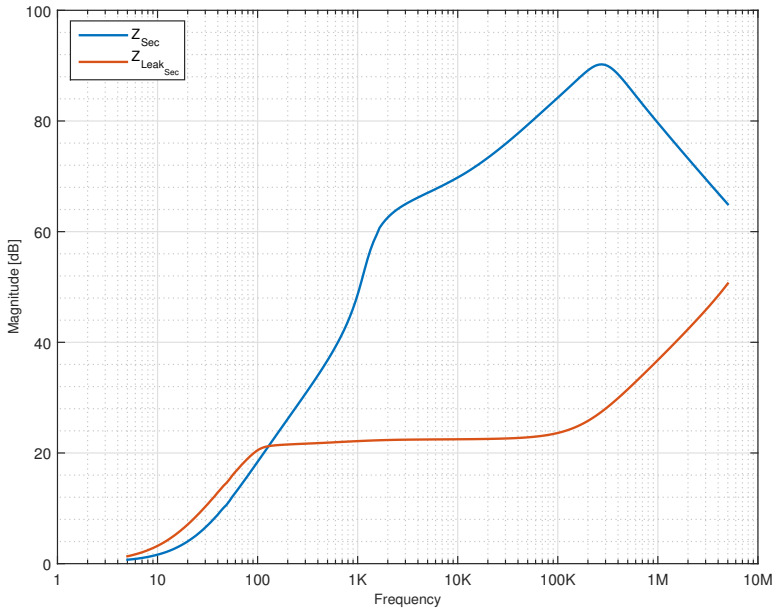

Figure 3.6 : Impedance of the secondary for open-circuited and short-circuited primary.

Analysis results of the secondary impedance is given in Figure 3.6.

First primary is open-circuited and analysis results is obtained, then, primary is short-circuited and analysis is repeated. Same calculations are done to find the leakage an magnetizing inductance of the secondary.

$$
\begin{aligned}
Z_{sec}[dB] &= 20log(2\pi fL) \\
L_{sec} &= \frac{10^{\frac{Z_{sec}[dB]}{20}}}{2\pi f}) \\
L_{sec} &= \frac{10^{\frac{80.5}{20}}}{2\pi 60.1113e+3}) \\
L_{sec} &\cong 28.361\text{mH}
\end{aligned}
\tag{3.10}
$$

$$
\begin{aligned}
Z_{leak_{sec}}[dB] &= 20log(2\pi fL) \\
L_{leak_{sec}} &= \frac{10^{\frac{Z_{leak_{sec}}[dB]}{20}}}{2\pi f}) \\
L_{leak_{sec}} &= \frac{10^{\frac{36}{20}}}{2\pi 4.6663e+6} \\
L_{leak_{sec}} &\cong 3.876\text{uH}
\end{aligned}
\tag{3.11}
$$

$$
\begin{aligned}
L_{mag_{sec}} &= L_{sec} - L_{leak_{sec}} \\
L_{mag_{sec}} &= 28.361m - 3.876u \\
L_{mag_{sec}} &\cong 28.357\text{mH}
\end{aligned}
\tag{3.12}
$$

As seen from the above equations measured magnetizing core inductance is larger than the calculated magnetizing core inductance. It shows that effective turn ratio is above

than its theoretical value. It is calculated in the 3.13

$$\begin{aligned} TR &= \frac{N_S}{N_P} \\ &= \sqrt{\frac{16.488}{2.6434}} \\ &\cong 2.4948 \end{aligned} \tag{3.13}$$

As seen from Figure 3.6, loss resistance of the secondary branch is approximately 1.08 Ω. Core loss resistance $R_{MAG_{core}}$ can be found by using impedance waveform of the primary when secondary is open circuited. The peak impedance value at the resonant frequency gives the loss resistance of magnetization core. It is approximately 4.7013 kΩ at 256.43 kHz. Capacitance terms of the equivalent transformer model can

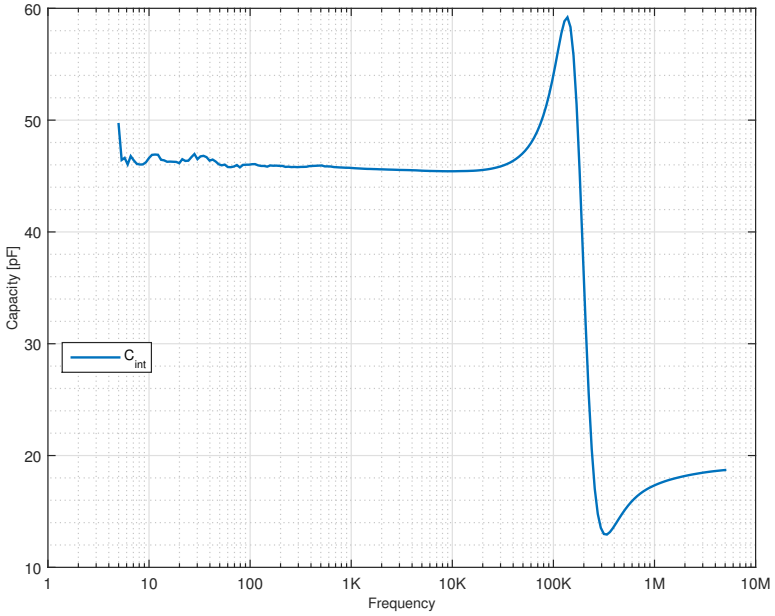

Figure 3.7 : Inter-winding capacitance between the primary and secondary.

be calculated by using gain bode plot of the transformer. However two port network analyzer must be used to obtain gain-frequency plot of the transformer. Instead of that, impedance analyzer is used to determine the capacitance terms in the equivalent model of the transformer. Most important capacitance terms is the inter-winding capacitance which is connected between primary and secondary side of transformer. High probe of the impedance analyzer is connected to the positive pin of the primary and the low probe of the impedance analyzer is connected to the positive pin of the secondary. Negative pins of the primary and secondary are shorted. Figure 3.7 demonstrates capacitive terms which is extracted from the impedance between high and low probe.

After the device values in the transformer model was determined, equivalent circuit is designed and analyzed whether its frequency characteristics are consistent with the measurement results. Figure 3.8 demonstrates the obtained results.

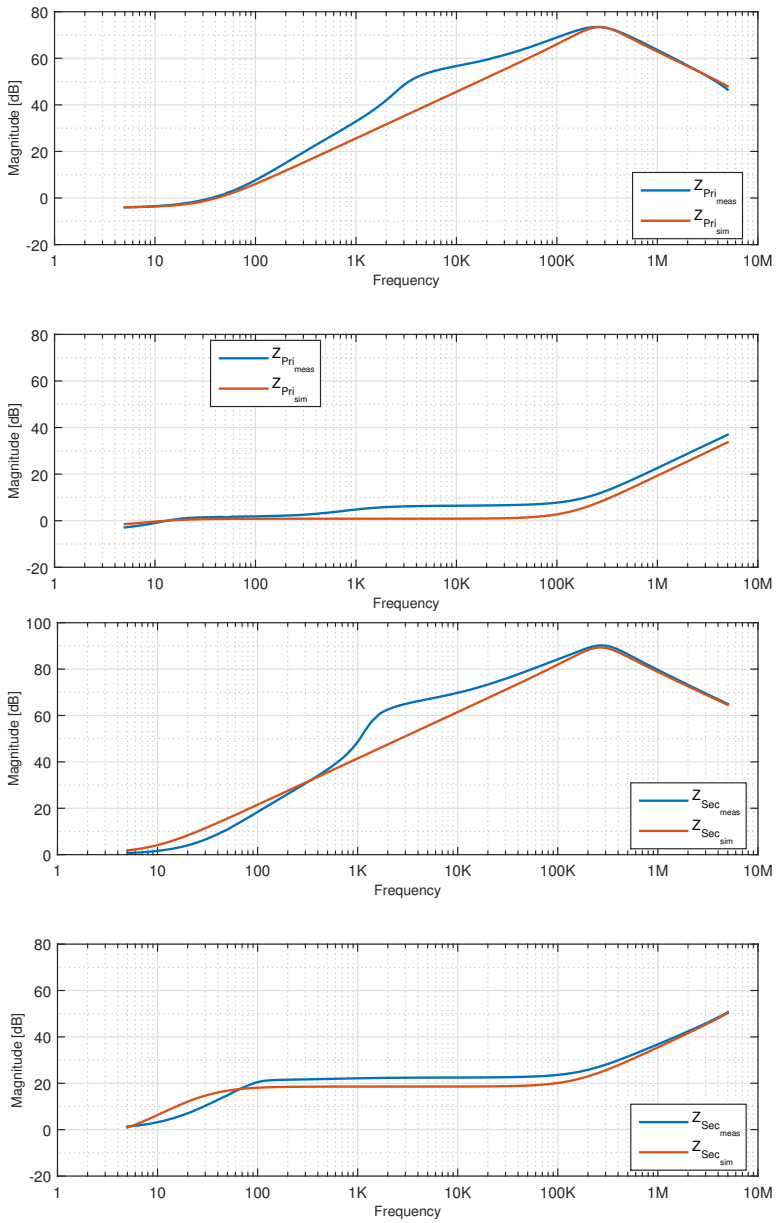

Figure 3.8 : Simulation results of the equivalent transformer model and the measurement results (Primary measurements and secondary measurements given in the two different configuration, open circuited output and short circuited output respectively).

3.2 Block Diagram of Proposed System

Figure 3.9 demonstrates the block diagram of the proposed output driver. The proposed

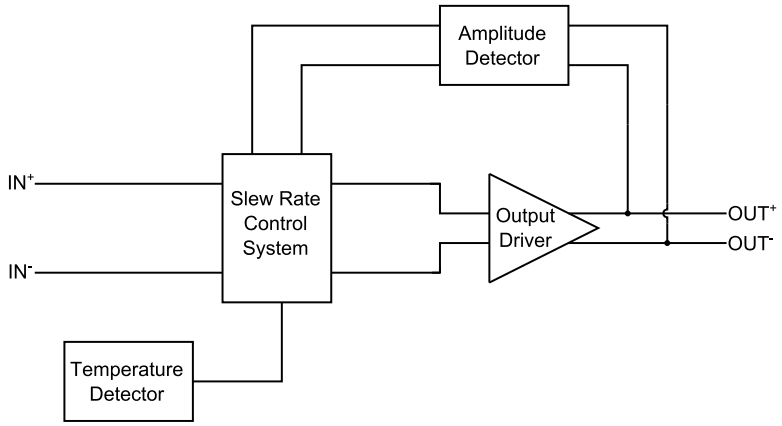

Figure 3.9 : Block diagram of the proposed output driver.

driver consists of the slew rate control block, the amplitude detection system, the output driver core and the temperature compensation circuit. First, input signals is applied to slew rate control block, the slew rate control block generates the signals which are sequential to each other with a time delay. These signals are applied to output driver core array and activate it. If the output signal level reaches to undesired value, amplitude detection system creates a signal and stops the increase of output signal. Slew rate control block is implemented as an digital control which consists of inverter based delay cells, D type flip-flops, multiplexers. Amplitude detection system is implemented by an comparator. Output driver core is implemented as switch controlled current sources array. The switches are controlled by the signal which is generated by a slew rate control block. Time delay between the signals provides that the current source array activates sequentially. The output current of the load is controlled and fixed to a certain value in a certain time. Thus, constant slew rate is obtained at the output nodes. To compensate slew rate variations over temperature, temperature compensation signal is generated by a temperature detector block which is implemented by an Band-gap reference circuit, PTAT and CTAT current generators.

3.3 Output Driver Core

Output driver core is implemented as switch controlled current sources which is based on commonly known current steering digital to analog converter. Transistor level schematic of the output driver core is given in Figure 3.10. The transistor arrays which

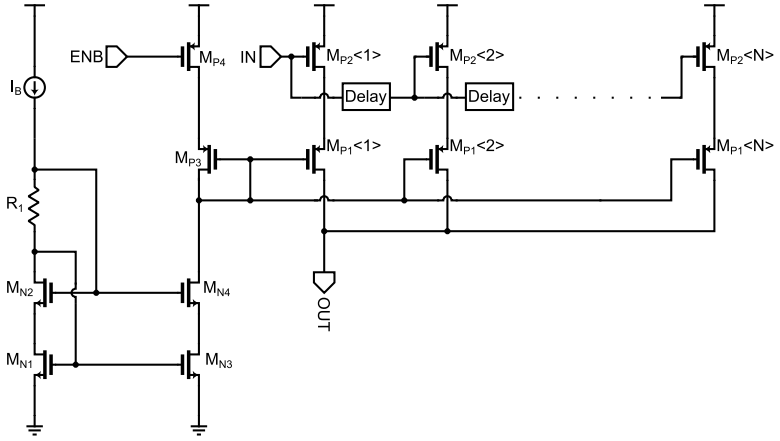

Figure 3.10 : Output driver core schematic (single ended).

consists of $M_{P1<1\ to\ N>}$ transistors are acting as current source array. These transistor arrays are biased by M_{P3} transistor. $M_{N1–4}$ are the cascode current mirrors that create a bias current for M_{P3} transistor. $M_{P2<1\ to\ N>}$ transistors are the switches arrays that control which element of current source array is activated. Transistor M_{P4} is used to match drain voltages of $M_{P1<1\ to\ N>}$ with M_{P3} in order to minimize the short channel effect. M_{P4} can be also used as the disable switch of the output driver core by cutting the current flow on M_{P3}. Figure 3.10 demonstrate the single ended version of the output driver. Implemented differential output driver core is given in Figure A.1 in appendices.

Operation principle of output core as follows, first all switches are disable and no current flows at the output, after that corresponding to input signal switches in the positive branch or the negative branch, are activated sequentially. The array size of output core is a significant parameter due to fact that it determines the current flow in each branch and the time delay of each delay element. Therefore, principle operation of circuit should be examined before determining these parameters.For the simulations, transistor array size, "‘N"’, is chosen as 40 and maximum output current of the driver is set to 100 mA by adjusting bias current. Switch arrays are controlled using ideal delay

element with an 2 ns delay. First different resistive loads are connected to the output of driver core and the performance is given in Figure 3.11 As seen in Figure 3.11, linearity

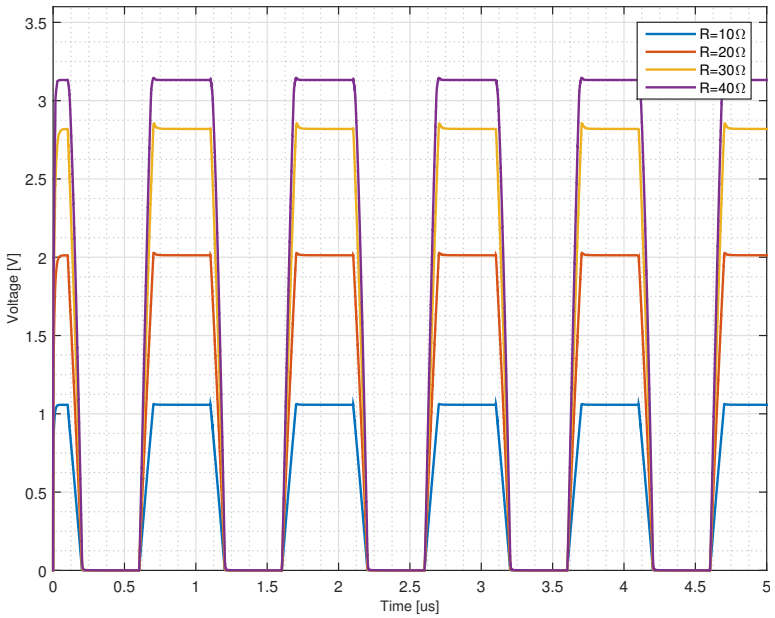

Figure 3.11 : Output driver core performance with different resistive load.

of output signal harms when the output voltage exceeds a certain level which forces output transistor to work in the linear region. As a result output current of each array will be lower and rise and fall time of an output signal will change. Therefore output voltage level must be controlled to provide that output transistors always work in the saturation region and linearity of output signal does not harm. The output signals are illustrated in the Figure 3.12 when driving a transformer with different resistive loads at the secondary. Figure 3.12 and 3.11 shows that the principle operation of output driver core is proper. The transistor sizes of output core are not well determined in this section due to they are the only parameter which affects the V_{DSSAT} of transistors for a fixed output current. After the output current capability and the time delays are determined, design of the output core is reconsidered.

3.4 Slew Rate Control and Amplitude Detection Circuit

As mentioned before, slew rate control circuit is implemented by using delay elements which controls the switches in the output driver. Figure 3.13 demonstrates the output driver core with slew rate control architecture. As shown, only positive branch is illustrated in Figure 3.13, it is obvious that same architecture is used to implement negative branch. This architecture provides to control the output current within a

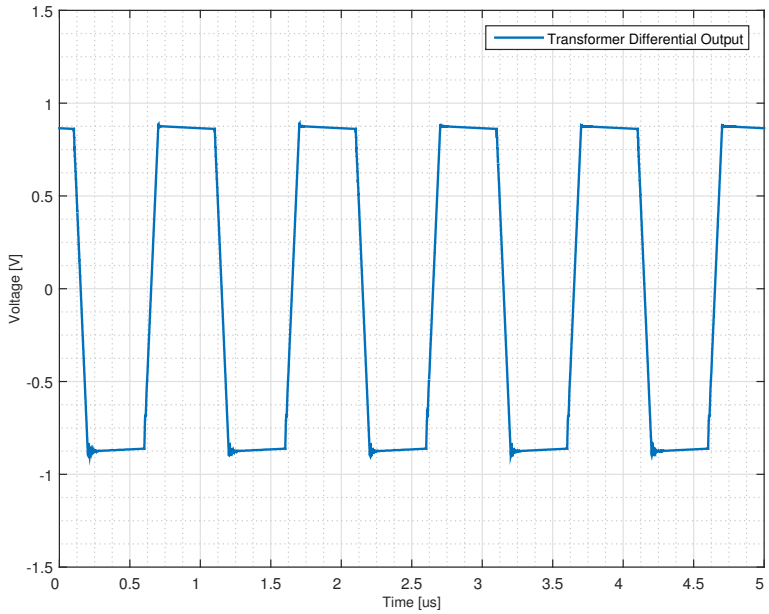

Figure 3.12 : Output signals when driving a transformer loads with different termination resistors at the secondary.

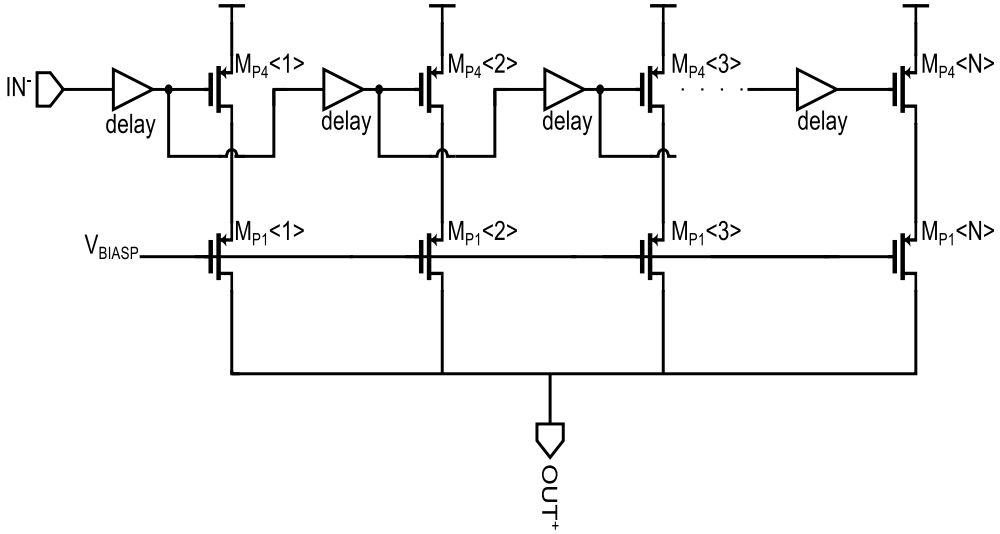

Figure 3.13 : Output driver core with slew rate control architecture.

certain time that corresponds to control output voltage for a fixed resistive load. However, as mentioned before linearity harms when the driver is used with a large resistive loads. To avoid that phenomena, amplitude detection system is design and implement to slew rate control architecture which is given in Figure 3.14. As seen from Figure 3.14, first input signal is delayed using a delay element and the output signals of delay cells control the rising edge triggered D type Flip-Flop. Data input of Flip-Flop is controlled by an comparator that compares output signal level with a reference signal. The output of Flip-Flop drives the IN_1 input of 2-1 Multiplexer, IN_0 input of 2-1 Multiplexer is tied to logic high and selection input of multiplexer is

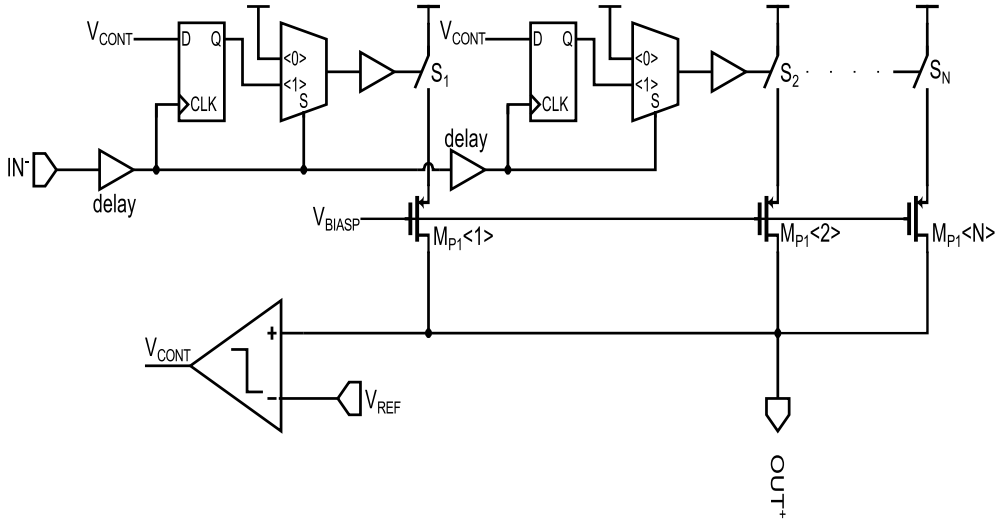

Figure 3.14 : Amplitude and slew rate control logic.

controlled by an delayed input signal. At last, output signal is buffered to drive PMOS switches in the output driver core. The operation principle of architecture as follows; when both inputs are logic zero multiplexer transmits IN_0 input to the output, which is logic high. So that PMOS switches will be off and no output current flows to the load and output voltages in the differential branches will be pseudo ground because of center tap of transformer. As comparator negative input is higher than positive input, comparator output will be logic zero. When one of inputs rise to logic high, this signal is delayed from delay element and triggers D Flip-Flop, as D-type Flip-Flop data input is logic zero, output of Flip-Flop will be logic zero. As selection input of multiplexer is high, IN_1 input will be transmitted to output. As PMOS switch is driven by logic zero it will be on and current starts to flow to the load from the activated branch. After a determine time delay, next PMOS switch will be on and the current flow on the load increase two times. This operation continues sequentially, until the output voltage level is higher than the reference signal level that causes comparator output and multiplexer output are logic high. As a result following switch will be off and output signal level does not exceed the reference signal due to fact that no more current flows to the load. Logic signals are given in Figure 3.15 to understand the operation better. The simultaneous switching noise is specified as the product of the current change in a certain time and the series inductance of line which is given in 3.14.

$$v(t) = L\frac{di}{dt} \tag{3.14}$$

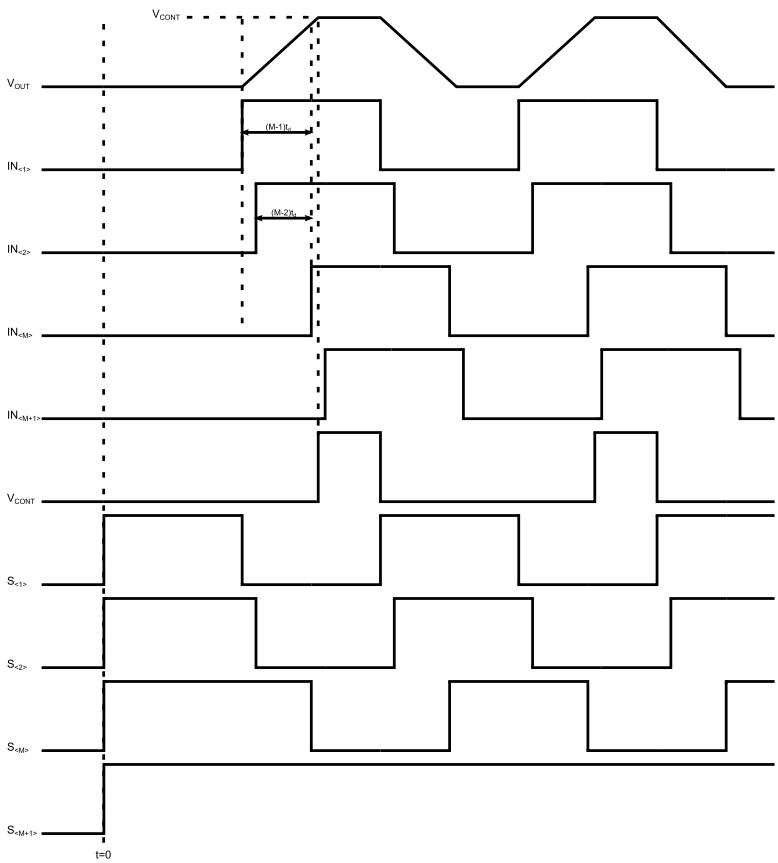

Figure 3.15 : Logic signal diagram of control system.

In the proposed circuit, it is obvious that current change is a function of array size and the output current capability, the time is fixed to time delay of delay elements. As a result noise function is written again as follows;

$$v(t) = L\frac{\frac{I_{tot}}{N}}{t_d} \tag{3.15}$$

where I_{tot} is the total current capability of output driver, N is the array size and the t_d is the time delay of one delay element. Output driver is designed with a two different mods, a high power which the driver has high current capability and low power mode which driver has low current capability. Mod selection is done by changing the output driver bias current. It is obvious that, driver core should be optimized in the high power mode since V_{DSSAT} voltages of the output driver transistor is at highest level in that mode. Besides, simultaneous switching noise is at the highest level in the high power mode due to increase in in total output current. Total output current is determined as 200 mA to meet the driver requirements for common applications. Figure 3.16 demonstrates the amplitude of ringing which is arisen from the simultaneous switching noise for different array size and different time delay. As seen from Figure 3.16,

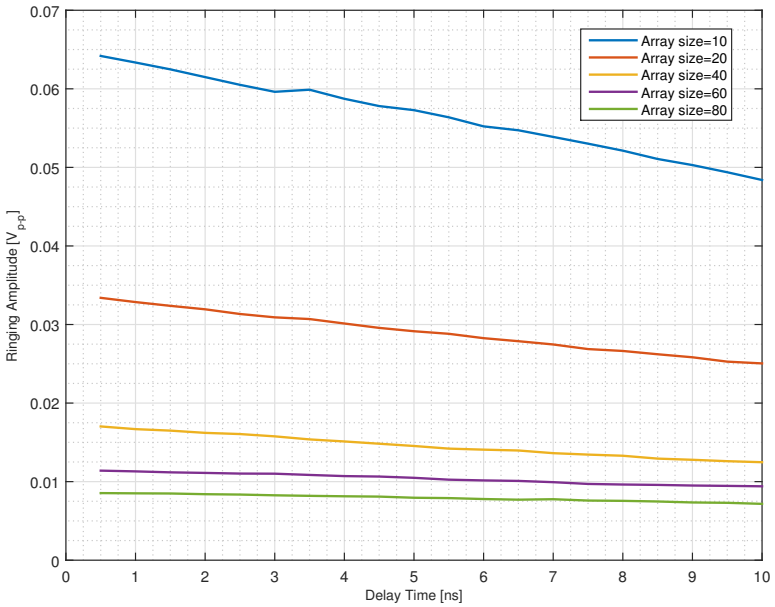

Figure 3.16 : Amplitude of ringing vs time delay for different array size.

increasing delay time for fixed array size decreases the simultaneous switching noise. However, there is a limit in increasing time delay as it causes a reduction in the speed of output driver. As seen from Figure 3.16, it is possible to obtain better simultaneous switching noise for a fixed time delay by changing the array size. The simultaneous switching noise decreases when the array size increases due to fact that reduction of array size leads to decrease an amount of current in a certain time. The speed of driver is affected again owing to the fact that increasing array size cause an raise in the time which total output current flows to the load. Besides, increasing array size causes a layout complexity because of the raise in the circuit elements. Therefore, array size and time delay must be well determined to obtain proper operation. Considering the layout challenges and the noise power caused by simultaneous switching, transistor array size N is determined 40.

It is obvious that, circuit elements and PVT variations has a significant effect on the time delays. The amplitude detection and slew rate control circuit has several digital circuits, which cause an impact on the time delay. As these circuits are not optimized in the PVT variations, it is certain that they variates by process, temperature and supply voltage. Therefore, time delay of circuit must be dominantly specified by the delay elements. The delay of the digital circuits is given in Figure 3.17 for different PVT corners. As seen from Figure 3.17, minimum delay is approximately 300 ps which occurs in the fastest process corner and maximum delay is approximately 700 ps which

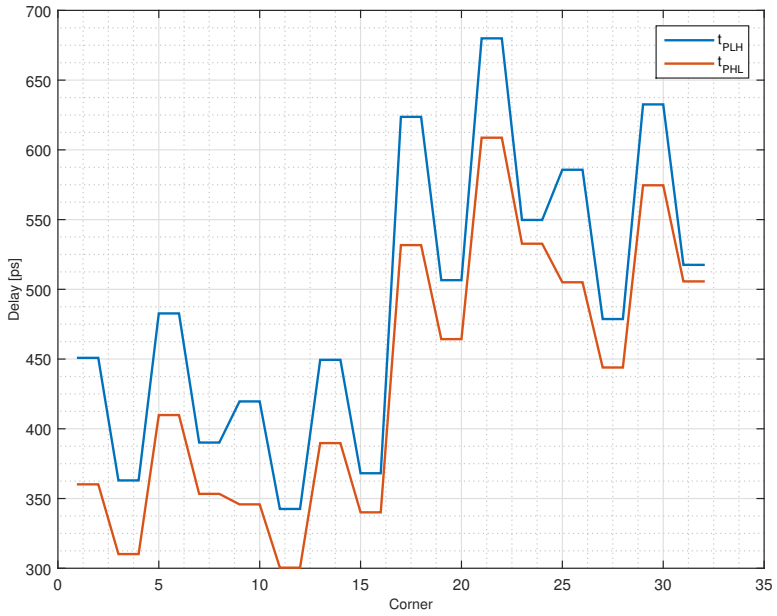

Figure 3.17 : Delay time of digital circuits in different process corners.

occurs in slowest process corner. As the variation of time delay is approximately 400 ps, time delay of the delay element must be large enough not to be affected by that variation. Choosing large time delay minimizes the delay effect of other cells, however it cause a reduction in the speed of output driver. Typical time delay is chosen as 5 ns which is large enough to minimize delay variation effect of other circuitry and provides the speed requirements for common applications.

After the transistor array size is chosen as 40 and output current capability in the high power mode and low power mode is determined as 100 mA, and 200 mA respectively, output current of each array is simply found as 2.5mA in low power mode and 5 mA in the high power mode. It is obvious that if the current is obtained in the integrated circuit, it cannot be exactly in the desired level because of the mismatches and process variations. Voltage to current converters are commonly used architecture to generate a reference current. As the resistive conversion technique is used in these architectures, reference current level is dependent to resistor variations directly. Figure 3.18 demonstrates the resistor variations with temperature in different process corners. As seen from Figure 3.18, resistor value variates approximately 20 percent from the its typical value. The $^{W}/_{L}$ ratio of output transistors should be determined to get approximately 200 mV $-$ 250 mV V_{DSsat} when carrying 6 mA which is 20 percent higher than ideal current. It is really important that high voltage PMOS transistor must be used at the output current source array, because output load is central tapped

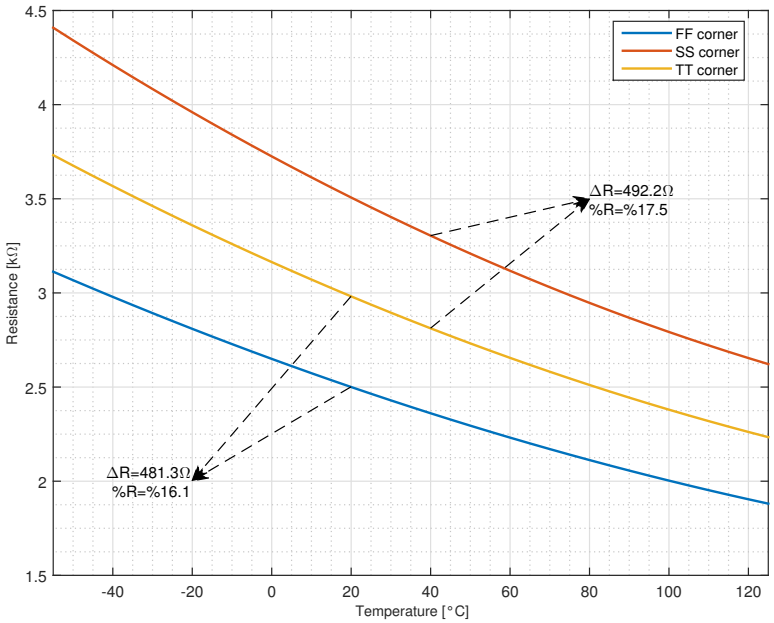

Figure 3.18 : Variations of resistor values with temperature in the different process corners.

transformer, one output goes higher the other output will follow it symmetrically to ground. For instance when the positive output is 2.5 V, negative output is -2.5 V. It is certain that, the source voltage of PMOS transistor is in the highest potential which is 3.3 V for circuit and the V_{DS} voltage of transistor will be approximately 5.8 V which is far above the V_{DS} breakdown voltage of standard 3.3 V PMOS. Therefore, a high voltage PMOS transistor which can operate in 3.3 V and has a 12 V V_{DS} breakdown voltage is used to work properly when driving a transformer. In the Figure 3.19, cross section of the high voltage PMOS device is given. In the Figure 3.20, $V_{DS_{SAT}}$

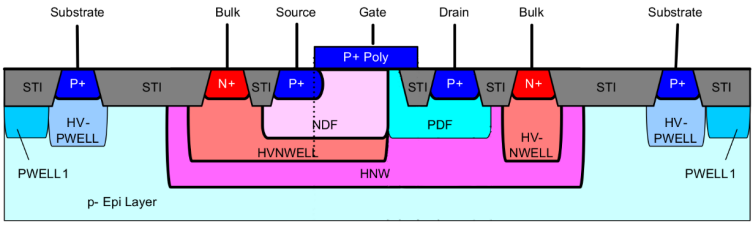

Figure 3.19 : Cross section of high voltage PMOS transistor.

voltage of high voltage PMOS transistor is given for different W/L ratio. This analysis is done in worst process corner and in the maximum current flow which is 6 mA. 150 mV $-$ 200 mV is a good region for $V_{DS_{SAT}}$ voltage for typical analysis. The values above this region leads to a degradation in maximum voltage level at the output without linearity distortion. The values below this region may cause an increase in V_{th}

mismatches. The output current of transistor is given in 3.16

$$I_d = \frac{1}{2}\mu_N C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{3.16}$$

$V_{DS_{SAT}}$ voltage is equals to V_{GS}-V_t, therefore decreasing $V_{DS_{SAT}}$ leads to decrease V_{GS} voltage as V_{th} is fixed. As the difference between V_{GS} and V_{th} minimizes, the variation in the V_{th} changes output current more effectively. Figure 3.20 demonstrates the $V_{DS_{SAT}}$ change within different $^{W}/_{L}$ ratio in the fastest, slowest and typical process corners. The region between 5000 and 8000 is proper region to determine the transistor sizes. For L is minimum which is 600 nm for the high voltage PMOS, W is chosen as 40um, using fingered type transistor with an 80 finger creates a transistor which has a 5333 $^{W}/_{L}$ ratio. After the transistor sizes of current source array are determined,

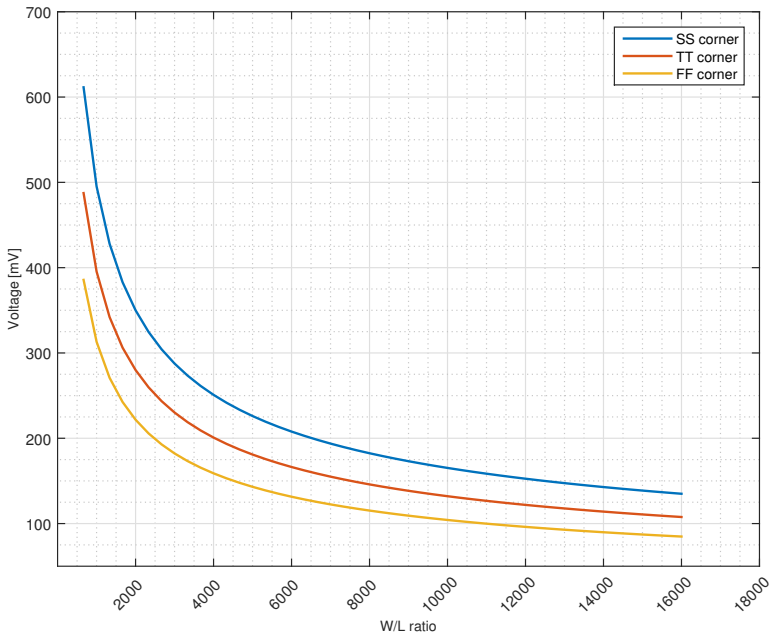

Figure 3.20 : $V_{DS_{SAT}}$ voltages versus $^{W}/_{L}$ ratio in different process corners.

switches in the output driver core are designed. As switches are tied to supply voltage and control by a logic signal, PMOS transistors are used to implement the switches. Switches must be sized to minimize voltage drop which may cause an operation of PMOS current sources in the linear region. Maximum output voltage without a linearity distortion is found as follows

$$V_{OUT_{max}} = V_{DD} - V_{DS_{SAT}} - V_{DS} \tag{3.17}$$

where V_{DS} is the voltage drop in the PMOS switches. The output current equation of switches, which operates in the linear region, is given in 3.18

$$I_d = \mu_N C_{ox}\frac{W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{3.18}$$

W/L ratio must be increased to minimize the V_{DS} voltage drop in the transistor which operates in the linear region. However, driving the switches are more inconvenient because of fact that an increase in W/L ratio leads to an increase in parasitic capacitance which is formulated approximately as follows

$$C_{GS} = C_{GD} = \frac{1}{2}WLC_{ox} + WC_{ov} \tag{3.19}$$

where C_{ox} is gate to channel capacitance per unit area and C_{ov} is the overlap capacitance per unit length. Figure 3.21 illustrates the V_{DS} voltages of PMOS switches for different W/L, the current flow of the switch is fixed to 6 mA and worst process corner is analyzed to get these results. As seen in Figure 3.21 to obtain maximum

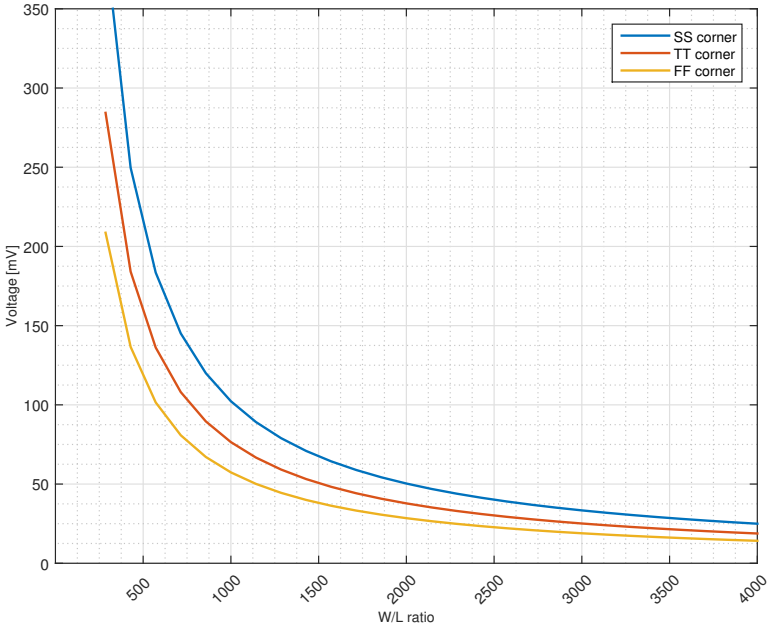

Figure 3.21 : V_{DS} drop in the PMOS switch for different W/L ratios.

50 mV voltage drop, W/L ratio must be higher than 2000 As L is minimum which is 0.35 μm, W must be chosen higher than 700 μm. Due to create proper layout plan, width of PMOS switches are chosen as same as transistor at the output current source array which is 40 μm. To minimize the parasitic capacitance, switches are designed in fingered structure with a 40 μm width and 20 finger that gives approximately 2285 W/L ratio and 35 mV V_{DS}drop at typical conditions.

After DC operating condition analysis is done to be sure that all transistors are in the saturation regime for all process corners. transient analysis is done due to examine the performance of amplitude and slew control system. As delay cells and comparator have not designed yet and ideal comparator and ideal delay cells, which are created

by using verilog-A, are used . In order to analyze system performance for different time delay of delay cells, reference voltage is fixed to $2.9V$ to provide that the output transistors work in the saturation region. As shown in Figure 3.22, output signals have

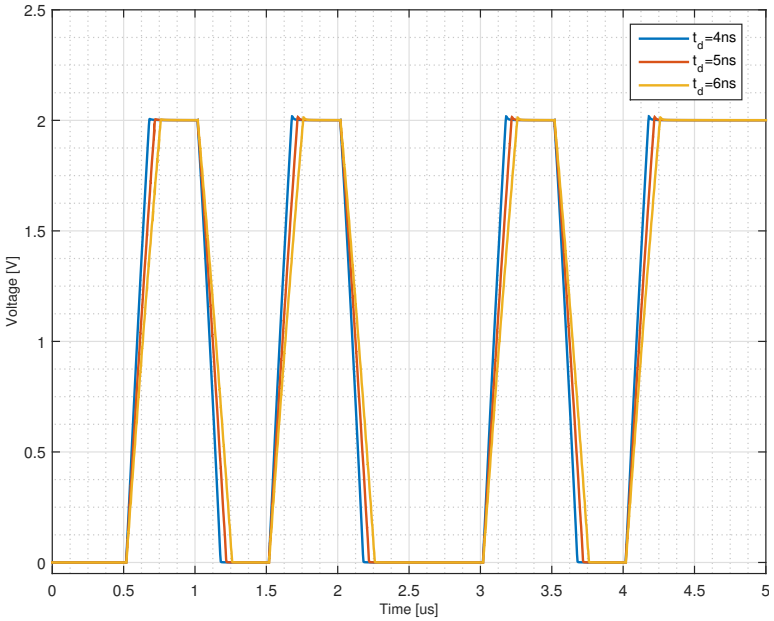

Figure 3.22 : Differential output signals with different time delays.

different rise and fall times which are 180 ns, 220 ns, 260 ns with respect to 4 ns, 5 ns and 6 ns delay times. After that, time delay is fixed to 5 ns and reference voltage is changed, Figure 3.23 demonstrate the output signal waveforms. As seen from Figure,

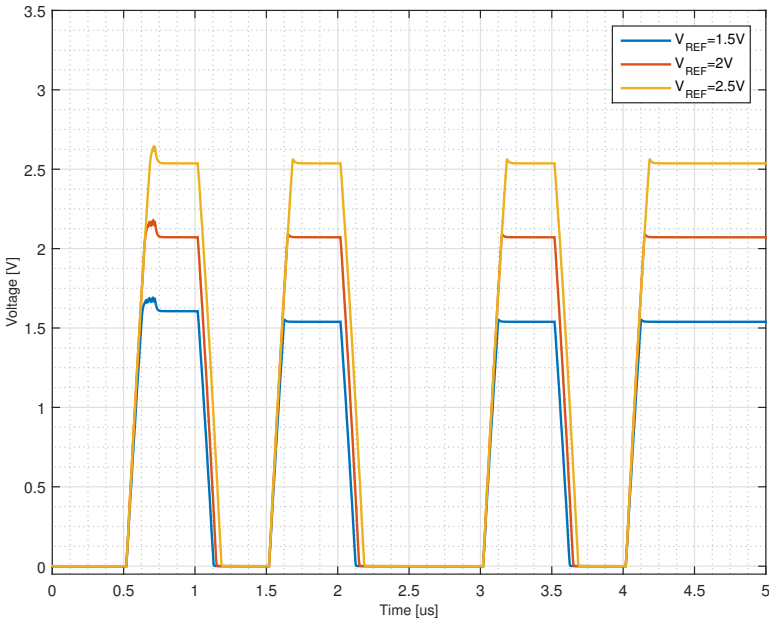

Figure 3.23 : Differential output signals for different amplitude thresholds.

after the output voltage level exceeds the reference voltage, amplitude detection system

disables the rest of output transistors, hence output voltage remains at the same level. Due to create reference voltage in the output more element in the current source array are activated.

3.4.1 Temperature compensated delay cell

An inverter is an commonly used delay cell in electronics. It can be used with an external load capacitance either it can be used benefiting from its parasitic capacitance as load capacitance. It is clear that using an external load capacitance leads each delay cell has more area in layout. However, benefiting parasitic capacitance is not a good solution to achieve accurate time delay. Because, process variations and temperature affects output current of inverter and the parasitic capacitance of transistor. As a result delay of inverter variates. Due to fact that accuracy of time delay is most important part of system, external load capacitor is the better solution to create time delay.

In the Figure 3.24, a two inverter with external load capacitance are seen. It is

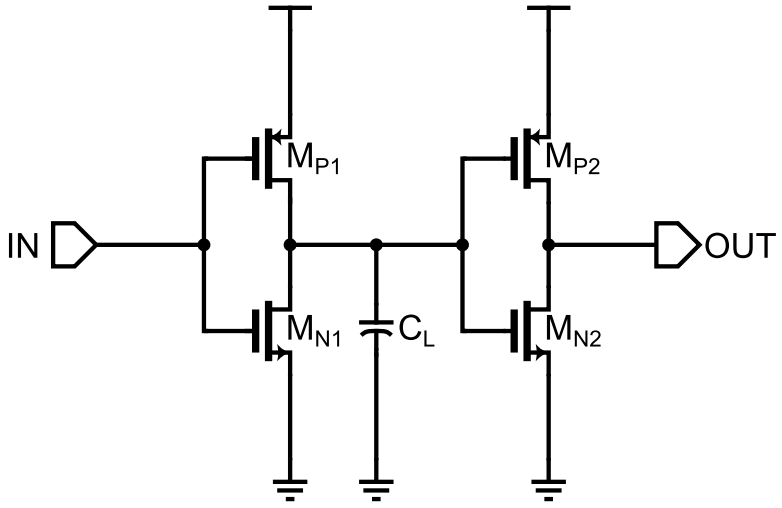

Figure 3.24 : Inverter based delay cell with external capacitance.

important that, while determining the delay time, delay cell should be analyzed with other logic circuitry due to they cause a delay too. W/L ratio of NMOS and PMOS transistor is chosen as 1 and 2 respectively to minimize current capability of inverters to create desired delay time at the output. Length of transistors are chosen as $1\,\mu$m to minimize the effect of mismatch and finally. First, ideal capacitive load is used to determine the exact value of capacitance which generates approximately 5 ns delay. It is obvious that the output signal falls logic low from to logic high by NMOS transistor and rises from logic low to logic high by PMOS transistor. Delay time can be found as

follows

$$t_{PHL} = t_{PLH} = C_L \frac{\frac{VDD}{2}}{\frac{1}{2}\mu_{N,P} C_{OX} \frac{W}{L} (V_{DD} - V_{th})^2} \tag{3.20}$$

$\mu_N C_{OX}$ parameter is approximately $50\,\mu\text{A}/\text{V}^2$ and $\mu_P C_{OX}$ parameter is approximately $25\,\mu\text{A}/\text{V}^2$ in the used process. Choosing a proper ratio between PMOS and NMOS transistor, which is approximately 2 for the used process, provides that low to high propagation delay and high to low propagation delay equals to each other. So, time delay is

$$\begin{aligned} t_d &= C_L \frac{\frac{VDD}{2}}{\frac{1}{2}\mu_{N,P} C_{OX} \frac{W}{L} (V_{DD} - V_{th})^2} \\ C_L &= \frac{t_d \frac{1}{2}\mu_{N,P} C_{OX} \frac{W}{L} (V_{DD} - V_{th})^2}{\frac{VDD}{2}} \\ C_L &= \frac{5e-9\frac{1}{2}50e-6(3.3-0.7)^2}{1.65} \\ C_L &= 440fF \end{aligned} \tag{3.21}$$

5.4 ns delay time is obtained with 440 fF load capacitance in the simulation because of the fact that parasitic capacitance of MOS transistors increase the effective load capacitance at the output node. C_L capacitance is decreased to 420 fF to obtain approximately 5 ns delay. After that, ideal capacitor is replaced with the MIM capacitor. MIM capacitors are the commonly used capacitor types due to low parasitic capacitance and good voltage linearity properties. MIM capacitor with a width of $18\,\mu$m and length of $18\,\mu$m for 418 fF capacitance generates a 4.97 ns time delay in the typical conditions. Figure 3.25 demonstrates the time delay variation over temperature. Main effect in the temperature dependency is based on a current variation of inverters over temperature. Controlling the current of inverters within temperature may create a chance to compensate the temperature dependency of delay cell. Therefore current bias is provided by an PTAT current which has a positive temperature coefficient. Designed delay cell is given in Figure 3.26 M_{P1} and M_{N1} are the first inverter cells which currents controlled by M_{P2} and M_{N2}. As same as that, M_{P3} and M_{N3} are the second inverter cells which are used to increase drive capability. Diode connected M_{P4}, which is biased by M_{N4} current source, is used to create proper bias voltage for M_{P2} transistor. $V_{N_{BIAS}}$ is the bias voltages of NMOS current sources.

First ideal current source and diode connected NMOS transistor is used to create $V_{N_{BIAS}}$ voltage. The current of the capacitive load at the node A, charges by the current of M_{P3}

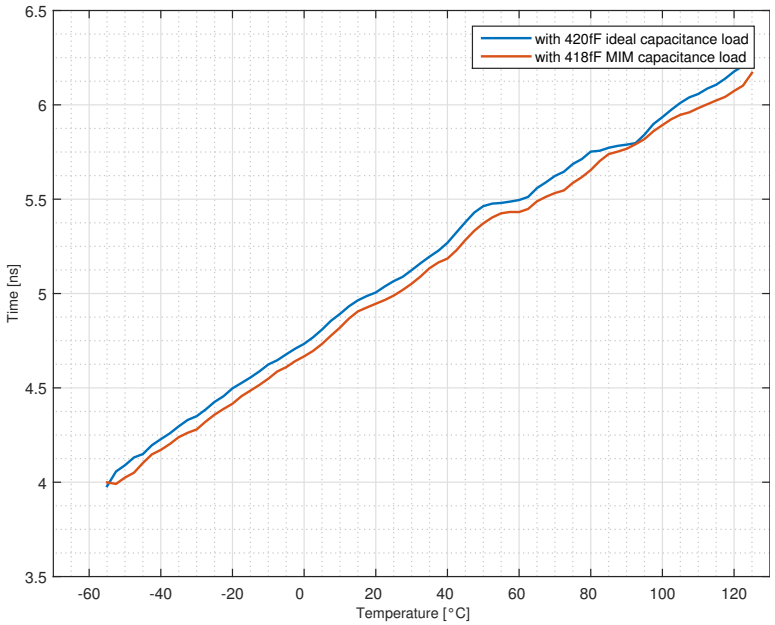

Figure 3.25 : Time delay change of a MIM capacitor loaded inverter based delay cell over temperature.

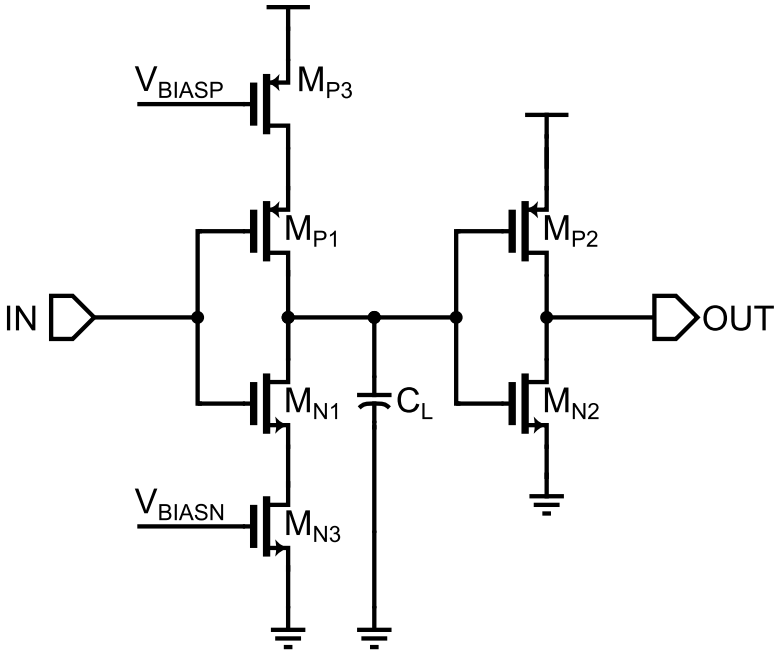

Figure 3.26 : Schematic of current starved delay cell.

and discharges by the current of M_{N3}. The delay time of cell can be find simply by using current-voltage equations of capacitor as follows

$$I_C = C\frac{dV_C}{dt}$$
$$I_C = C\frac{\Delta V_C}{\Delta t} \qquad \textbf{(3.22)}$$
$$I_C = C\frac{V_{C2} - V_{C1}}{t_2 - t_1}$$

As voltage change in the capacitor equals to $^{VDD}/_{2}$ which is the approximate threshold of the second inverter, and the desired time delay equals to 5 nss, 3.22 is rewritten as follows when the current of current starved inverter is $100\,\mu$A

$$\begin{aligned} I_C &= C\frac{V_{C2}-V_{C1}}{t_2-t_1} \\ C &= I_C\frac{t_2-t_1}{V_{C2}-V_{C1}} \\ C &= 100\mu\frac{5n}{1.65} \\ C &\cong 303.3fF \end{aligned} \tag{3.23}$$

Using a capacitor with a value 303 fF and $100\,\mu$A bias current gives a 4.3 ns time delay. Because channel length modulation cause an increase in the current of current starved inverter cell. So load capacitance is changed and determined as 330 fF with a $16\,\mu$m width and $16\,\mu$m length, which gives a 5.03ns time delay. Time delay variation corresponding to temperature is given in Figure 3.27. As seen from Figure

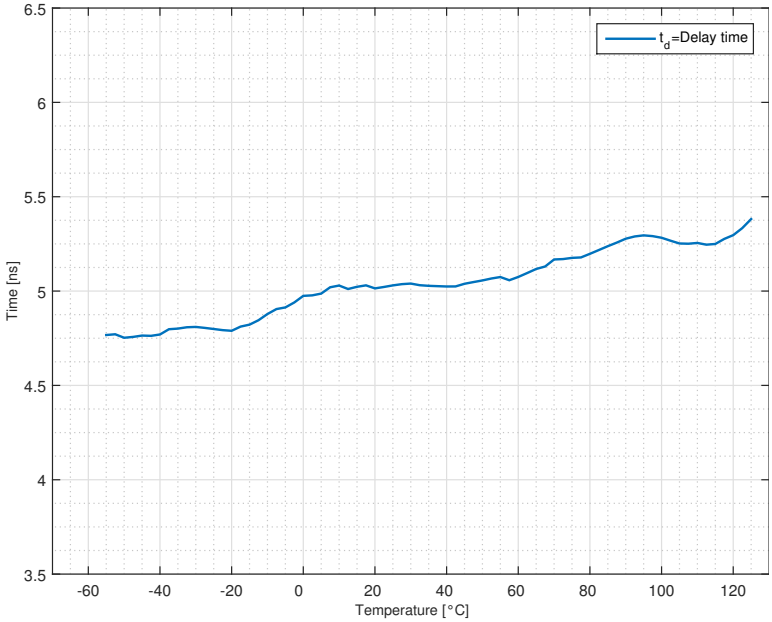

Figure 3.27 : Time delay change with temperature, ideal current source is used to bias circuit.

3.27 temperature dependency is better than the inverter based delay cell due to its controlled by current of M_{P3} and M_{N3}. As the current flow in the current starved inverter can be controlled, it is possible to obtain a temperature invariant time delay by adding a positive temperature coefficient to the current of current starved inverter cell. First, temperature dependent ideal current source is used to determine the exact temperature coefficient, the results are given in the Figure 3.28. As seen in Figure

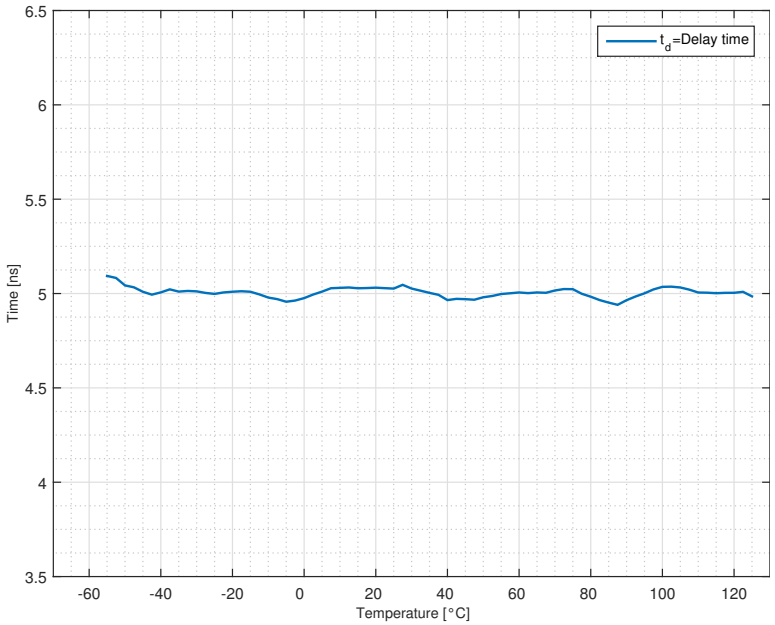

Figure 3.28 : Time delay change with temperature, ideal current source with temperature coefficient is used to bias circuit.

3.28, using an ideal current source with 800 $^{ppm}/_{^\circ C}$ temperature coefficient compensates the output time delay properly. This current can be created with a CTAT and PTAT current in the proper ratio. Although temperature effect is compensated, process and mismatch effects are not compensated. In the Figure 3.29, time delay changes with different process corners are given. In additional to process corners which are fast-fast,

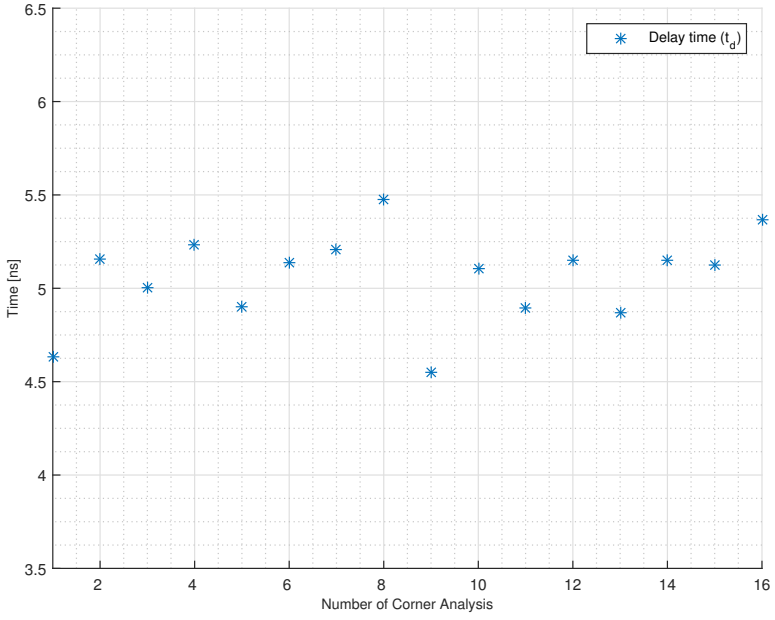

Figure 3.29 : Time delay change with different process corners.

slow-slow e.t.c, supply voltage variation and minimum-maximum temperature cases are added to corner points. Also MOS models and capacitor models are added

separately to corner points. Thus, MOS models may be in the fast corner when capacitors are in the slow corner, vice-versa. Figure 3.30 illustrates the time delay variation in the mismatch analysis. Statistical analysis shows that maximum time delay is 5.22 ns and minimum time delay 4.72 ns. The mean value is 4.998 ns and the standart deviation is 104.15 ps. All these analysis must be repeated after implementing

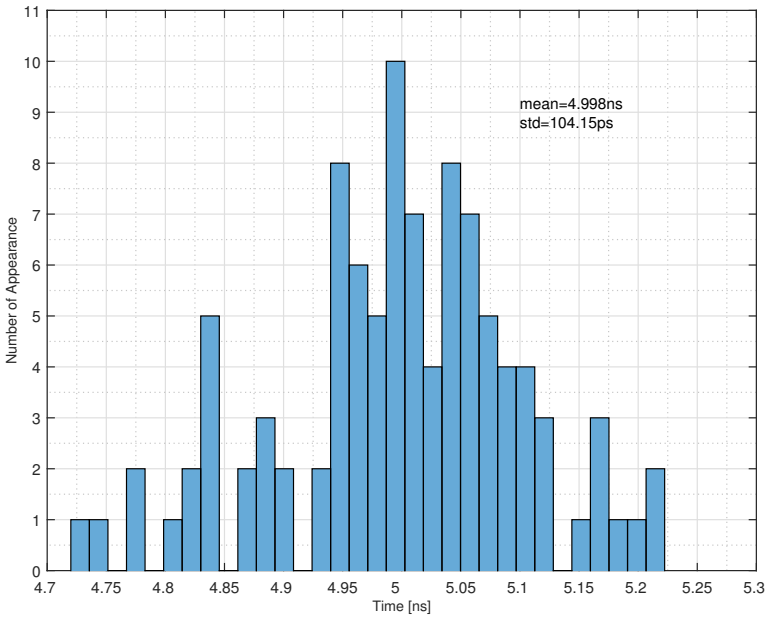

Figure 3.30 : Time delay change in mismatch analysis.

temperature proportional current source due to fact that current variations directly effects temperature dependency of time delay.

3.4.2 Comparator

A Miller Op-amp based comparator is implemented to control whether the output voltage level exceeds the reference level or it is below the reference level which is seen in Figure 3.31. M_{N1} and M_{N2}, NMOS transistors are used in the input pair. The offset of input pair is not critical because of the fact that the comparison is done between a constant reference signal and output signal. Hence, length of input transistors are chosen minimum to minimize the parasitic capacitance. M_{P1} and M_{P2} are the active loads of input differential pair which creates the bias voltages for the input transistors of the second stage and replica stage. M_{P4} is the input pair of second stage which bias current is provided by M_{N4} current source. To create proper bias voltage for M_{N4}, replica of second stage is created using M_{P3} and M_{N3}. 2 pair of inverters are used at the output of second stage due to maximize the open loop gain of comparator, also

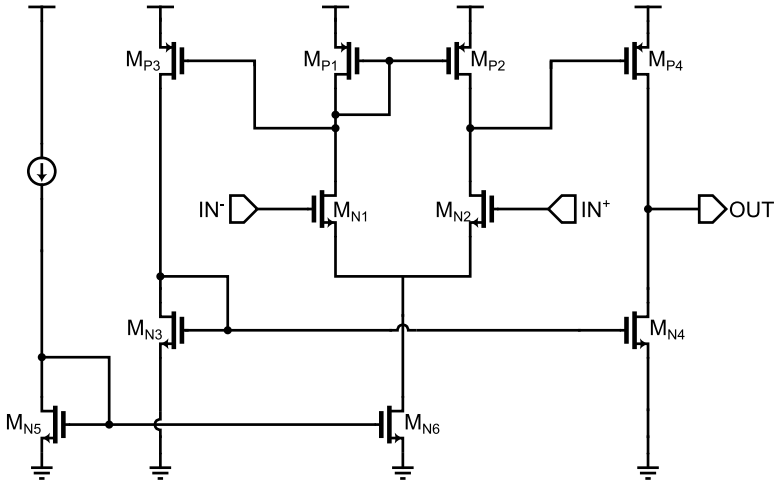

Figure 3.31 : Schematic of Miller opamp based comparator.

to increase the driving capability of comparator. Transistors in the miller op-amp based comparator must be sized properly due to avoid from the systematic offset which is a common problem in the design of miller op-amps and miller op-amp based comparators (Gray, Hurst, Lewis, & Meyer, 2009).

Input bias current is chosen as $10\,\mu$A, therefore the current of M_{N5} is $160\,\mu$A in the typical conditions, since the ratio between M_{N6} and M_{N5} is 16. It is obvious that, same current flows from M_{P1} and M_{P2} transistors and create same voltages on the drain of these transistors while input voltages of the comparator is equal. Therefore, gate voltage of M_{P3} and M_{P4} is same and these transistors acts as a current mirrors. The ratio between M_{P3} and M_{P4} is chosen as 2. So, M_{N3} must be sized twice of M_{N4} due to avoid systematic offset. A constant reference signal is implied to negative output of comparator and a square wave with a 200ns rise and fall time is implied to positive input of comparator to analyze performance of comparator. The result of transient analysis is given in Figure 3.32. Although, speed of comparator does not harm the operating of amplitude and slew control system, it must be well considered. In the system, comparator output controls the data of D type flip-flop and the delay cells controls the clock input of each D type flip-flop. So that, if comparator output cannot rise to high level before the time delay of delay cells. Output amplitude will increase redundantly. This property is the response time of comparator. In the Figure 3.33 zoomed signals is given, as shown high to low response time is approximately 2.16 ns and low to high response time is approximately 2.94 ns. However, in the worst speed process corners and in the higher temperature, comparator response time may

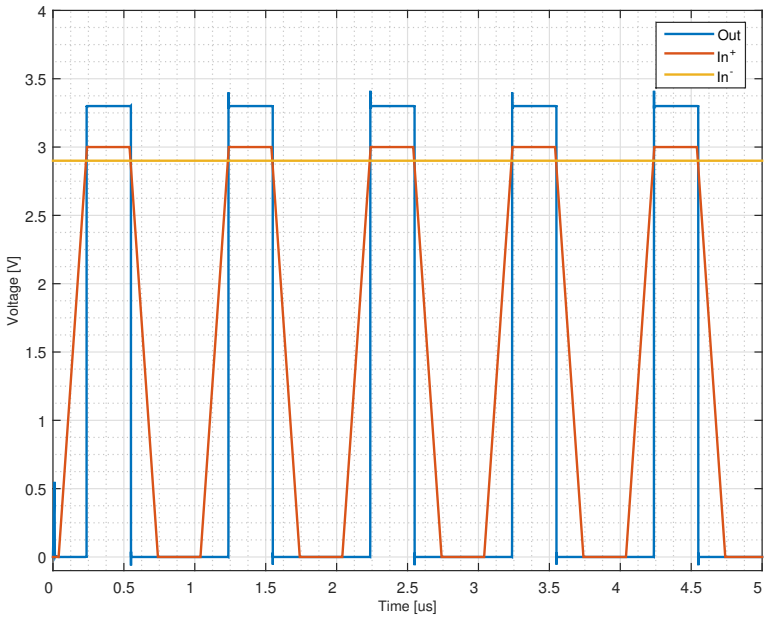

Figure 3.32 : Transient analysis result of miller opamp based comparator.

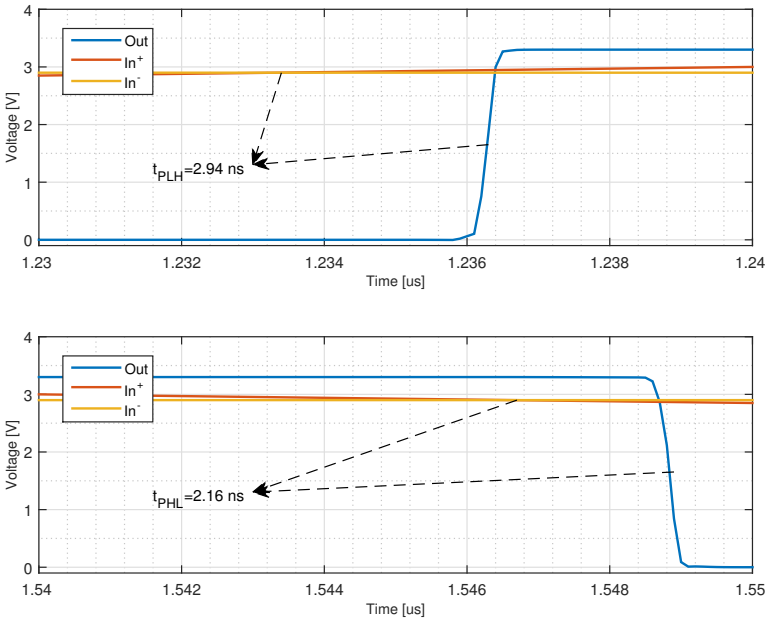

Figure 3.33 : Response time of comparator in typical conditions.

increase. So that, this analysis must be repeated at the worst speed configuration, where temperature is 125°C, supply voltage is 3.15 V and slowest process corner is applied. The results which is seen in Figure 3.34 shows that, high to low response time is 2.58 ns and low to high response time is 3.78 ns which are still below the minimum expected time delay of delay cells. Out of that offset of input pair does not harm the system, mismatch analysis are not necessary for designed comparator.

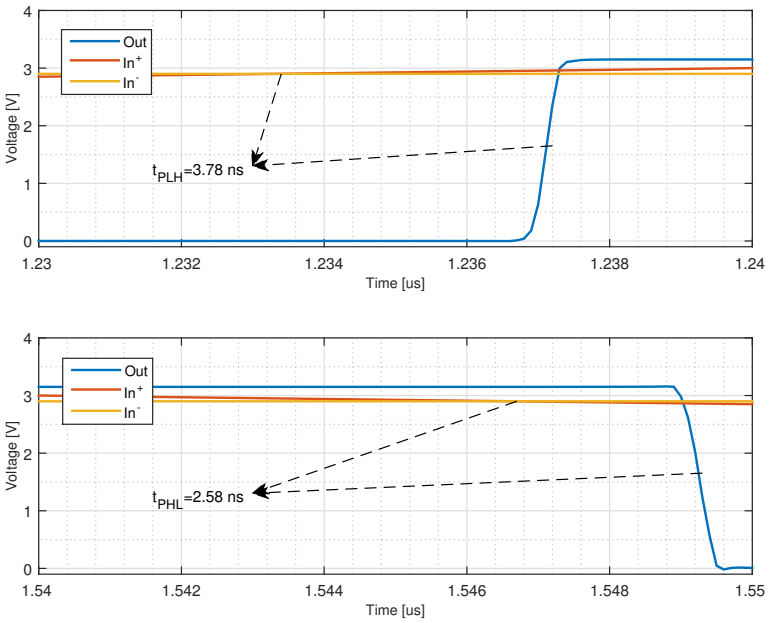

Figure 3.34 : Response time of comparator in the worst speed conditions.

3.5 Other Sub-blocks

Main system is working properly with ideal current sources and voltage references. Current reference of output current source array and current reference of delay cells are important parameters which affect circuit performance directly. Also, voltage reference of comparator is another important parameter. As mentioned before, current reference of delay cells must have a specific temperature coefficient. This reference must be created using PTAT and CTAT currents together. There are several different ways to create this currents. Benefiting from V_{BE} and ΔV_{BE} voltages of Bipolar transistors is one way to create these currents.Also using a resistors with different temperature coefficient is another way. For the second way, temperature independent voltage must be created to get proper temperature coefficient current. This voltage can be created by a band-gap voltage reference circuit easily. Also it is clear that band-gap reference circuits can be used to create PTAT and CTAT currents.

3.5.1 Band-gap reference

Band-gap reference circuits was first published in 1964 by David Hilbiber (Hilbiber, 1964). After that Bob Widlar publishes a voltage regulator (Widlar, 1971). Finally a new band-gap reference circuit is published in 1974 by Paul Brokaw is shown in

Figure 3.35 (Brokaw, 1974). This architecture always have been a mile stone for the

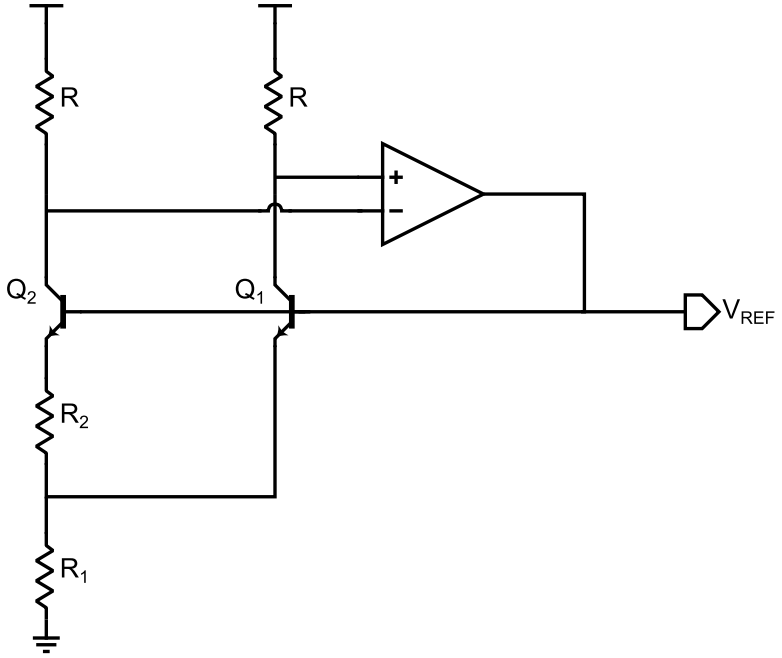

Figure 3.35 : Band-gap reference circuit which is published in 1974, commonly known as Brokaw Band-gap Reference (Brokaw, 1974).

developed reference circuits for all time. In the Brokaw band-gap reference circuit, emitter area of Q_2 is chosen larger than Q_1. If we assume, I_{C1} current flows from Q_1 and I_{C2} current flows from Q_2, the current which flows from R_1 will be the sum of I_{C1} and I_{C2}. Voltage of Q_2 emitter can be written as following

$$V_{E2} = R_1(I_{C1} + I_{C2}) \tag{3.24}$$

As base voltage of Q_1 and Q_2 is same, emitter voltages of these transistor can be written as following

$$\begin{aligned} V_{E1} &= V_B - V_{BE1} \\ V_{E2} &= V_B - V_{BE2} \end{aligned} \tag{3.25}$$

As a result current flow of I_{C1} can be written using 3.25

$$\begin{aligned} I_{C1} &= \frac{V_{E1} - V_{E2}}{R_2} \\ &= \frac{V_B - V_{BE1} - (V_B - V_{BE2})}{R_2} \\ &= \frac{V_{BE2} - V_{BE1}}{R_2} \\ &= \frac{V_t \ln \frac{I_{C2}}{I_{S2}} - V_t \ln \frac{I_{C1}}{I_{S1}}}{R_2} \\ &= \frac{V_t \ln \frac{I_{S1}}{I_{S2}}}{R_2} \end{aligned} \tag{3.26}$$

As emitter area of Q_1 is N times greater than Q_2, I_{S1} is N times greater than I_{S2}. So 3.26 is written again according to this information

$$\begin{aligned} I_{C1} &= \frac{V_t \ln \frac{I_{S1}}{I_{S2}}}{R_2} \\ &= \frac{V_t \ln N}{R_2} \end{aligned} \tag{3.27}$$

It is known that inputs of an ideal operational amplifier must be same because of the negative feedback. So R_3 and R_4 have same voltage differences. If this resistors are chosen same, same current flows through the Q_1 and Q_2. As base current of transistors is much smaller than collector current, emitter currents can be assume equal. Finally, V_{REF} can be written using 3.24 and 3.27,

$$\begin{aligned} V_{REF} &= V_{E2} + V_{BE2} \\ &= R_1(I_{C1} + I_{C2}) + V_{BE2} \\ &= R_1(2I_{C1}) + V_{BE2} \\ &= V_{BE2} + \frac{R_1}{R_2} V_t \ln N \end{aligned} \tag{3.28}$$

Temperature variance of V_{REF} is given in 3.29

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE2}}{\partial T} + \frac{R_1}{R_2} \ln N \frac{\partial V_t}{\partial T} \tag{3.29}$$

It is known that base-emitter voltage has a negative temperature coefficient, however V_t is thermal voltage of p-n junction and it can be described as following

$$V_t = \frac{kT}{q} \tag{3.30}$$

where k is Boltzmann constant, T is temperature and q is the electrical charge on the electron. As seen from 3.30, V_t, thermal voltage is proportional to temperature, so it has positive temperature coefficient and can be calculated as following

$$\begin{aligned}\frac{\partial V_t}{\partial T} &= \frac{k}{q}\frac{\partial T}{\partial T} \\ &= \frac{k}{q} \cong \frac{1.38x10^{-23}}{1.602x10^{-19}} \cong 0.08614 \text{ mV/°C}\end{aligned} \tag{3.31}$$

Calculating temperature coefficient of V_{BE} is more complicated. Thus, there are many different component which is related to temperature.Formula of V_{BE} is given in 3.32

$$V_{BE} = V_t \ln J_C \frac{W_B}{q\overline{D_n} n_p 0} \tag{3.32}$$

where J_C is collector current density, $\overline{D_n}$ is electron's average diffusion constant, W_B is base width, n_{p0} is equilibrium concentration of electrons in base. Equilibrium concentration in base can be written as following

$$\begin{aligned}n_{p0} &= \frac{n_i^2}{N_A} \\ n_i^2 &= DT^3 \exp\frac{-V_{GO}}{V_t}\end{aligned} \tag{3.33}$$

N_A is acceptor impurity concentration, D is temperature independent constant and V_{GO} is the band-gap voltage of silicon which is approximately 1.205 V. So if V_{BE} is written again using 3.33,

$$V_{BE} = V_{GO} + V_t \ln J_C \frac{W_B N_A}{q D_n D T^3} \tag{3.34}$$

If temperature coefficient is calculated benefiting from temperature coefficient of collector current density and silicon band-gap voltage. It is given in 3.35 (Allen, 2001).

$$\frac{\partial V_{BE}}{\partial T} = \frac{-V_{GO}}{T_0} + \frac{V_{BE0}}{T_0} - \frac{3.2k}{q} + \frac{k}{q} \tag{3.35}$$

As T_0 is room temperature, V_{BE0} equals to approximately 650 mV and V_{GO0} at the room temperature equals to 1.205 V, as a result temperature coefficient of V_{BE} can be found as following

$$\begin{aligned}\frac{\partial V_{BE}}{\partial T} &= \frac{-1.205}{300} + \frac{0.65}{300} + (-3.2+1)\left(\frac{1.3806x10^{-23}}{1.602x10^{-19}}\right) \\ &= -4.01667x10^{-3} + 2.16667x10^{-3} - 1.896x10^{-4} \\ &= 2.04 \text{mV/°C}\end{aligned} \tag{3.36}$$

In the Figure 3.36, a band-gap circuit is shown which is originated from Brokaw band-gap reference. Due to fact that idea is as same as Brokaw architecture, reference

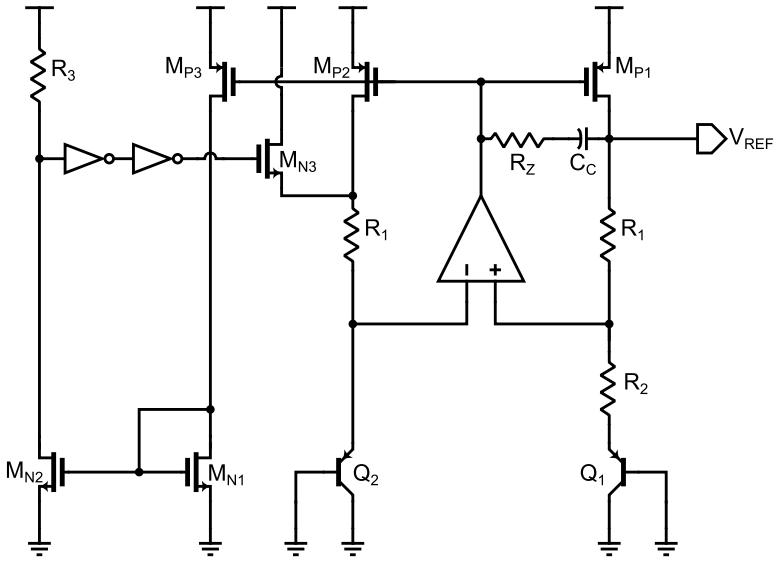

Figure 3.36 : Designed band-gap reference circuit.

voltage equation is equal to reference voltage equation of Brokaw architecture. Length of M_{P1} and M_{P2} is chosen as $1\mu m$ due to increase output resistors of transistors. As a result current mismatch is minimized and the voltage gain of PMOS common source stage is increased too. As seen from 3.28 R_1 and R_2 ratio determines the temperature dependency.

First, N which is the emitter area ratio between bipolar transistors is determined. As bipolar transistors have a square type layout, N should be chosen as $k^2 - 1$, where k is even number to get a conceptional layout. As a result k is chosen 5 and so that N is determined as 25 which generates a 5x5 square layout. After that, dc temperature sweep analysis is done due to investigate temperature coefficient of output reference voltage. First, ideal resistors are used to determine the exact ratio, which is found as 5.86 in typical conditions, to cancel temperature coefficients. In order to minimize the mismatch effect, higher resistor values are chosen as R_2 value is $11\,k\Omega$ and R_1 value is $64.5\,k\Omega$. As shown in Figure 3.37, temperature coefficient of reference voltage is approximately $14.6\,ppm/^{\circ}C$. It is clear that, replacing ideal resistors with the real ones effects temperature dependency of output voltage because of the temperature coefficients of the real resistors. There are several different resistors which have different temperature coefficients and different square resistance e.t.c. in the process design kit. As the matching between the resistors is one of the most significant point of band-gap reference circuit design, it is important to minimize the mismatch effect. Thus, unit resistor, which is chosen as approximately $5.47\,k\Omega$ with a $2\,\mu m$ width and

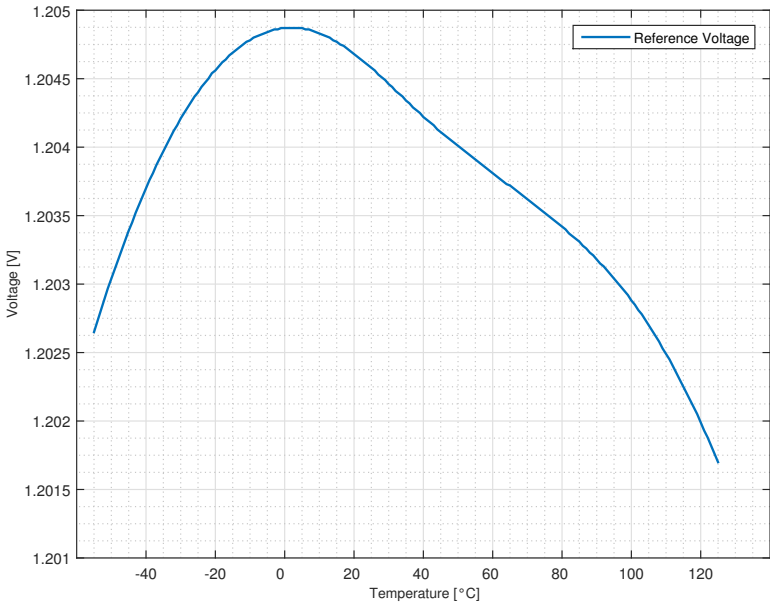

Figure 3.37 : Reference voltage versus temperature (ideal resistor is used).

10 μm length, is used to implement R_1 and R_2 resistors. Two unit resistor is used to generate R_2 resistor and eleven resistor is used to generate R_1 resistor. However, this ratio did not satisfy desired temperature cancellation because of the fact that the ratio between R_1 and R_2 is 5.5 which is below than theoretical value 5.86. To increase that ratio R_1 is increased by adding some parallel unit resistors in series to R_1. 5 unit resistor is paralleled and added to R_1 resistors and dc sweep analyzed is repeated again. Results are given in Figure 3.38. As shown in Figure 3.38 output

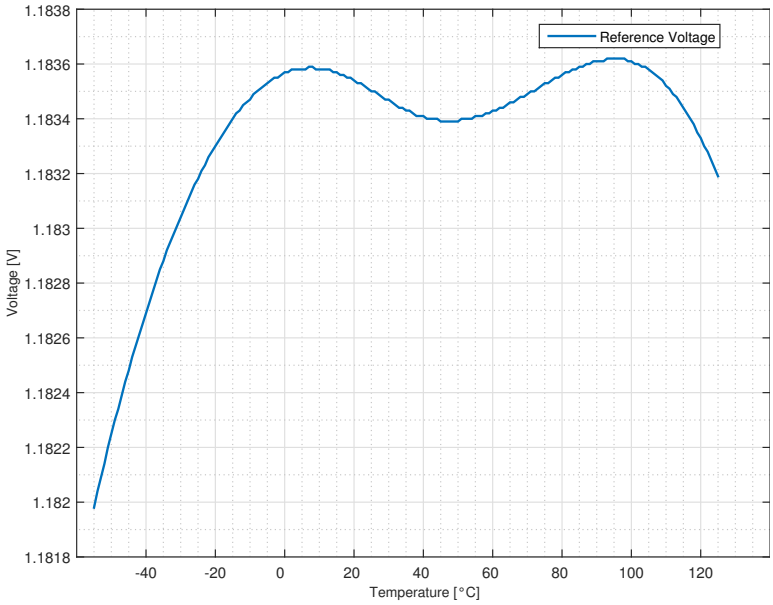

Figure 3.38 : Reference voltage versus temperature.

temperature curve is third degree polynomial. In that, temperature coefficients of the

poly resistors modulates the second degree output curve. This leads better circuit performance, approximately 7.8 ppm/°C. It is clear that, this temperature coefficient is in the typical conditions. Process corners and mismatches modulates this curve. The results of corner and mismatch analysis are given in Figure 3.39 and 3.40. The

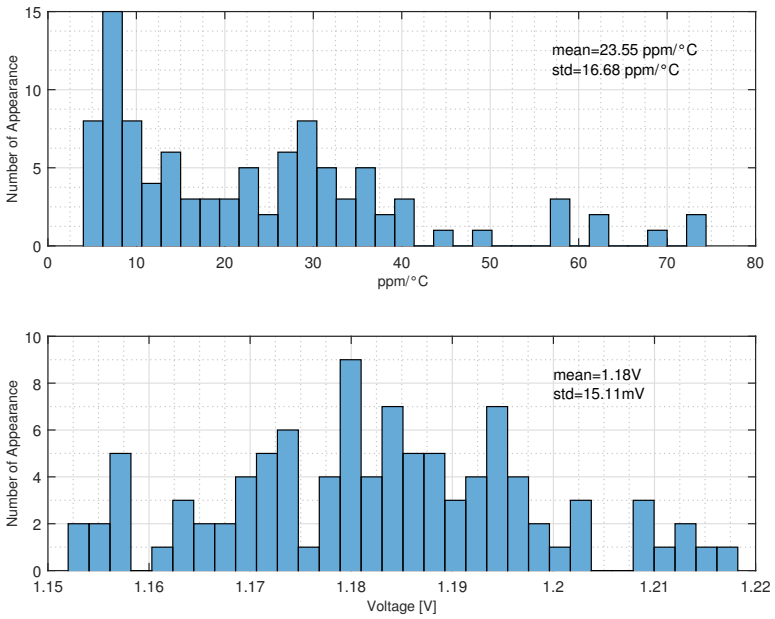

Figure 3.39 : Variation of temperature coefficient and reference voltage at @25°C in mismatch analysis.

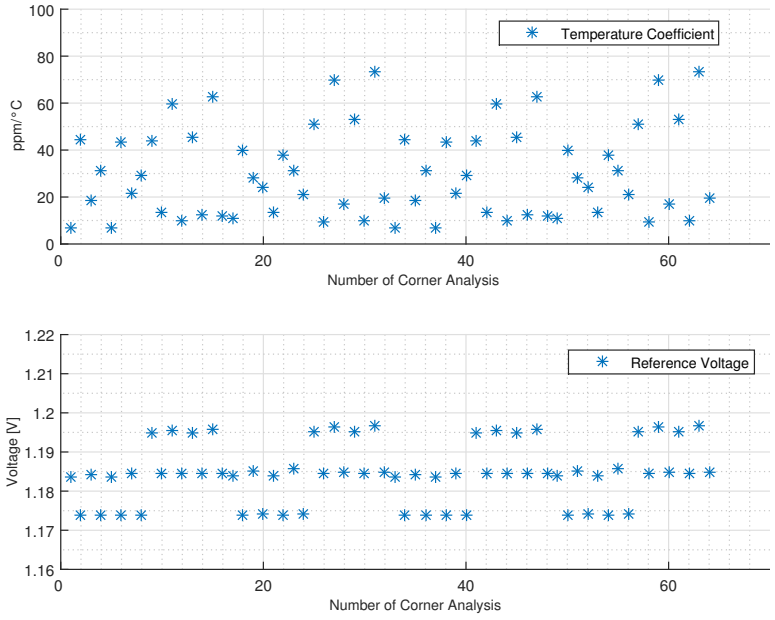

Figure 3.40 : Variation of temperature coefficient and reference voltage at in corner analysis.

band-gap circuit is analyzed in time domain due to see the performance of start-up circuit. Start-up circuit works as follows; assume that supply voltage is zero in the

time at 0, when the supply voltage increase, input of first inverter is raised to logic high by R_3 resistor. As a result, output of the second inverter raises to logic high from logic low. A V_{BE} voltage occurs on the input of the amplifier because of the fact that current starts to be sourced to Q_1 by M_{N3}. As positive input of amplifier is ground and negative input of amplifier is approximately V_{BE} voltage, output of the amplifier falls to the ground potential which leads M_{P1} and M_{P2} transistors to conduct. M_{P3} transistor source a current, which is determine by its ratio between M_{P1} and M_2. This current is mirrored to M_{N2}, corresponding to ratio between M_{N1} and M_{N2} and generates voltage drop on R_3 resistor. R_3 is chosen as large enough to create a necessary voltage drop which falls input voltage of the inverter below the threshold voltage. As a result, the output of the inverter is logic low and M_{N3} is off. Figure 3.41 demonstrates the time domain analysis of circuit. There are two feedback loops in the Brokaw band-gap

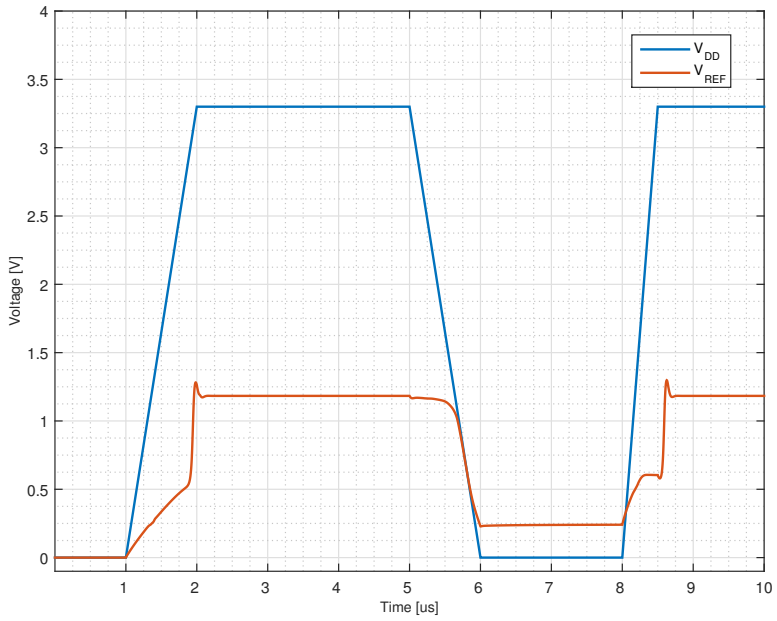

Figure 3.41 : Time domain analysis of start-up circuit and band-gap core.

architecture, one is negative feedback loop and the other is positive feedback loop. In the designed circuit, negative feedback loop consists of opamp and common source gain stage which is implemented by M_{P1} with resistive load. Positive feedback loop is similar which consists of opamp and M_{P2} common source gain stage. It is obvious that gain of negative feedback loop must be larger than the positive feedback and compensation must be added to circuit due to avoid oscillation. Loop stability analysis is illustrated in Figure 3.42. Phase margin of the loop is approximately 88 °C and gain margin is approximately 41.2 dB which are decent numbers to obtain stable loop.

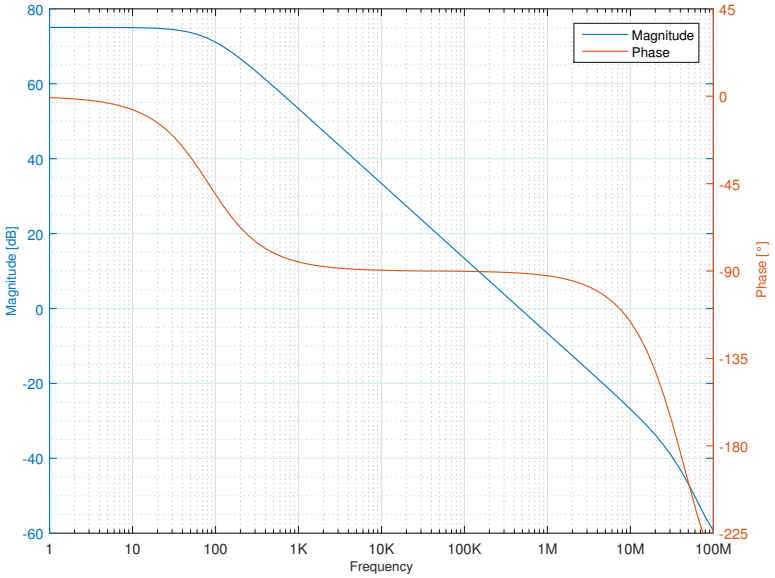

Figure 3.42 : Loop stability analysis of band-gap core.

3.5.1.1 Voltage to current converter

A current reference which is used in the circuit can be generated by using temperature invariant voltage reference of the band-gap reference circuit. Figure 3.43 demonstrates the the circuit that is used to convert voltage to current. Cascode current mirror is

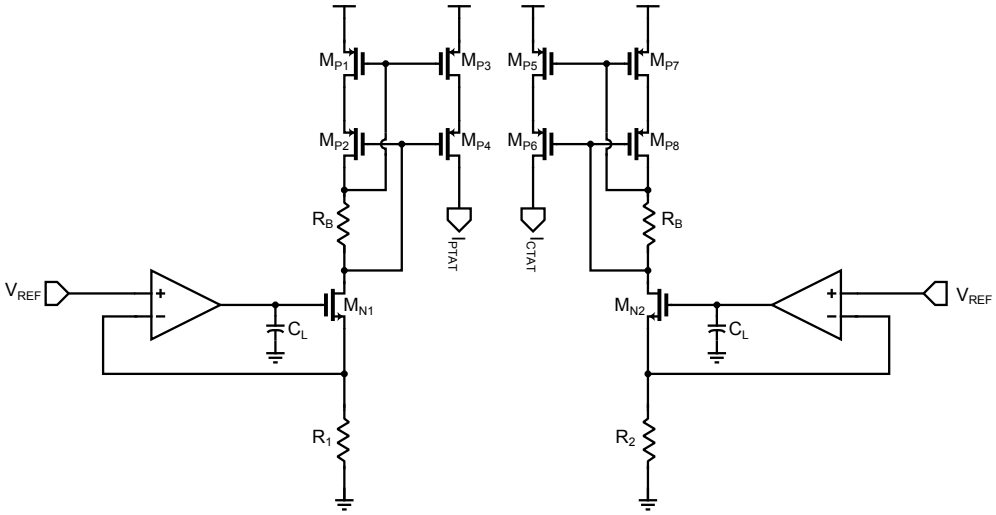

Figure 3.43 : Schematic of voltage to current converter circuit.

used to generate bias voltages for the current sources. There are two independent voltage to current converter architecture in the circuit, one is used to create PTAT current and the other is used to create CTAT current. Resistor with different temperature coefficients are used to create CTAT and PTAT currents. R_1 is a N+ type doped polysilicon resistor which has a negative temperature coefficient approximately

$-2.9\,e^{-3}/K$. R_2 is a silicided polysilicon resistor which has a positive temperature coefficient approximately $0.4\,e^{-3}/K$. Assuming reference voltage, which is obtained by band-gap reference, is temperature invariant, the current generated by R_1 branch is PTAT current and the current generated by R_2 branch is CTAT current.

Main operation of the circuit as follows, the feedback loop which consist of an amplifier and source follower stage forces the negative input node of the amplifier to be equal with reference voltage. Hence, the current flow on the source follower stage can be written as follows

$$I_{B1} = \frac{V_{ref}}{R_1}$$
$$I_{B2} = \frac{V_{ref}}{R_2} \tag{3.37}$$

Figure 3.44 demonstrates the obtained PTAT and CTAT currents. PTAT current is adjusted to approximately $20\,\mu A$ and CTAT current is adjusted to approximately $80\,\mu A$ at the typical conditions. 3.37 shows that the current is determined by resistor values

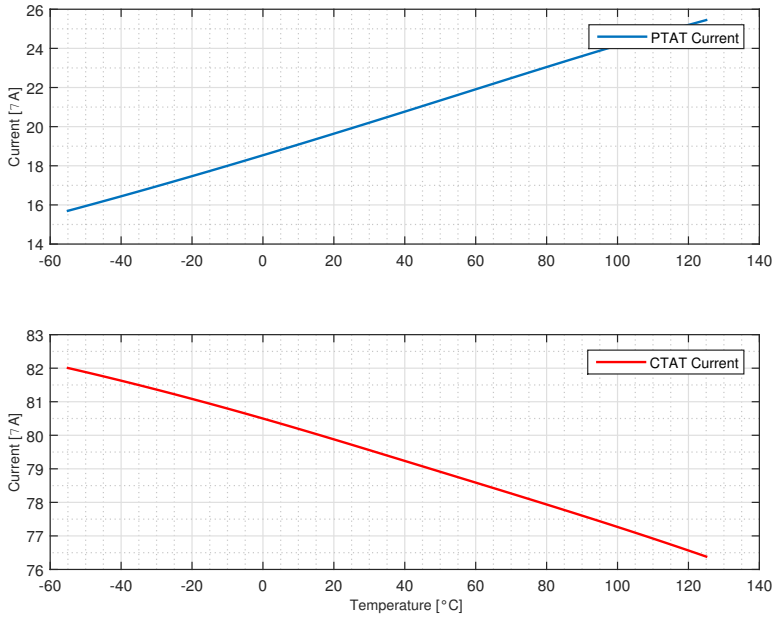

Figure 3.44 : PTAT and CTAT currents vs Temperature.

directly, therefore any variation which can get the maximum value in the process corners, cause a change in the reference current. As shown in Figure 3.45, the variation of reference current is approximately 10 percent in the process corners and variations are gathered in the maximum and minimum regions corresponding to whether fastest corner or slowest corner occurs. Other component which affects the current variation is the mismatch effect. As the current is transferred the other circuitry by current

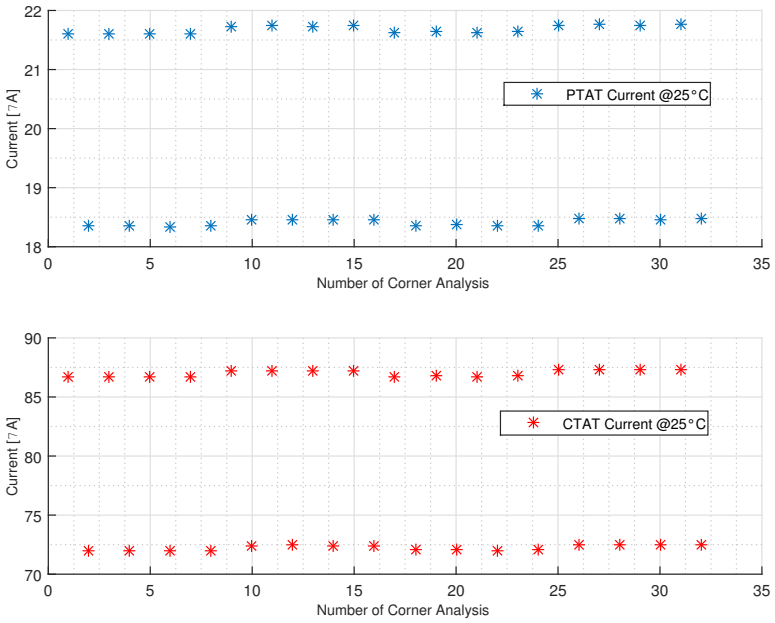

Figure 3.45 : PTAT and CTAT current variations in the process corners.

mirrors, it is important to design current mirror with minimizing the mismatch effect. Choosing a large geometry transistors reduce the main mismatch effect which caused by the V_t mismatch and the geometry mismatches. Resistor mismatches make a major contribution to the current variations. There are several solution to minimize the resistor mismatch effects which are proper layout, design with unit resistors and large geometry. Large geometry reduces the effect of geometrical mismatch which is occur in the production. Furthermore, it is possible to reduce random mismatch effect by implementing resistors with unit resistors and inter-digitized layout. Figure 3.46 illustrates the Monte Carlo analysis of PTAT and CTAT currents.

3.5.1.2 Current reference with a fixed temperature dependency

As mentioned before a current reference with a fixed temperature dependency is needed to obtain a temperature independent delay time. PTAT anc CTAT currents are summed with certain ratios to obtain required temperature coefficient which is determined as $800\,\mathrm{ppm}/^{\circ}\mathrm{C}$. Temperature ceofficient of the CTAT and PTAT currents are $-300\,\mathrm{ppm}/^{\circ}\mathrm{C}$ and $530\,\mathrm{ppm}/^{\circ}\mathrm{C}$ respectively. Therefore, a reference current with a $800\,\mathrm{ppm}/^{\circ}\mathrm{C}$ temperature coefficient can be obtained by summing 2 times PTAT current and $3/4$ times CTAT current. Figure 3.47 demonstrates the ideal current source with a $800\,\mathrm{ppm}/^{\circ}\mathrm{C}$ temperature coefficient and the generated reference current. Corner analysis and Mismatch analysis result is given in Figure 3.48. Delay time analysis is repeated

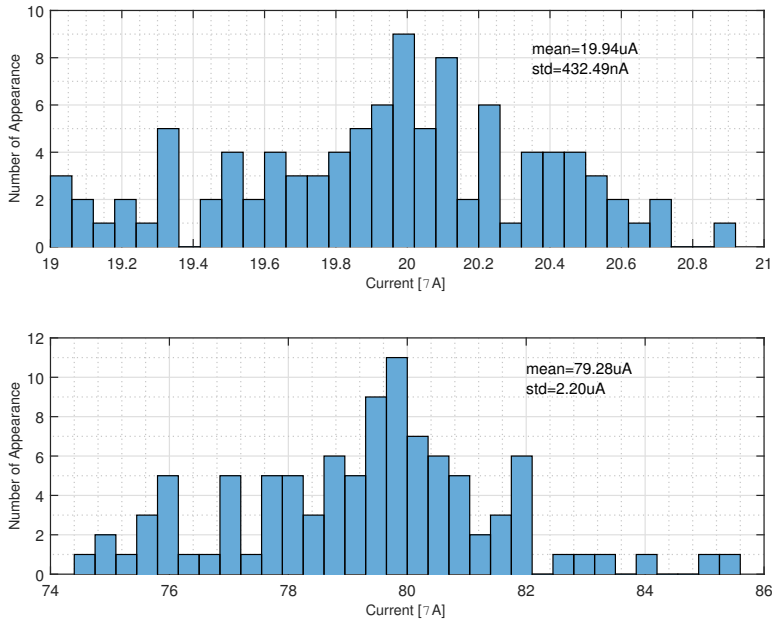

Figure 3.46 : Monte carlo analysis results of PTAT and CTAT current.

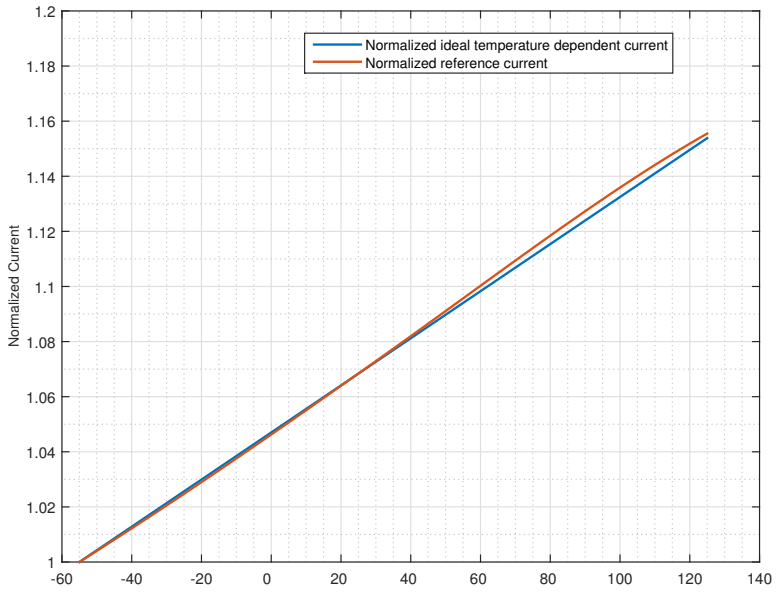

Figure 3.47 : Temperature dependency of ideal current with temperature coefficient and generated reference current.

after the reference current is generated by using PTAT and CTAT currents. As shown in Figure 3.49, percentage variations in delay time are almost same, however a small shift occurs in the mean value.

3.5.2 Power on reset circuit

Power on reset circuit is used to initialize circuit in the known and desired point when supply voltage is applied. Even it is used to generate reset signal for analog parts of circuit, main importance of the circuit is generating a reset signal for digital circuitry

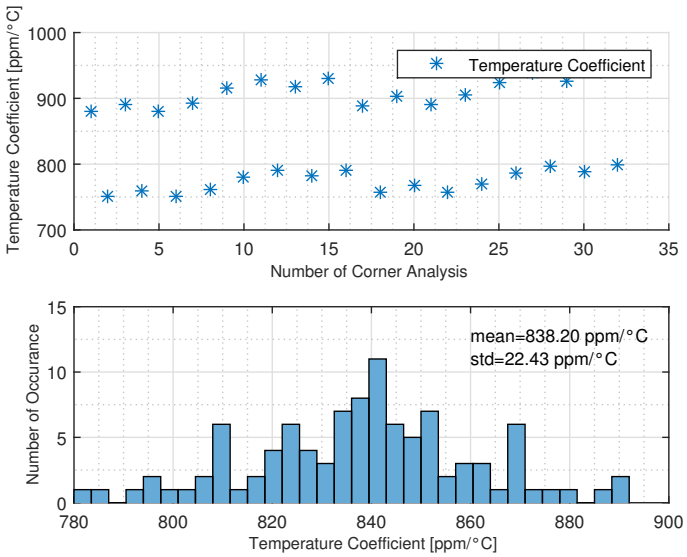

Figure 3.48 : Corner and Mismatch analysis of reference current with fixed temperature coefficient.

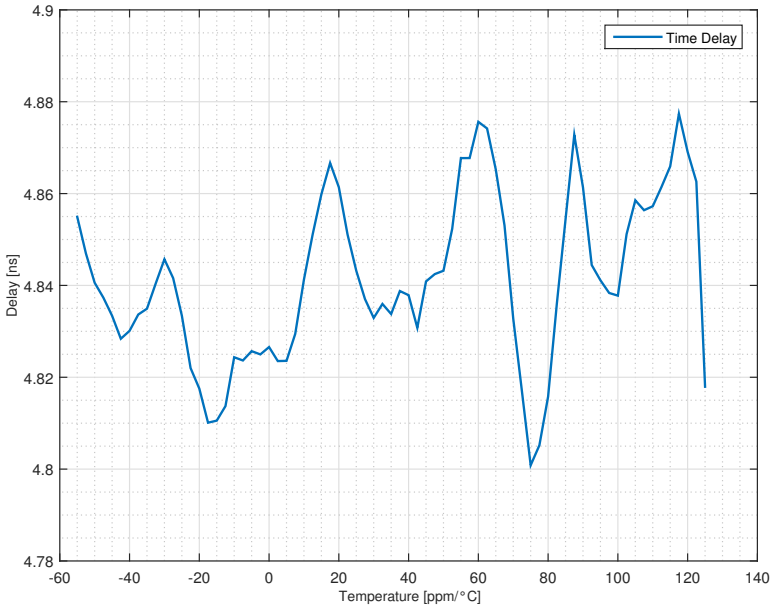

Figure 3.49 : Temperature dependency of delay time.

such as latches, flip-flops e.t.c. Common architecture which is used in integrated circuit design consists of a resistor and a capacitor. When the supply voltage ramps up, capacitor charges a certain voltage with RC time delay which is generated by resistor and capacitor. An inverter, which is connected to the charging node of the capacitor, creates a reset signal for the other circuitry when the charging node voltage is below than the threshold voltage of inverter. Figure 3.50 demonstrates the schematic of power on reset circuit. Diode connected M_{P1}, M_{N1} transistors and R_1 resitor are used to create a bias current for the circuit. That current is mirrored to M_{P3} transistor

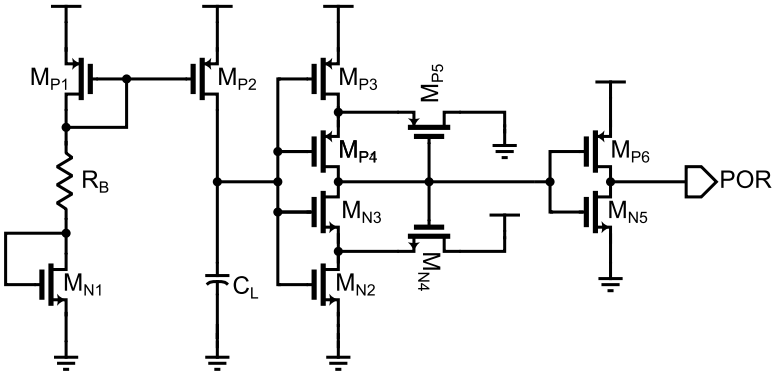

Figure 3.50 : Schematic of power on reset circuit.

by M_{N2} and M_{P2}. M_{N3} transistor are used as capacitor by connecting it drain, source and bulk terminal to the ground. The capacitance at the node A equals to overlap capacitance of NMOS transistor. As V_{DD} raises from ground potential to a certain level, M_{P3} transistors starts to source a current to parasitic capacitance of NMOS transistor and node A starts to raise. Voltage change in the NMOS capacitor can be written as following

$$\frac{dV}{dt} = \frac{I_C}{C} \tag{3.38}$$

I_C is determined from the bias current which equals to

$$I_{Bias} = \frac{V_{DD} - V_{GS_P} - V_{GS_N}}{R_1} \tag{3.39}$$

as the mirroring ratio is assumed as k, I_C is equals to k times I_{Bias}. So, 3.38 is written again

$$\begin{aligned} \frac{dV}{dt} &= \frac{I_C}{C} \\ \frac{dV}{dt} &= \frac{kI_{Bias}}{C} \\ \frac{dV}{dt} &= \frac{k\frac{V_{DD}-V_{GS_P}-V_{GS_N}}{R_1}}{C} \end{aligned} \tag{3.40}$$

As seen from 3.40 voltage change at the node A has a RC time constant. A CMOS schmitt trigger is connected to node A to create reset signal for the system. Output signal of power on reset circuit and the supply voltage is illustrated in the Figure 3.51.

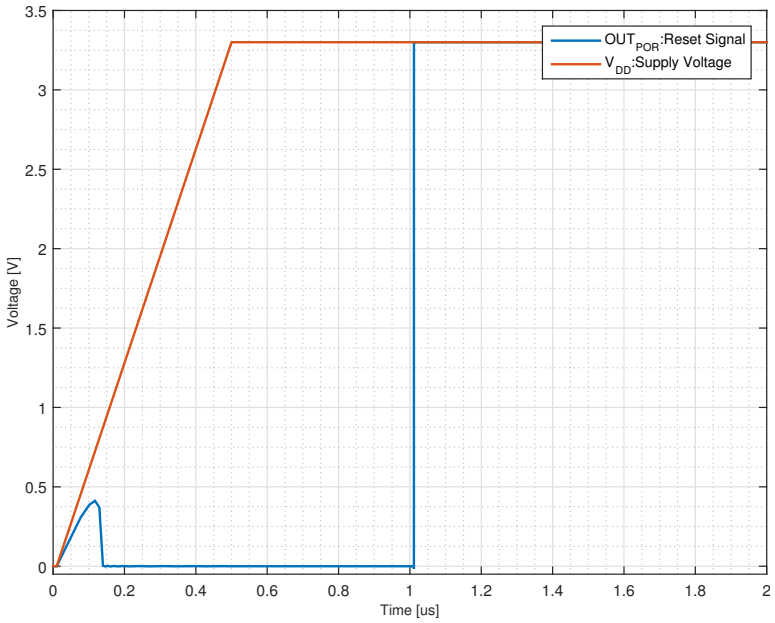

Figure 3.51 : Time domain analysis of power o reser circuit.

3.6 Top Level Simulations

Implemented output driver is simulated with resistive and inductive loads to examine the performance of circuit. Random data pattern is generated by verilog-A code and applied to the input of the driver. Figure 3.52 and 3.53 demonstrate the differential output signals at different data rates with resistive and transformer load configurations respectively. A value of resistive load is chosen as 8 Ω which cause a 1.6 V signal

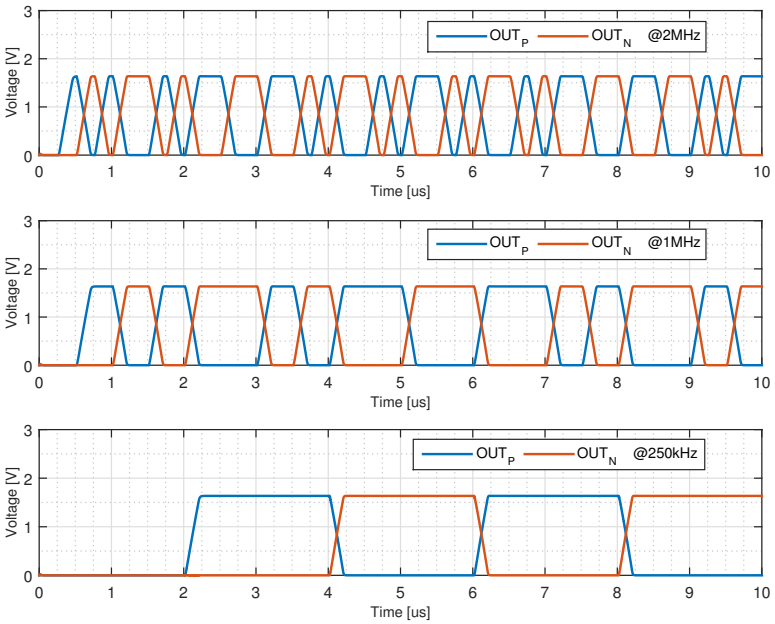

Figure 3.52 : Output signals in the resistive load configuration for different data rates.

amplitude at the output of the driver and a 1 nF capacitive load is connected parallel

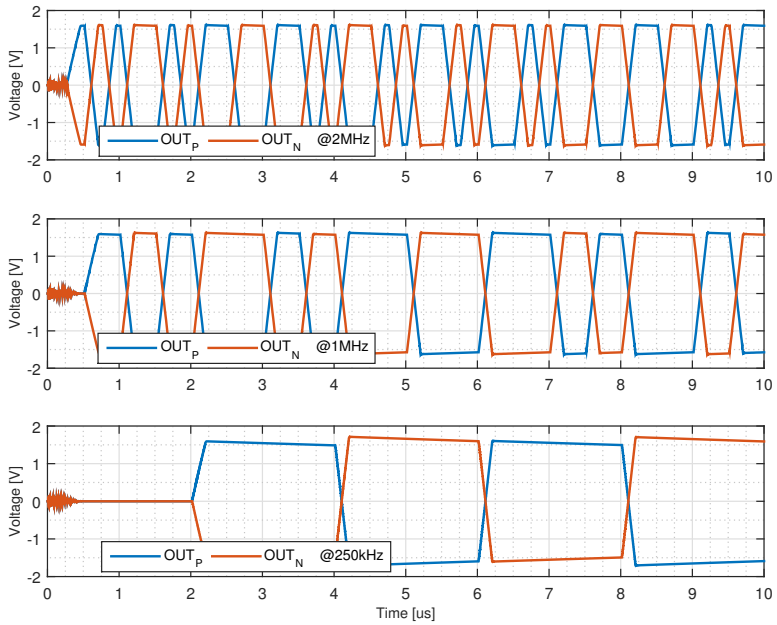

Figure 3.53 : Output signals in the transformer load configuration for different data rates.

to the resistive load. In the transformer load configuration, a transformer, which has a $1:2.5$, primary to secondary ratio, is used with a resistive load at the secondary. It is obvious that voltage amplitude at positive and negative branch will be twice of the value which is obtained in the resistive load configuration due to center-tapped transformer. If the positive signal level of positive branch or negative branch is adjusted to $1.6\,\mathrm{V}$, $6.4\,\mathrm{V_{p-p}}$ differential peak to peak signal will occur in the primary of the transformer. As the primary to secondary ratio is $1:2.5$, differential amplitude at the secondary equals to $16\,\mathrm{V_{p-p}}$ and the current at the secondary equals to $80\,\mathrm{mA}$. Therefore a value of load resistor at secondary must be $200\,\Omega$ to satisfy the desired voltage level at the primary.

3.6.1 Corner and mismatch analysis

It is obvious that output slew rate changes by PVT and mismatch effect due to variation in the delay time. Therefore corner and mismatch analysis is done due to examine output slew rate variations for a fixed load impedance. Slew rate of output signal is $7.96\,\mathrm{V/us}$ in the typical conditions for a load impedance which consists of $8\,\Omega$ resistor and $1\,\mathrm{nF}$ capacitor. Figure 3.54 demonstrates slew rate variations in different process corners and different monte carlo analysis.

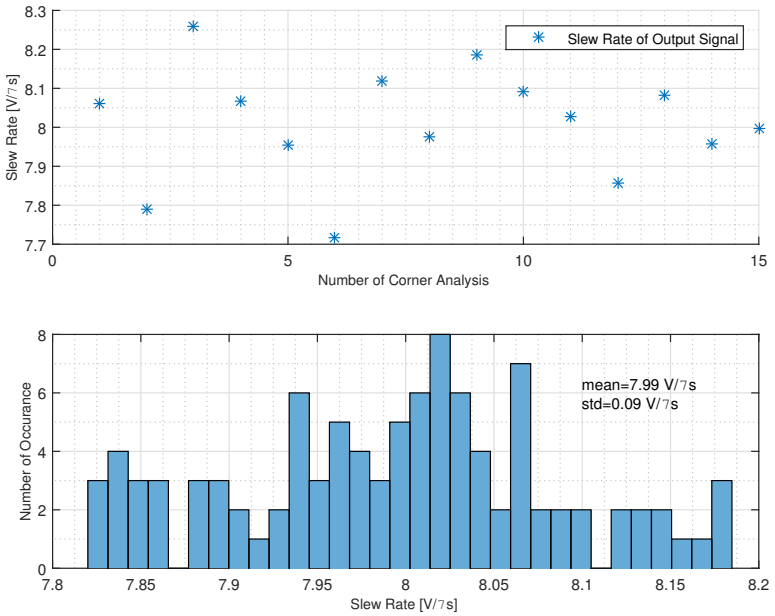

Figure 3.54 : Slew rate variations in different process corners and monte carlo analysis.

3.7 Post Layout Verification of Slew Rate Controlled Output Driver

Designed chip layout is given in Figure 3.55. As shown in Figure 3.55 output driver core covers the largest area in the in the layout due to high W/L ratios of output PMOS transistors. There are two independent driver in the circuit which has independent supply and ground lines and also different inputs and outputs. The reason for implementing two drivers is to satisfy the minimum area criteria which is determined by the foundry. During layout, several factors such as IR drop, matching factors, parasitic in the crucial nodes, e.t.c. are taken in account to obtain a proper layout design.

IR drop, is the voltage drop which occurs in the lines due to resistance of physical line in the layout. As the current flow on the line is determined precisely during the design of circuit, reducing resistance is the only way to minimize the IR drop. The IR drop in the analog supply line can be determined easily due to fact that the current flow is certain. However, current flow in the digital supply line may variates with time and it is at the maximum value during the transitions from logic high to logic low or vice-versa. Therefore, IR drop estimation must be done during the transitions. Supply lines and the output signal paths are implemented by using thick metal and metal paralleling options are used in order to reduce the parasitic resistance of the lines.

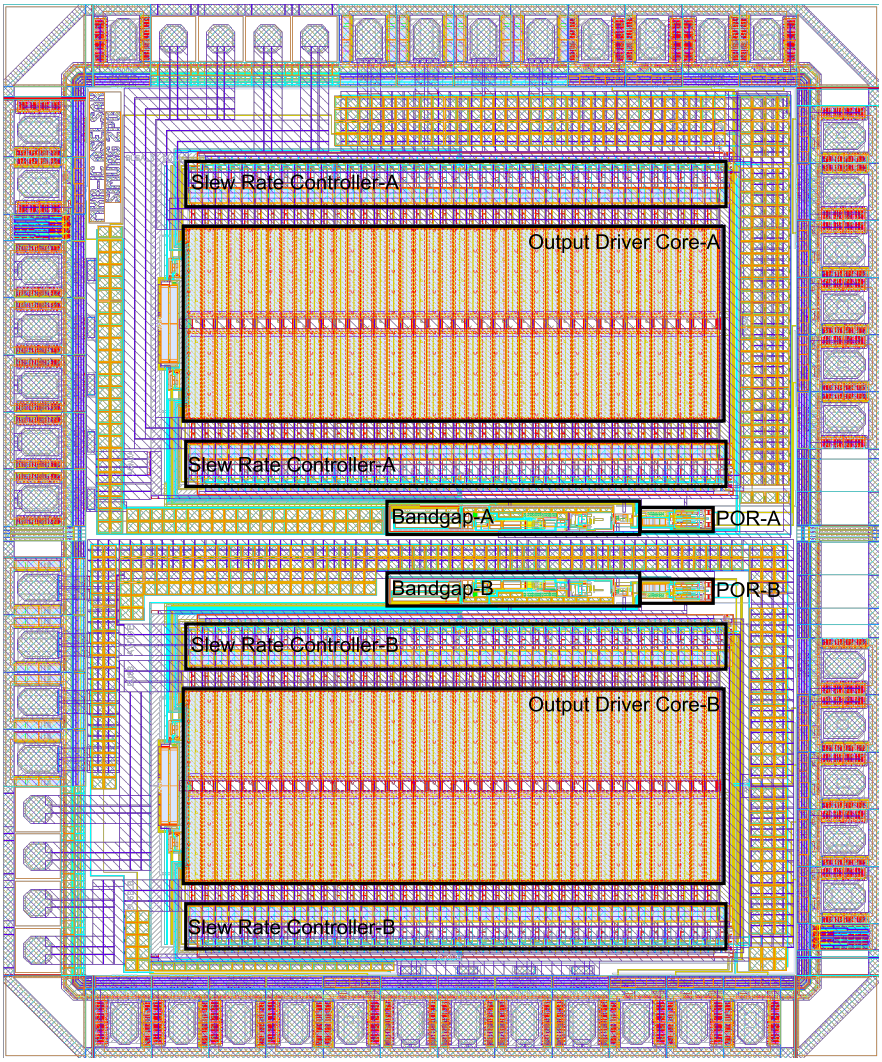

Figure 3.55 : Layout of designed circuit.

There are several design blocks which harms from mismatch effects. In the designed circuit, band-gap circuit and the bias circuit of the output driver core are the most sensitive part to mismatches. Therefore, certain layout techniques such as inter-digitizing, common centroid, dummy devices e.t.c. are used to reduce mismatch effect. For instance, resistor array in the band-gap circuit, which specifies the temperature coefficient of the band-gap voltage directly, are designed in inter-digitized architecture. Besides, dummy devices are used at the borders of array avoid mask misalignment and minimize effects of etching process.

After, the layout is drawn considering the effects mentioned above, physical extraction is done in order to examine effect of parasitic in the layout of the circuit. Simulation results are given in Figure 3.56, slew rate is obtained as approximately $7.92\,\mathrm{V}/\mu\mathrm{s}$ in the extracted simulations. Variation of the slew rate in different temperature is given in

Figure 3.57. Maximum and minimum slew rates are found as $8.217\,\mathrm{V}/\mu\mathrm{s}$ and $7.82\,\mathrm{V}/\mu\mathrm{s}$ respectively.

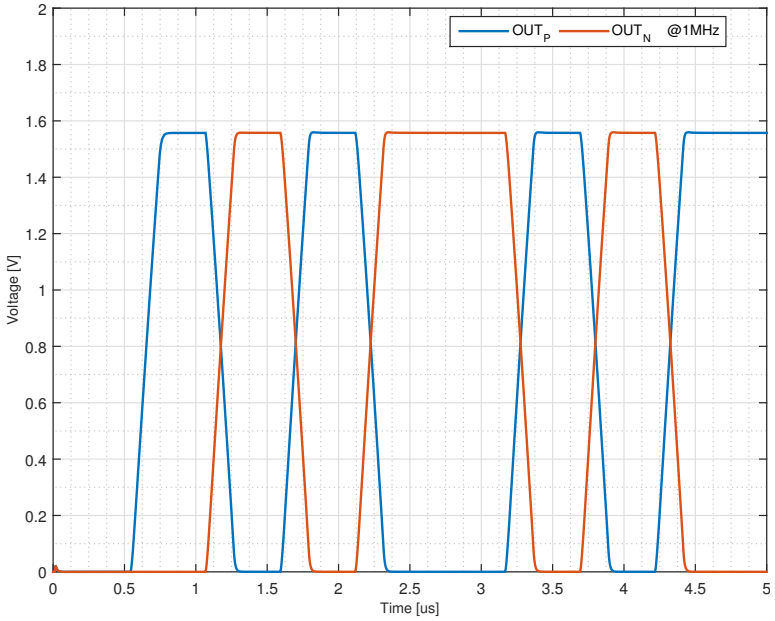

Figure 3.56 : Output signals of the physically extracted circuit.

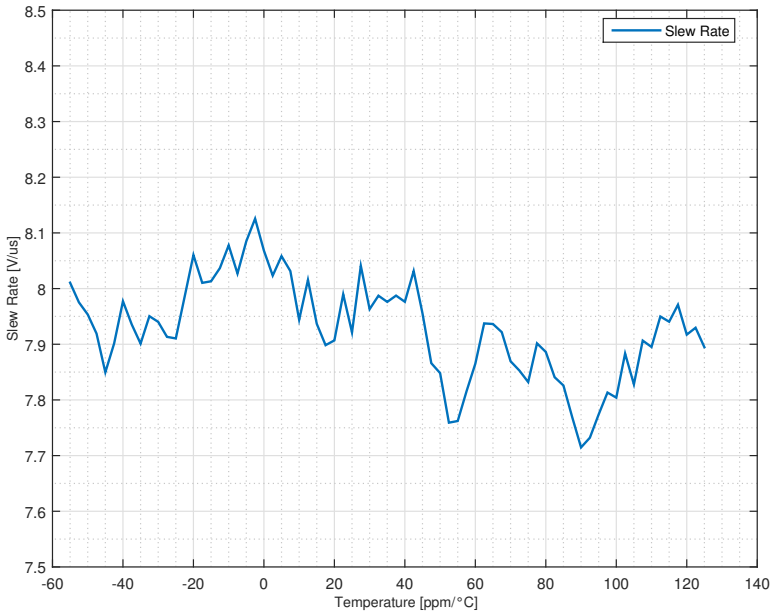

Figure 3.57 : Slew rate variations for different temperatures.

4. MEASUREMENT OF SLEW RATE CONTROLLED OUTPUT DRIVER

In this section, the measurements made so far and to be planned to done are presented. Measurement setup is explained in the first subsection and obtained results are given in the second section.

4.1 Measurement Setup

The die micrograph of the manufactured output driver is given in Figure 4.1. The

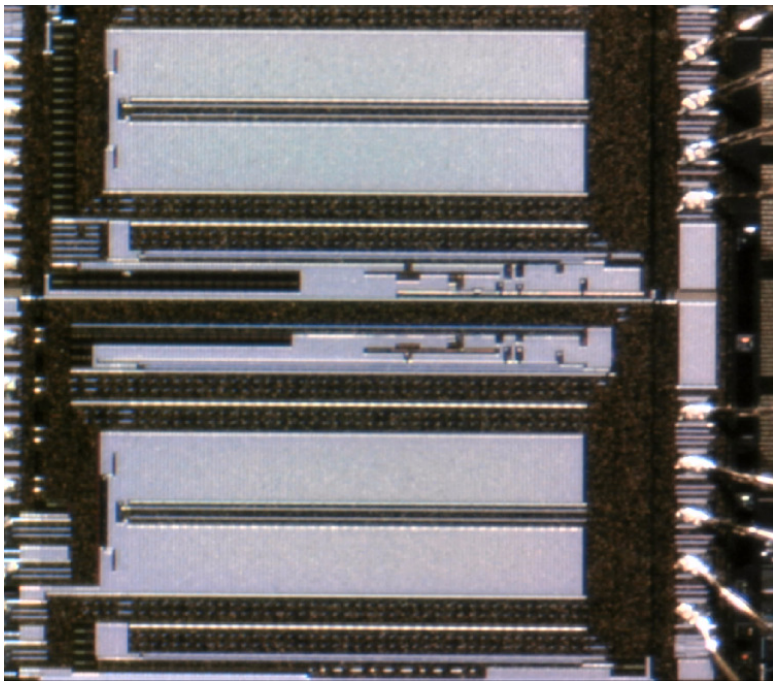

Figure 4.1 : Die micrograph of the manufactured circuit.

die area is $2x2.45\,\mathrm{mm}^2$ and the size of one driver core without pads is approximately $1.6x1.05\,\mathrm{mm}^2$. When the driver is operating, high current flow cause a large amount of consumed electrical energy which is transformed into heat. Heat dissipation may cause the integrated circuit to exceed the desired operating temperature limits. A plastic chip-scale package, QFN with a 44 pin is chosen for integrated circuit package. This package also includes a metal heat sink located at the bottom of package to minimize heat dissipation in the integrated circuit. The heat sink is soldered to the printed circuit board to obtain optimum thermal dissipation. Thermal resistance of the package is

45 °C/W. As the maximum current flow in the integrate circuit is 240 mA and the supply voltage is $3.3V$, approximate power dissipation is 0.8 W. Maximum junction temperature is taken as 125 °C in the simulation environment, so maximum ambient temperature can be find as follows

$$\begin{aligned} T_{AMB_{max}} &= T_{JUNC_{max}} - P_{dis}\theta_{JA} \\ &= 125 - 0.8x45 \\ &= 89°C \end{aligned} \tag{4.1}$$

where θ_{JA} is the thermal resistance of the package. Junction temperature may be defined above 125 °C to increase the maximum ambient temperature. However 125 °C is the maximum value where the device models provided from the foundry are still valid.

Wire wound resistors and carbon resistors are used at the output node because of the high power dissipation. As the footprints of these resistors cover larger area than the surface mount type resistors, the size of the designed test board have been $24x14\,cm^2$. Transformer and the resistive loads are used at the output of the load and a jumper is used to switch between these load types. Measurement setup is given in Figure 4.2. A FPGA is used to drive input of the output driver. Thus it has been possible to generate any data pattern for input signal. DC Power analyzer is used as power supply of circuit and an oscilloscope is used to collect output signals.

4.2 Measurement Results

First, output driver is used in the resistive load configuration and 16 Ω load is tied at the output nodes of driver to ensure that amplitude detection system is operating properly. The output voltage may reach the 3.2 V with the 16 Ω load due to fact that output current is 200 mA in the typical case. However, Figure 4.3 demonstrates that, output voltage level is limited to 3 V by an amplitude detection system. The voltage level at the output node is below its typical value 2.9 V, approximately 2.86 V. That's because the process variations and mismatches cause an decrease in the band-gap voltage level. The band-gap voltage level is measured as approximately 1.16 V by using up to 8-digit sensitive multimeter. Figure 4.4 demonstrates the zoomed output signal. After that, transformer load is tied to the output of the driver and slew rate control system of the driver is analyzed. 200 Ω resistive load is connected to the secondary of the transformer

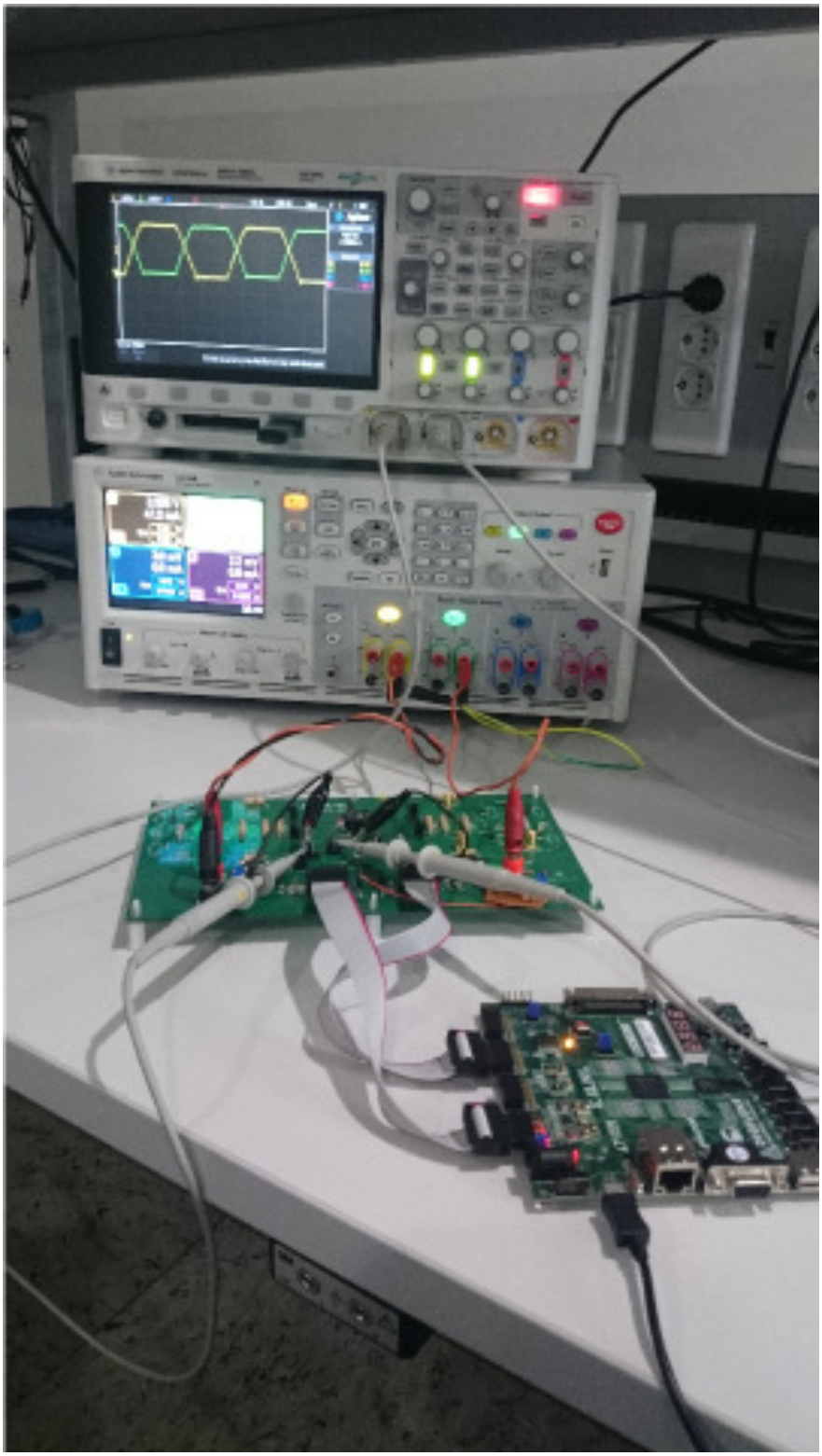

Figure 4.2 : Measurement setup of the output driver.

to create a 3.2 V amplitude at the output of the driver. The results are given in Figure 4.5. Output amplitude is approximately 2.94 V and the slew rate of the signal is about 15.6 $^{\mathrm{V}}/_{\mu\mathrm{s}}$ in the transformer load configuration. That shows that bias current of the driver is lower than desired value. Decrease is approximately 5 %, however, as the slew

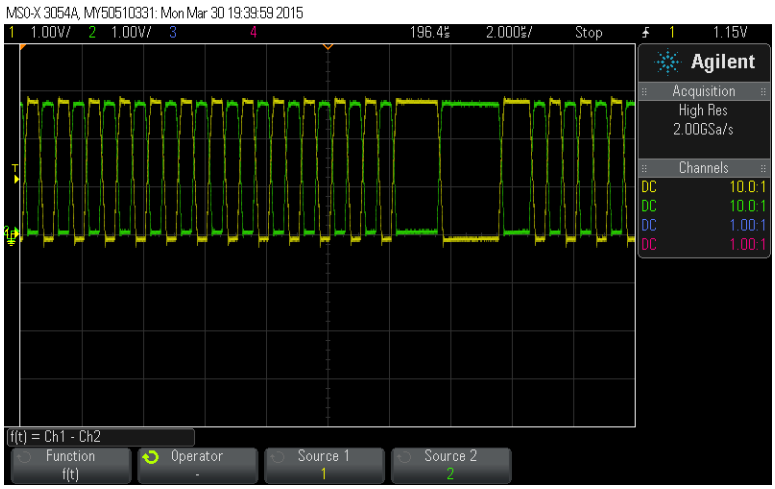

Figure 4.3 : Measurement results of the output driver in the resistive load configuration.

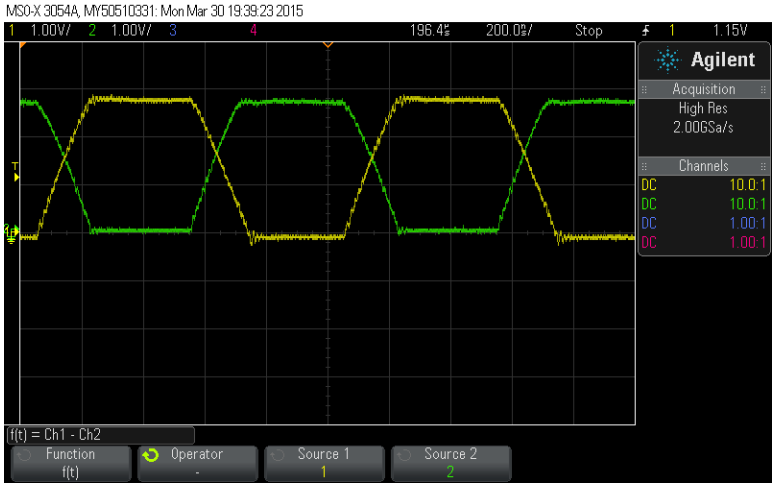

Figure 4.4 : Measurement results of the output driver in the resistive load configuration (zoomed version).

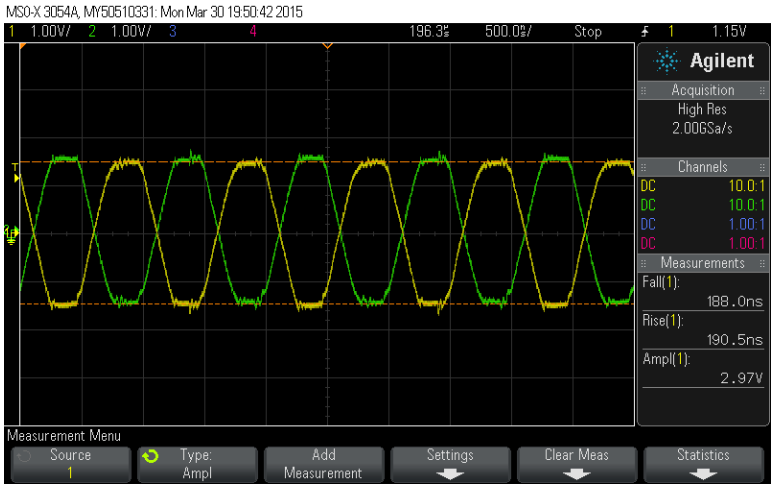

Figure 4.5 : Measurement results of the output driver in the transformer load configuration.

Table 4.1 : Comparison between simulation and measurement results.

	Typical Simulation Results	**Extracted Simulation Results**	**Measurement Results**
Slew Rate [$V/\mu s$] @16Ω Resistor Load	15.92	15.84	15.44
Slew Rate [$V/\mu s$] @Transformer Load	16.01	15.9	15.6
Amplitude Limit [V] @16Ω Resistor Load	2.9	2.88	2.86
Amplitude Limit [V] @Transformer Load	2.9	2.88	2.86
Power Consumption [mW] no transmitting	15.84	15.84	18.15
Power Consumption [mW] transmitting (except load)	48.84	48.84	55.11

time is determined by using the current which is complementary to the bias current of driver, the slew rate changes approximately 2.5 % from its typical case. Temperature variations of the slew rate circuit is given in Figure 4.6. As seen from the Figure 4.6

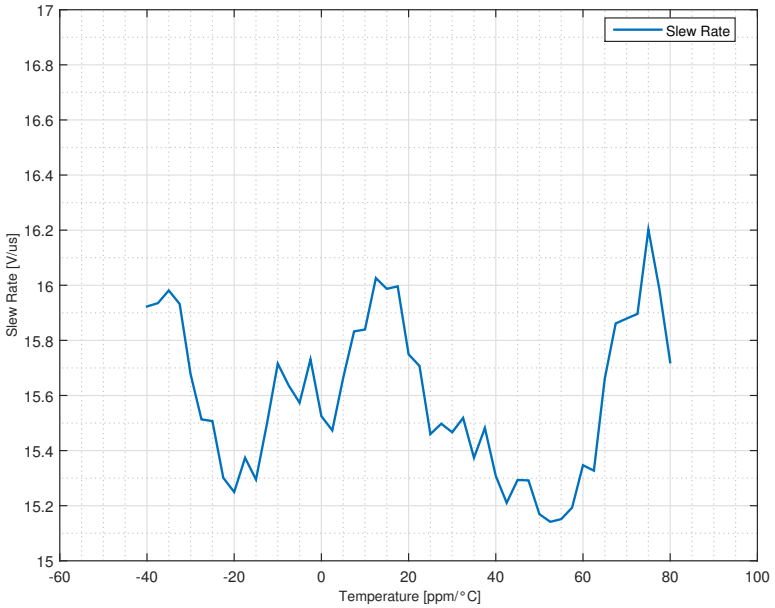

Figure 4.6 : Measurement results of slew rate variations over temperature.

variation over temperature is approximately 5 % which is quiet small enough to ignore. Table 4.1 summarizes the comparison between simulation and measurement results.

5. CONCLUSIONS AND RECOMMENDATIONS

In this thesis, a slew rate controlled output driver is implemented using XFAB 0.35 μm CMOS process with high voltage option. The design details and simulation results are given. Slew rate control is provided using digital control architecture which is based on delay cells. The driver is capable to drive resistive and inductive loads. A transformer which has a large primary inductance approximately 4.5 mH is used as inductive load. The voltage spikes are eliminated due to fact that current rate of the output driver well controlled.

Temperature compensation is added to the circuit in order to minimize slew rate variations over the temperature. Simulation results shows that slew rate change is approximately 3 % within temperature range between -55°C and 125°C. Measurements are done in the temperature range between -40°C and 80°C, because of the available lab equipment. The slew rate variations are analyzed and maximum change is determined as approximately 5 %.

As a follow up to this study, process detection circuit can be implemented to the slew rate control architecture. Process detection circuit defines the process corner and applies a compensation to the slew rate control architecture. As the slew rate control is implemented by delay cells, process detection circuit can be easily combined to the digital control architecture. Thus, output driver gives a better slew rate performance within process variations.

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APPENDICES

APPENDIX A.1: Schematics and Layouts

APPENDIX A.1

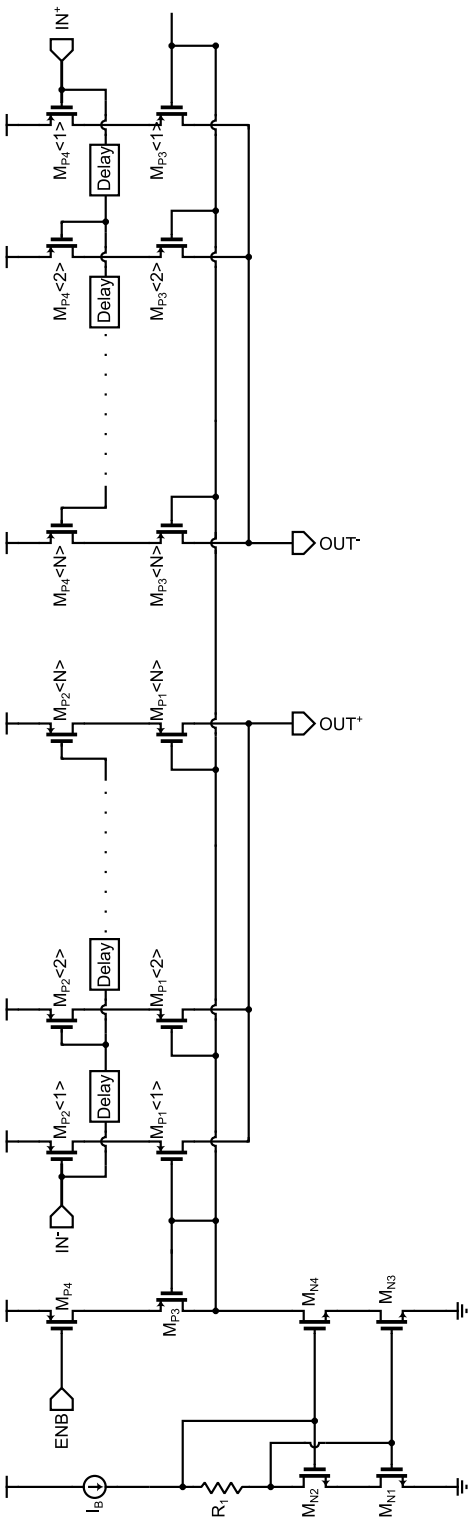

Figure A.1 : Schematic of Output Driver Core.

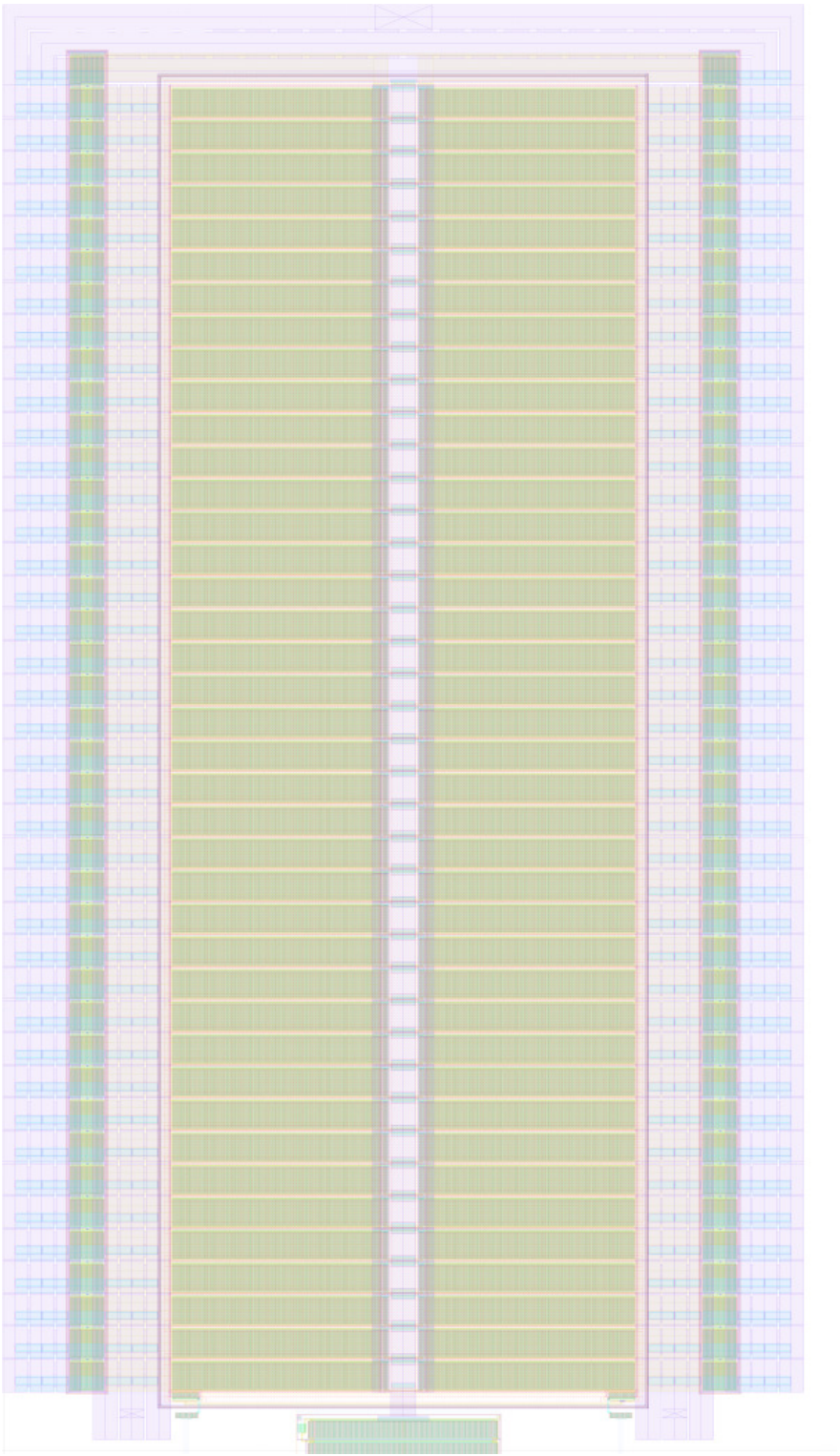

Figure A.2 : Layout of Output Driver Core.

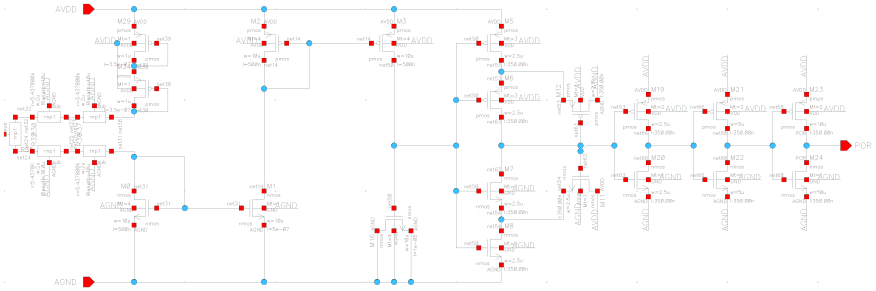

Figure A.3 : Schematic of Slew Rate Control System.

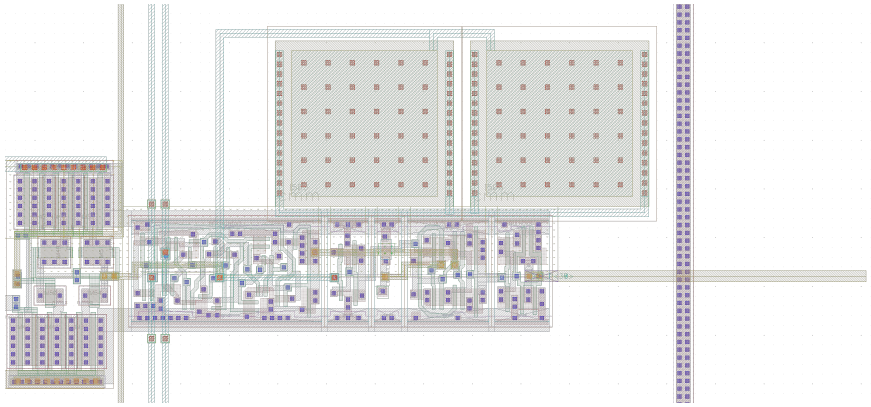

Figure A.4 : Layout of Slew Rate Control System (One cell of system).

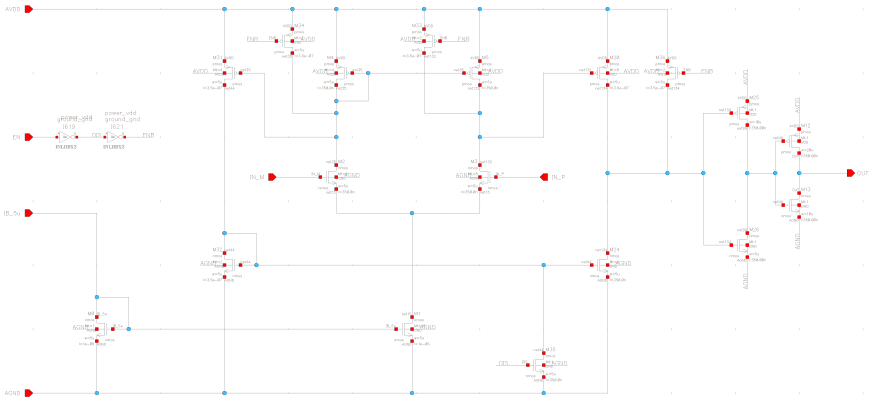

Figure A.5 : Schematic of Comparator.

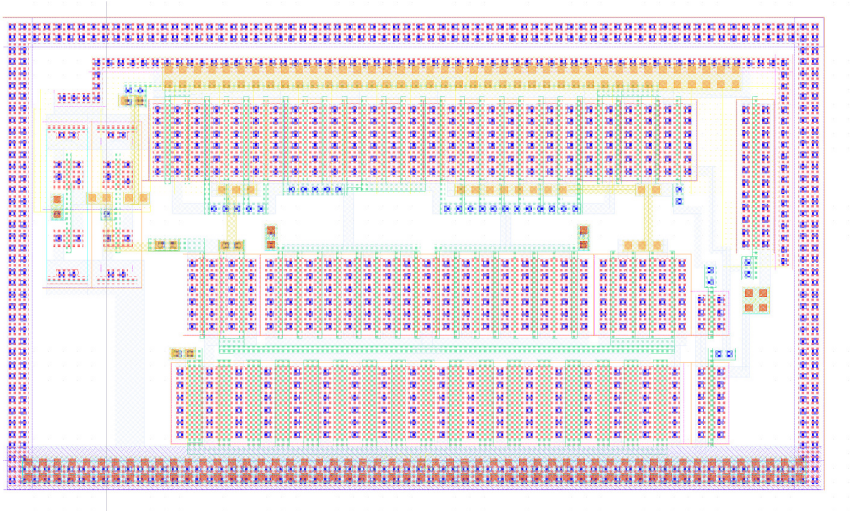

Figure A.6 : Layout of Comparator.

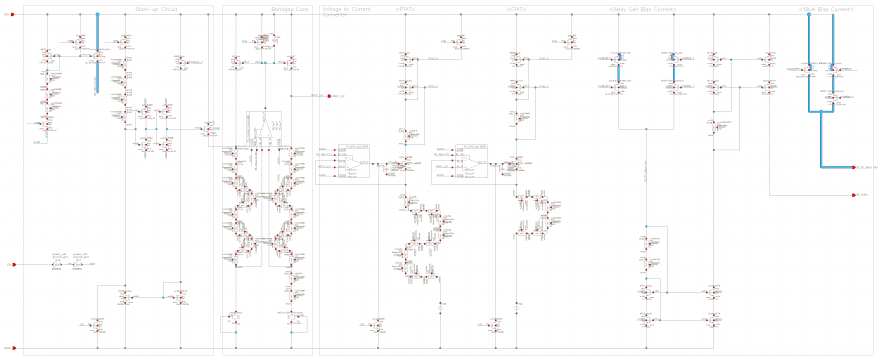

Figure A.7 : Schematic of Band-gap and Voltage to Current Converter.

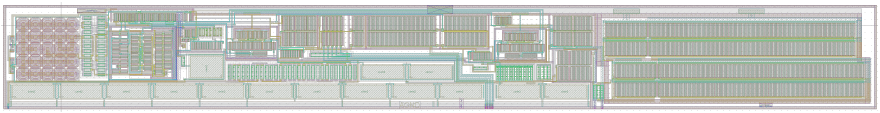

Figure A.8 : Layout of Band-gap and Voltage to Current Converter.

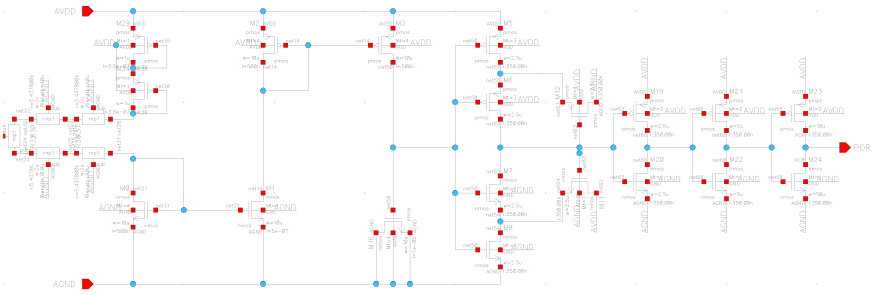

Figure A.9 : Schematic of Power on Reset Circuit.

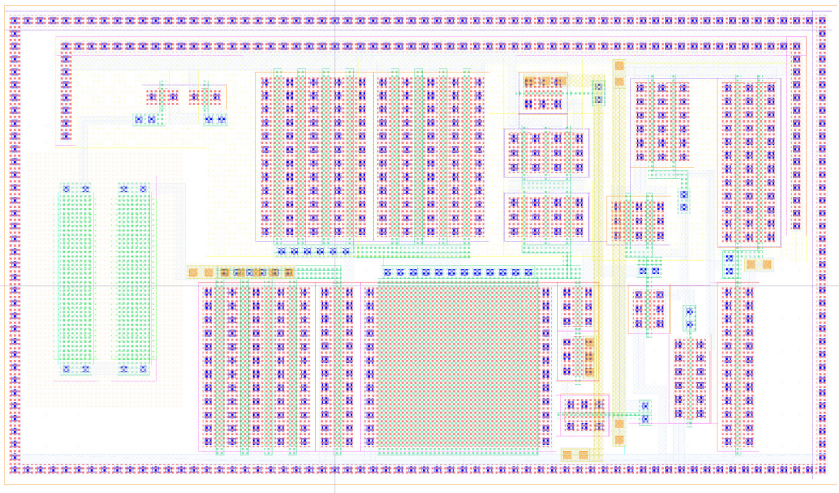

Figure A.10 : Layout of Power on Reset Circuit.

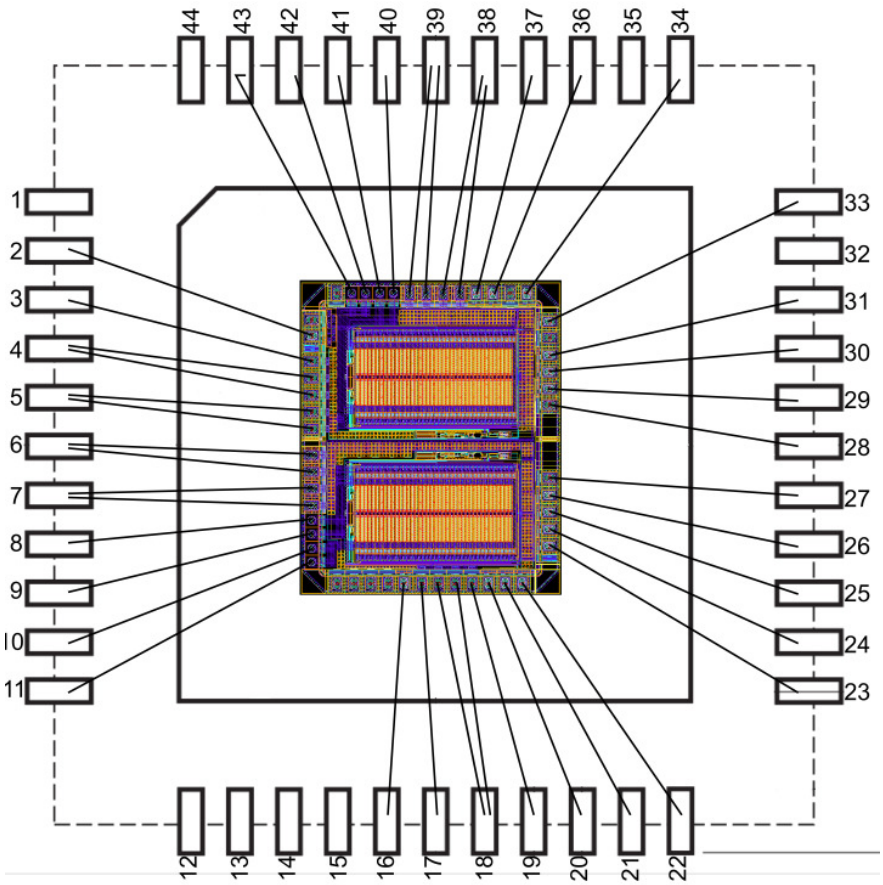

Figure A.11 : Bonding Diagram.

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