ENVELOPE TRACKING RF POWER AMPLIFIER DESIGN

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ABSTRACT

ENVELOPE TRACKING RF POWER AMPLIFIER DESIGN

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In modern wireless communication systems, the requirement of achieving high data rates results in non-constant envelope signals with high peak to average power ratio (PAPR). However, the operation of conventional power amplifiers (PAs) at back-off power levels creates significant degradation in efficiency. Since efficiency is a critical design consideration for PAs to avoid high power consumption and heating problems, several techniques were introduced to maintain the high efficiency for a wide range of power levels.

We designed an envelope tracking power amplifier (ETPA) that uses the supply modulation technique which is a promising solution to the efficiency degradation problem. In ETPA, the high efficiency is maintained at back-of levels by adjusting the supply voltage in accordance with the time varying signal envelope. The supply voltage was efficiently generated by using a synchronous buck converter operating at 10 MHz switching frequency. The converter was integrated to the designed class-AB PA by using a proper low pass filter. In order to improve the signal bandwidth that can be tracked, an envelope bandwidth elimination algorithm was used. The efficiency of the resulting ETPA system was measured as 26% for the signal that has 3 MHz bandwidth and 12 dB PAPR. The system has an efficiency of 20% with the signal that has 5 MHz bandwidth and 13 dB PAPR.

Keywords: Supply modulation, envelope tracking, power amplifier, back-off efficiency enhancement.

ÖZET

ZARF TAKİP METODU RADYO FREKANS GÜÇ YÜKSELTECİ TASARIMI

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Modern kablosuz iletişim sistemlerinde, yüksek veri hızlarına ulaşma gereksinimi sebebiyle yüksek tepe - ortalama güç oranına sahip değişken zarflı sinyaller kullanılır. Bununla birlikte, geleneksel güç yükselteçlerin maksimum güç seviyelerinin çok gerisinde çalışması, verimlilikte önemli bir bozulma yaratır. Verimlilik, yüksek güç tüketimi ve ısınma sorunlarından kaçınmak için kritik bir tasarım değerlendirmesi olduğundan, yüksek verimliliği geniş bir güç seviyesi aralığında korumak için çeşitli teknikler uygulanmaktadır.

Bu çalışmada düşük verimlilik sorununa çözüm olarak, bir besleme modülasyonu tekniği olan zarf takibi metodu güç yükseltecin tasarımı sunulmuştur. Besleme voltajı, zamana göre değişen sinyal zarfına göre ayarlanarak yüksek verimlilik maksimum güç seviyelerinin gerisinde de korunmuştur. Besleme voltajı, 10 MHz anahtarlama frekansında çalışan bir senkron buck dönüştürücü kullanılarak verimli bir şekilde üretilmiştir. Dönüştürücü, uygun bir alçak geçiş filtresi kullanılarak, AB-sınıfında tasarlanmış güç yükseltece entegre edilmiştir. Takip edilebilecek sinyal bant genişliğini artırmak amacıyla bir zarf bant genişliği eleme algoritması kullanılmıştır. Tasarlanan sistemin verimliliği, 3 MHz bant genişliği ve 12 dB tepe - ortalama güç oranına sahip sinyal için %26 olarak ölçülmüştür. 5 MHz bant genişliği ve 13 dB tepe - ortalama güç oranına sahip sinyal için sistem, %20'lik bir verimle çalışmaktadır.

Anahtar sözcükler: Besleme modülasyonu, zarf takibi, güç yükselteci, düşük-güç verimi artırma.

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In the memory of my father...

Chapter 1

Introduction

1.1 Motivation

RF power amplifiers are widely used devices in wireless communication systems and radars to deliver RF power to the antennas. Since they are highly energy dissipating devices, the power amplifiers have significant roles in the overall transmitter efficiency. To minimize the energy consumption, improve the battery life of the portable devices and avoid heating problems, efficiency is an important design consideration.

Early wireless systems such as Advanced Mobile Phone Systems and Global System for Mobile used constant envelope modulation techniques in which the information is carried on the phase and frequency [1]. In these systems, the RFPAs are designed to operate in their most efficient mode, since the linearity is not the main concern.

With the development of communication technologies, the number of the wireless communication devices and the quantity of data increased dramatically. Since the frequency spectrum allocated for the wireless systems essentially remained the same, efficiently usage of the spectrum became more important. Therefore, more

complex modulation techniques were developed to obtain high data rates for the available and expensive bandwidths. Some features of modern mobile communication standards are displayed in Table 1.1 [2].

Table 1.1: Features of Modern Communication Standards

Gen	**Standard**	**Interface and Modulation**	**Max. Frequency (GHz)**	**Bandwidth (MHz)**	**Max. Bit-Rate (Mbit/s)**	**Max. PAPR (dB)**
2G	GSM/EDGE	TDMA/FDMA, GMSK , 8PSK	1.9	0.2	<1	3.3
3G	UMTS	W-CDMA, QPSK/64QAM	3	5	100	10.6
4G	LTE	OFDMA, MIMO 4x4, 64QAM	5.9	20	300	12
4G	LTE-Advanced	OFDMA/SC-FDMA, MIMO 8x8, CA, 64QAM	5.9	20 (100 with CA)	>300	12
4G	WiMAX	OFDMA, MIMO 2x2, QPSK/64QAM	5.8	20	100	12
5G	5G	OFDMA, HetNet, massive MIMO, advanced CA, CoMP, . . .	40	>100 (800-2000)	>800	>12

The non-constant envelope modulation techniques such as QPSK, W-CDMA and OFDM are very popular in modern wireless systems to use the spectrum more efficiently [3]. For these non-constant envelope signals, the peak to average power ratio (PAPR) is a measure of how different signal amplitude levels the signal contains. High data rates can be achieved by using high PAPR signals. In these systems, both linearity and efficiency need to be satisfied for a wide range of power levels. However, the conventional classes of PAs are designed to operate efficiently for the nearly saturated power levels. The efficiency reduces at the back off power levels because full rail to rail voltage swing is not maintained.

The existing solutions to the efficiency degradation includes load modulation and supply modulation techniques which are based on dynamical adjustment of the load line. Outphasing amplifiers [4–6], Doherty amplifiers [7–9] and load modulated balanced amplifiers [10, 11] are the examples of the load modulation techniques. On the other hand, supply modulation techniques include envelope elimination and restoration (EER) [12,13] and envelope tracking power amplifiers (ETPA) [14, 15].

In this study, the aim is to design an envelope tracking power amplifier that can be operated efficiently under the high PAPR signals used by the modern wireless communication technologies. The high efficiency will be maintained for a wide range of power levels by enhancing the back-off efficiency. The design will be fabricated and verified for auxiliary LTE signals.

1.2 Thesis Outline

Chapter 2 explains the basics of RF power amplifiers and back-off efficiency enhancement techniques. Envelope tracking concept and the literature review are presented.

In Chapter 3, a detailed explanation of the envelope amplifier is given. Starting from the important parameters of a power MOSFET, design of the converter and the output filter are explained. In Chapter 4, the design steps of the RF power amplifier and the constant supply measurement results are presented.

Chapter 5 presents the slow tracking concept. The envelope bandwidth elimination algorithm that is applied to the system is explained. In this chapter, the supply signal is generated by mapping RF input power levels to proper supply voltages.

In Chapter 6, the efficiency and linearity performances of the fabricated envelope tracking power amplifier are measured by using AM and LTE signals. The results are compared to the constant supply systems. Lastly, Chapter 7 includes the conclusion of the thesis.

Chapter 2

Background

2.1 RF Power Amplifier Basics

In an RF transmitter signal chain, RF power amplifier is the device that drives the antenna by boosting the power of the RF signal to the level necessary for the design. Since it has a key role in the RF transmitter performance, there are strong requirements of an RFPA such as output power, linearity, energy efficiency and cost.

The efficiency of the RFPA is the measure of its ability to convert the DC power to RF signal power delivered to the antenna. Because of the limited efficiency of RFPAs, only some of the DC power can be converted to RF power. The DC power that is not converted to RF signal power is dissipated as heat. Since RFPAs are generally most energy consuming components of the transmitter, efficiency is a critical design consideration for the devices such as portable devices and satellites that have limited power sources. Due to the cooling problems, the efficiency is also important for the systems in which the power consumption is not the main issue.

For an ideal linear amplifier, the output power increases linearly with the increasing input power. However, gain of a real power amplifier does not stay constant for all power levels. The nonlinearity behavior changes the signal characteristics and creates distortion on the signal. For the modulation techniques in which the information is carried on the frequency or the phase, the input RF signal has a constant envelope. In this case, linear amplitude transmission is not required, hence the linearity is not the main issue. On the other hand, the RF envelope is non-constant for the more adaptive modulation techniques that allow higher data rates. OFDM, QPSK and QAM are the examples of the non-constant envelope modulations, and they require linear amplitude transmission. Therefore, linearity of the RFPA is critical for these modulation techniques.

In order to achieve different specifications, RFPAs are designed with different modes of operation called classes. Class-A, class-AB and class-B are called linear mode amplifiers that use the transistor as a voltage controlled source. In linear mode amplifiers, the class is determined by the bias condition applied to the transistor. The bias condition controls the conduction angle which is defined as the duration of the period in which the transistor is conducting.

In addition to the linear amplifier classes, the other mode of operation is called switching-mode classes. In switching mode classes such as class D, class E and class F, the transistor is overdriven and operates as a switch instead of a current source. Using these classes, higher efficiencies can be obtained for narrowband operations with a high nonlinearity.

The conventional classes cannot provide high efficiency and good linearity at the same time. In order to have good linearity, the amplifier can be operated with small input power levels. However, the efficiency drops significantly at back-off power levels. On the other hand, the amplifier is efficient but nonlinear at the power levels near saturation.

2.2 Back-Off Efficiency Enhancement Techniques

In modern wireless communication systems, non-constant envelope modulation techniques such as QPSK, W-CDMA and OFDM are widely used to increase the spectrum efficiency. In these modulation techniques, signals designed for high data rates result in high peak-to-average power ratio (PAPR) waveforms.

However, the conventional RF power amplifiers are designed to operate efficiently at the power levels near compression, and the high efficiency is not maintained for back-off power levels. The drain efficiency of a PA can be written in terms of the load impedance R_L, the fundamental frequency current I_{ds} and DC voltage and current components V_{DS} and I_{DS}, as given in Eqn. 2.1. Since I_{DS} and I_{ds} change in proportional to the drive power level, the efficiency at the low drive levels is degraded. The overall efficiency drops in the case of non-constant RF envelope with high PAPR because of the inefficient operation at the back-off levels.

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{R_{load} I_{ds}^2}{2 V_{DS} I_{DS}} \tag{2.1}$$

In order to maintain the high efficiency at a large range of power levels, different methods have been implemented. The two popular methods to enhance the back-off efficiency are load modulation and supply modulation that are based on dynamical adjustment of the load line.

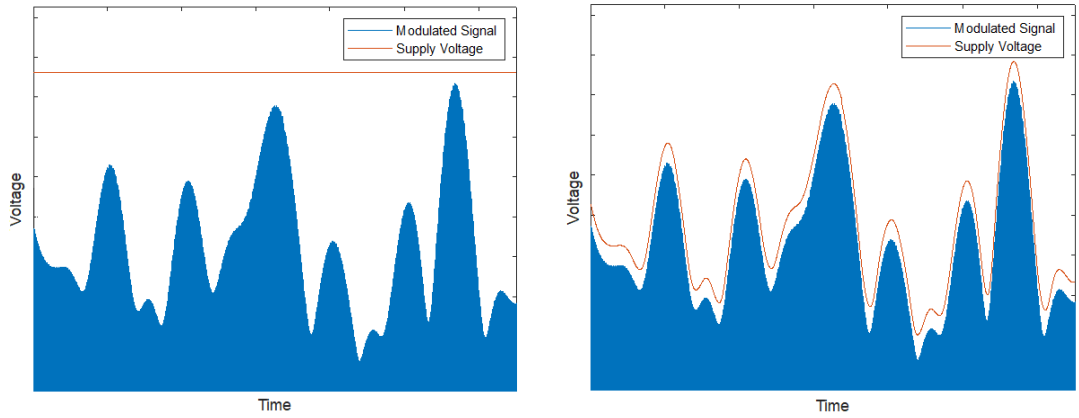
In load modulation methods, the load impedance is adjusted inversely proportional to the drive level. Thus, the high efficiency is maintained for different drive levels. Doherty PA, varactor based load modulation, chireix outphasing and load modulated balanced amplifiers are the popular examples of dynamic load modulation.

In dynamic supply modulation, the high efficiency is achieved by adjusting

the V_{DS} in proportional to the drive level. Envelope elimination and restoration (EER) and envelope tracking (ET) are the examples of dynamic supply modulation techniques.

2.3 Envelope Tracking Power Amplifier Systems

Envelope tracking is one of the dynamical supply modulation methods to enhance the back-off efficiency. The envelope tracking theory suggests that full rail-to-rail voltage swing in the power amplifier can be maintained by adjusting the supply voltage in accordance with the time varying signal envelope. In this case, the PA is kept near compression for different RF power levels. Thus, the overhead voltage is kept minimum and the maximum efficiency is maintained. Figure 2.1 illustrates the overhead voltages during the amplification of a non-constant envelope signal for constant supply voltage and ET system.



(a) Constant Supply Voltage (b) Envelope Tracking

Figure 2.1: Overhead Voltages in Constant Supply and Envelope Tracking Systems

In an ET RFPA, the supply voltage dynamically tracks the time varying RF envelope using an envelope amplifier. The basic configuration of the ET RFPA is shown in Figure 2.2. The configuration contains an RFPA, an envelope amplifier

and an output stage low pass filter. In contrast to the EER, the RF signal carries all the phase and amplitude information in an ET system. Therefore, envelope tracking operation operates independently from the RF signal.

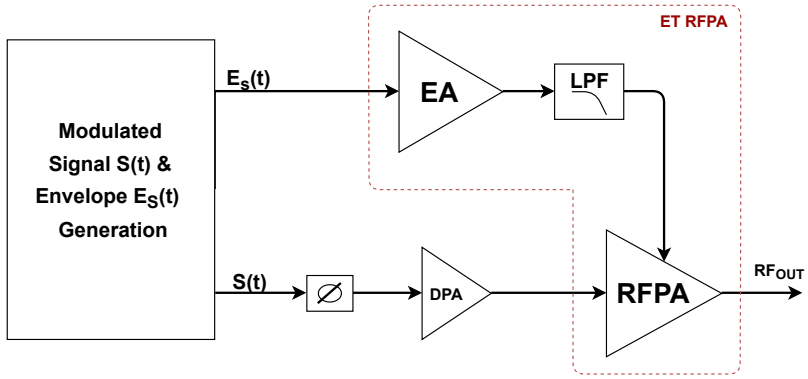


Figure 2.2: Envelope Tracking RFPA System

The envelope amplifier is a controllable voltage converter that has strong requirements such as high slew rate, high efficiency and high accuracy. High slew rate is an important parameter showing how fast the supply modulator can track the RF signal envelope. The bandwidth of the envelope would be higher than the modulated signal bandwidth [16]. Therefore, the supply modulator needs to be able to generate high power voltage supply that has a high bandwidth. In order to get a high bandwidth, high switching frequency is required. However, high switching operation leads to a significant drop in the converter efficiency because of switching losses at every cycle [17]. Therefore, a good compromise needs to be found considering all of these parameters.

The output stage filter in this configuration passes the all envelope bandwidth to the RFPA while eliminating the switching frequencies of the envelope amplifier. A flat response in the pass band is necessary to avoid distortion on the envelope signal. Additionally, the filter may need to satisfy the impedance requirements of the RFPA drain.

The RFPA should be designed to work with a range of supply voltages. Therefore, it needs to be designed and tested to be operated with different supply voltages. Since the nonlinear impedances at the fundamental and harmonics depend on the supply voltage, specific mode of operations are not generally preferred such as Class E or Class F [3]. The maximum efficiency values of the RFPA under different supply voltages constitute an upper bound to the maximum overall efficiency of the system. Therefore, the peak obtainable efficiency of the PA is important for the overall efficiency.

2.4 Literature Research

Envelope tracking theory has its origin in a closely related technique, envelope elimination and restoration (EER), that was introduced by Leonard R. Kahn [18]. In Kahn's technique, the power amplifier is driven by a constant envelope signal while the amplitude modulation is imposed by a dynamical voltage supply. With the extensive studies on the usage of dynamic voltage supply, early examples of ET technique were introduced in [19] and [20].

The need for back-off efficiency enhancement in the modern wireless communication systems, increased the interest in ET technique. In [21] and [22], significant efficiency improvement of ET technique was reported. On the other hand, wide bandwidth in the modern communication systems brought the requirements of high envelope amplifier bandwidth and high switching frequencies. In order to satisfy the bandwidth requirements without sacrificing much power, hybrid envelope amplifiers are used in [23] and [24]. In hybrid amplifiers, high frequency components of the envelope are amplified by a low efficiency linear amplifier. Since most of the power in the envelope resides at the low frequencies, the overall efficiency is not expected to drop dramatically.

Envelope bandwidth elimination is another method to track the signals that have high bandwidth. Using this method, a slew rate limited version of the envelope is tracked. In [25], the performance of a reduced bandwidth envelope

tracking amplifier is reported.

Due to their efficiency advantages, GaN transistors are widely used in power switching applications. In [26–28], switching frequencies above 100 MHz are achieved efficiently by using GaN transistors in integrated designs. As an alternative method, the discrete level envelope amplifier that is demonstrated in [29], has digitally controlled eight voltage levels.

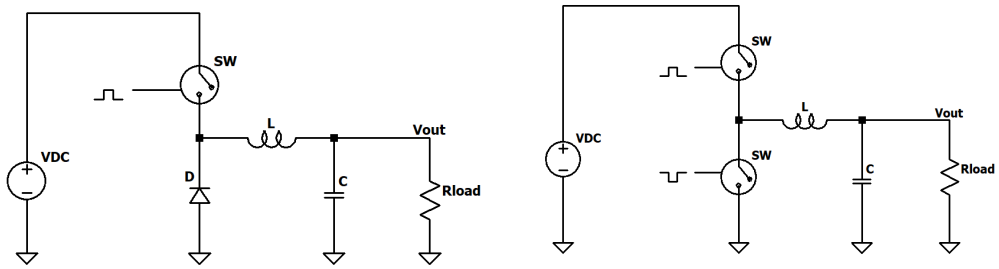
Chapter 3

Design of the Envelope Amplifier

3.1 Fundamentals of Power MOSFETs and Buck Converters

As a conventional and useful method, a buck converter can be used as the supply modulator. A buck converter is a switching voltage step-down converter. The basic buck converter topology is given in Fig. 3.1. The topology consists of an active switching device, a diode and the output filter. The circuit supplies a continuous current to the load using the energy stored at the inductor during the on time of the switch. During the on time, the inductor current passing through the switch increases due to the voltage supply. When the switch is turned off, the inductor current continues to flow through the diode decreasingly. Using a synchronous control, the diode can be replaced by another switching device in order to avoid the power dissipation of the diode. The synchronous converter topology is given in Fig. 3.1.

Since a voltage controlled switching device is easier to control, MOSFETs are generally used in high power and high speed switching converters. In a basic n-type MOSFET, if a voltage higher than the threshold is applied between the gate and the source, electrons entering the n-channel establish a conducting channel



(a) Buck Converter (b) Synchronous Buck Converter

Figure 3.1: Buck Converter Topologies

between the source and the drain. Voltage and current ratings, on state resistance ($R_{ds(on)}$), parasitic capacitances and packaging inductances are the fundamental parameters that determine the converter performance.

The voltage and current ratings state the maximum drain to source voltage and the continuous drain to source current that the transistor can work with. The substrate properties and the dimensions of the transistor determine the voltage and current ratings.

The drain to source resistance at the on-state of the transistor ($R_{ds(on)}$) is another important parameter for switching applications since it contributes directly to conduction losses. The N- epitaxial layer thickness and the doping level constitutes a tradeoff between the breakdown voltage and the on state resistance. The high breakdown voltage is obtained with a thick layer and lower doping level. However, a thin layer and high doping level are required for low resistance.

The parasitic capacitances of the transistor are the parameters that limit the speed of the converter. Because of the parasitic capacitances, the transistor cannot turn on and off immediately. A real MOSFET transistor inherently has a gate-source capacitance (C_{gs}), a gate-drain capacitance (C_{gd}) and a drain-source capacitance (C_{ds}) as shown in Fig. 3.2.

The input capacitance (C_{iss}) is defined as the sum of the gate-source capacitance (C_{gs}) and the gate-drain capacitance (C_{gd}). In order to turn on or off a transistor, the input capacitance needs to be driven. The total gate charge (Q_g)

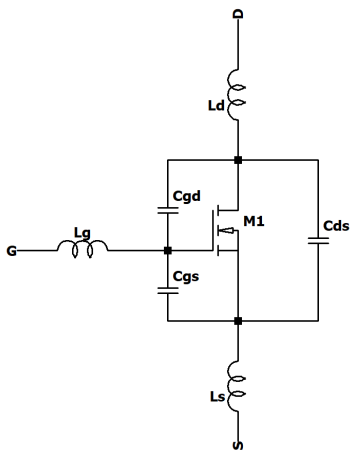
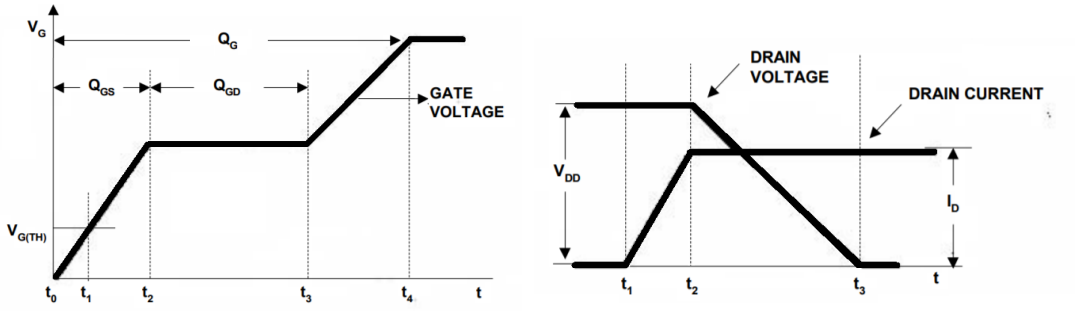


Figure 3.2: Parasitic Elements of a MOSFET

is the amount of charge necessary to open the transistor. Since the gate charge includes the required drive voltage information together with the gate capacitance, comparing the gate charge instead of the capacitances can give a better perspective to select a device. The driver losses arise from the requirement of supplying the gate charge at every cycle. Also, the time it takes to supply this charge, determines the switching speed of the transistor and has a significant impact on the switching losses.

The voltage and current waveforms during the turn on time are displayed in Fig. 3.3. When the transistor is turned on, gate capacitances begin to charge. After the gate to source threshold voltage is exceeded, a highly resistive channel is established between the drain and the source. The resistance reduces down to $R_{ds(on)}$ when the final gate drive voltage is reached. Similarly, when the transistor is turning off, gate voltage cannot drop to zero immediately. The drain to source channel stays resistive while the gate capacitances discharge. The voltage and current overlap in the resistive channel during these periods yields power dissipation at every cycle and decreases the efficiency.

Therefore, the parasitic capacitances are directly related to the efficiency performance in high frequency operations. However, there is another trade off between the parasitic capacitances and the on-state resistance. The larger active



(a) Gate Voltage (b) Drain Voltage and Current

Figure 3.3: Voltage and Current Waveforms During Turn On

area of the transistor decreases the on state resistance while increasing the parasitic capacitances.

Packaging and PCB inductances are also important at high frequency operations. The high inductance at the gate of the transistor significantly slows down the charging and discharging periods [30]. Thus, the switching loses are also affected by the packaging and PCB inductances.

$$P_{loss} = P_{switching} + P_{conduction} + P_{driver} + P_{other} \tag{3.1}$$

The total loss of the converter is obtained by adding the main causes of losses that are switching loss ($P_{switching}$) due to the $I - V$ overlap, conduction loss ($P_{conduction}$) due to the resistive components and gate drive loss (P_{driver}). The term, P_{other}, represents the all other losses arising from other causes such as dead time, reverse recovery charge of the body diode and parasitic inductances.

The switching loss of a synchronous buck converter can be approximated as

$$P_{switching} = V_{DD} I_{rms} (t_{on} + t_{off}) f_{sw} \tag{3.2}$$

where V_{DD} is the supply voltage, $Irms$ is the rms current on the inductor, f_{sw} is the switching frequency, and t_{on} and t_{off} are turn on and off delays. The rms current, that is higher than the output current, depends on the inductor value

and the waveform of the signal that is tracked. t_{on} and t_{off} are calculated by using the equations 3.3 and 3.4 where I_{source} and I_{sink} are the drive currents of the driver.

$$t_{on} = Q_g / I_{source} \tag{3.3}$$

$$t_{off} = Q_g / I_{sink} \tag{3.4}$$

$P_{conduction}$, that is mainly caused by the on-state resistance of the switching device and the DC resistance of the inductor, is calculated as in Eqn. 3.5. The term, R_{cond}, is the total resistance.

$$P_{conduction} = I_{rms}^2 R_{cond} \tag{3.5}$$

Lastly, $\mathrm{P_{drive}}$ is the loss of the driver circuit to supply the gate charge at every cycle. The calculation of $\mathrm{P_{drive}}$ is given in Eqn. 3.6.

$$P_{driver} = Q_g V_{GS} f_{sw} \tag{3.6}$$

3.2 Synchronous Buck Converter Design

In this ET RFPA design, a synchronous buck converter was used as the supply modulator. The selection of the switching devices has a key role in efficiency and speed of the converter. In past a few years, GaN technology has become very popular in power switching devices with its significant advantages. Comparing with the conventional silicon devices, GaN transistors with the same performance are much smaller. They have lower $R_{ds(on)}$ and lower gate charge yielding less switching losses. Several switching transistors are given in the Table 3.1. EPC8009 transistor was selected due to its dramatically low gate charge by comparing to

other similar devices. EPC8009 is an enhancement mode e-GaN type MOSFET that is controlled by 5 V V_{gs} control signal.

Table 3.1: High Power Switching Transistors

	EPC8009 (GaN)	EPC2007C (GaN)	BSP320S (Si)	SUD15N06-90L (Si)
Max V_{DS}(V)	65	100	60	60
$R_{ds(on)}$(mΩ)	130	24	120	90
Qg(nC)	0.37	1.6	9.7	12
Qgs(nC)	0.12	0.6	1	2
Qgd(nC)	0.055	0.3	4.7	3.5
Ciss(pF)	45	170	275	524
Coss(pF)	19	110	90	98

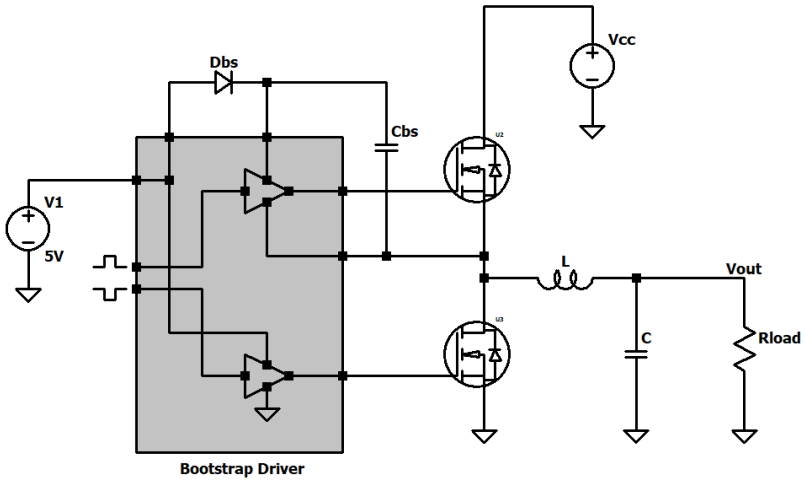


Figure 3.4: Bootstrap Topology

The bootstrap circuit is given in the Fig. 3.4. When the low side is on, the bootstrap diode turns on and charges the bootstrap capacitor to 5 V. When the high side transistor is turned on, the voltage of the switching node rises up to V_{DC}. The bootstrap capacitor keeps the voltage difference of 5 V, the diode turns off and the drive voltage increases the up to V_{DC}+5 V. The required gate charge of the high side transistor is supplied by the proper bootstrap capacitor for a while. However, because of the quiescent current of the driver, the high side drive voltage cannot keep its value permanently. The capacitor value needs to be carefully selected by considering the gate charge and on period of the high

side transistor. In addition to that, the bootstrap diode should turn on and off very fast in order to allow high speed bootstrap operation. Therefore, a schottky barrier diode with small capacitances was used in the driver.

For high frequency switching, another important parameter is the drive current capabilities of the driver. Since the required charge in the gate capacitances is supplied by the driver, the delays for turn on and off are inversely proportional to the drive currents. Source current is the ability of the driver to supply current to the gate capacitances. On the other hand, the sink current shows the ability of the driver to receive current to discharge the gate capacitances.

The minimum required bootstrap capacitor is calculated in Eq. 3.7 where Q_{rr} is the reverse recovery charge of the bootstrap diode, Q_g is the gate charge of the high side transistor, I_{HBS} is the leakage current during on time period, t_{on} is the maximum on time of the high side transistor, I_{HB} is the quiescent current of the high-side driver and ΔV is the maximum allowed drop on the high side drive voltage.

$$C_b = (Q_{rr} + Q_g + I_{HBS}t_{on} + I_{HB}/f_{sw})/\Delta V \tag{3.7}$$

There are several bootstrap half-bridge e-GaN gate drivers available in the market. By comparing the driving capabilities, LMG1210 by Texas Instruments was selected as the gate driver. It provides 1.5 A peak source current and 3 A peak sink current. Also, it allows high speed operations up to 50 MHz.

LMG1210 can be controlled by a single PWM input in addition to independent control mode for high side and low side. In this design, single PWM input mode was selected for easy control. In the single PWM mode, the drive signals are generated such that the high side turns on simultaneously when the low side turns off. Since the transistors cannot turn on and off immediately, one transistor begins to turn on while the other one is turning off. During this period, the power supply is connected to ground with a resistive channel, and a significant current may flow on the transistors. This current degrades the efficiency, even damages

the devices. To prevent this, a short delay named dead-time, is generated between the high side and low side drive signals. The dead-time is selected according to the turn on and off time of the transistors. LMG1210 can generate dead-time from 0 to 20 ns adjusted by the resistor value at the control pins.

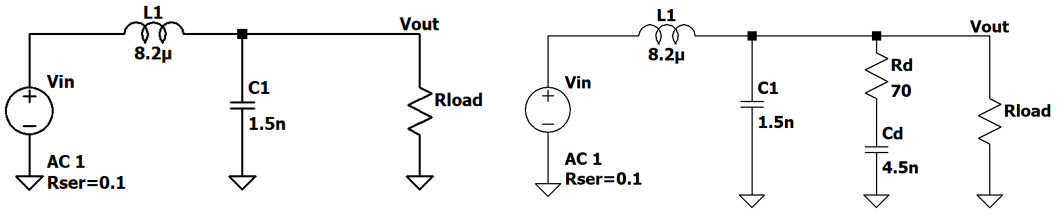
3.3 Output Stage Filter Design

The converter is controlled by a PWM signal which carries the envelope information. The voltage at the switching node between the transistors is an amplified version of the PWM control signal. Hence, the switching frequency needs to be filtered out by a low pass filter at the output of the converter. The filter should have a flat response in the passband covering the entire envelope bandwidth in order to prevent any distortion on the envelope information.

The filter design started with the conventional LC low pass filter shown in Fig. 3.5(a). Considering that the supply voltage is approximately 30 V, a filter that has 34 dB attenuation at 10 MHz, can reduce the ripple to approximately 700 mV. This ripple was accepted in order to widen the passband without further increasing the switching frequency.

A small valued inductor in the filter increases the RMS current and the power dissipation of the converter. Thus, a high valued inductor with low resistance needs to be used to prevent extra losses. On the other hand, the capacitor cannot be too low because of the impedance requirements of the RFPA drain. The capacitor bonds the quarter wavelength transmission line at the drain to the ground. If the capacitance is low, the quarter wavelength transmission line is not grounded for low frequencies. This situation may cause low frequency oscillations in the RFPA.

By considering these requirements, a low ESR 1.5 nF ceramic capacitor and a 8.2 μH power inductor with low resistance were used in the filter. The frequency response of the conventional LC filter is shown in Fig. 3.7. The resonance peaking



(a) Conventional Low Pass Filter (b) Filter with RC Damping Branch

Figure 3.5: Filter Schematics

arises from the underdamped characteristic of the filter. A big voltage oscillation occurs at this frequency since the LC circuit has a high output impedance at the resonance. In order to get a flat frequency response in the passband, the filter needs to be damped. For this purpose, a parallel damping method shown in Fig. 3.5(b) was applied to the filter. On the other hand, the resistor in the damping branch dissipates extra power because of the AC current components flowing through this circuit.

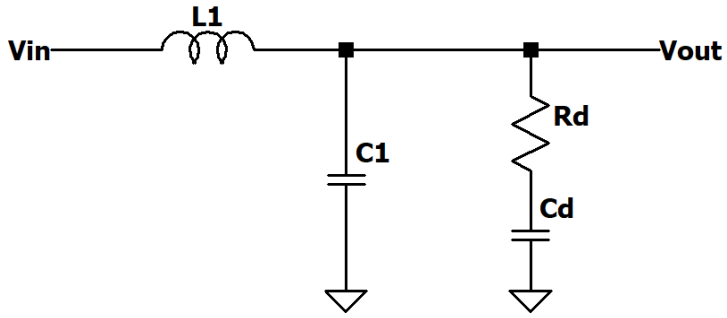


Figure 3.6: Low Pass Filter Topology

Transfer function of the filter given in Fig. 3.6 is as follows:

$$G(s) = \frac{V_{out}}{V_{in}} = \frac{R_d C_d s + 1}{R_d C_d L_1 C_1 s^3 + L_1(C_1 + C_d)s^2 + R_d C_d s + 1} \tag{3.8}$$

In [31], several optimization methods of this transfer function are presented. These methods provide different damping levels. The higher damping leads to

high C_d and higher power loss. In order to minimize the extra loss, Butterworth optimization results were used to design the damping branch. By applying a_1=a_2=b_2=1 to Eqs. 3.9, 3.10 and 3.11, the components are calculated as C_d=4.5 nF and R_d=70 Ω.

$$R_d C_d = \frac{(a_1 + a_2)}{\omega_0} \tag{3.9}$$

$$L_1(C_1 + C_d) = \frac{(a_1 a_2 + b_2)}{\omega_0^2} \tag{3.10}$$

$$R_d C_d L_1 C_1 = \frac{a_1 b_2}{\omega_0^3} \tag{3.11}$$

The effect of the RC damping branch is shown in Fig. 3.7. The resonance peaking was reduced from 12 dB to 3 dB by using this method. The resulting filter will be used the track the signals up to 1 MHz.

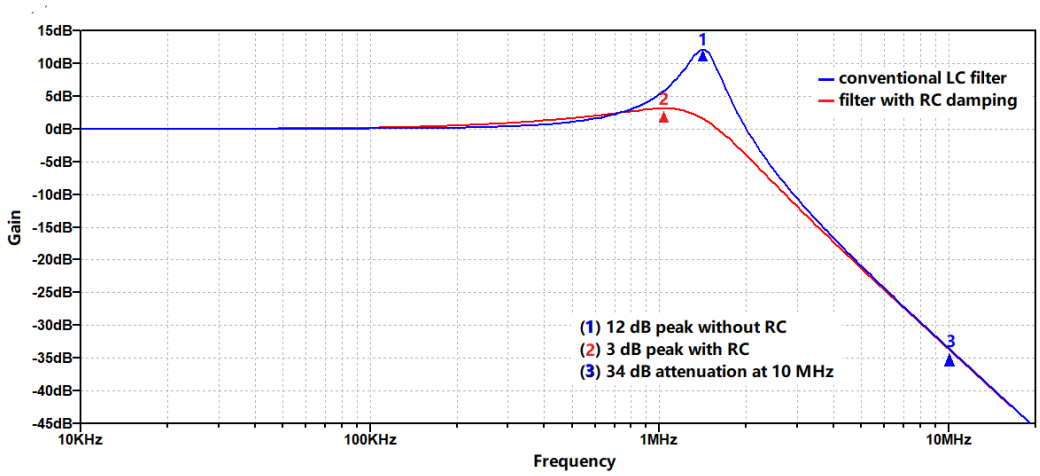


Figure 3.7: Frequency Responses of the Filters

3.4 Envelope Amplifier Measurement

Efficiency performance of the converter including the driver losses is displayed in Fig. 3.8. The measurements were taken for 10 MHz and 20 MHz switching frequencies with 30 V input voltage and 80% duty cycle. Since the efficiency drop is significant with 20 MHz, switching frequency of 10 MHz was used in the design.

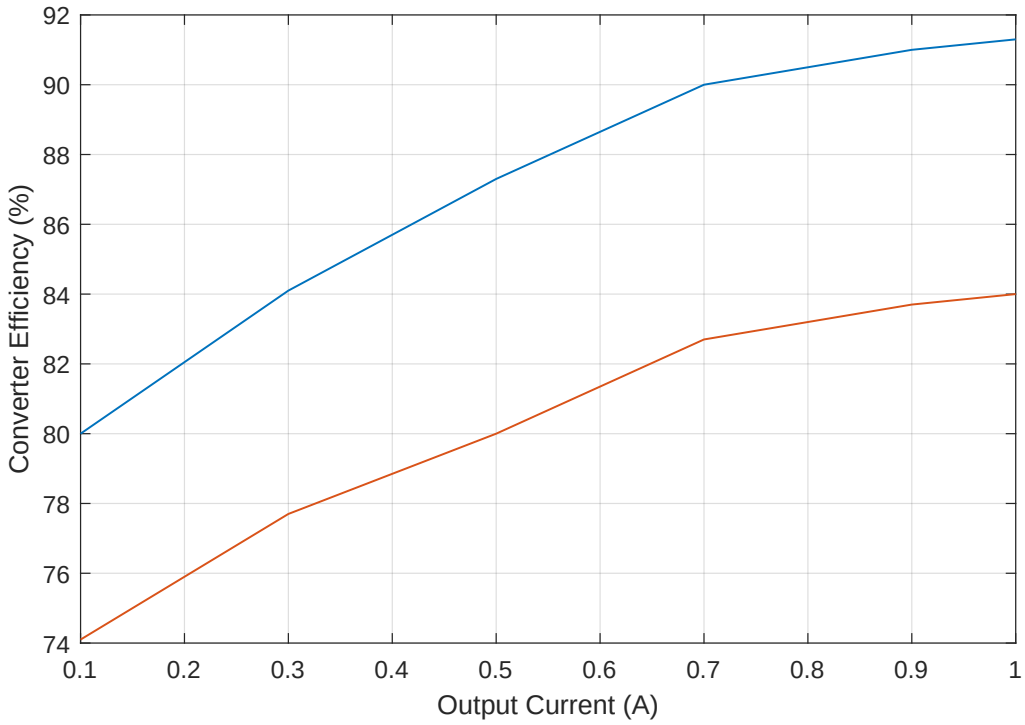


Figure 3.8: Measured Efficiency of the Envelope Amplifier for 10 MHz (Blue) and 20 MHz (Red)

Chapter 4

Design of the RF Power Amplifier

4.1 Class AB Power Amplifier Design

In this ET RFPA system, a class-AB type power amplifier was designed using 10 W CGH40010 RF Power GaN HEMT transistor from Cree. The matching circuits were designed for the 50 MHz band centered at 2.1 GHz. Large signal model of the transistor in AWR Microwave Studio was used in the simulations. The block diagram of the design is given in Fig. 4.1.

The algorithm followed in the design is given below.

- Determine and apply the bias condition
- Measure the input impedance and provide conjugate matching to the input
- Perform load-pull analysis to find the optimum output impedance for high power and efficiency
- Design the input and output matching circuits with real elements

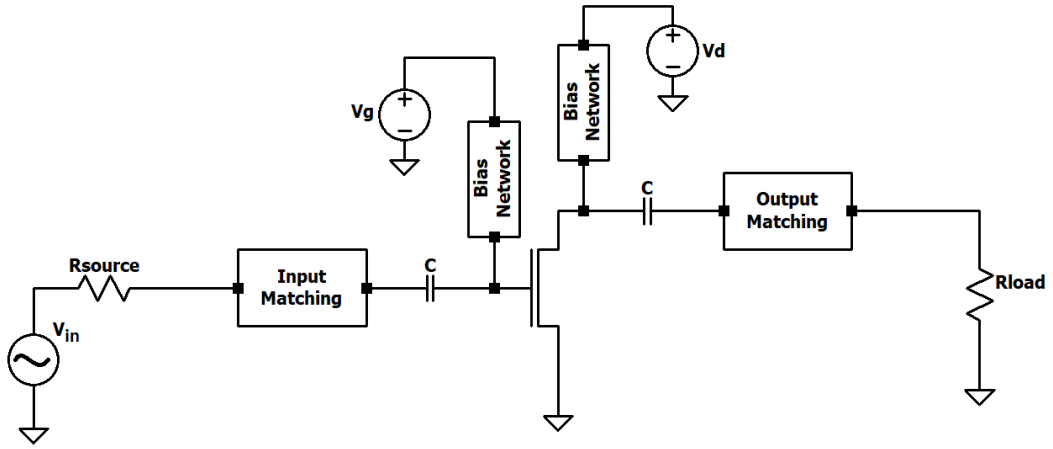


Figure 4.1: Power Amplifier Circuit

- Satisfy the stability conditions by using RC stability circuits at the input
- Optimize the matching circuits for the required output power, efficiency, stability and small signal S-parameters

For the class-AB design, the bias point was selected at V_{DD}=28 V and I_{DQ}=200 mA. Then, the gate voltage was adjusted as −2.72 V for the selected drain current. Under this bias condition, the input impedance was measured as in Fig. 4.2. For the load pull analysis, an ideal matching tool was used at the input to provide conjugate matching. The result of the load pull analysis is given in Fig. 4.3. As shown in the figure, 23+j8 Ω load impedance is considerably close to the maximum output power and maximum PAE.

In order to satisfy the input and output impedance requirements obtained by the simulations, the input and output matching circuits were designed with real components. The bias circuits were designed as shorted quarter wavelength transmission lines. In the matching circuits, transmission lines ended with shunt capacitors were preferred for easy tuning. In the input matching circuit, two RC circuits were included to satisfy unconditional stability. Both circuits were designed to establish resistive paths for the low frequencies that are inclined to oscillate.

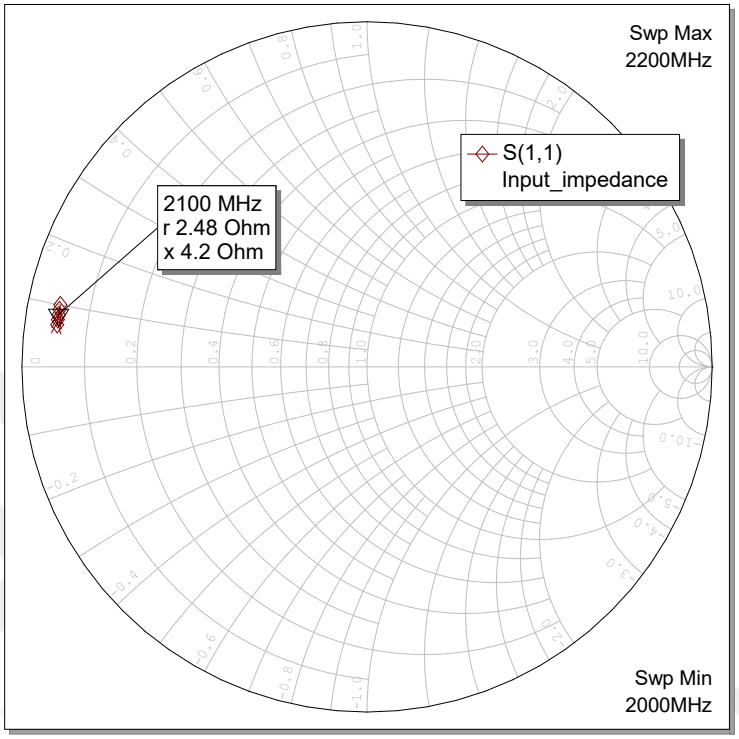


Figure 4.2: Input Impedance Analysis

After the final optimization, the input matching circuit given in Fig. 4.4 and the output matching circuit given in Fig. 4.5 were obtained. The layout of the PA circuit is displayed in Fig. 4.6. The circuit was fabricated on Rogers 4350 substrate material with 20 mil thickness together with the envelope amplifier as shown in Fig. 4.7.

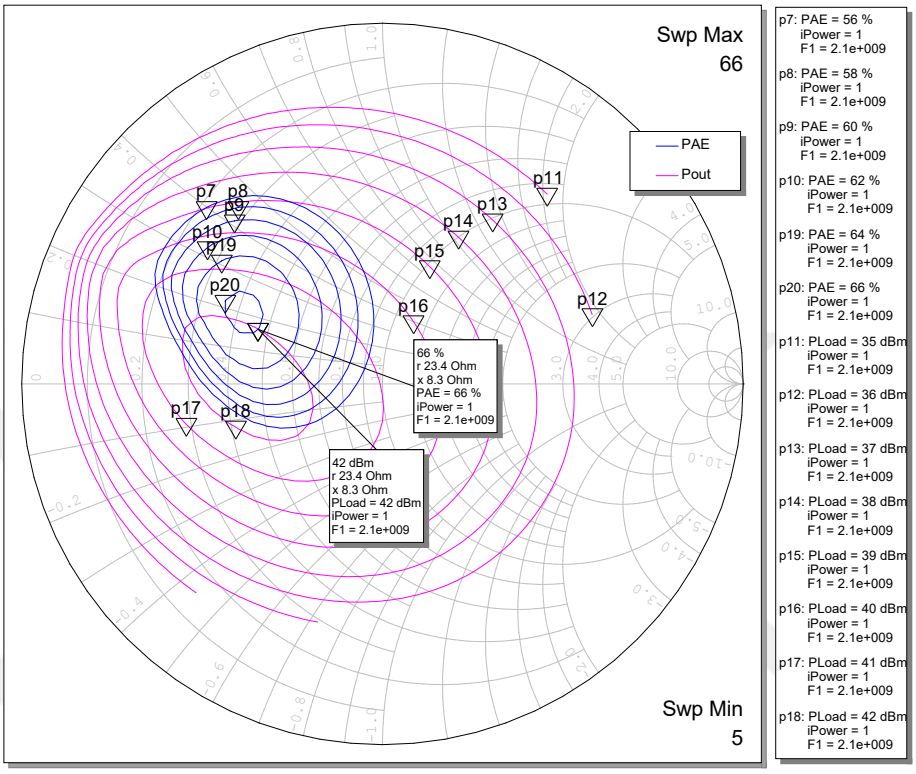


Figure 4.3: Load Pull Simulation

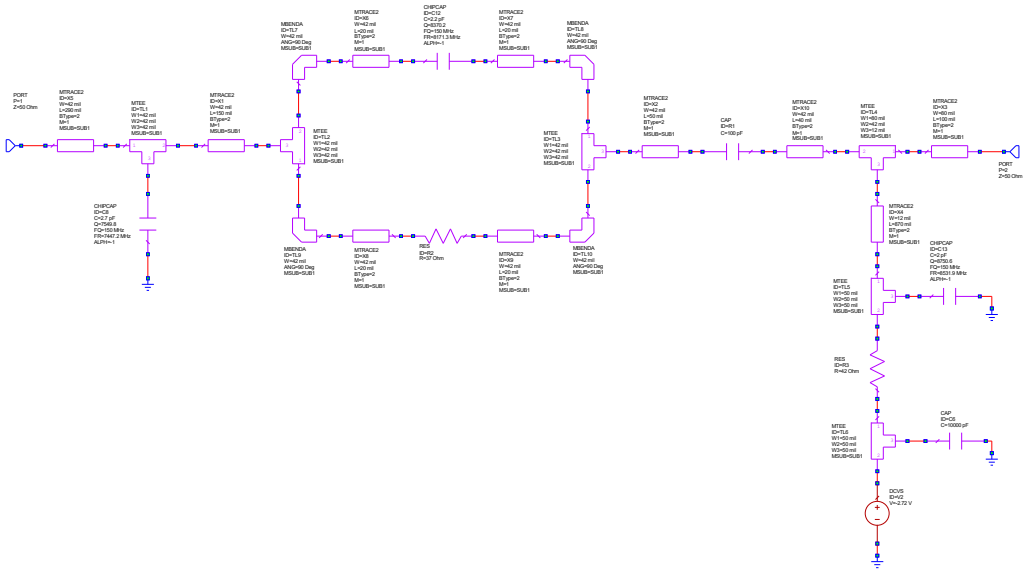


Figure 4.4: Input Matching Circuit

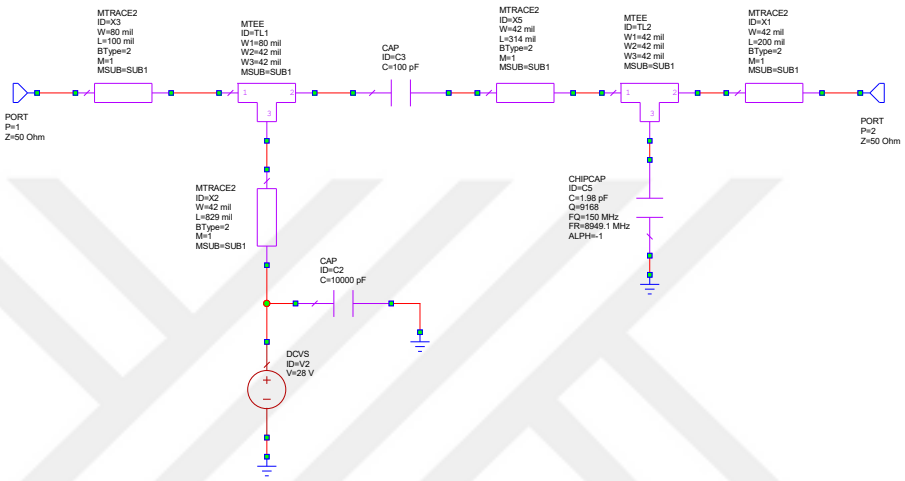


Figure 4.5: Output Matching Circuit

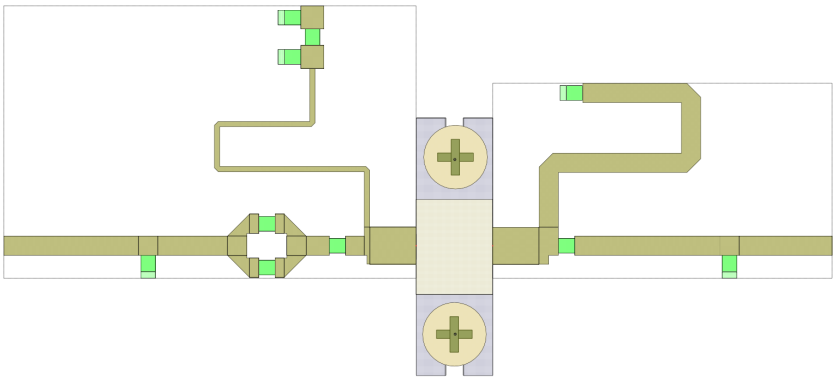


Figure 4.6: RFPA Layout

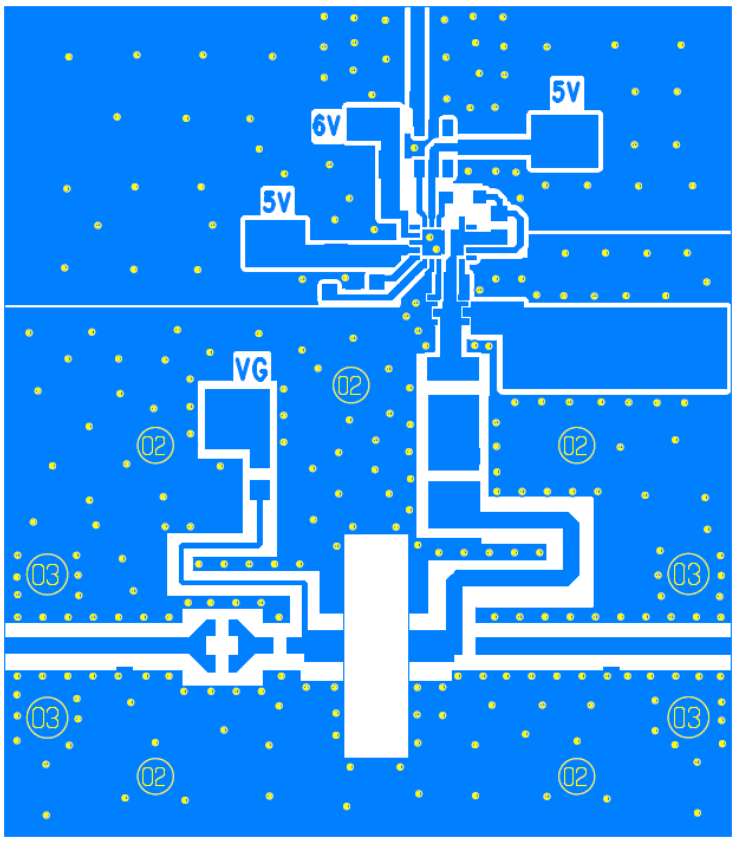


Figure 4.7: Layout of the ET RFPA Circuit

4.2 Simulation Results

As the small signal S-parameter results given in Fig. 4.8 indicate, the input and output return losses are higher than 20 dB in the band. The small signal gain is 16.4±0.25 dB.

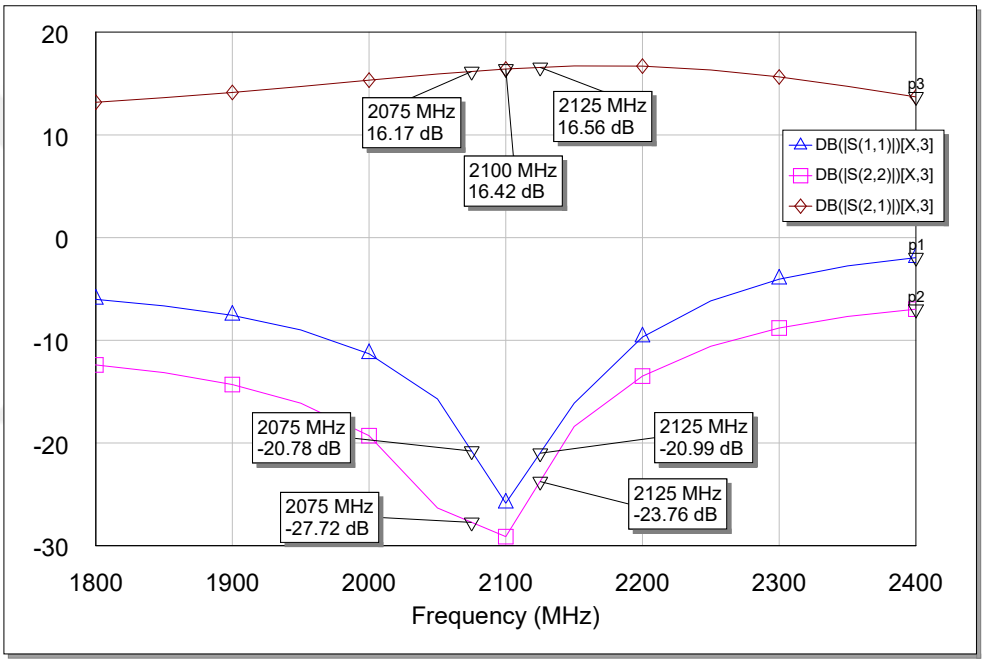


Figure 4.8: S-Paratemer Simulation

As shown in Fig. 4.9, the stability factor K is higher than unity for all frequencies where the transistor has high gain. Since the drain voltage of the amplifier will be dynamically adjusted, the stability was checked for different supply voltages.

To check the large signal performance, output power and PAE are plotted over a range of input power. As displayed in Fig. 4.10, nearly 41 dBm output power with 65% PAE can be obtained with 30 dBm input power.

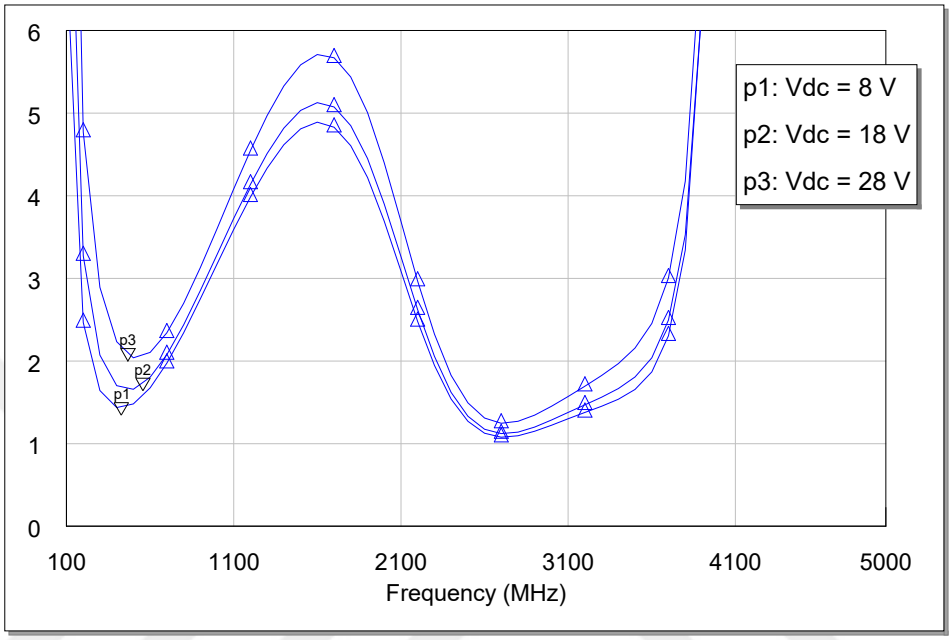


Figure 4.9: K Factor Simulation

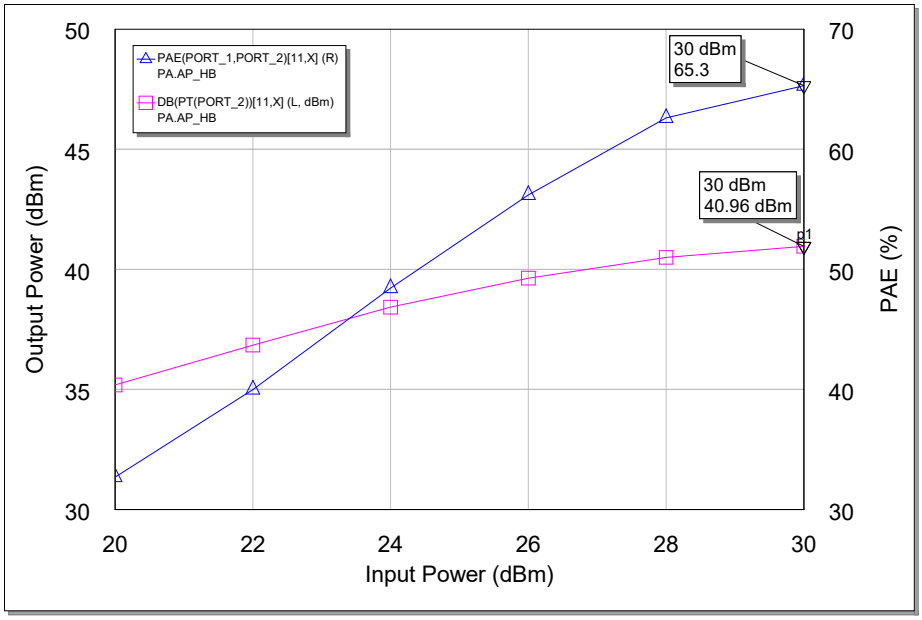


Figure 4.10: Output Power and PAE Simulation

4.3 Measurement Results

After some tuning on the fabricated circuit, the results shown in Figs. 4.12 and 4.13 were obtained. The large signal measurements were repeated for different supply voltages. As expected, the power amplifier requires 28 V supply to get 41 dBm output power. However, the back off power levels can be obtained with lower supply voltages by maintaining the high efficiency. On the other hand, the gain drops with lower supply voltages. These measurement results will be used to do proper mapping between the input power and the required supply voltage.

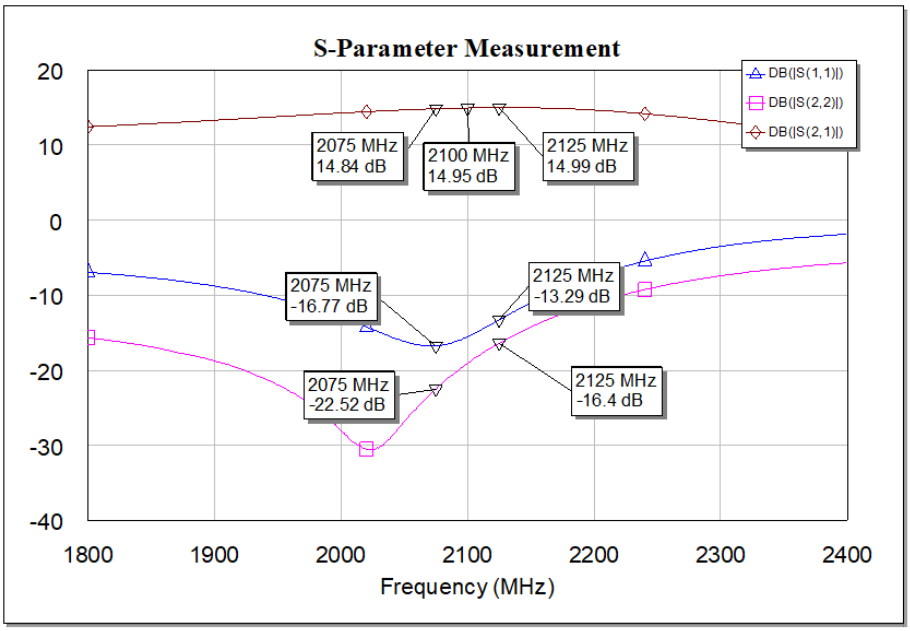


Figure 4.11: S-Parameter Measurement

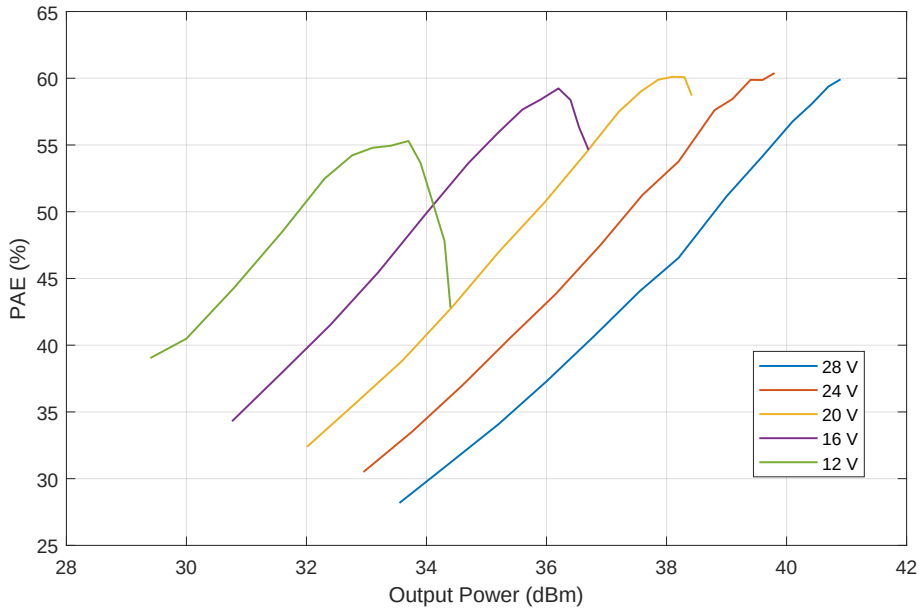


Figure 4.12: Output Power and PAE Measurement

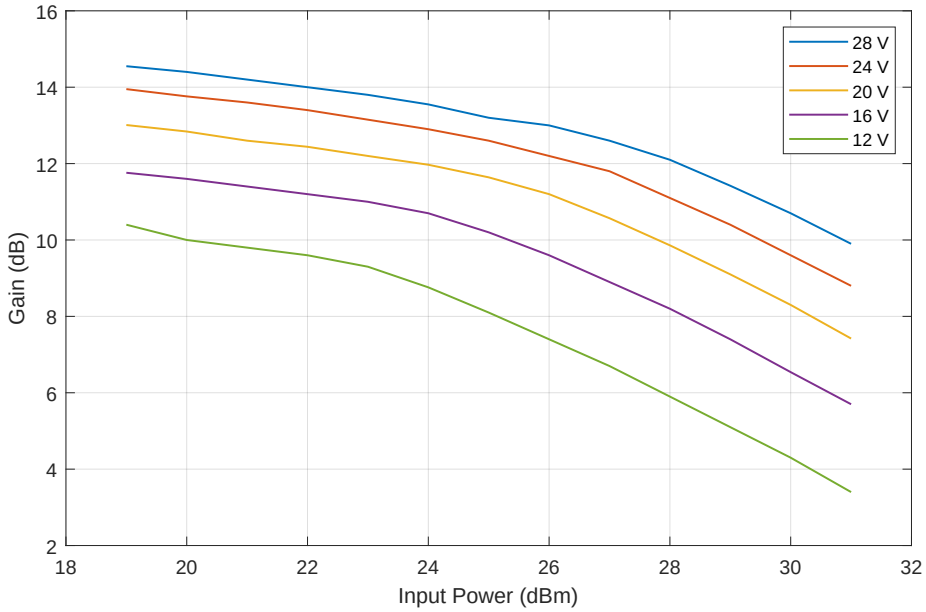


Figure 4.13: Gain Measurement

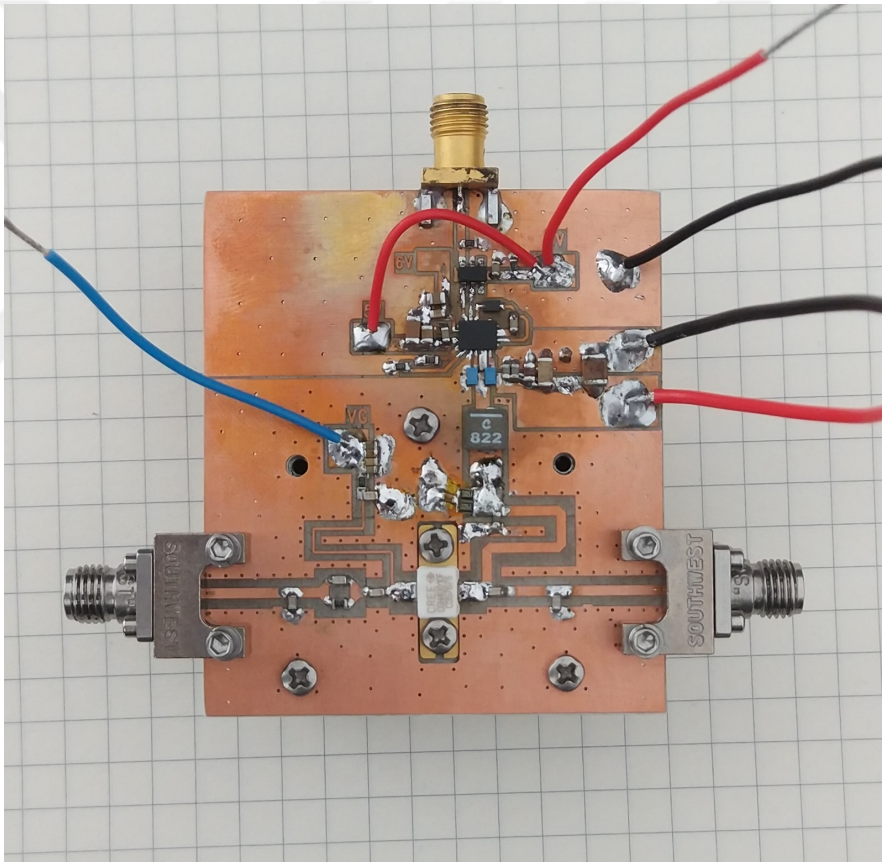


Figure 4.14: Photograph of the Fabricated Circuit

Chapter 5

Slow Tracking and Supply Signal Generation

5.1 Envelope Bandwidth Elimination

For high switching frequencies, switching losses become dominant and degrade the efficiency significantly. Therefore, the signal bandwidth that the converter can track is limited by the switching losses. In order to apply envelope tracking for the signals with wider bandwidth, slow tracking methods are used. Using these methods, a slew rate limited version of the envelope is tracked instead of tracking the exact envelope. On the other hand, slow tracking reduces the efficiency because, the bandwidth eliminated envelope does not keep the RFPA in compression region all the time. However, the efficiency degradation due to the slow tracking may not be so crucial since most of the envelope's energy is concentrated at low frequencies.

In generating such a bandwidth eliminated envelope, there is an important restriction that needs to be taken into account. As given in Fig. 4.12, it is not possible to reach high RF power levels with low supply voltages. If the slow envelope is lower than the real envelope, a lower voltage than the minimum

required voltage is supplied to the RFPA yielding that the required RF power level cannot be obtained. Hence, the slow envelope must be higher than the real envelope at every time instance. Generating such an envelope is not possible by using a conventional causal low pass filter. In order to avoid missing any peak points, non-causal methods are used.

In this design, the envelope bandwidth is eliminated by using the algorithm described in [32] that is based on tracking the input signal with a predetermined maximum slew rate. The algorithm works based on the following rules:

- At each time n, the increase and decrease must be lower than the determined slew rate.
- At each time n, next N values must be known to see if there is a need for increase in order to catch the next peaks. The N is selected such that the original slew rate allows us to catch the peaks after N values.

Let $E(n)$ be the real envelope signal, $E_s(n)$ be the slew rate limited version and d is the maximum change between two adjacent points (i.e., the maximum slew rate = $d\times$ Sampling Rate), the mathematical expression of the algorithm can be written as given below.

$$y(n) = \max_{i=0,1,\ldots,N}(E(n+i) - i \times d) \tag{5.1}$$

$$E_s(n) = \max(y(n), E_s(n-1) - d) \tag{5.2}$$

The original envelope and the slew rate limited versions are shown in Fig. 5.1 and Fig. 5.2.

In order to determine the appropriate slew rate limit for this application, the final supply signal corresponding the limited envelope was displayed in frequency domain. The cumulative distribution function of the frequency components were

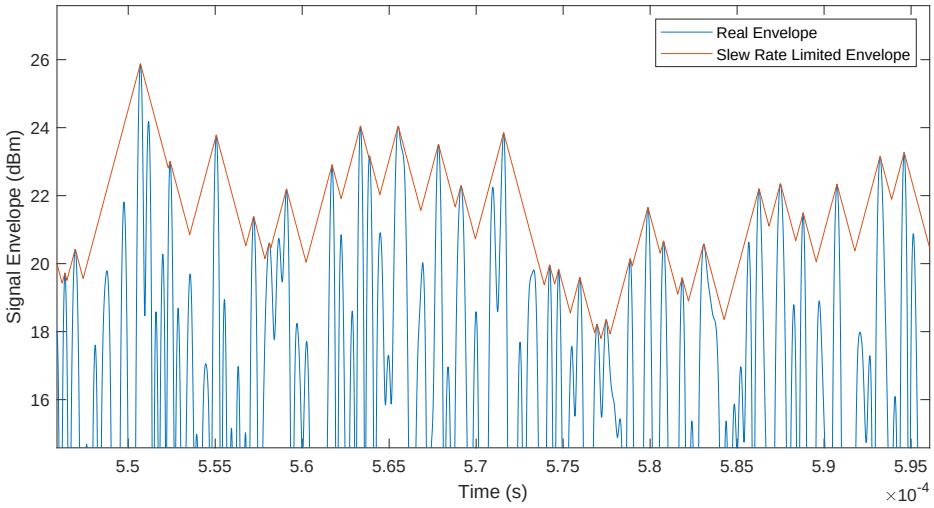


Figure 5.1: Real Envelope and Slew Rate Limited Version in Time Domain

examined. Since the envelope amplifier and the filter were designed to have a flat tracking response in 1 MHz band, the maximum slew rate was selected such that 90% of the frequency components resides at less than 1 MHz as shown in Fig. 5.3.

5.2 Supply Signal Generation

In this application, the supply signal is generated at the digital side in PWM format. After the generation of the baseband signal, the envelope of the RF signal at the input of the power amplifier, is calculated in dBm format. The overall gain of the transmitter signal chain before the RFPA is required for this calculation. The envelope bandwidth elimination is applied after this stage. Then, the required supply signal is calculated based on the envelope of the RF signal at the input of the PA.

The RFPA measurement results in Figs, 4.12 and 4.13 were used for the proper mapping between the input power and the required supply.

- In Fig. 4.12, note the output powers at the peak efficiency points for each

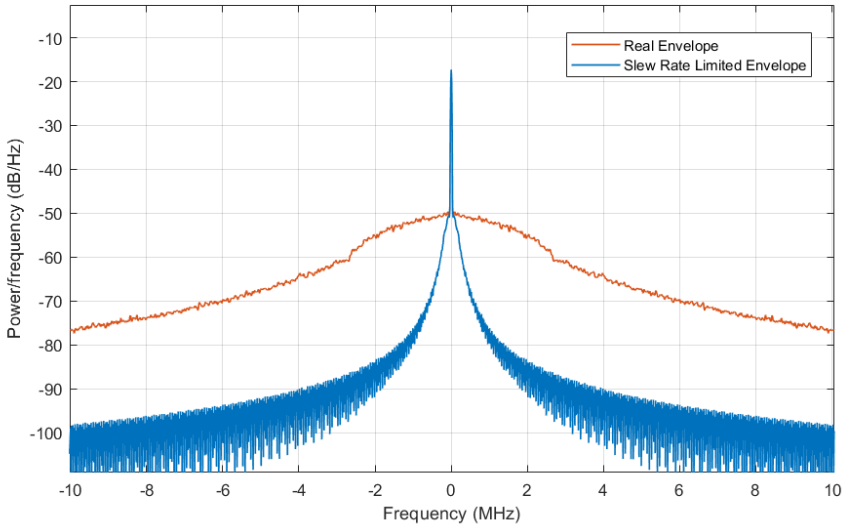


Figure 5.2: Real Envelope and Slew Rate Limited Version in Frequency Spectrum

supply voltage. In order to maximize the overall efficiency, the mapping between the input power and the supply signal is done by interpolating these peak efficiency points.

- In Fig. 4.13, for each peak points, find the required input power to generate the corresponding output power with that supply voltage.

The look up table showing these values is given in Table 5.1.

Table 5.1: Lookup Table of the Peak Efficiency Points

Supply Voltage	Output Power	Input Power
28 V	41 dBm	31 dBm
24 V	39.5 dBm	30 dBm
20 V	38 dBm	28 dBm
16 V	36 dBm	26.5 dBm
12 V	33 dBm	24 dBm

The discrete values in the look up table were put in a continuous form by using polynomial interpolation. The quadratic polynomial in Eqn. 5.3, was used

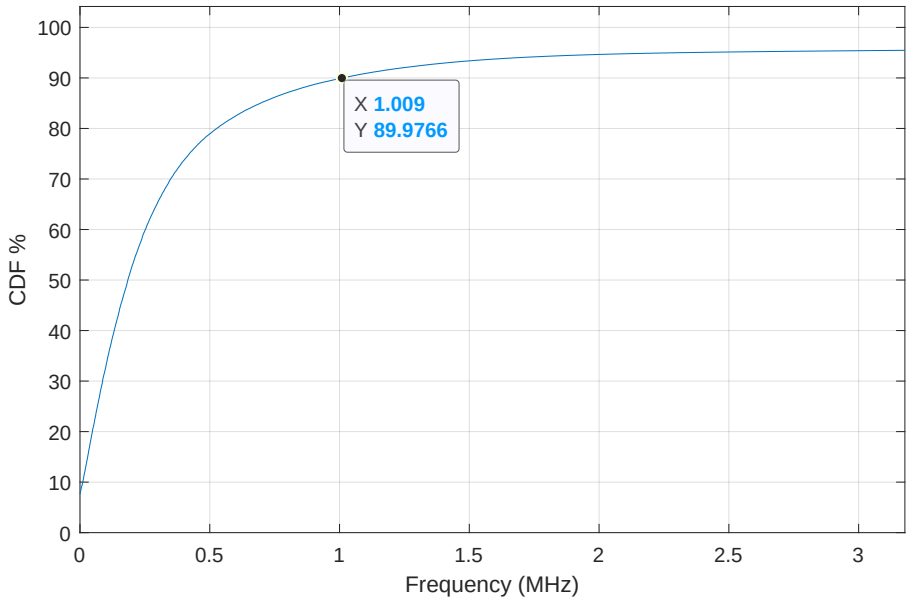


Figure 5.3: CDF of the Supply Signal

to generate the supply signal (V) as a function of the input power (dBm) of the RFPA. The discrete points and the interpolation are shown in Fig. 5.3.

$$y(x) = 0.12285x^2 - 4.5208x + 49.737 \tag{5.3}$$

The RFPA gain significantly drops for lower supply voltages than 10 V. In order to prevent the nonlinearity because of the gain drop for lower supply voltages, a detroughing factor is applied. The envelope corresponding low supply voltages, is not tracked by applying a minimum voltage limit. In this application, the minimum supply was selected as 10 V. So, the supply signal changes between 10 V and 28 V.

Finally, the PWM signal is generated based on the calculated supply signal. As a simple method, the PWM signal is generated by comparing the supply signal with a saw tooth waveform. The sawtooth frequency determines the PWM period and switching frequency.

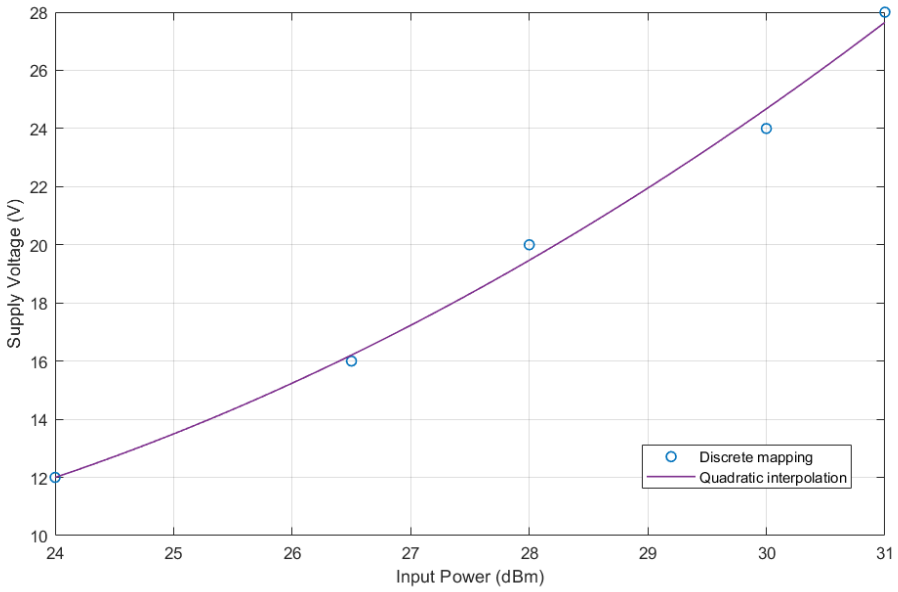


Figure 5.4: Discrete Mapping and Quadratic Interpolation

Chapter 6

Measurement

6.1 AM Signal Measurement

The test setup that was used in the measurements is given in Fig. 6.1. The baseband signal and its envelope are generated in Matlab. The required supply signal is calculated from the envelope, and envelope elimination is applied if necessary. Then, the supply signal is converted to a PWM signal and sent to the arbitrary waveform generator.

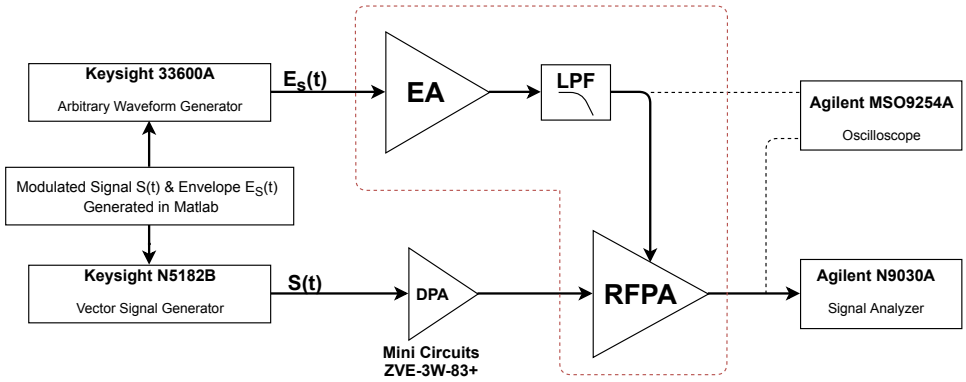
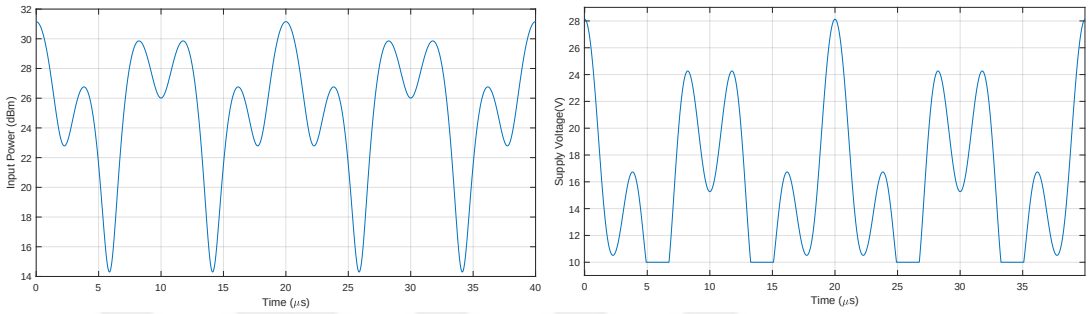


Figure 6.1: Measurement Setup

The baseband signal that is uploaded to the vector signal generator, is modulated onto the carrier frequency of 2.1 GHz. Then, a driver amplifier is used to amplify the modulated signal to the required drive level.



(a) Input Signal (b) Supply Voltage

Figure 6.2: Modulated Signal Envelope and Supply Voltage Generated for AM Measurement

The first measurement was taken by using an AM signal with unsuppressed carrier. The baseband signal contains two equal amplitude frequency components which are 100 KHz and 250 KHz. The modulated signal is shown in Fig. 6.2(a) has 6.2 dB PAPR. Since the envelope resides in the passband region of the envelope amplifier, the envelope bandwidth elimination algorithm is not required at this measurement. By using the mapping described in Eq. 5.3, the supply signal given in Fig. 6.2(b) is generated from the modulated signal envelope.

The modulated signal output and the supply voltage observed on the oscilloscope are displayed in Fig. 6.3. The frequency spectrum of the output signal is also given in Fig. 6.4. The intermodulation components appear at 37 dB below the carrier frequency.

When the generated baseband and envelope signals are applied to the system, the overall efficiency appears to be 45% by considering the driver losses and envelope amplifier losses. The efficiency with the same baseband signal under 28 V constant supply, was measured to be 32%.

Table 6.1: Summary of the Efficiency Performance in AM Measurement

	Average Output Power	Power Dissipation	Overall Efficiency
Constant Supply	3.1 W	9.7 W	32 %
Envelope Tracking	3.0 W	6.7 W	45 %

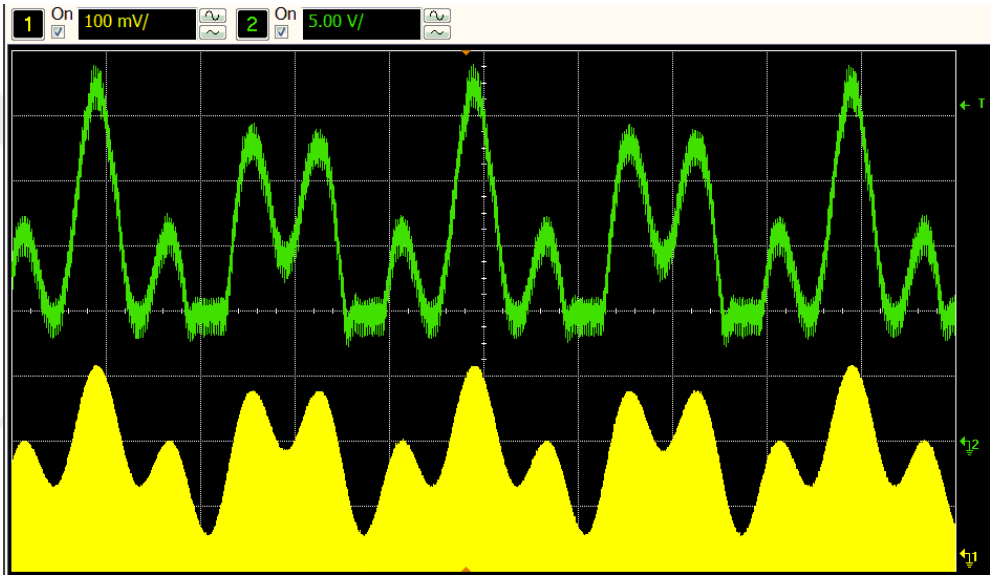


Figure 6.3: AM Signal (Yellow) and Supply Voltage Waveform (Green)

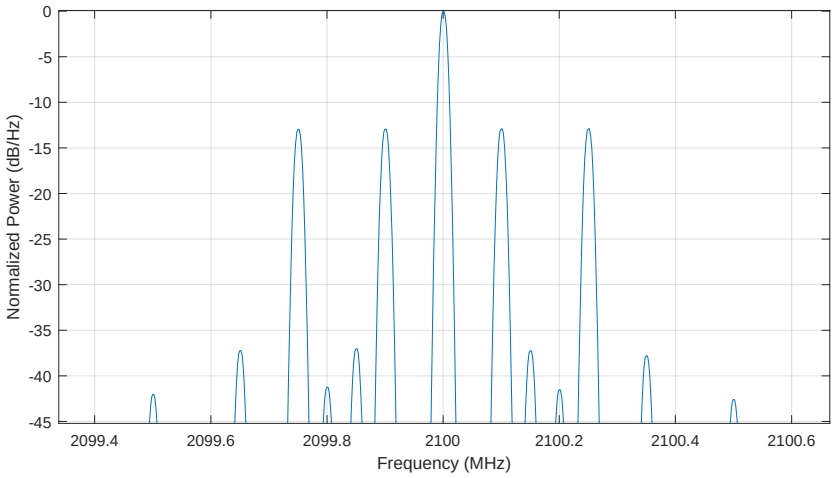


Figure 6.4: Measured Output Power Spectrum of ET RFPA by Using the AM Signal

6.2 LTE Signal Measurement

In the second measurement, 3 MHz and 5 MHz LTE signals with 12 dB and 13 dB PAPR were applied to the system. For both of the signals, the envelope bandwidth was reduced to 1 MHz by using the envelope elimination algorithm. The supply voltage and the modulated signal observed on the oscilloscope are displayed in Fig. 6.5.

Table 6.2 summarizes the efficiency performance of the ET RFPA by comparing to using a 28 V constant supply. In Fig. 6.6, the normalized output power spectrum of the ET RFPA is displayed for the 5 MHz signal. The adjacent channel leakage ratio (ACLR) is measured as 26 dBc.

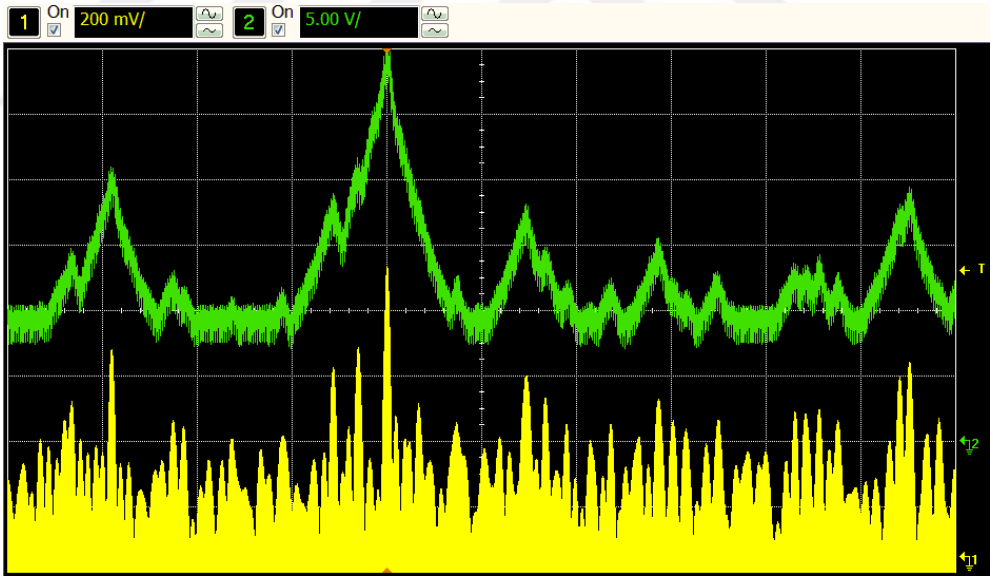


Figure 6.5: LTE Signal (Yellow) and Supply Voltage Waveform (Green)

Table 6.2: Summary of the Efficiency Performance in LTE Measurement

	PAPR	Average Output Power	Power Dissipation	Overall Efficiency
Constant Supply (3 MHz)	12 dB	0.81 W	6.2 W	13 %
Envelope Tracking (3 MHz)	12 dB	0.79 W	3.0 W	26 %
Constant Supply (5 MHz)	13 dB	0.65 W	5.9 W	11 %
Envelope Tracking (5 MHz)	13 dB	0.63 W	3.1 W	20 %

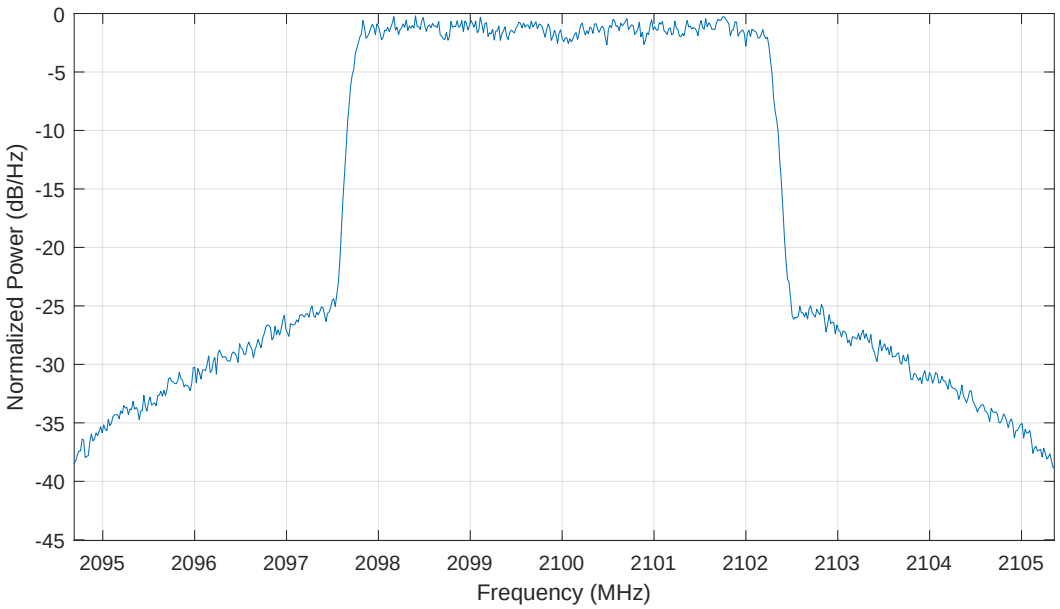


Figure 6.6: Measured Output Power Spectrum of ET RFPA

Chapter 7

Conclusion

In this thesis, the aim was to design and fabricate an ET RFPA to improve the back-off efficiency in order to operate efficiently with high PAPR signals. A synchronous buck converter which is one of the most fundamental topologies was adopted in the envelope amplifier. In order to attain a converter with high slew-rate and efficiency, GaN switching transistors and a fast driver circuit were chosen. Design steps of the filter at the converter output and the class-AB power amplifier were mentioned. The resulting envelope amplifier has a bandwidth of 1 MHz with the switching frequency of 10 MHz. In order to improve the bandwidth that can be tracked by the ET RFPA, a slew-rate elimination technique was used. At the end, the performance of system was tested by applying time-varying envelope signals. The resulting ET RFPA has 26% overall efficiency with the LTE signal that has 3 MHz and 12 dB PAPR. The overall efficiency is 20% in the case of 5 MHz and 13 dB PAPR signal.

Since the modern communication systems use signals with high bandwidth to achieve high data rates, the envelope amplifier has strong requirements of slew-rate and efficiency. In a design with discrete components, the efficiently achievable switching frequency is limited because of the parasitic loss and delay components on the circuit. Due to the significant switching losses at higher frequencies, the switching frequency of the envelope amplifier could not be increased

above 10 MHz. Then, 1 MHz bandwidth was achieved by using the output filter of the converter to have an acceptable switching ripple.

The design of the filter has critical importance in the envelope amplifier performance. The underdamped characteristic of the conventional low pass filter at the output of the converter may cause significant resonance peaking that may cause distortion and even damage the switching devices. Therefore, an efficient and damped filter topology is required with carefully selected components.

The envelope bandwidth elimination method helped to track the signals with higher bandwidth. However, this techniques have considerable drawbacks. By decreasing the maximum allowable slew-rate of the algorithm, the efficiency improvement of the ET system is decreases as expected. In addition to that, using the slow version of the envelope, causes a nonlinear memory effect that degrades the linearity. LTE measurement results confirm these expectations. The adjacent channel leakage ratio of the system (ACLR) is measured as 26 dBc in the 5 MHz LTE measurement.

In this design, the GaN transistors provided considerably high switching efficiency that is not easy to achieve with silicon devices. For future work, the bandwidth of the envelope amplifier can be improved more by using a linear-assisted hybrid topology together with the GaN switching devices. Also, an integrated design may lead to achieve higher switching frequencies efficiently. With a high bandwidth envelope amplifier, tracking the exact envelope without using the bandwidth elimination may be possible. In this case, a better linearity is expected since the memory effect distortion is cancelled. In addition to that, digital predistortion techniques can be employed to improve the linearity. As given in [33, 34], nonlinear behavior of the ET systems can be modelled and compensated by applying predistortion on the input signal.

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