ZnO, TiO_2 AND EXOTIC MATERIALS FOR LOW TEMPERATURE THIN FILM ELECTRONIC DEVICES

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By
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August 2012

I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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August 2012

The metal-oxide-semiconductor field-effect transistor (MOSFET) technology is the core of integrated circuit industry. Nearly all electronic devices around us contain transistors for various purposes like electronic switches, amplifiers or sensors. As the need for more complex and miniature circuits has arisen, scaling down transistor sizes become the top priority. As Moore's law indicates, number of transistors on integrated circuits doubles every two years but in future fabrication challenges and limitations like quantum effects seen in small devices will block further miniaturization. New growth techniques are required for depositing conformal, high quality films -like high-k dielectrics instead of SiO_2- with atomic thickness control to reduce possible problems. Atomic layer deposition techniques are developed to meet these requirements.

The field of thin film transistors (TFT), which is a subset of MOSFET's have first started to be used in flat panel displays but now they are used in various fields, since their functional properties make them powerful candidates for sensor applications.

ALD technology is important also for TFT applications since its low temperature growth mechanism allows fabricating TFT's on various substrates like flexible and/or transparent ones. With ALD technique, transistors can be built even on cloths which makes the dream of e-suits real.

In this thesis, thin film transistors are designed and fabricated using atomic layer deposition technique both for channel and dielectric layer growth. Design and fabrication steps of the TFT devices are realized in a cleanroom environment. The fabricated TFT's are mainly characterized by measuring their current-voltage relations. A parameter analyzer with a probe station is used for such measurements.

ALD grown ZnO TFT's and the effect of growth temperature on performance characteristics are examined. High performance devices having very high I_{on}/I_{off} ratios are fabricated at a temperature low as 80°C. ALD grown TiO_2 TFT's are also fabricated and effects of annealing temperature on device performance are analyzed. This study is, to the best of our knowledge, the first demonstration of TiO_2 TFT's grown by a thermal-ALD system. GaN and pentacene TFT's are also fabricated and showed promising results. Pentacene TFTs have a special importance since it is a p-type organic semiconductor which gives us the opportunity to work on hybrid organic-inorganic structures.

In conclusion, TFT devices based on ALD grown channel and/or dielectric layers show very encouraging results in terms of low cost, low temperature fabrication opportunities and freedom of using any substrate that can handle ALD processing temperature.

Keywords: TFT, ALD, ZnO, TiO_2, Al_2O_3, pentacene, GaN

ÖZET
ZnO, TiO_2 VE BAZI EGZOTİK MALZEMELER KULLANILARAK DÜŞÜK SICAKLIKTA OLUŞTURULMUŞ İNCE FİLM ELEKTRONİK AYGITLAR

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Metal oksit-yarıiletken alan etkili transistör (MOSFET) teknolojisi entegre devre sanayinin çekirdeği konumundadır. Neredeyse çevremizdeki tüm elektronik cihazlar elektronik anahtarlar, amplifikatörler veya sensörler gibi çeşitli amaçlar için transistörler içerirler. Zamanla daha karmaşık ve daha küçük boyutlarda devrelere duyulan ihtiyaç arttığı için transistör boyutlarını aşağı ölçekleme konusu öncelikli hale gelmiştir. Moore kanunundan anlaşılacağı gibi, entegre devrelerin üzerindeki transistör sayısı her iki yılda bir iki katına çıkar ama bu küçülmenin bir limiti olacaktır. Küçük cihazlarda görülen kuantum etkileri ve küçük cihazların üretim zorlukları aşağı ölçeklemeyi sınırlandıracaktır. Yeni film büyütme teknikleri bu noktada çok büyük önem kazanmaktadır. Konformal, yüksek kaliteli ve yüksek dielektrik katsayılı filmler kullanılarak SiO_2 ile yaşanabilecek olası sorunlar azaltılabilmektedir. Diğer yöntemlere kıyasla daha yeni bir yöntem olan atomik katman kaplama (ALD) teknikleri bu gereksinimlere cevap vermektedir.

İnce film transistörler (TFT) MOSFET ailesinin bir alt kümesidir ve onları önemli kılan özellikleri işlevsellikleridir. İnce film transistörler ilk düz panel ekranlarda kullanılmaya başlanılmış olup şu anda sensör uygulamaları başta olmak üzere çok çeşitli alanlarda kullanılmaktadırlar.

Düşük sıcaklıklarda büyüme mekanizmasına sahip ALD tekniği ile çok çeşitli yüzeylerde, esnek ve / veya şeffaf olanlar gibi, TFT teknolojisini geliştirmek ve çeşitli uygulamalarda kullanmak mümkündür. Bu şekilde çok önemli ve sıra dışı uygulamalara imza atılabilir hatta elektronik kıyafetler gibi hayal ürünü konseptler gerçekleştirilebilir.

Bu tez çalışmasında, ince film transistörler tasarlanmış ve hem kanal hem de dielektrik katmanlarının büyütülmesinde atomik katman kaplama yöntemi kullanılmıştır. TFT cihazlarının tasarımı ve fabrikasyonu temiz oda ortamında gerçekleştirilmiştir. Fabrike edilen TFT cihazları akım-gerilim ilişkisinin gözlemlenmesiyle karakterize edilmiştir. Bu ölçümlerin tamamlanabilmesi için bir prob istasyonu ve bir parametre analizörü kullanılmıştır.

ALD ile büyütülmüş ZnO TFT performans özellikleri üzerinde büyütme sıcaklığının etkisi incelenmiştir. Çok yüksek I_{on} / I_{off} oranlarına sahip yüksek performanslı cihazlar 80 ° C gibi düşük bir sıcaklıklarda üretilmiştir. İkincil olarak yine ALD tekniği ile üretilmiş TiO_2 TFT cihaz performansı ve sıcaklıkla tavlamanın performans üzerindeki etkileri analiz edilmektedir. Bu çalışma, termal-ALD kullanılarak TiO_2 TFT üretilmesi bakımından bir ilktir. Son olarak da egzotik malzemeler kanal yapısı olarak kullanılmış ve GaN ile pentacene malzemelerinden üretilen cihazların ölçüm sonuçlarının ümit verici olduğu göstermektedir. P-tipi organik bir yarı iletken olan pentacene, hibrid organik-inorganik yapılar üzerinde çalışma fırsatı veren bir malzeme olduğundan ayrıca bir öneme sahiptir.

Sonuç olarak, ALD tekniği kullanılarak büyütülmüş kanal ve / veya dielektrik katmanlarına dayalı TFT cihazları düşük sıcaklıkta ve düşük maliyetli bir şekilde çok çeşitli substratlar üzerine üretilebilmekte ve çok orijinal uygulamalr geliştirilebilmektedir.

Anahtar Sözcükler: TFT, ALD, ZnO, TiO_2, Al_2O_3, pentacene, GaN

To my own family and UNAM clean room family.

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Chapter 1

Introduction

1.1 Historical Background

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most-important device for integrated circuits like microprocessors and memories. The principle of the field-effect transistors was first demonstrated by Lilienfeld and Heil in the early 1930s. In the late 1940s Shockley and Pearson took over the research and showed the first Ge based bipolar point-contact transistor. Ligenza and Spitzer worked on MOS systems using Si-SiO relationship in 1960 and in the same year, Atalla showed the first MOSFET.

The requirement for increasing the performance and need for more dense integrated circuits (IC's) caused scaling down of device dimensions. The number of components per IC has grown exponentially. After a certain point, the minimization rate will be limited with technological challenges and fabrication cost.

There are many ways to categorize the versions of FETs. According to charge carrier type, devices can be categorized as n-channel and p-channel devices. n-channels are formed by electrons and current flowing through the channel increases with increasing gate bias, while p-channels are formed by holes and the current increases with increasing negative gate bias. Also, it is important to describe the state of the transistor according to on/off characteristics. FETs are called enhancement-mode if they are off under zero gate bias and depletion-mode if they are on under zero gate bias.[1]

Thin-film transistors (TFTs) that are based on MOSFETs became the "rice" of electronic flat panel industry. In 1968, it was apparent that the use of TFTs to make high performance electroluminescent matrix displays was an exciting opportunity and starting from that time, TFT's have been mainly used for display technologies.[2]

In this thesis, atomic layer deposition (ALD) technique is used for thin film growth due to its unique advantages like accurate thickness control over large areas, reproducibility, conformal coatings and trench-fill capability.

1.2 Motivation

Our motivation is to investigate atomic layer deposition, a new and alternative technique for low temperature, low cost, flexible and transparent electronic devices. There is a wide field based on transparent and flexible transistors. The technology can be used in military (smart displays), health (biosensors), security (tracking and locating devices) and commercial (smart displays used in cell-phones and computers) technologies. Especially, sensor applications based on TFT technology is very attractive. Biological sensors for the detection of glucose or DNA, chemical sensors for detecting humidity or pH levels, temperature sensors, mechanical force sensors and many others fabricated based on TFT devices are shown in the literature.[3-5]

Many applications based on transparent/flexible TFT displays can be found in the literature. (See Fig. 1.1)

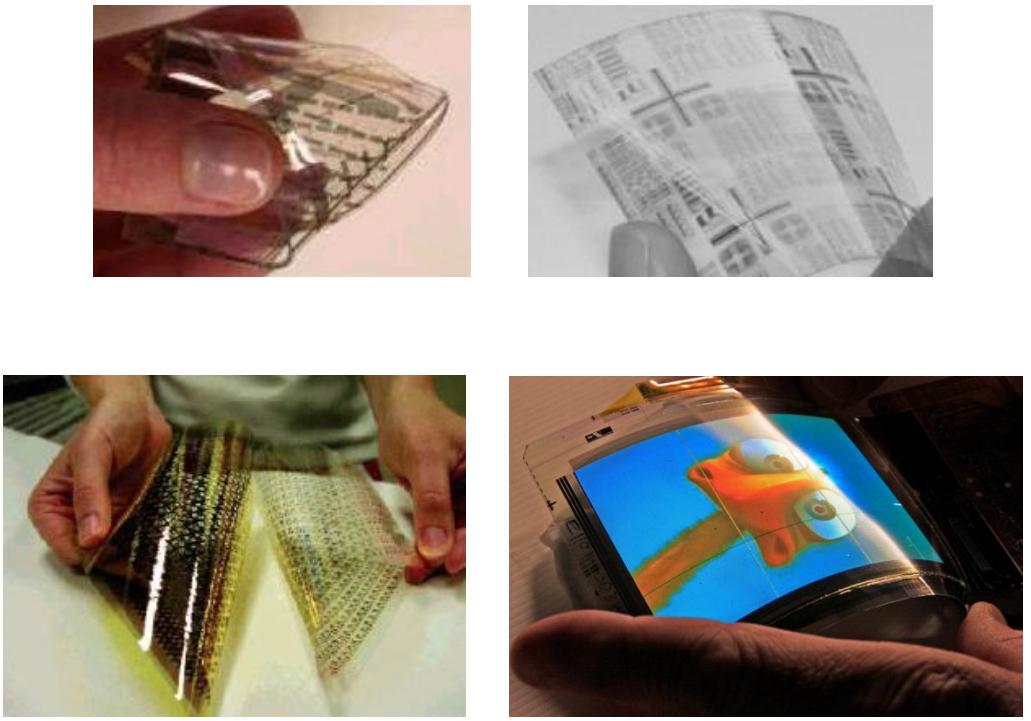


Figure 1.1 Examples of flexible device technology [6-9]

For this thesis, we fabricated inorganic TFT devices based on ALD deposited semiconducting ZnO and TiO_2 channel layers. We chose these materials according to the following criteria:

- Both are metal oxides able to be grown by ALD technique.[10,11]
- Both are wide band-gap materials having innovative optical characteristics besides electrical ones which allow them to be used in not only electrical but also optical sensor applications.[12-14]
- Both are transparent oxides.[10]
- Both have the advantage of controllable doping concentration.

1.3 Thesis Overview

This thesis will continue by introducing basics of ALD technique and later on TFT device physics. In Chapter 4, ZnO-based thin film transistors will be presented with an emphasis on the effect of growth temperature on device performance. Chapter 5 will discuss TiO_2 film growth and characterization, TiO_2 TFT fabrication and device analysis. Chapter 6 will continue with TFT fabrication and characterization based on exotic channel materials. The final chapter will summarize the thesis and give some future directions based on this work.

Chapter 2

Atomic Layer Deposition: Fundamentals

2.1 Introduction

Atomic layer deposition (ALD) is a chemical vapor deposition (CVD) technique based on sequential saturative surface reactions. The basic difference of ALD from other CVD techniques is that in ALD systems, precursors are pulsed to the surface one at a time, allowing each precursor to saturate the surface with a monolayer of itself. With this self-limiting mechanism, highly conformal and controllable films can be deposited.

ALD was first developed by Suntola and co-workers in Finland, under the name of Atomic Layer Epitaxy (ALE). The first experiments are performed at 1974, which are based on element reactants. In the subsequent studies, compound reactants were also used. One of the oldest researchers of ALD technology is Aleskovskii from the Soviet Union. In the proceedings of a conference

organized in 1960s, one of his co-workers describes a method which deposits TiO_2 using $TiCl_4/H_2O$.

Starting from mid 90s, due to continuing scaling down in Si-based microelectronics, the need for highly conformal and highly controllable films with a slow deposition rate has extensively increased. For this reason, ALD has gained considerable interest due to its ability to deposit high quality films at low temperatures with excellent conformality and thickness control at the atomic level.

A wide variety of materials have been deposited using ALD, such as nitrides (semiconductors, metallic, dielectric), oxides (ternary oxides, semiconductors, dielectric, transparent conductors), fluorides, sulphides, selenides, tellurides, elements, II-IV compounds and III-V compounds.

2.2 ALD Growth

ALD film growth is a cyclic process composed of four main steps which are repeated for as many cycles as desired,

1. Exposure of first precursor,
2. Purge or evacuation of chamber,
3. Exposure of second precursor,
4. Purge or evacuation of chamber.

After completion of these four steps, a known amount of material is deposited on the surface, named as *growth per cycle* (GPC). ALD cycles can be repeated until the desired film thickness is obtained.

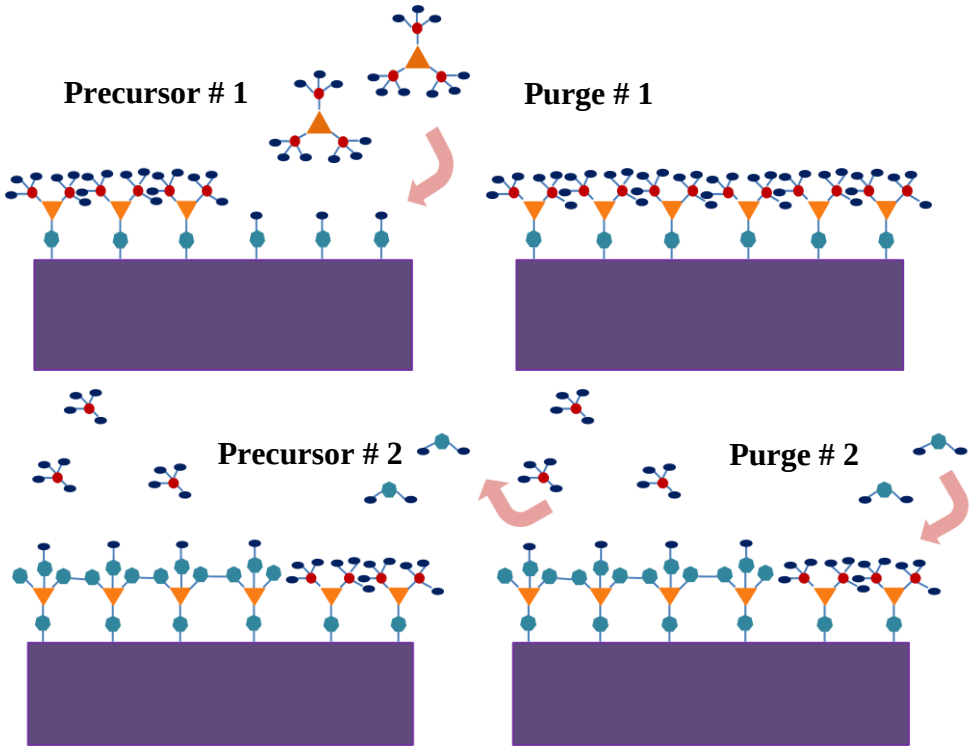


Figure 2.1 A schematic of an ideal ALD cycle

In an ALD process, deposition starts from the reactions between first precursor and surface reactant groups. For example, in order to grow metal oxides, surface should be terminated with hydroxyl groups to react with metal precursor and release some of the ligands. If there are no functional groups on the surface, in this case hydroxyl groups, incoming precursor can only chemisorb to the surface. As distinct from other CVD techniques, in ALD, reactants application is separated in time which prevents the gas phase reactions between the precursors. After completion of one ALD cycle, surface is saturated with one monolayer of the film.

Two factors are shown to cause saturation on the surface: steric hindrance of ligands and the number of reactive surface sites. Steric hindrance of relatively large ligands can cause part of the surface to remain un-reacted. Also if the number of reactive sites is less than the required for maximum coverage, some

space remains available on surface with no bonding sites accessible. Due to these two factors, growth per cycle may become less than a monolayer per cycle.

2.2.1 Major Advantages of ALD

1. Self-limiting: ALD is a self-limiting process; therefore, growth per cycle (GPC) can be known precisely, allowing an accurate thickness control.
2. Good conformality and trench fill: If the precursor purge time is long enough, the surface becomes saturated by the precursor and all excess molecules are removed properly. This property of ALD makes the technique very effective in terms of conformal deposition and trench-fill capability.

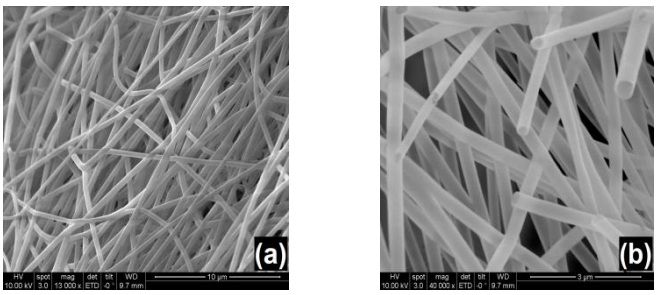


Figure 2.2 (a) Fibers grown by electrospinning, (b) AlN hollow nanotubes after calcination[15]

3. Reproducible: Due to self-limiting behavior, ALD is very reproducible and simple to implement.
4. Low temperature process: With ALD technique, it is possible to grow high quality films at low temperatures since it is a chemical process. This is a unique property of ALD among all CVD methods.
5. Digital alloying is possible to deposit ternary and quaternary alloys with an easy and accurate composition control.

2.2.2 ALD Reactors

Mainly there are two types of reactors: flow-type ALD reactors with inert gas valving and flow-type ALD reactors with moving substrates. Reactor types and their effects on film growth are not going to be analyzed in this thesis.

The reactor used in this thesis is Savannah S100 ALD reactor (Fig. 2.3) from Cambridge Nanotech Inc. It is a flow type reactor with a 4" diameter x 0.25" deep reaction chamber. It has a single gas injection point and a single evacuation point for reaction gases to be pumped continuously. ALD systems having single injection point like the one used for this thesis may cause thickness non-uniformities. In order to solve non-uniformity problems, shower-head injectors are preferable since they improve the gas distribution and reduce non-idealities.

Figure 2.3 Recipe window and external appearance of Savannah S100 ALD reactor[16]

2.2.3 ALD Precursors

Requirements for ALD precursors,

Volatility

Vapor pressures and the highest applicable source temperatures are the two very important parameters defining the volatility of precursors.

Stability against self-decomposition

If precursors decompose at the deposition temperature, self-limiting growth mechanism becomes no longer applicable. To learn whether the precursor is thermally decomposing or not, decomposition experiment on both bare substrate and previously deposited films can be performed.

Decomposition is a thermally activated process which increases the growth rate exponentially with temperature. In order to avoid decomposition of the precursors, growth temperature can be lowered.

Decomposition may cause incorporation of contaminants in the film, so that it must be minimized until reaching a self-limiting growth with a contamination level that can be tolerated.

Aggressive and complete reactions

Due to separate dosing of reactants, precursors which aggressively react with each other can be comfortably used in ALD systems. Actually, these reactions are preferable in ALD systems short cycle times and effective precursor usage.

No etching reactions

In some cases, etching reactions may occur in between consecutive precursor pulses. A testing mechanism similar to the one explained in self-decomposition section can be run.

Unreactive byproducts

Precursors should produce unreactive byproducts that can be evacuated easily. Reactive byproducts may damage both the chamber walls and exhaust lines. Also they may reabsorb on the film surface and decrease the growth rate by blocking adsorption sites.

Others

Low cost, easy synthesis and handling, nontoxicity and environmental friendliness are other important precursor requirements.

How should the user select suitable precursors for a specific deposition will be explained with an example:

ALD Precursor Selection for TiO_2 deposition

ALD users should be careful since in ALD systems there is always a possibility to have impurities because of non-reacted ligands. It is observed that according to the type of precursor used, additional atoms can be found in the film. For example, it is likely to find carbon and hydrogen if titanium alkoxides are used like titanium isopropoxide ($Ti_4(OCH_3)_{16}$); and it is likely to find chlorine if titanium halides are used like titanium tetrachloride ($TiCl_4$). These impurities serve as sources for defects and additional trap states.[17]

Reported Ti precursors and reactants for TiO_2 deposition are as follows:

- Ti isopropoxide and tetrakis-dimethylamido titanium (TDMAT) are two widely used precursors. For low temperature deposition, high growth per cycle (GPC) was observed for depositions performed with TDMAT precursor and H_2O as reactant. The reason is the phyisorption mechanism which results with bonding of more than one monolayer to the surface in one cycle.[18]
- Titanium tetrachloride is another precursor that has been used with H_2O for TiO_2 deposition. This precursor is not preferable because of the reaction by-product which is a corrosive material: HCl.[18]
- Titanium ethoxide ($Ti(OC_2H_5)_4$) can also be used for TiO_2 thin film deposition.[17]

In our experiments, TDMAT and H_2O are used for TiO_2 channel deposition. As it is recommended in the literature, TDMAT precursor is heated to obtain enough vapor pressure and stability control.[1] Also delivery lines are heated to avoid condensation. In our experiments, we heated delivery lines to 120°C and TDMAT precursor bottle to 75°C.

2.2.4 ALD Window

The temperature range, where the ideal growth mechanism is observed with a constant growth rate, is called ALD window. Outside this window, decomposition of the precursors may occur, resulting in higher growth rates or at lower temperatures, reaction kinetics may cause incomplete saturation of the surface. In addition to temperature, precursor pulse and purge times should also be studied in detail to reach self-limiting growth mechanism.

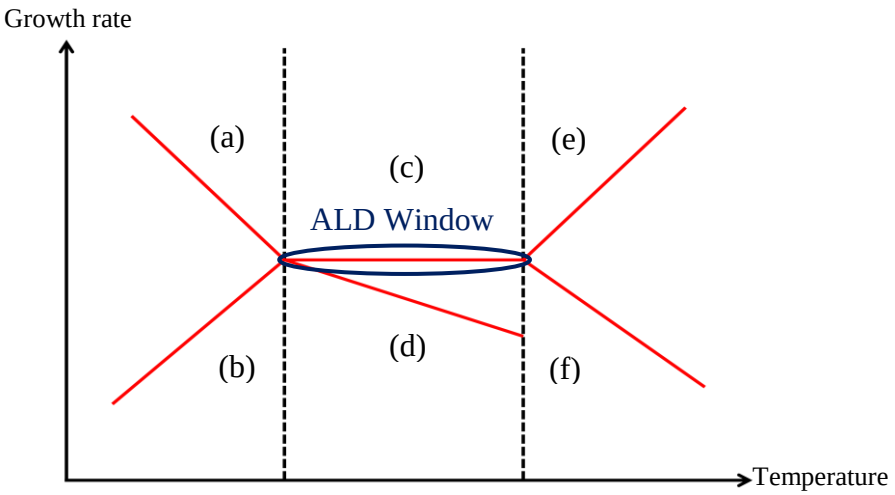


Figure 2.4 Growth rate vs temperature curves

(a) not self limiting, multilayer adsorption or condensation
(b) not self limiting, limited activation energy
(c) self limiting, temperature independent GPC
(d) self limiting, temperature dependent GPC
(e) not self limiting, precursor decomposition
(f) not self limiting, precursor desorption

2.3 Conclusion

ALD is a cyclic chemical vapor deposition technique which is a self-limiting process. Precursors are pulsed to the surface in a cyclic manner to prevent gas phase reactions and control the thickness atomically. With this method, highly conformal and controllable films can be deposited at low temperatures. The need for ALD technique increased due to scaling down device dimensions and increasing aspect ratios. Many materials like oxides, nitrides, fluorides, elements and compounds can be deposited.

Chapter 3

Thin Film Transistor Basics

3.1 MOS Structure

In order to understand physics behind MOSFET operation, basic MOS structure should be analyzed. Fig. 3.1 shows energy band diagrams of MOS structures under different conditions.

q$\varphi_m$is the energy difference between Fermi level of the metal and conduction band of the oxide. qφ_s is the work function at the semiconductor-oxide interface. q$\varphi_F$is the energy difference between Fermi level and intrinsic level of the semiconductor.

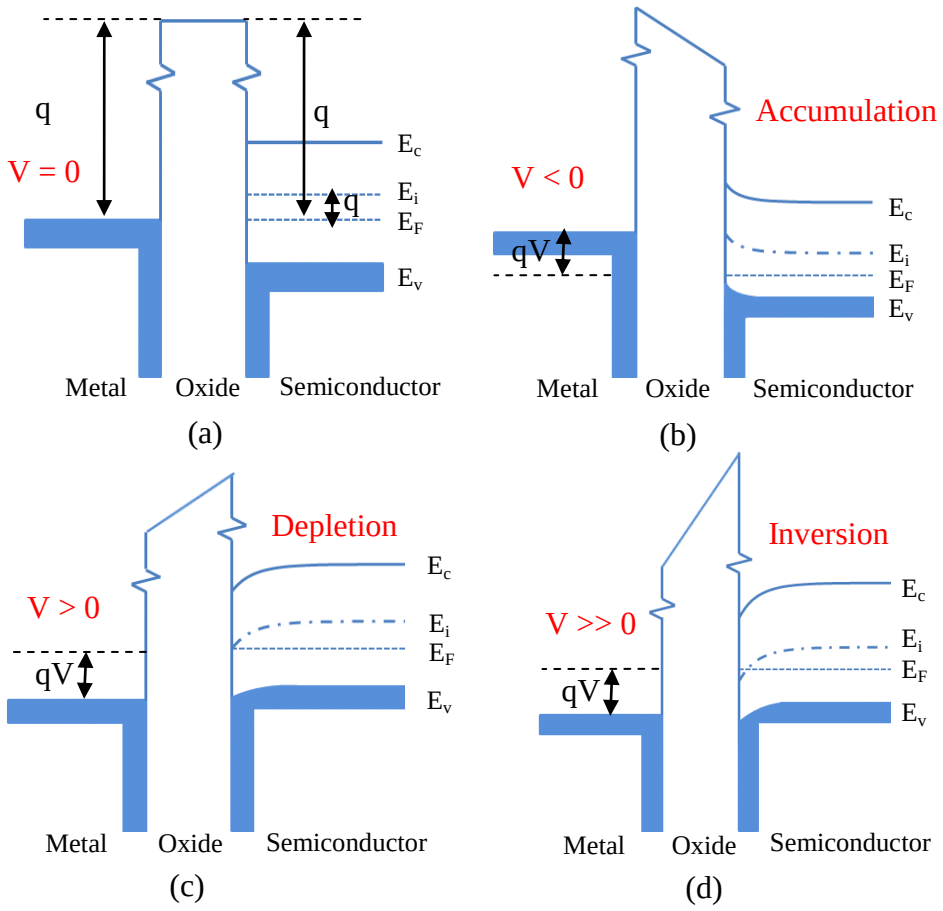


Figure 3.1 Energy band diagrams of MOS structure

When a voltage is applied from the metal side, an equal and opposite signed charge accumulates at the metal-oxide and semiconductor-oxide interfaces (positive charge accumulates at the semiconductor-oxide interface for negative applied voltage at the metal). The applied negative voltage increases the electron energies in the metal relative to the semiconductor. Difference between the Fermi level of metal and semiconductor under negative bias is given by qV, where V is the applied voltage. Since $\varphi_m$and φ_s do not change with applied voltage, oxide band starts to bend. Also the energy bands of the semiconductor region bend near the interface, since hole concentration increases, according to the formula

$$p = n_i e^{(E_i - E_F)/kT} \tag{3.1}$$

$E_i - E_F$ increases. (See Fig. 3.1 (b)) Therefore, this state is named as accumulation, as the number of holes is now larger compared to the equilibrium state.

In the case of positive applied voltages, the story becomes reversed. When a positive voltage is applied from the metal side, negative charges accumulates at the semiconductor-oxide interface. Since φ_m and φ_s do not change with applied voltage, oxide band again starts to bend but in the reverse direction. The difference $E_i - E_F$ decreases which indicates a decreasing hole concentration at the interface (See Fig. 3.1 (c)). This is called the depletion state when the interface is depleted of charge carriers.

If positive voltage bias is increased further, E_i becomes smaller than E_F. According to eqn. 3.1, if E_F becomes higher than E_i, electron concentration starts to increase. The charge carriers at the interface change from holes to electrons giving the name for this condition as inversion state. (See Fig. 3.1 (d))

This inversion property is the key of MOS transistor operation. Channel formation in the semiconductor layer is based on the inversion principle.

3.2 Transistor Basics

Consider a current flowing through a slab of semiconductor.

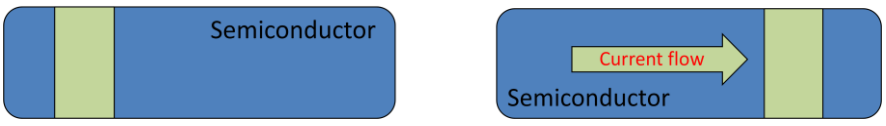


Figure 3.2 Current flowing through the semiconductor slab by the migration of carriers

The amount of current travelling in the semiconductor will be charge density times velocity of the charge, so that we can obtain the famous equation of I = Q / t (Ampere) $A = C/s$,

$$I = \mathrm{Q}_d \left(\frac{C}{m}\right).v\left(\frac{m}{s}\right) \tag{3.2}$$

Consider that three different structures are constructed around this semiconductor bar constructed: gate, source, drain.

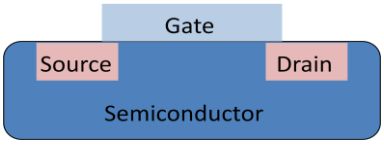


Figure 3.3 Gate, source and drain structures constructed around semiconductor slab

Applying voltage from gate structure we are forcing this semiconductor bar to transport charge from source side to drain side by constructing an inversion layer at the interface between the bar itself and the gate oxide layer. The charge density in the inversion layer can be calculated using the eq. 3.2; but this time charge density equals to

$$Q_d = W.C_{ox}.(V_{GS} - V_{TH}) \tag{3.3}$$

The V_{GS} - V_{TH} expression stands for the requirement of semiconductor bar (channel) to transport charge carriers. The inversion layer onset occurs in the channel when V_{GS} equals to V_{TH}. At gate voltages higher than V_{TH}, any charge placed on gate is mirrored in the channel.

Next think that we have an additional player in the scene: drain voltage. If drain voltage is not 0, channel potential which is 0 at the source side becomes V_D at the drain side. As a result, local voltage difference affecting channel starts to

differ from V_G to $V_G - V_D$. So that, channel charge density at a point x along the channel becomes,

$$Q_d = W.C_{ox}.(V_{GS} - V_x - V_{TH}) \tag{3.4}$$

V_x stands for voltage difference at a specific point x.
As can be calculated from eq. 3.2 and 3.4,

$$I_D = -W.C_{ox}.(V_{GS} - V_x - V_{TH}).v \tag{3.5}$$

v is the velocity of electrons in the channel and is equal to

$$v = \mu.E \tag{3.6}$$

$\boldsymbol{\mu}$ is the mobility of charge carriers and E is the electric field created in the channel. Since,

$$E = -\frac{dV}{dx}, \tag{3.7}$$

$$I_d = W.C_{ox}.(V_{GS} - V_x - V_{TH}).dV/dx \tag{3.8}$$

As mentioned before, voltage difference at the beginning of the channel is 0, and at the end of the channel is V_{DS}; so that,

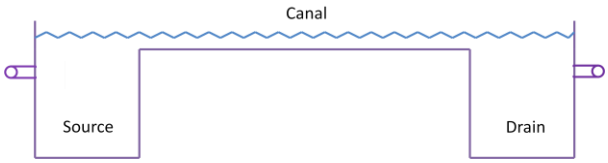
$$\int_0^L I_D.dx = \int_0^{V_{DS}} W.C_{ox}.\mu_n.(V_{GS} - V_x - V_{TH}).dV \tag{3.9}$$

$$I_d = \frac{W}{L}.C_{ox}.\mu_n.[(V_{GS} - V_{TH}).V_{DS} - \frac{1}{2}.V_{DS}^2] \tag{3.10}$$

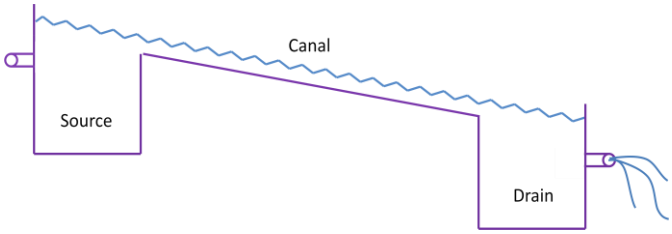
L is the effective channel length.
I_{Dmax} occurs at $V_{DS} = V_{GS} - V_{TH}$,

$$I_{d,max} = \frac{1}{2}.\frac{W}{L}.C_{ox}.\mu_n.(V_{GS} - V_{TH})^2 \tag{3.11}$$

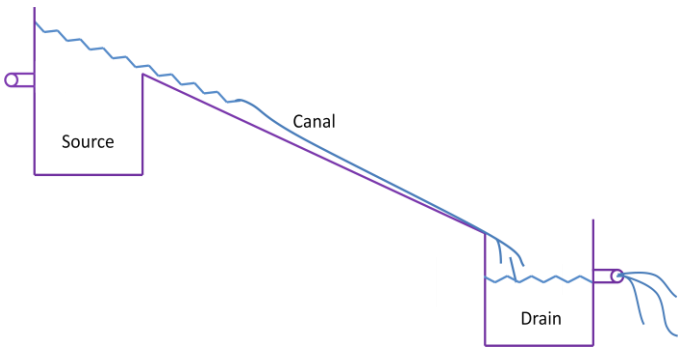
Now let's move to device illustrations and make these I_D and I_{Dmax} expressions meaningful in the practical world. There is a famous water analogy which makes transistor concepts easy to understand. According to the water analogy, mobile carriers can be thought as water droplets. Source and drain are like deep reservoirs and channel is like a canal. When source and drain reservoirs are level, there is no water flow in the canal but when drain reservoir is lower than the source, water starts to flow in the canal, but the flow is limited with the canal capacity; so further lowering of drain reservoir cannot increase the amount of water travelling in the canal.



Source and drain reservoirs, no water flow



Drain reservoir is lower than the source, water flows in the canal



Further lowering of drain reservoir, amount of water travelling in the canal is same as before

Figure 3.4 Water analogy

If the amount of electrons (water droplets) flowing in the channel (canal) is increasing with V_{DS} (drain reservoir lowering), I_D can be calculated by eqn. 3.10; if is not increasing, I_D can be calculated by eqn. 3.11. (See Fig. 3.5)

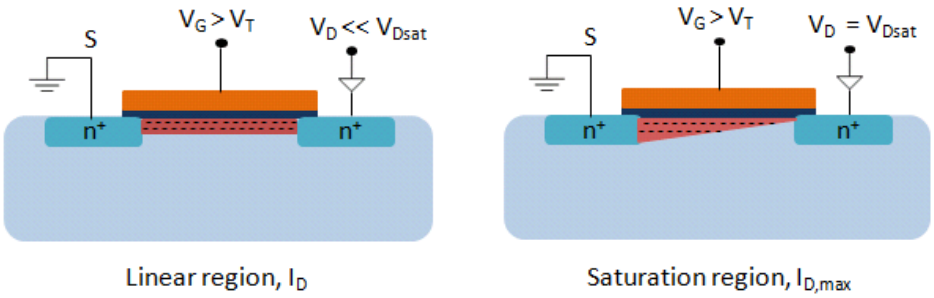


Figure 3.5 Adaptation of water analogy into transistor operation

3.3 Short Channel Effects

There are further considerations for devices with short channel lengths.

Drain Induced Barrier Lowering (DIBL)

DIBL refers to the influence of drain voltage on barrier near the oxide surface at the source end. The density of electrons entering channel layer from source increases exponentially as the barrier to electron flow at the source side of the channel is lowered linearly. In long channel devices, only V_{GS} can lower the barrier but in short channel devices, drain voltage also may reduce the source barrier. (See Fig. 3.6)

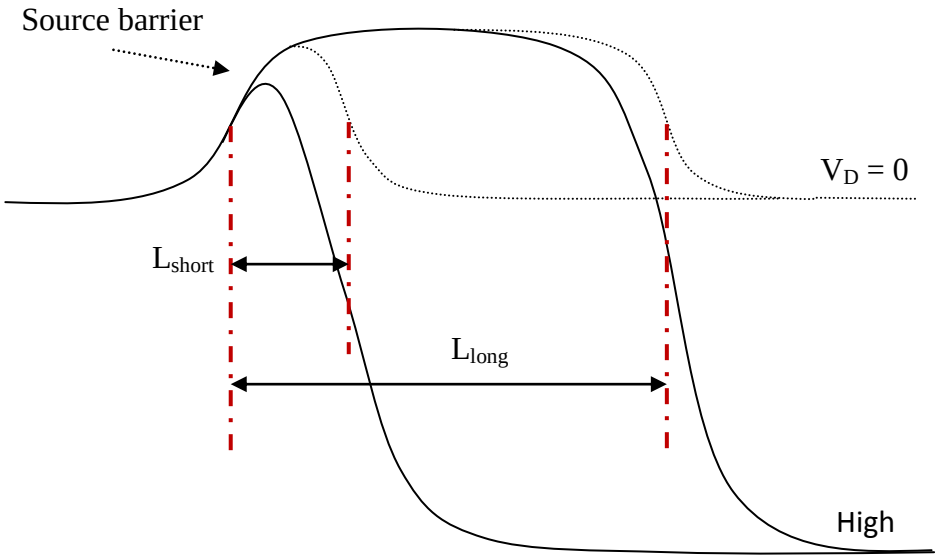


Figure 3.6 Drain Induced Barrier Lowering (DIBL)

Channel Length Modulation

Starting from pinch-off situation (beginning of saturation), as voltage applied from the drain side increases, actual length of the inverted channel decreases. In other words, effective channel length becomes L' which is a function of V_D. This effect is called channel length modulation.

$$L' = L - \Delta L \tag{3.12}$$

$$I_d = \frac{1}{2}.\frac{W}{L}.C_{ox}.\mu_n.(V_{GS} - V_{TH})^2.(1 + \lambda V_{DS}) \tag{3.13}$$

where λ is the channel-length modulation coefficient. This effect also causes a nonzero slope in the I_D/V_D characteristics.

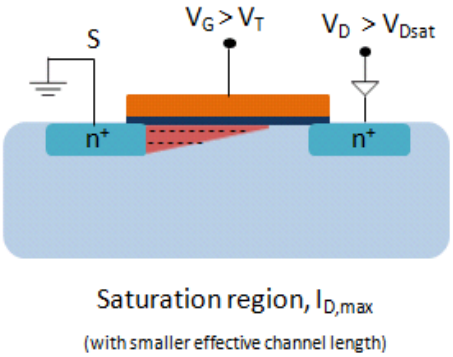


Figure 3.7 Effect of channel length modulation

Drain Current Saturation

There is a limitation caused by carrier-velocity relationship. Drain current is expected to saturate when electrons reach at the drain side with their velocity v_{sat}. In the long channel theory, saturated drain current does not change with further increase in drain voltage while in short channel theory, drain current continues to change with drain voltage in saturation region.

Mobility Degradation

The electrons forming channel layer are scattered by collisions at the interface, with charged acceptor sites and thermal phonons. As expected, these collisions degrade the mobility of electrons. Although mobility degradation affects long-channel devices, it is a more serious limitation in short channel devices.

3.4 Conclusion

In this chapter, the basic principles of transistor operation are shown. The current – voltage characteristics are defined in two regions: linear region and saturation region. The characteristic behavior of devices in these regions are tried to be explained using water analogy. In linear region, current level increases with the increase in drain lowering. On the other hand, since the drain current is limited with channel capacity, further increase in drain lowering (drain voltage) cannot change drain current.

Long channel devices and short channel devices differ in characteristics since at short channel length devices, second order effects like channel length modulation and DIBL become significant.

Chapter 4

ZnO-Based Thin Film Transistors and Effect of Growth Temperature on Performance Characteristics

4.1 Introduction

Functional metal oxides like ZnO are promising materials for technological developments in transparent electronics like field effect transistors and technologies based on transistors like transparent flat panel displays.[26-28] In addition, simple and low-cost processing technology and compatibility with inexpensive substrates like glass make such materials attractive.[29] There is a wide literature on ZnO channel TFT's deposited with different methods like physical vapor deposition, chemical vapor deposition, chemical solution deposition, molecular beam epitaxy and atomic layer deposition.[26, 27] In this thesis, atomic layer deposition is used as the main deposition technique for ZnO.

Table 4.1 compares electrical device characteristics of ZnO-channel TFTs from previous works in the literature fabricated by a number of different methods.

Reference No	**Subthreshold Slope (V/dec)**	**Threshold Voltage (V)**	**I_{on}/I_{off} Ratio**	**Mobility ($cm^2/V.s$)**
27	-	1.8	10^7	1
28	1.24	21	$2x10^5$	20
29	-	10 – 20	10^7	0.3 – 2.5
30 (70°C)	4.19	14.7	$3.63x10^4$	6.435
30 (90°C)	1.21	13.1	$2.43x10^6$	16.13
30 (110°C)	24.1	-12.5	1.13x10	56.43
30 (130°C)	-	-	1.28	152.5
31	-	20	$4.05x10^4$	0.56
32	0.67	4.1	$9.5x10^7$	6.7
33	0.68	1.8	$5x10^5$	70
34	0.95	4.3	10^7	>8
35	1.02	6.9	$>10^4$	20.65
36	-	9	$>10^5$	31
37	1.39	19	$3x10^5$	27
38	-	-	$>10^5$	0.031
38	-	-	$>10^2$	0.97
39	0.82	-0.1	$2x10^6$	14.9
40	0.25	1.2	$1.5x10^8$	2.3

Table 4.1 Characteristics of different ZnO-channel TFT's

4.2 Device Fabrication

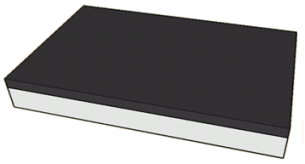
Two different device designs are used in ZnO-channel TFT device preparation:

1. Patterned gate architecture
2. Blanket bottom gate architecture

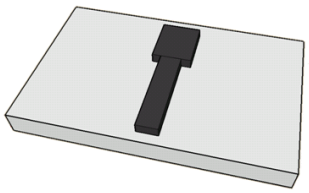
Substrates are cleaned using H_2SO_4 : H_2O_2 solution for 5 min. After the chemical cleaning, a short solvent cleaning is done including acetone, isopropanol and DI water rinsing steps.

The masks are designed using Layout Editor (GNU GPL) software and produced by the mask writer equipment (Heidelberg Instruments DWL-66) in UNAM clean room facilities (UCF).

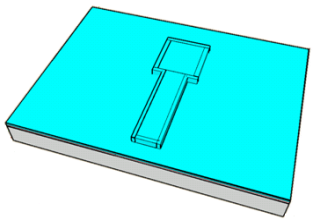
Fabrication process,



Thermal evaporation of 100-nm-thick Al layer for creating gate contact pads of devices.



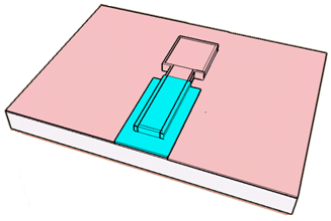
After the photolithography process, Al layer is etched using Aluminum Etchant Type A (contains 80wt% Phosphoric Acid, 5%, Nitric Acid, 5% Acetic Acid, and 10% Distilled Water).



20-nm-thick Al_2O_3 gate oxide layer and 14-nm-thick ZnO are deposited with atomic layer deposition technique. The growth temperatures of Al_2O_3 and ZnO films are both 200°C.

For ALD deposition, Cambridge Nanotech Inc., Savannah 100 system is used. Precursors used are diethyl-zinc (DEZ) (purchased from Sigma Aldrich Chemical Co.) and milliQ water (H_2O). Nitrogen is used as the carrier gas with the flow rate of 20 sccm. To avoid precursor condensation, valves and delivery lines are kept at 120°C.

The processing cycle consists of a 0.015 s DEZ pulse, 10 s for purging, 0.015 s H_2O pulse and 10 s for purging. The deposition rate of ZnO is found to be 1.4°A/per at 200°C.

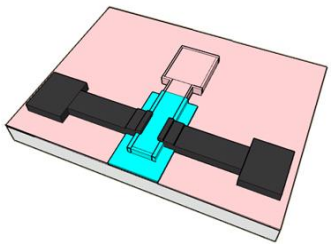


ZnO layer is etched with Ar plasma in an inductively coupled plasma (ICP) system for 2 min.

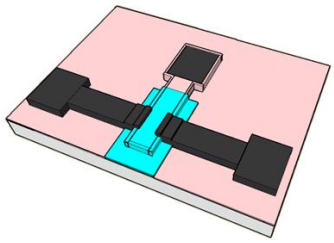
Ar plasma etch hardens photoresist which is used as hard mask for subsequent dry etching. Hardened photoresist cannot be removed from the substrate by only acetone rinsing; therefore, O_2 plasma treatment is applied for 1 h using Asher system or 20 min using ICP system.

In an alternative process, dry etching of ZnO is replaced with a wet etching procedure using H_2SO_4 : H_2O (2:98).

The etching step is performed using a separate channel mask (or using the gate mask for some devices). See Fig. 4.2 and 4.3 for optical images of mask sets.



100-nm-thick Al layer is thermally evaporated and patterned by lift-off technique to form source and drain contacts.

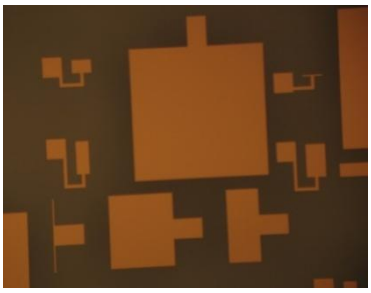


Gate oxide layer is etched from the gate pad surface in order to take electrical contacts.

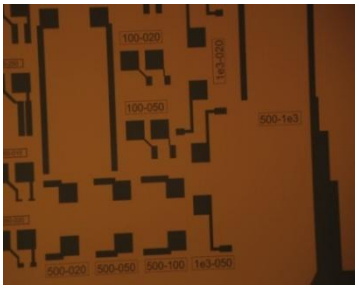
Actually, this step does not have to be the final step, it can be performed also after ZnO etch but in order to reduce the contamination, we preferred etching after completely forming the active area.

Since glass substrates pose a contamination risk in ALD equipment at high temperatures (>150C) we used quartz as an alternative substrate and deposited both Al_2O_3 and ZnO layers at 250°C.

Various size channel length and width devices are fabricated. Fig. 4.4 illustrates overall device fabrication.



Gate mask

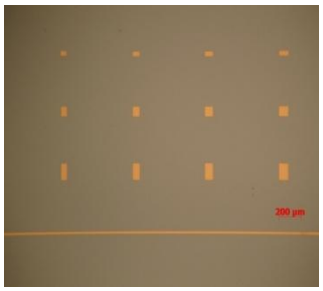


Source/Drain mask

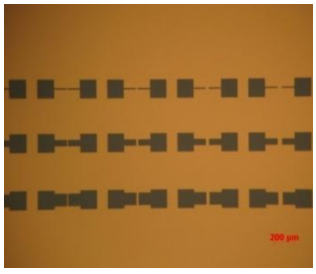
Oxide etch patterning for gate pads

Figure 4.1 Mask set without a channel mask.

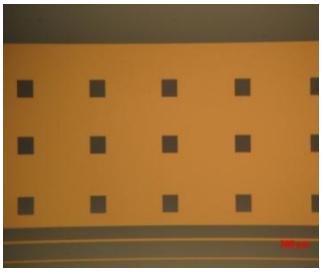
Gate mask



Channel mask



Source/Drain mask



Oxide etch mask for gate pads

Figure 4.2 Mask set including a separate channel mask.

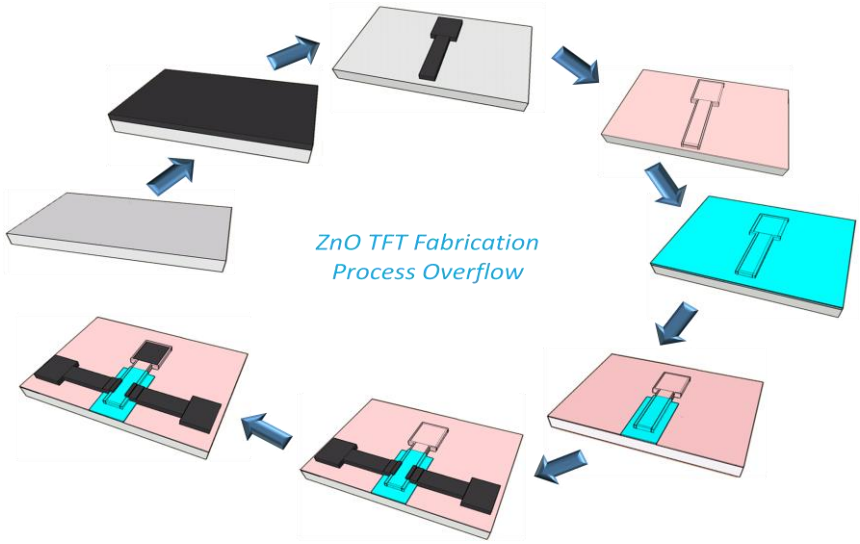
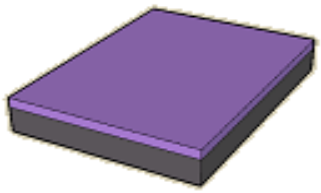
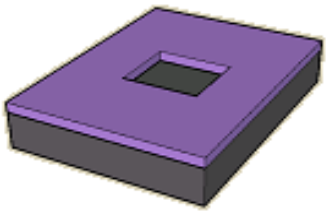


Figure 4.3 ZnO-channel TFT device fabrication with patterned gate device architecture

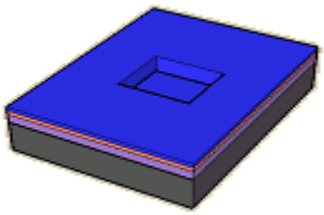
Blanket bottom gate fabrication design starts with chemical cleaning of highly doped (0.010-0.018 ohm-cm) p-type (111) Si wafer. Si substrates are cleaned using H_2SO_4 : H_2O_2 solution for 5 min and buffered oxide etch (BOE) solution for 5 min.



210-nm-thick PECVD SiO_2 layer is deposited for isolating devices from each other.



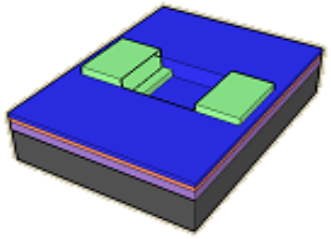
Gate areas are created in the SiO_2 layer by photolithography and wet etching using BOE solution.



20-nm-thick Al_2O_3 and 10-nm-thick ZnO layers are deposited with ALD system and ZnO layer is etched with H_2SO_4 : H_2O (2:98) solution for 2 s.

The growth temperature of both Al_2O_3 and ZnO layers is 250°C. The ALD steps are performed consecutively. The reason for this integrated deposition step is to reduce interface traps by depositing the channel immediately after the gate oxide without breaking the vacuum.

The processing cycle consists of 0.015 s DEZ pulse, 5 s for purging, 0.015 s H_2O pulse and 5 s for purging.



80-nm-thick Al is deposited for electrical pads.

Blanket bottom gate fabrication process flow is shown in Fig. 4.5.

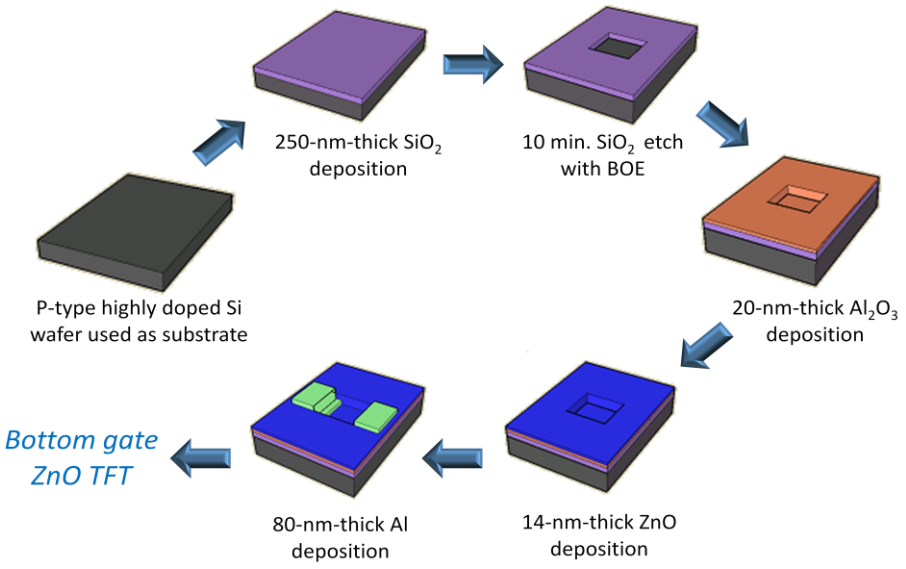
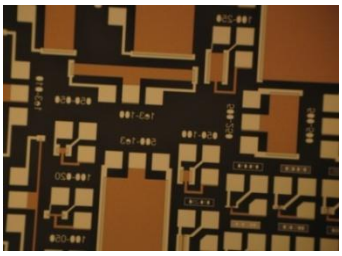
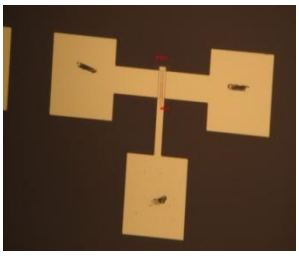


Figure 4.4 ZnO-channel TFT device fabrication process flow for blanket bottom gate design

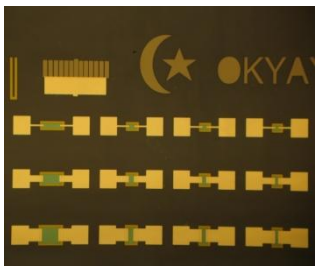
The blanket-bottom-gate architecture uses the substrate as the gate electrode, therefore, can be realized with lesser process steps compared to patterned gate architecture.

Patterned gate design, mask set with no channel mask





Patterned gate design, mask set including channel mask



Blanket bottom gate design, blanket bottom gate mask set

Figure 4.5 Optical microscope images of devices fabricated with two different fabrication designs and three different mask sets.

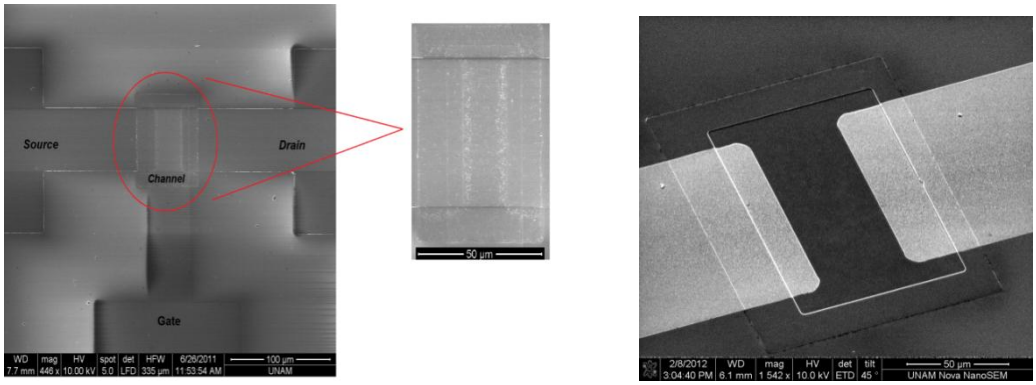


Figure 4.6 SEM images of some completed devices

4.3 Results and Discussion

4.3.1 ZnO Material Characterization

The surface chemical composition of the ZnO films are analyzed by X-ray photoelectron spectroscopy (XPS) measurements, performed at a vacuum level of $3x10^{-9}$ Torr (K-Alpha - Monochromated high-performance XPS spectrometer) instrument.

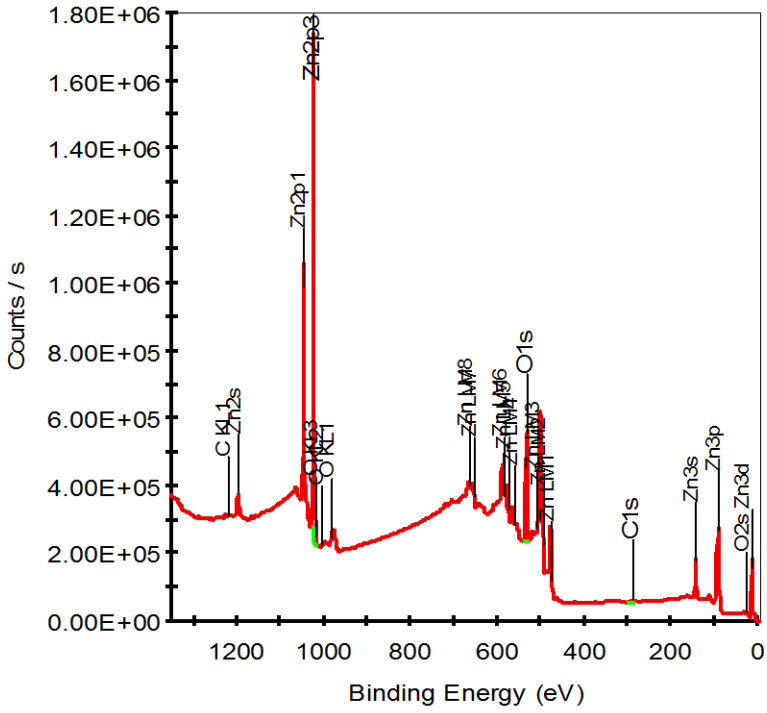


Figure 4.7 Wide scan survey XPS spectrum of ZnO thin film.

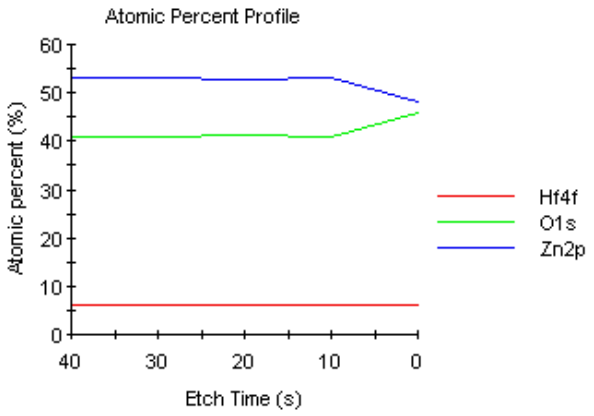


Figure 4.8 Atomic percentage values of elements that ALD ZnO film contains

According to the results obtained by XPS measurements, it is clear that the film contains Zn interstitials and O vacancies. The atomic percentage ratios show that Zn/O rate is not equal to 1, as supposed to be in a stoichiometric ZnO film. These results show that we have Zn interstitials and oxygen vacancies which act as shallow donors in the film.

Grains can be clearly seen in the TEM image of a stack composed of consecutive Al_2O_3, ZnO layers. The existence of grains in ZnO films shows that as-deposited ALD ZnO films are polycrystalline. (See Fig. 4.10)

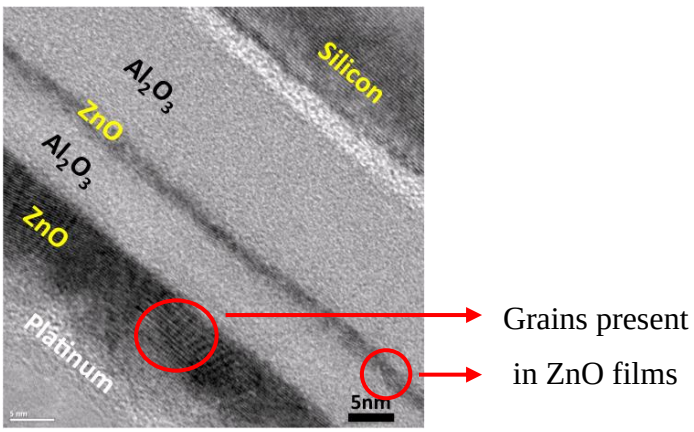


Figure 4.9 TEM image of a stack composed of : Al_2O_3 and ZnO layers one after the other.

4.3.2 Device Characterization

4.3.2.1 ZnO TFT Characterization

Charge traps in ZnO channel, dielectric and the interface between ZnO channel-dielectric layers are very important for operational stability and reliability of device characteristics. Accordingly, dielectric layer should be chosen carefully in ZnO TFT's since charges trapped in oxide or oxide-semiconductor interface may lead to threshold voltage shifts, oxide leakage currents and even oxide breakdown.[41, 42]

Interface trapped charges and oxide trapped charges may be formed in following regions,

- Between channel surface and gate oxide layer
- Extra states on the surface due to one-sided crystal structure (dangling bonds)
- Crystal defects
- Defects created by impurities like bonded foreign atoms at the surface[23]

Also there may be hot carrier stress generated oxide traps. When an electron traveling through the channel gains kinetic energy at the pinch-off region due to high electrostatic potential energy, it becomes a hot electron. At the conduction band, due to the increase in its kinetic energy, it exceeds the potential barrier between oxide and semiconductor and gets injected into the oxide layer. Then it may either be collected as gate current or be trapped in the oxide and changes the threshold voltage.[25]

In our work, we choose 20 nm Al_2O_3 ALD-deposited dielectric layer since as this produced the lowest traps, possibly due to less extra energy states at the oxide – semiconductor interface compared with other high-k dielectrics like HfO_2.[42]

In order to observe the charge trapping behavior of devices, multiple measurement techniques can be used like I–V, C-V, charge pumping and other measurements.[43, 44] We chose I-V measurement to test our oxide layers' charge trapping behavior. Bidirectional sweep is applied and the hysteresis effects are examined with a parameter analyzer (Keithley 4200-SCS) and a manual probe station Cascade PM-5.

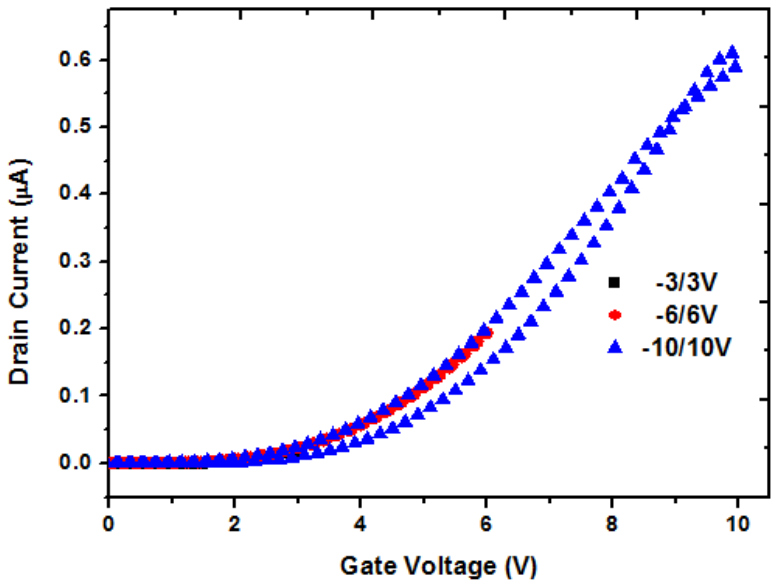


Figure 4.10 Hysteresis characteristics of ZnO TFT's

As Fig. 4.11 shows, ZnO TFT's fabricated with Al_2O_3 dielectric layer have acceptable hysteresis characteristics when compared with the ones shown in literature before. (See Ref. 45, 46, 47)

Fig. 4.12 shows typical I_D - V_D characteristics and Fig. 4.12 shows transfer characteristics of devices fabricated with the patterned gate design.

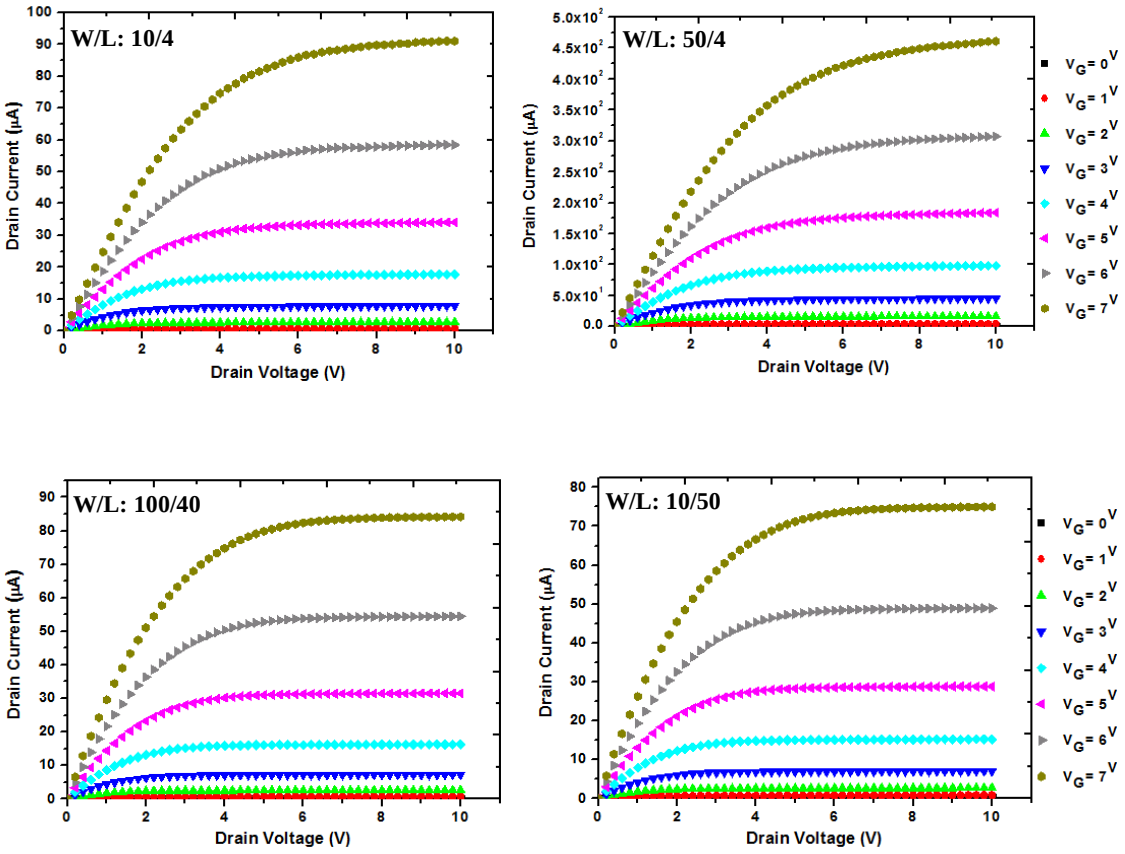


Figure 4.11 I_D - V_D characteristics of devices with various W/L ratios.

Results show that devices exhibit n-type field effect transistor behavior since drain current increases with increasing gate voltage.

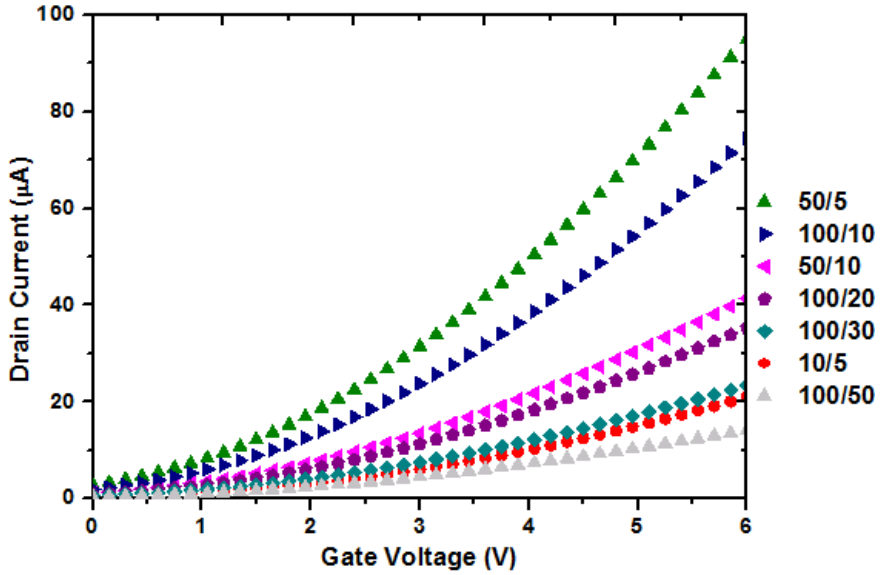


Figure 4.12 Transfer characteristics of devices having several W/L ratios.

Drain current is directly proportional to the channel W/L ratio in long channel devices, as expected in eqn. 3.9 and 3.10. On the other hand, for short channel devices, even if the W/L ratios are equal to each other, drain current levels are different.

Channel W/L Ratio	Drain Current(μA)
50/5	94.52
100/10	74.48
50/10	41.41
100/20	34.73
10/5	21.07
100/50	13.7
100/30	23.61

Table 4.2 Drain current values belong to devices with different channel W/L ratios

As results show numerically, ratio between current levels of long channel devices having the same channel width is almost same with the ratio of their channel lengths.

In order to observe the scaling behavior more clear see Fig. 4.14.

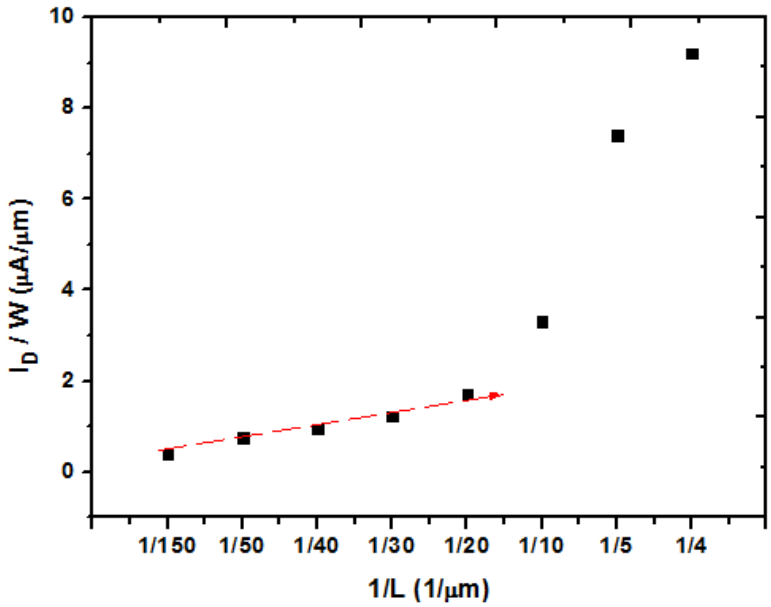


Figure 4.13 Scaling behavior of ZnO TFT's.

This graph explicitly shows that in long channel devices drain current increases linearly with channel W/L ratio.

Scaling behavior of ZnO TFT's are examined previously and it is observed that short channel effects such as reduced threshold voltages, degradation of subthreshold slope and loss of hard saturation, arise for channel lengths typically shorter than 5 μm.[34] For our devices, these effects become observable for channel lengths smaller than 10 μm which is acceptable compared to reports in literature.

One possible reason of this nonlinear behavior in current level is the channel length modulation effect observed in short channel devices. As explained in chapter 3, channel length modulation is the effect that is caused by the difference between gate and drain voltages. As this potential difference increases, effective channel length becomes smaller. Therefore, in short channel devices, the W/L ratio becomes W/L' which has a higher value due to the

decrease in effective electrical length of the channel, resulting with higher drain currents.[24]

This effect can also be observed by looking at the change in threshold voltage value with respect to channel length.

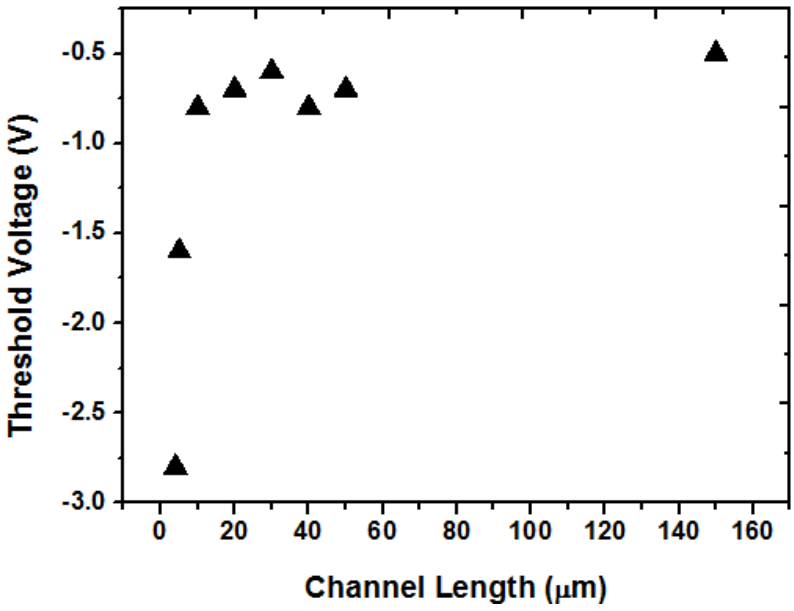


Figure 4.14 V_{th} change with respect to channel length

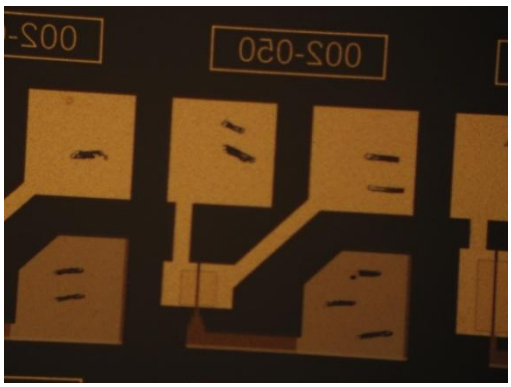
Fig. 4.15 shows that for short channel devices, threshold voltage value decreases. There are two reasons explaining this effect: channel length modulation and drain induced barrier lowering. In short channel devices, V_{Th} depends on both L and V_D.

$$\Delta V_{TH} = -\frac{q.N_A.W_{DM}}{C_{ox}}\left(1-\frac{L+L'}{2L}\right) \quad (4.1)$$

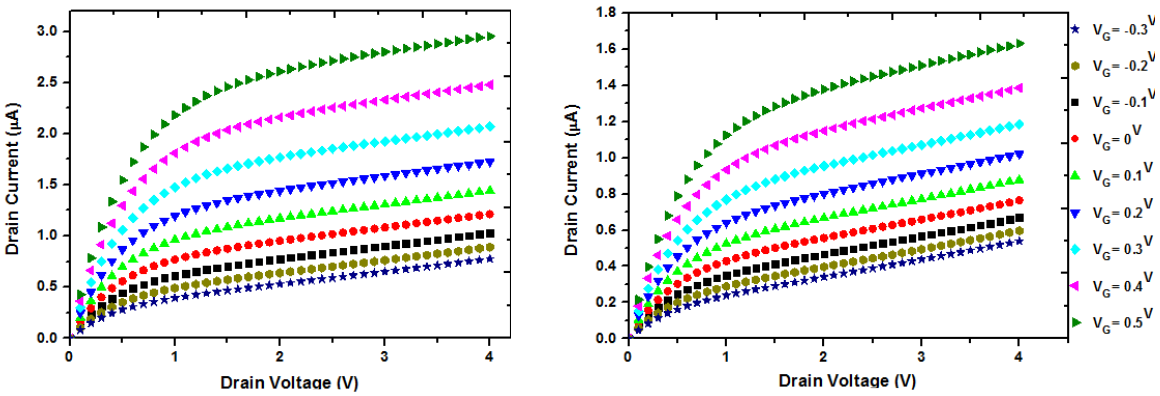
As L' decreases, the value of ΔV_{Th} increases and V_{Th} decreases.[1]

As a result of DIBL, as the voltage applied from drain side increases, due to large band bending, barrier at the source end gets lowered and barrier height becomes dependent on V_D in addition to V_G.[23]

The final effect that is observed during measurements is also caused by channel length modulation: finite saturation region slope. The effect is caused by the change in effective channel length with increasing drain voltage as explained before. (See Fig. 4.16)



(a)



(b) (c)

Figure 4.15 (a) Optical microscope image of a device having channel length of 2μm and channel width of 50μm, (b) I_D-V_D characteristics of a device having channel length of 2 μm and channel width of 100μm, (c) I_D-V_D characteristics of the device shown in (a).

4.3.2.2 Effect of growth temperature on ZnO TFT characteristics

For ZnO thin films grown by ALD technique, growth temperature is very important since it changes the doping concentration of the material due impurity atoms and ratio of Zn:O atoms. At higher growth temperatures, oxygen vacancies, zinc interstitials and hydrogen incorporation causes high effective doping concentration and therefore high conductivity. On the other hand, below 130°C carrier concentration decreases and current flowing through the channel becomes more controllable by the gate.[27]

Role of Impurity Atoms in ZnO Films

- Hydrogen acts to increase the conductivity of ZnO films since it behaves like a shallow donor. Doping concentration of ZnO films can be controlled by careful control of hydrogen concentration in the film. Typically H content of the film decreases with increasing growth temperature.[45]

- At lower growth temperatures, water molecules may be trapped in ZnO film or un-reacted OH groups may bind to the surface resulting with traps which lower electron mobility. These OH groups prevent oxygen vacancies which otherwise act as donors in ZnO films.[27] In other words, as growth temperature increases, O/Zn ratio in the film decreases which results in higher effective doping. This can be attributed to residual O-H bonds in the ZnO film which can easily be replaced with oxygen vacancy. Films deposited at low temperature contain more O-H bonds than that of high temperature since reactions go to completion at high temperatures and O-H bonds switch to oxygen vacancies. As a result, high O-H concentration means high O/Zn ratio which results with less doping concentration.[30]

- Rapid thermal annealing (RTA) of ZnO films at O_2 environment at 600-800°C improves crystallinity as well as electrical characteristics due to increasing O/Zn ratio in the film.[29]

- N_2 behaves like a dopant for ZnO films, too. On the contrary to hydrogen, N_2 acts like a shallow acceptor.[48] Results show that ZnO:N films have lower effective doping concentrations resulting in better TFT performance. In order to controllably dope ZnO films with N_2 in an ALD system, ammonium hydroxide can be used.[44] We observed the effect of annealing the film in N_2 + H_2 environment. Results showed that after annealing, doping concentration in the film is reduced. Our hypothesis is that although hydrogen acts as a shallow donor, N_2 existence in the film compensates the effect of hydrogen and reduces overall doping concentration of the film.

Results and Discussion

We fabricated blanket back gate TFT devices. The growth temperatures and ALD recipes used are as follows,

Growth Temperature	DEZ pulse	Purge Time	Water pulse	Purge Time
80°C	0.015 s	60 s	0.015 s	60 s
100°C	0.015 s	60 s	0.015 s	60 s
120°C	0.015 s	60 s	0.015 s	60 s
130°C	0.015 s	60 s	0.015 s	60 s
250°C	0.015 s	5 s	0.015 s	5 s

Table 4.3 ALD recipes used for several growth temperatures

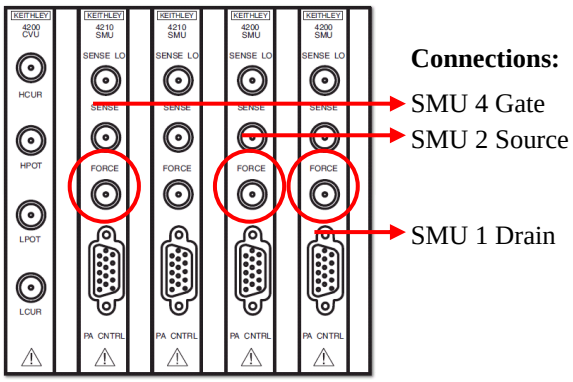
Precursor delivery times and purging times are used same for all low temperature depositions in order not to spend additional effort for optimizing

recipes according to deposition mechanisms at different temperatures. The recipe used for deposition at 80°C is commercially provided by the equipment vendor, so we use it as a starting point. As a result, using the purge times of 80°C for temperatures higher than 80°C is a time consuming but safe way because with this approach, one can be sure that precursors have sufficient time for interacting with the surface.

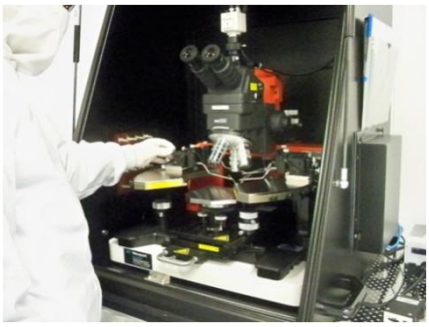
Measurement Setup

Measurements of the devices are performed at UNAM cleanroom facility. A parameter analyzer (Keithley 4200-SCS with 4200-CVU) and a manual probe station (Cascade PM-5) are used for experiments.

(a)



(b)



(c)

Figure 4.16 Measurement setup (a) semiconductor parameter analyzer,[49] (b) parameter analyzer connections,[50] (c) probe station.[49]

I_D - V_G characteristics of devices are shown in Fig. 4.18.

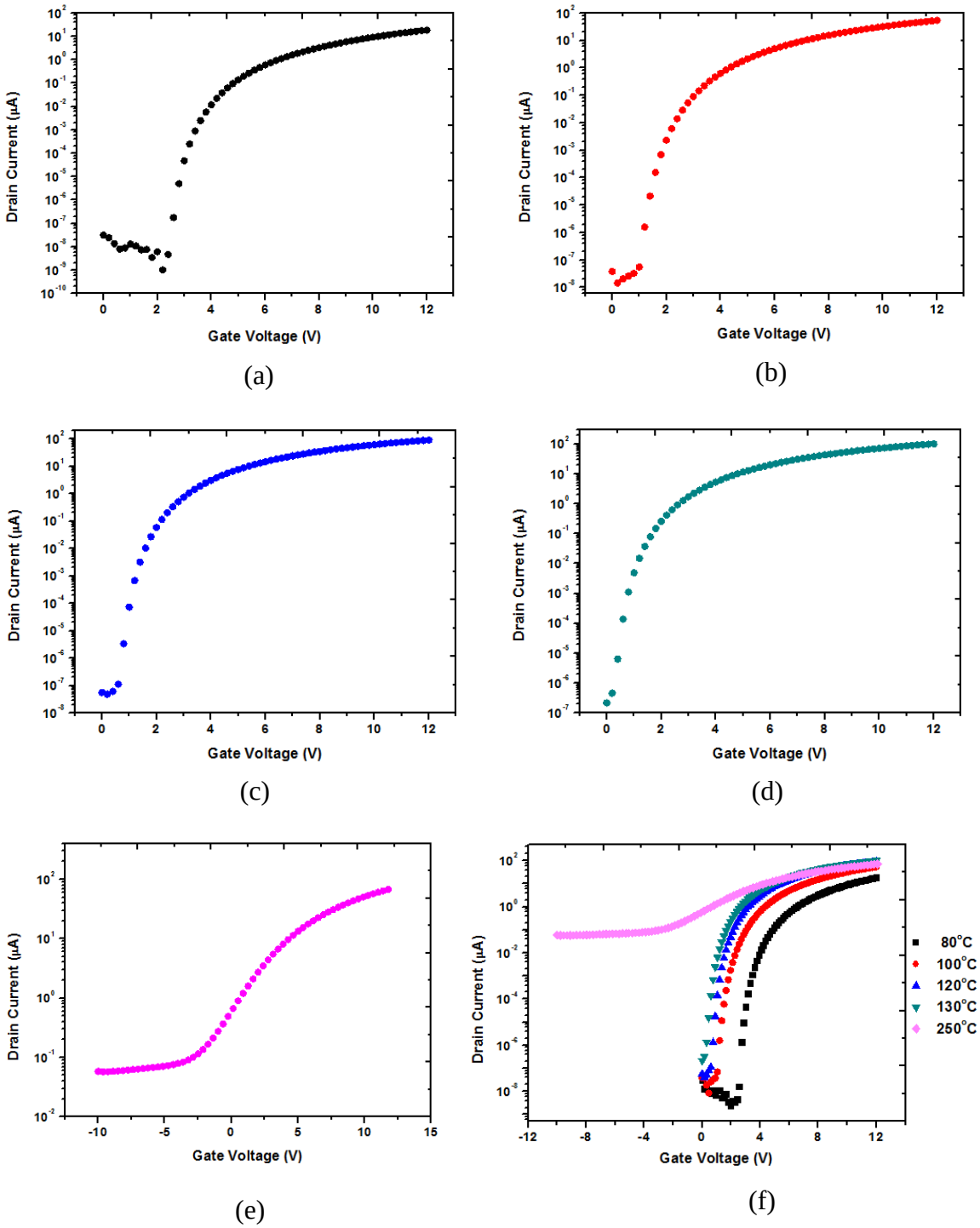


Figure 4.18 I_D - V_G characteristics of devices having ZnO channel grown at (a) 80°C, (b) 100°C, (c) 120°C, (d) 130°C, (e) 250°. In (f) all characteristics are shown together to observe differences more easily.

Table 4.4 shows extracted threshold voltage values, subthreshold slopes, I_{on}/I_{off} ratios and mobility values of devices.

Annealing Temperature (°C)	**Threshold Voltage (V)**	**I_{on}/I_{off} Ratio**	**Subthreshold Slope (V/dec)**	**Mobility ($cm^2/V.s$)**
250	-0.7	10^3	3	23
130	1.58	$4.5x10^8$	0.165	15.91
120	2.09	$1.8x10^9$	0.140	14.9
100	2.8	$2x10^9$	0.170	8.94
80	4.3	$7.8x10^9$	0.116	3.96

Table 4.4 Transistor characteristics changing with growth temperature.

Extrapolation method in the saturation region (ESR) is implemented on measured $\sqrt{I_D} - V_G$ characteristics of devices.[51] The method used for extracting threshold values are shown in Fig. 4.19.

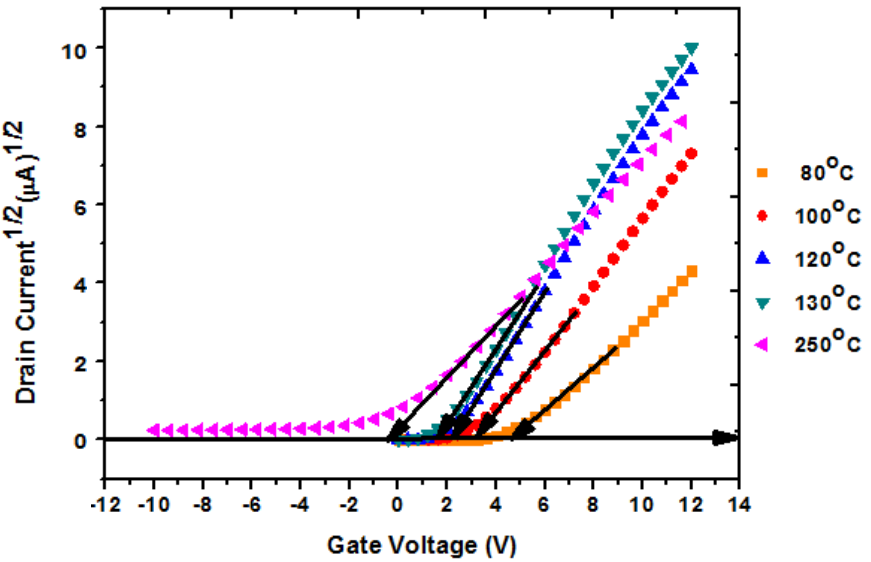


Figure 4.19 ESR method applied to ZnO-channel TFT device measurements

Subthreshold slopes are extracted from $\log(I_D - V_G)$ characteristics of devices using the formula of $dV_G/dLog(I_D)$.[52] Mobility values of devices were calculated using $I_D - V_D$characteristics of devices by the formula given at eqn. 3.10. Every parameter except mobility and oxide capacitance are obtained from measured $I_D - V_D$ characteristics. Oxide capacitance is calculated using the equation,

$$C_{ox} = \varepsilon_{ox}/t_{ox} \tag{4.2}$$

$$C_{ox} = \varepsilon_0.\varepsilon_r/t_{ox} \tag{4.3}$$

Where ε_r denotes dielectric constant of ALD deposited Al_2O_3 (taken as 9 in calculations[53, 54]) With calculated oxide capacitance, there remains no unknown parameter. So, mobility value can be extracted using the formula given at eqn. 3.10.

4.4 Conclusion

Two different device architectures for ALD ZnO-channel TFT fabrication are investigated. For ZnO-channel TFT fabrication, blanket bottom gate design is more preferable since it has one less fabrication step which is etching the dielectric layer from top of the gate pad. Results show that growth temperature affects the doping concentration of ZnO films. As growth temperature increases, doping concentration increases too. Devices fabricated at 80°C show best performance values in terms of I_{on}/I_{off} ratios and subthreshold slopes. On the other hand, TFT's with ZnO layers grown at 250°C have far less I_{on}/I_{off} ratio due to high carrier concentration and therefore, less gate control over the channel layer.

Short channels effects, like channel length modulation and drain induced barrier lowering, are observed for devices with channel lengths smaller than 10μm.

In our work, we used diethylzinc and H_2O vapor as precursors for ALD ZnO deposition. In the literature, it is stated that O_3 instead of H_2O results in improved material properties. Also it is observed that plasma enhanced ALD gives better results since plasma activated reactant species make chemical reactions easier. Moreover remote plasma PEALD is much better since plasma damage is minimized.[1] These two methods can also be tested and effects on device characteristics may be compared with the ones already achieved as a future work.

Chapter 5

TiO_2-Based Bottom Gate Thin Film Transistors

5.1 Introduction

TiO_2 is a very attractive semiconductor owing to its wide bandgap and functional optical properties such as transparency and photocatalytic activity. Such properties make TiO_2 an important material for dye sensitized solar cells (DSSCs) and functional coatings. Adjustable doping concentration property of TiO_2 thin films is very interesting in terms of electronic applications. Undoped TiO_2 has a very high dielectric constant (~100) and behaves like an insulator; on the other hand, doped TiO_2 behaves like a wide-bandgap semiconductor.[55] As a result, flexible and transparent TFT's can be built using TiO_2 either as the dielectric layer or as the channel layer according to its doping concentration.[56]

As we preferred in our experiments, ALD technique can be chosen for TiO_2 channel layer deposition of transparent flexible TFT fabrication. In this case, the

flexible substrate should be chosen carefully, it should be durable under high temperatures because ALD TiO_2 films are generally amorphous as deposited, so they should be annealed to obtain crystalline and semiconducting TiO_2 films.[56, 57]

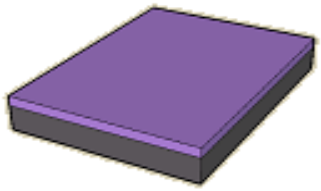
Transistor characteristics based on TiO_2 channel layers are shown in Table 5.1.

Reference No	**Phase of TiO_2 film**	**Threshold Voltage (V)**	**I_{on}/I_{off}**	**μ_{sat} ($cm^2/V.s$)**
57	Amorphous	3.8	10^3	0.087
	Anatase	2.3	10^4	10.7
58	-	7.5	$1.45x10^2$	0.03
59	Single crystal rutile	-	10^4	10.7
60	-	-8.5	$2x10^2$	3.2
	After N_2O treatment	7.4	$4.7x10^5$	1.64
61	Anatase	-	10^5	0.3
62	Amorphous	-4.05	$2.7x10^5$	0.063

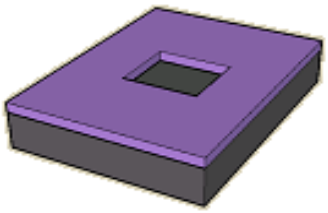
Table 5.1 TiO_2-channel TFT characteristics reported in the literature

5.2 Device Fabrication

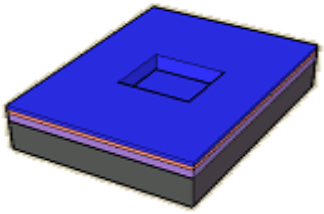
Devices are fabricated on highly doped (0.010-0.018 ohm-cm) p-type (111) Si wafer. Blanket bottom gate fabrication design is used for TiO_2 TFT devices. Fabrication process starts with chemical cleaning of highly doped (0.010-0.018 ohm-cm) p-type (111) Si wafer. Si substrates are cleaned using H_2SO_4 : H_2O_2 solution for 5 min and buffered oxide etch (BOE) solution for 5 min.



210-nm-thick PECVD SiO_2 layer is deposited for isolating devices from each other.



Gate areas are created in the SiO_2 layer by photolithography and wet etching using BOE solution.



30-nm-thick Al_2O_3 and 18-nm-thick TiO_2 layers are deposited with ALD system.

ALD is performed using the Cambridge Nanotech Inc., Savannah 100 system. The precursors used in the experiments are tetrakis(dimethylamido)titanium(IV) (TDMAT) and milliQ water (H_2O). TDMAT (99.999%) is purchased from Sigma Aldrich Chemical Co. The TDMAT precursor is kept at 75°C. Nitrogen is used as the carrier gas with the flow rate of 20 sccm. The deposition temperature of TiO_2 and Al_2O_3 layers are 150°C and 250°C respectively.

The processing cycle consists of a 0.1 s TDMAT pulse, 1 min for purging, 0.015 s H_2O pulse and 1 min for purging. The deposition rate of 0.4 Å/per cycle is extracted.

After TiO_2 deposition, devices are annealed at different temperatures (250°C, 300°C, 330°C, 475°C, 550°C, 600°C) for 1 h in air environment. Annealing temperatures are selected according to Differential Scanning Calorimetry (DSC) results (See Fig. 5.1).

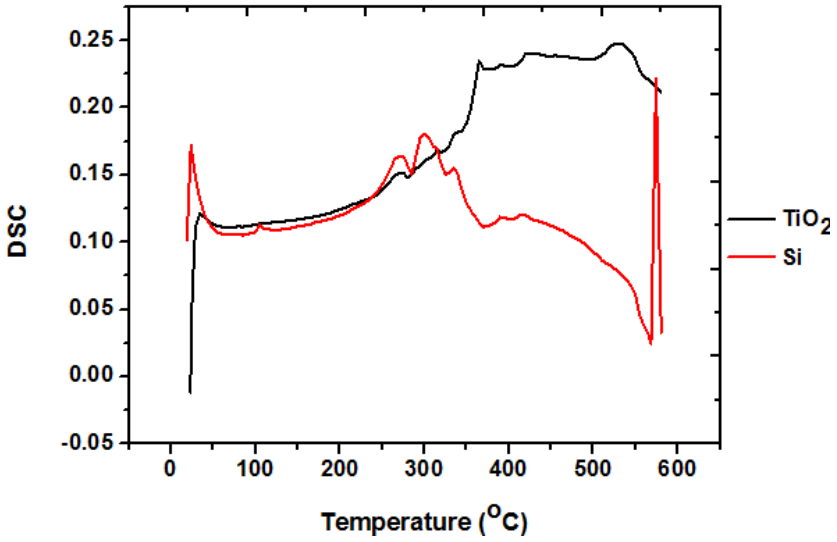
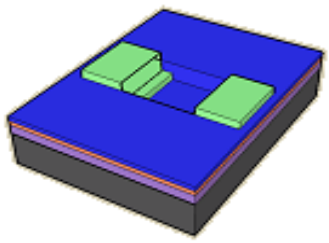


Figure 5.1 DSC measurements of 150°C-ALD-deposited TiO_2 films showing possible phase formations with respect to temperature change



80-nm-thick Al layer is thermally evaporated and patterned by lift-off technique to form source and drain contacts.

Devices with various channel length and size are fabricated.

Fig. 5.2 shows overall device fabrication.

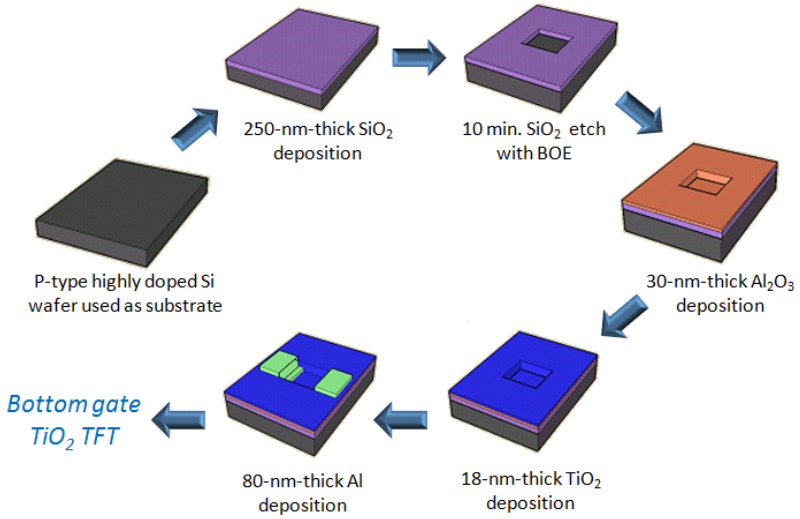


Figure 5.2 Blanket bottom gate design for TiO_2 device fabrication.

5.3 TiO_2 Material Characterization

Material properties of TiO_2

- Material properties of TiO_2 films are strongly dependent on their phase. There are several natural polymorphs of titanium including anatase, rutile and brookite forms.[56] Rutile is the most stable form of TiO_2; on the other hand, anatase is a meta-stable form which transforms to rutile with heat treatment.[55, 63] Usually anatase-rutile transformation occurs at temperatures below 600°C, but this transition depends on factors like defects and impurities in the film.

- Analysis on TiO_2 thin films showed that anatase inclusions occur in the amorphous film which develop into crystalline phase by additional treatments like annealing. XRD analyses are used to confirm the above which show amorphous as-deposited phase with anatase inclusions

transforms into a non-oriented anatase form when annealed at 300°C. (See Ref. 2, 4.)

In our work, we analyzed the effect of annealing temperature on the ratio of mixed phases existing in the film. For this purpose, XRD and XPS measurements are performed. The phase structures of samples are identified using a Pananalytical (X'pert Pro MPD) XRD instrument. The surface chemical composition of the TiO_2 films are monitored by X-ray photoelectron spectroscopy (XPS) system. XPS experiments are performed with a K-Alpha - Monochromated high-performance XPS spectrometer.

Fig. 5.3 shows the XRD analysis of TiO_2 films with different annealing temperatures. All diffraction peaks can be indexed to the anatase and rutile phases of TiO_2.

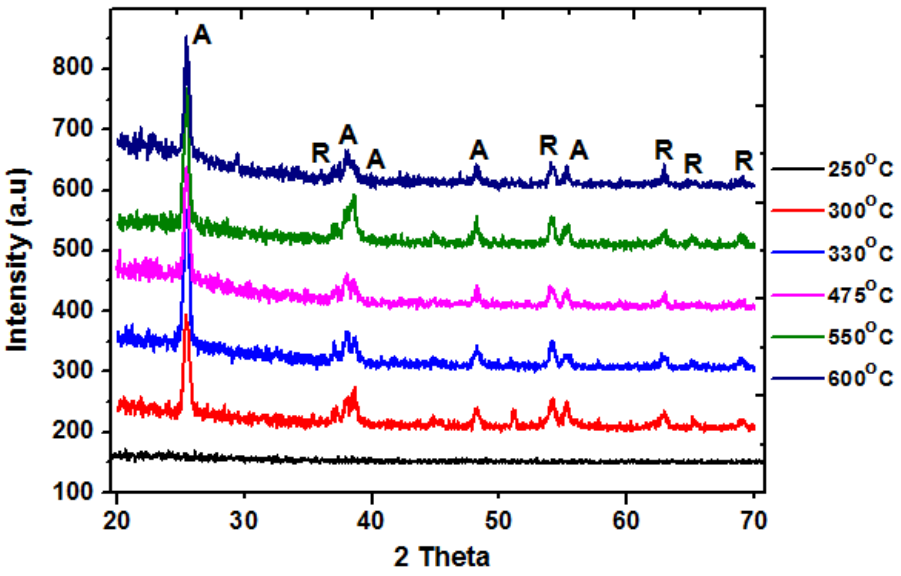


Figure 5.3 XRD patterns of TiO_2 films showing anatase and rutile phases

Films annealed at 250°C are in the amorphous phase. Anatase and rutile phases start to be formed in the film at temperatures higher than 300°C. The same

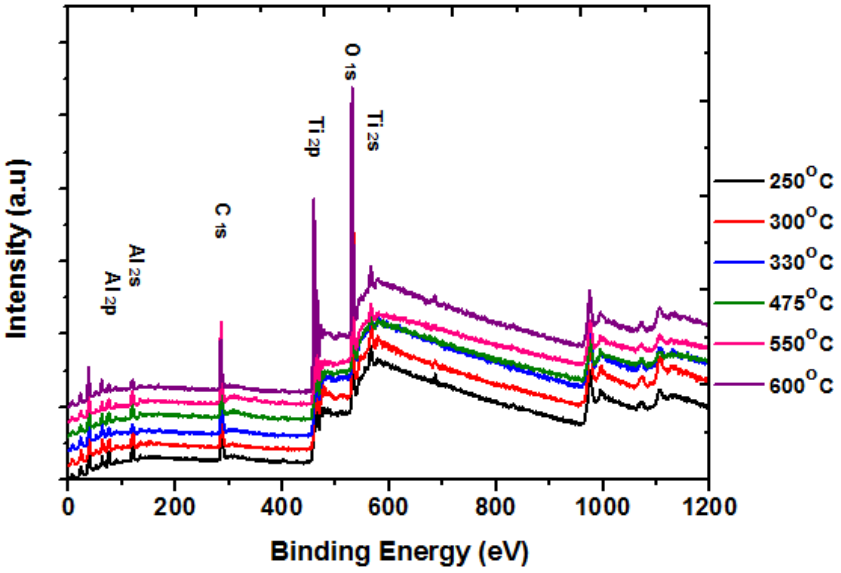
amorphous structure is also observed for films grown at 250°C. Similar crystallization pattern is observed for films annealed at 300°C with a rapid thermal annealing system for 10 min in O_2 atmosphere as compared to the ones annealed in a furnace at 300°C in air.

Table 5.2 shows the summary of Rietveld quantitative analysis for TiO_2 films annealed at different temperatures.[64]

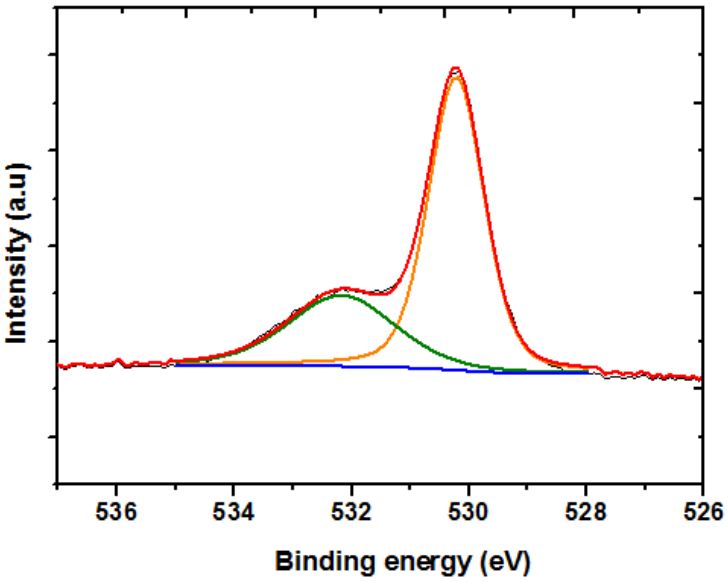
Temperature of Annealing	**Anatase**	**Rutile**
300	73.56	26.44
330	84.99	15.01
475	98.81	1.19
550	88.21	11.79
600	96.42	3.58

Table 5.2 Amount of mixed phases formed in films

XPS survey-scan spectra of TiO_2 films are shown in Fig. 5.4 (a). All XPS spectral peaks are fitted with Thermo Scientific Advantage software. As required by theory, O 1s and C 1s spectral lines consist of single peaks whereas the Ti 2p spectrum consists of two peaks.[65] The C 1s spectral line is standardized to 285.0 eV and the O 1s and Ti 2p spectra are adjusted to this energy. Fig. 5.4 (b) shows narrow scan of O 1s.



(a)



(b)

Figure 5.4 (a) Wide scan survey XPS spectrum of TiO_2 films, (b) narrow scan of O 1s

Based on the literature, the main peak at the 530.2 is due to the oxygen lattice and Ti-O bond while the peaks at 531.2 eV correspond to water (O-H) and hydroxide absorbed on the surface. Table 5.3 summarizes the atomic percentage of ratio of O-H and Ti-O bonds.

Annealing Temperature	*Atomic percentage (%) At Peak Regions*			Absorbed O/O lattice
	530.31	***531.84***	***532.94***	
300	11.28	3.4	-	0.301
330	10.1	4.85	-	0.480
475	7.08	5.56	-	0.785
550	6.75	3.11	2.24	0.461
600	9.26	4.57	-	0.494

Table5. 3 Atomic concentrations calculated from XPS results for TiO_2 films

5.4 Results and Discussion

Electrical properties of TiO_2

TiO_2 films can be used as either insulator or channel layer in transparent flexible TFT devices according to the doping concentration values.

- The adjustable doping concentration property of TiO_2 films is caused by a well-known issue with materials containing Ti-O bonds. There is always a possibility to have reduced oxide which contains oxygen vacancies that act as donors in the film.[17]

- In the literature, it is stated that for decreasing the doping concentration and making the TiO_2 layers more suitable as insulators, TiO_2 films can be doped with Al ions because they act as acceptors in the film which compensate n-type nature.[66, 28]

Electrical measurements of TiO_2 TFT's are performed with Keithley 4200-SCS parameter analyzer and a manual probe station Cascade PM-5.

Fig. 5.5 shows I_D - V_D characteristics of devices annealed at 250°C. It is observed that there is no gate control on the drain current, device acts like a resistor.

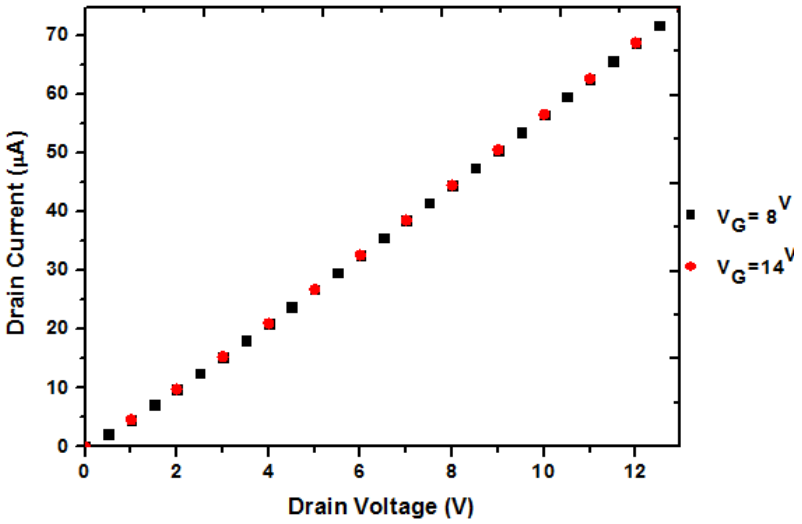


Figure 5.5 Transfer characteristics of devices annealed at 250°C which show ohmic behavior

Fig. 5.6 shows typical I_D – V_D characteristics of devices annealed at 475°C, which has channel dimensions of 50 μm width and 40 μm length.

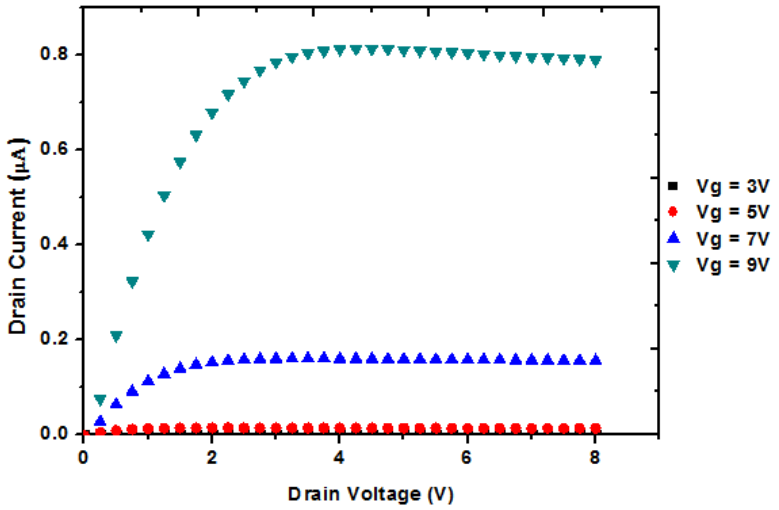


Figure 5.6 Typical output characteristics of TiO_2 TFT's

Fig. 5.7 shows typical transfer characteristics of devices annealed at different temperature values. V_D is varied in the range of 0.2^V to 0.5^V for I_D -V_G measurements. Results show that devices exhibit n-type behavior.

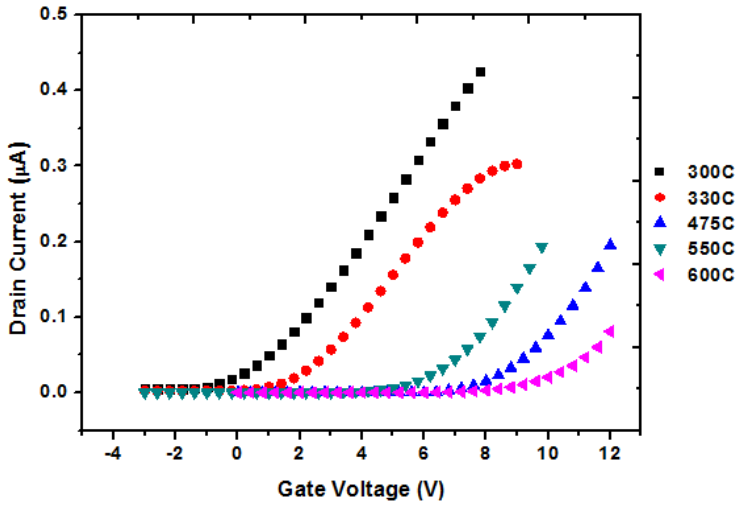


Figure 5.7 Transfer characteristics of TiO_2 TFT's

Fig. 5.8 shows the scaling behavior of I_D with respect to channel W/L ratio as expected from eqn. 3.10 and 3.11.

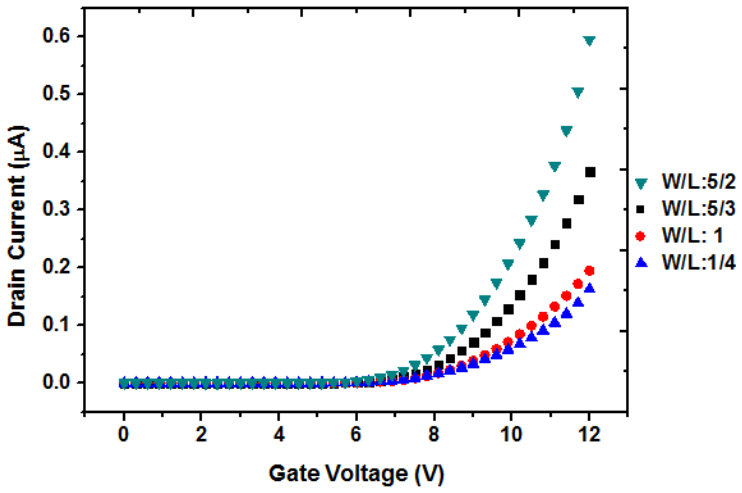


Figure 5.8 Drain current increases linearly with W/L ratio

Fig. 5.9 shows the change in I_D with changing drain voltages. Measurements are taken for drain voltages of 0.5^V and 5^V. The increase in drain current results from higher attraction applied on electrons in the channel from drain side.

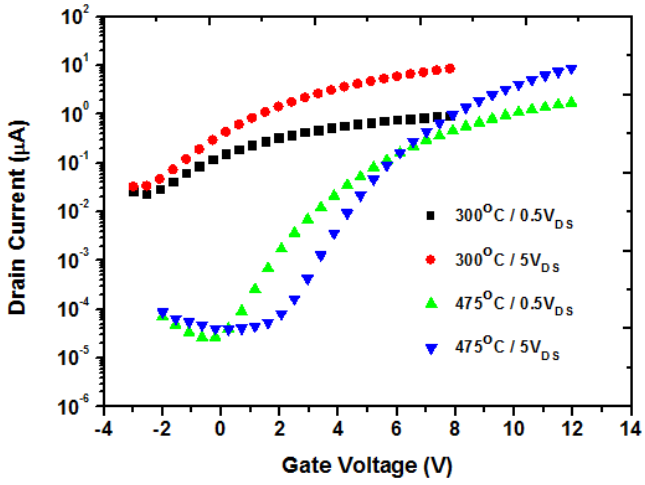


Figure 5.9 Drain current changes with respect to applied drain voltage in $I_D - V_G$ measurements

Electrical characteristics of devices are extracted as explained in chapter 4. Threshold voltages, sub-threshold slopes, I_{on}/I_{off} ratios and mobility values of devices are shown in Table 5.4.

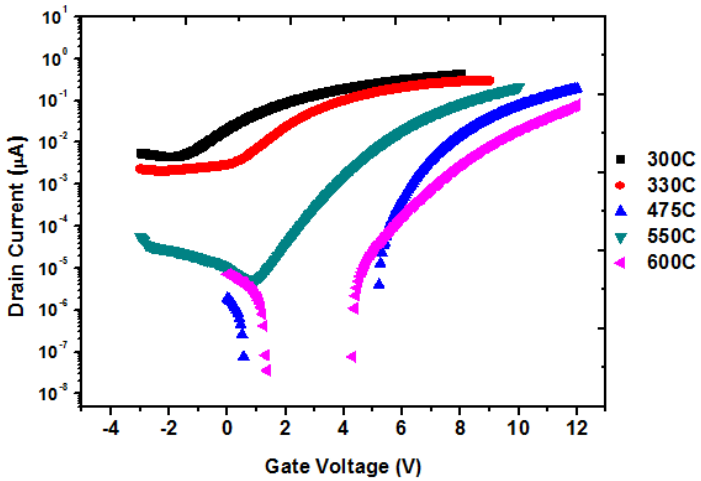


Figure 5.10 Log(I_D) vs V_G characteristics of devices

Analysis of electrical data using the material characterization results:

Annealing Temperature (°C)	*Atomic percentage (%) At Peak Regions*			Absorbed O/O lattice
	530.31	***531.84***	***532.94***	
300	11.28	3.4	-	0.301 ↗
330	10.1	4.85	-	0.480 ↗
475	7.08	5.56	-	0.785 ↗
550	6.75	3.11	2.24	0.461 ↙
600	9.26	4.57	-	0.494 ↗

XPS results

Annealing Temperature (°C)	Anatase	Rutile
300	73.56 ↗	26.44
330	84.99 ↗	15.01
475	98.81 ↗	1.19
550	88.21 ↙	11.79
600	96.42 ↗	3.58

XRD results

Annealing Temperature (°C)	Threshold Voltage (V)	I_{on}/I_{off} Ratio	Subthreshold Slope (V/dec)	Mobility $cm^2/V.s$
300	-1.8 ↗	10^2 ↗	6.55 ↙	0.337 ↗
330	0.2 ↗	10^2 ↗	5.21 ↙	0.409 ↗
475	6.5 ↗	$2.5x10^6$ ↗	0.35 ↙	0.672 ↗
550	4.3 ↙	$4x10^5$ ↙	1.36 ↗	0.19 ↙
600	7.1 ↗	10^6 ↗	0.35 ↙	0.29 ↗

Electrical measurement results

Table 5.4 Combination of material characterization and electrical measurement results

Transistor characterization and material characterization results show consistent trends. XRD, XPS and electrical measurements are used to obtain information about anatase phase composition, absorbed oxygen in the film and electrical performance parameters (subthroshold slope and threshold voltage) of devices, respectively. Results show that each indicator increases up to 475°C, decreases until 550°C and increases again until 600°C.

As mentioned in Table 5.5, as absorbed oxygen/oxygen lattice ratio increases, transistor characteristics improve in terms of I_{on}/I_{off} ratio and subthreshold slope. Absorbed oxygen/oxygen lattice ratio increases linearly with annealing

temperature because vacancies resulting from missing oxygen atoms get filled with oxygen diffusion at higher annealing temperatures. As a result, I_{on}/I_{off} ratio increases due to decreasing carrier concentration. In other words, gate control over the less doped channel layer becomes more effective.

The doping concentration of TiO_2 films is lowered with diffusing oxygen into the film. As a result, carrier mobility values increase with increasing temperature, too.

5.5 Conclusion

We conclude that as-deposited ALD TiO_2 films are amorphous and not suitable as TFT channel material. In order to fabricate a TFT with ALD TiO_2 films, a post-annealing process is needed. Annealed films transform into a polycrystalline form containing mixed anatase and rutile phases. Transistors built on annealed TiO_2 films show different characteristics with respect to annealing temperature. Devices annealed at 475°C showed best TFT characteristics in terms of threshold voltage values (6.5^V), subthreshold slopes (0.35 V/dec), I_{on}/I_{off} ratios ($2.5x10^6$) and mobility values (0.672 $cm^2/V.s$). When compared with literature, our devices show better characteristics for gate and drain voltages $<15^V$.

These characteristics are observed for non-patterned blanket TiO_2 films. If TiO_2 channel layer is patterned performance characteristics may become better. Also the dielectric thickness of TiO_2 TFT devices are 30 nm in our devices. If the dielectric layer is used thinner, although there may be possible parasitic leakage currents, gate control over channel may become better.

Chapter 6

Exotic Materials for TFT Devices

6.1 Introduction

In this chapter, results of TFT experiments based on exotic channel materials will be discussed. Experiments performed with four different channel materials will be explained: ZnO nanowire, GaN and pentacene structures.

- One-dimensional ZnO nanowires are very useful for nanoscale sensing applications in terms of sensitivity. Such structures are useful for ultraviolet lasers, light-emitting diodes, photodetectors, chemical sensors, and solar cells using the advantage of direct wide bandgap characteristics.

- GaN is an attractive channel material for high power transistors applications and good electron transport properties.[67] Advantages and disadvantages of GaN over other well known semiconductors used in transistor technology are shown in Table 6.1.

Where Gallium Nitride Outstrips Other Semiconductor Materials

Semiconductor (commonly used compounds)		Silicon	Gallium arsenide (AlGaAs/ InGaAs)	Indium phosphide (InAlAs/ InGaAs)[a]	Silicon carbide	Gallium nitride (AlGaN/ GaN)
Characteristic	Unit					
Bandgap	eV	1.1	1.42	1.35	3.26	3.49
Electron mobility at 300 K	cm2/Vs	1500	8500	5400	700	1000-2000
Saturated (peak) electron velocity	$X10^7$ cm/s	1.0 (1.0)	1.3 (2.1)	1.0 (2.3)	2.0 (2.0)	1.3 (2.1)
Critical breakdown field	MV/cm	0.3	0.4	0.5	3.0	3.0
Thermal conductivity	W/cm•K	1.5	0.5	0.7	4.5	>1.5
Relative dielectric constant	ε_τ	11.8	12.8	12.5	10.0	9.0

[a] The compounds are loosely known as indium-based.

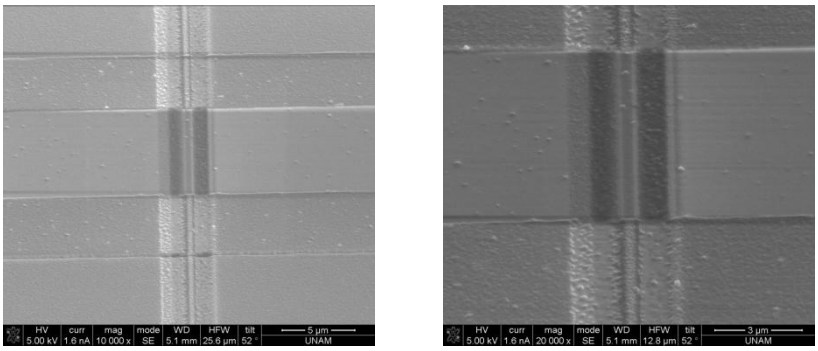
Table 6.1 Properties of GaN compared with other commonly used semiconductors[67]

- Organic field-effect transistors (OFETs) can be seen as alternatives to inorganic TFTs, owing to low cost fabrication and compatibility with plastic substrates. These advantages are very important for large area fabrication of low-cost devices.[68, 69] Pentacene based devices will be presented in this chapter as examples of OFET's.

6.2 Device Fabrication

The results presented in this chapter are collaboration efforts with various research groups. As a result, fabrication processes consist of two separate parts. In the first part, transistors are fabricated using designs shown in chapter 4. The channel materials (except for ZnO nanowires) are prepared by other research groups.

The fabrication of ZnO nanowire based devices is completed with focused ion beam (FIB) etching of ZnO channel layers to form nanowires. (See Fig. 6.1) Koray Mızrak, FIB engineer, performed this step at UNAM facilities.



(a) (b)

Figure 6.1 (a) SEM image of FIB etched ZnO-channel TFT, (b) closer view of the nanowire

GaN channel layer deposition is performed by Bıyıklı group, UNAM, using a plasma enhanced ALD system (see Ref. 70 for material deposition and characterization details) and pentacene films are deposited by Danışman group, METU Dept. of Chemistry.

6.3 Results and Discussion

ZnO nanowire TFT's

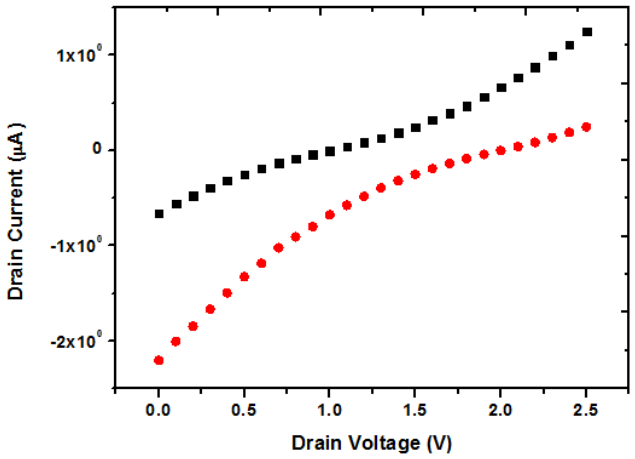


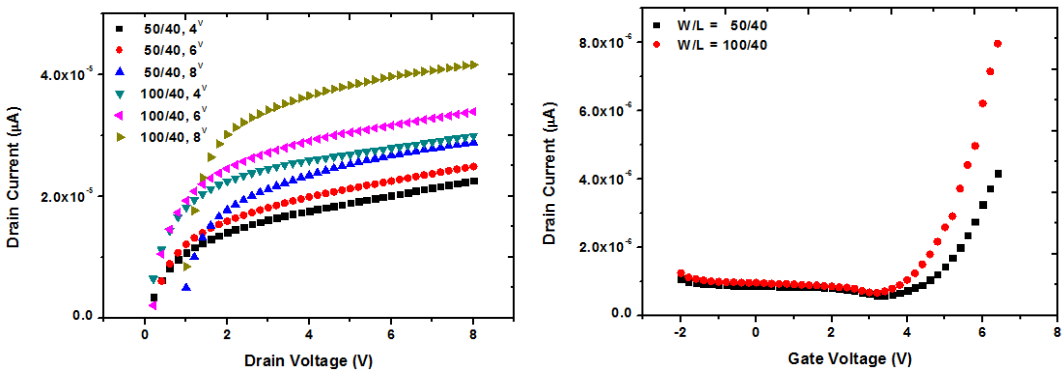
Figure 6.2 I_D – V_D characteristics of ZnO nanowire TFT's with different W/L ratios

As Fig. 6.2 shows, transistor operation could not be observed, devices show nonlinear resistor characteristics. FIB etching is not suitable for forming nanowires because during the operation Ga ions may be doping the channel material. This side-effect is assumed to be responsible from reduced gate control.

GaN TFT's

Fig. 6.3 shows I_D – V_D characteristics and transfer characteristics of GaN TFT's. Devices show fundamental transistor characteristics, but with very weak gate control. The gate leakage current is relatively high. Also I_{on}/I_{off} ratios and drain current values of devices are very low, highest drain current value shown in Fig. 6.3 is around $4x10^{-11}$ Amperes. These characteristics are attributed to undesired oxygen concentration in ALD-grown GaN layer, originating from oxygen

leakage into the reaction chamber. Further efforts are needed to reduce the oxygen concentration in GaN layers.



(a) (b)

Figure 6.3 (a) $I_D - V_D$ characteristics of GaN TFT's with different W/L ratios and gate voltages, (b) transfer characteristics of devices

Pentacene TFT's

Pentacene ($C_{22}H_{14}$) based TFT's which have one of the highest charge carrier mobilities[69] among organic materials should be measured under vacuum environment in order to prevent degradation of channel material but since we do not have a measurement setup like that, we took measurements under ambient room conditions right after pentacene deposition.

Electrical measurements show that devices exhibit p-type characteristics. $I_D - V_D$ characteristics shown in Fig. 6.4 (a) belong to a device having a channel width of 100 μm and a channel length of 20 μm. In Fig. 6.5 (b), characteristics of a device having channel W/L ratio of 100 μm/50 μm is shown. Device shown in (a) has a channel thickness of 15 nm and (b) 20 nm.

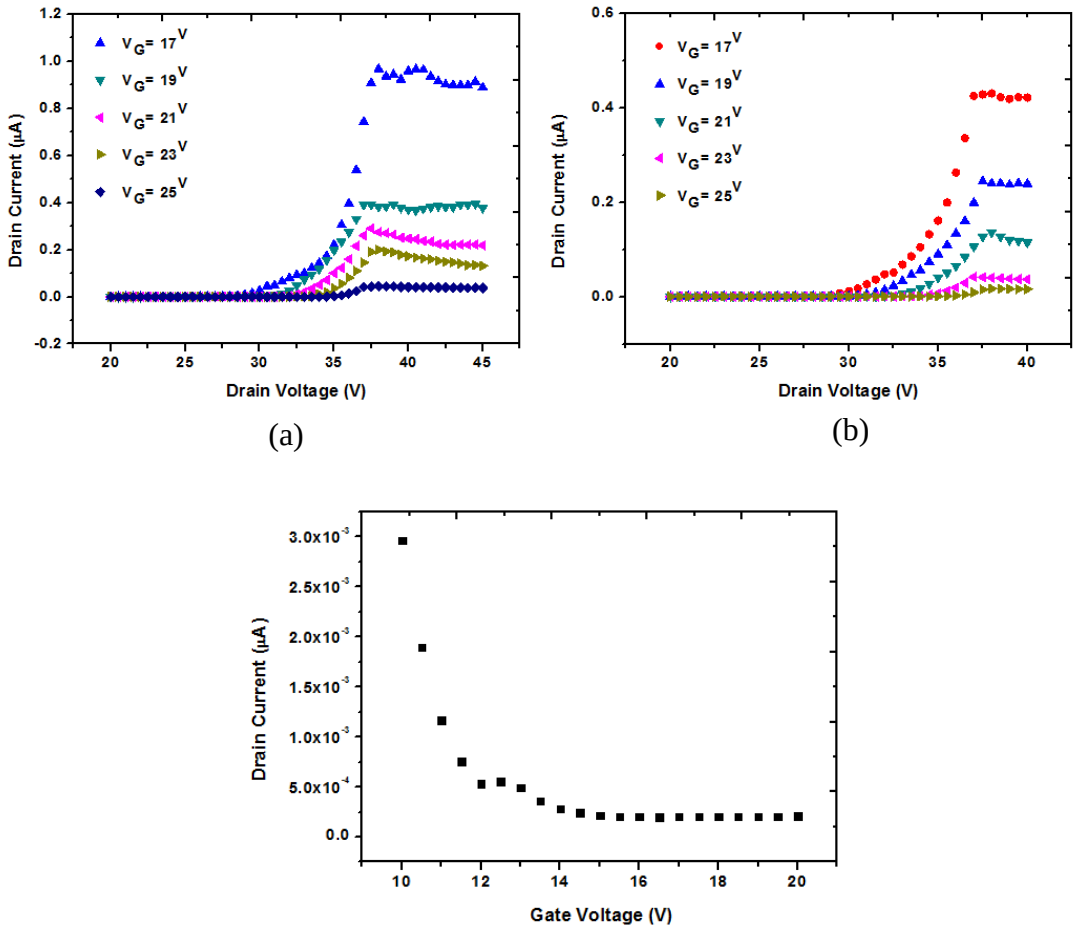


Figure 6.4 (a), (b) $I_D - V_D$ characteristics of pentacene TFT's with different W/L ratios (c) transfer characteristics of device having W/L ratio of 100μm /20μm

Results look very promising and comparable with literature in terms of device performance. Although pentacene TFT's operate at very high voltage values, they are suitable for inorganic-organic hybrid structures.

6.4 Conclusion

In this chapter, measurement results of devices fabricated with exotic materials are shown. Results showed that GaN and pentacene TFT's initial results are promising.

As explained in chapter 4, chemisorption of oxygen severely affects the performance of ZnO nanowire TFT's.[1] This non-ideality makes ZnO nanowire TFT's suitable for oxygen sensors which can be a very interesting future work on the topic. It is observed that sensitivity of ZnO nanowire TFT's to oxygen is higher with smaller radii nanowires and oxygen detection sensitivity can be changed with the gate voltage. (See Ref. 71)

Further research can be made to optimize channel layer and dielectric thicknesses of all devices mentioned in this chapter to increase gate control over channel layers. Patterning channel layers can also be tried to distribute the electric field more effectively.

Chapter 7

Conclusions

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a very important device for integrated circuit industry. Its history goes back to early 1930s. After several decades of important discoveries in the field of transistors, denser integrated circuits and smaller devices are achieved. With scaling down transistors, technological challenges and fabrication costs started to limit this miniaturization process. In addition to the big race in computational chips, MOSFETs are also used as thin-film-transistors (TFTs) especially for the display industry. Among the core requirements of TFT technology for display industry is large area and low cost process capability. TFT technology heavily employs CVD deposited amorphous and polycrystalline Silicon as the transistor active material. Recently, ZnO based materials such as indium-gallium-zinc-oxide (IGZO) has attracted significant attention due to low temperature and large area applicability. In addition ZnO is a wide bandgap semiconductor material that is optically transparent in the visible spectrum.

In this thesis, we investigate ALD-deposited ZnO and TiO_2 as candidate technologies for TFT applications for low cost electronics. By using ALD

systems, highly conformal, highly controllable, low deposition rate, low temperature, low cost, high quality films can be grown on many substrates including transparent and flexible ones. Transparent electronic devices can be used in many fields like military, space, health and security in addition to displays.

Nitrides (semiconductors, metallic, dielectric), oxides (ternary oxides, semiconductors, dielectric, transparent conductors), fluorides, elements, II-IV compounds and III-V compounds can be deposited with ALD technique.

Various TFT fabrication methods with different channel materials and their electrical characteristics are demonstrated. Among all these channel materials, ZnO has the largest literature due to its attractive optoelectronic properties. Results showed that by lowering the growth temperature and so Zn interstitials, O vacancies and the amount of H in the film, one can fabricate TFT's having I_{on}/I_{off} ratio high as $7.8x10^9$, and subthreshold slope of 0.116 V/dec.

This thesis demonstrates thermal-ALD deposited TiO_2 TFT's for the first time in the literature. Results showed that TFT's fabricated with as-deposited films do not show gate field control over the channel layer but after a thermal treatment performed at temperatures higher than 300°C, relatively high performance TFT's can be obtained. According to characteristics shown here, TFT's annealed at 475°C have the best characteristics. ($2.5x10^6$ I_{on}/I_{off} ratio, 0.35 V/dec subthreshold slope)

Devices based on exotic channel materials are also briefly investigated. Further research on pentacene and GaN devices could potentially lead to significant results.

In the future, these devices may be used in several applications in fields like memories, functional and three-dimensional IC's and sensor applications. Personally, my dream is to modify these devices for bio-sensing applications.

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